applications handbook

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UNITRODE

The Linear IC Company Everyone Follows

Unitrode's reputation and success as an innovator is evidenced by the strong market acceptance to the products described in this book. The Company has achieved significant technological breakthroughs in all areas of power management, motion control, and high speed data communication ICs.

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Please Refer to Unitrode Data Book IC-1050 for Complete Product Data Sheets

Unitrode Corporation is a world leader in the design and manufacture of innovative, high performance linear and mixed signal ICs. This catalog will introduce you to our products for commercial, industrial and mil/aero applications.

With a focus on power management, motion control and high speed data communications, our product portfolio includes:

- Off-line Power Management
- DC/DC Power Management
- Protection/Supervisory Circuits
- Portable Power Management
- Motion/Motor Controls
- High Speed Interface

Unitrode also offers an assortment of special function ICs including fiber to curb ringers, CAN transceivers, IrDA transceivers, cellular power management products and pager/PDA power controllers.

All our products are backed by a design and applications team that really understands how our ICs interact with the rest of your system/subsystem. We take special pride in the intelligence of our designs and their ability to anticipate as well as respond to customer needs.

Whatever your applications – Power Management, Motion Control or Ultrafast Data Communications – we are an innovative, dependable and customer-driven source for catalog, semi-custom and custom linear/mixed signal ICs.

Around The World Service

Unitrode serves its customers around the world from:

- its design centers in New Hampshire, California and North Carolina;
- its extensive test, assembly subcontractor coordination, and customer service facility in Singapore;
- and from our network of manufacturers' representatives and distributors.

Process Capabilities

Unitrode's bipolar process, optimized for both precision analog and power functions, is constantly updated to incorporate leading edge process options such as:

- operating voltage ranges from 4 to 65 volts;
- Schottky and integrated injection logic;
- ion implant;
- thin film resistors for high accuracy;
- double-level metallization for high density, high current layouts;
- and buried zener reference.

Its BiCMOS process is ideal for high density linear and mixed mode designs, especially where speed and low power consumption are of primary importance.

Options include:

- 3, 2.5, and 1 micron processes;
- up to 15V operation;
- high current, double level metallization;
- fully isolated, vertical NPN transistors;
- and thin film resistors

This year, there is a new BCDMOS process. It offers all the options available with BiCMOS, plus a lateral DMOS device with up to 35V operation for added power handling capability.

An ISO9001 and 9002 Firm

Unitrode was one of the first U.S. electronics companies to achieve IS/ISO 9001/EN29001 registration.

In order to be registered, the Company had to pass a rigorous examination of its quality systems – from product design through shipment. The registration thus assures customers all over the world that the Company is adhering to very high, precisely defined standards.

Listening To Customers

In the development of custom and semi-custom parts, Unitrode design engineers work very closely with customers. This close cooperation assures that all requirements are accurately understood, that all possibilities are fully explored, and that the resulting products meet and exceed specified needs.

Unitrode also pays careful attention to customers and markets to help guide its development of catalog parts. Continuing close contact makes it possible to anticipate industry requirements, and to create devices that will satisfy them.

A Resource You Can Count On

Unitrode Corporation has earned its reputation for excellence in computer, Communications, Industrial, Commercial, Automotive and Mil/Aero markets. It is totally committed to continuing excellence in everything it does.

With products and services that are among the most innovative in the industry, with proven quality and reliability, and with superb design engineering and the industry's best applications technical support, Unitrode is a resource you can depend on.

This book describes Unitrode's linear and mixed signal IC solutions in detail. Ideally, it will stimulate your interest to request further information, request product samples and/or to check for available evaluation boards.

For additional information on devices offered in this catalog, or if you need a customized product, please contact Unitrode Marketing at 603-429-8725. You may also consult our website for current information about Unitrode and its products at http://www.unitrode.com.

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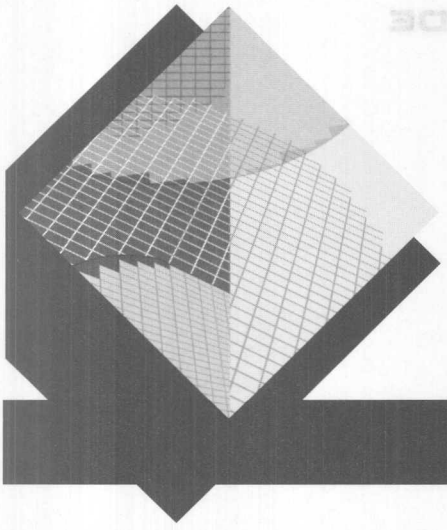
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Unitrode offers an excellent series of Power Supply Design Seminars throughout the United States and around the world, with a new series beginning every eighteen months. Below is a review of several abstracts from topics presented at some of the past seminars.

Please call Unitrode Marketing at 603-429-8725 for copy of any of these tutorials. If you are interested in attending a future Unitrode Seminar, please call Marketing or return the postcard included in the Databook.

High Power Factor Preregulator for Off-Line Power Supplies (SEM-600)

Switching power supplies operated off the AC line usually employ a simple capacitor input filter. The input charging current waveform is a narrow pulse rather than a sine wave, resulting in a power factor of only 0.5 - 0.65 and high harmonic content. The rms input current is much greater than necessary. A 120V, 15A line may be inadequate for a 1kW power supply input. High power factor specification requirements are beginning to appear. The innovative techniques described in this paper provide input power factor of 0.95 to 0.999, reduced harmonics, switchless operation over the full 120V - 220V line voltage ranges, crudely regulated bulk capacitor voltage, smaller capacitor size, and greater reliability because of reduced rms current. A downstream switching power converter can be designed for higher efficiency and lower cost because it operates from the narrowed bulk capacitor voltage range.

- Lloyd Dixon

Isolating the Control Loop (SEM-700)

In the interests of safety, all power systems operating from primary line voltage must provide galvanic isolation somewhere in the system between the power mains and a human operator or technician. The various potential locations for inserting isolation, and the possible methods of its implementation, are presented in this topic. Specific attention is paid to alternative solutions, such as the use of small signal coupling transformers, and are described and illustrated with practical applications.

- Bob Mammano

Spice Simulation of Switching Power Supply Performance (SEM-900)

Spice simulation is a useful and important tool for power supply design. Spice models are used to demonstrate the performance and stability of a proposed design and to evaluate the effects of circuit parasitics and parameter variation on power supply performance. Switched models are best suited to assess high frequency aspects of the design, while averaged models are used for overall performance evaluation. A new simplified averaged model is presented. Several practical examples demonstrate how switched and averaged models can be used to evaluate specific aspects of switching power supply performance.

- Lloyd Dixon

An Electrical Circuit Model for Magnetic Cores (SEM-1000)

A brief tutorial on magnetic fundamentals leads into a discussion of magnetic core properties. A modified version of Intusoft's magnetic core model is presented. Low-frequency hysteresis is added to the model, making it suitable for magnetic amplifier applications.

- Lloyd Dixon

Deriving the Equivalent Electrical Circuit from Magnetic Device Physical Properties (SEM-1000)

Following a brief review of basic magnetics, two techniques are discussed for generating the electrical circuit model based upon the physical dimensions of a magnetic device: the reluctance-duality method and the capacitance-gyrator method. These techniques are demonstrated in several examples.

- Lloyd Dixon

Portable Power - A Designer's Guide to Battery Management (SEM-1000)

While demands for portability have created great interest in battery technology, this is a field with many choices, few absolutes, continuously improving performance characteristics, and the constant lure of future developments. Since the designer of portable electronic systems is vitally dependent upon his power source, while also sharing a major responsibility for its performance, a good understanding of battery technology becomes mandatory. This paper attempts to aid in this effort by characterizing and comparing a range of battery technologies and providing insight into their selection and application. Since charging techniques are critical to battery performance, practical examples of charging algorithms and associated hardware implementations for the various battery chemistries are also discussed and a versatile battery system evaluator is described.

- Bob Mammano

Switching Power Supply Control Loop Design (SEM-1000)

This paper surveys many practical aspects of control circuit design. Topics include: different approaches for achieving Nyquist stability criteria, transient response vs. phase margin, low frequency accuracy vs. the shape of the Bode plot, why it is dangerous to depend on conditional stability, achieving the maximum crossover frequency of a switched loop, other factors which may limit loop bandwidth, sources of error, and where to place the gain needed for correction.

Other practical aspects include large signal behavior and how to minimize offset error delays of compensation capacitors in the feedback path.

- Lloyd Dixon

Control Loop Cookbook (SEM-1100)

Switching power supplies use closed-loop feedback to achieve design objectives for line and load regulation and dynamic response. Fortunately, the closed-loop systems used in switching power supplies are usually not very complicated, permitting the use of simple analytical techniques to achieve loop stabilization. A simplified version of the Nyquist stability criteria can be used because unity gain crossover occurs only once in the gain vs. frequency characteristic. Bode plots provide a simple and powerful method of displaying and calculating the loop gain. This paper begins with a quick review of basic control loop theory.

- Lloyd Dixon

Design Considerations for Active Clamp and Reset Technique (SEM-1100)

Performance of the single-ended forward and flyback converters can be significantly enhanced by use of the active clamp/reset technique. The benefits of this technique include higher efficiency at high switching frequencies, lower EMI/RFI and lower component stresses. A previous Unitrode Seminar (SEM-1000) and other publications have provided a qualitative overview of this technique by highlighting various modes of operation. This paper addresses the design considerations required for designing single-ended active clamp forward and flyback converters. Major performance trade-offs are identified and quantified. A design procedure with relevant equations is provided. This procedure is used to design an off-line forward converter with active clamping. Operating results of this converter are presented with effects of certain design choices highlighted.

- Dhaval Dalal

High Power Factor Switching Preregulator Design Optimization (SEM1100)

Design of a high power factor active preregulator using the UC3854 is optimized to achieve less than 3% harmonic distortion and power factor better than 0.995 without a sample/hold. The circuit operates over a line voltage range exceeding 3:1 and at loads approaching zero. Under these wide-ranging conditions, the loop gain is constant and the dynamic response to large transient changes in line and load is excellent.

- Lloyd Dixon

Unitrode engineers have published conference papers on many different subjects. Listed below is a selection of these titles. If you are interested in receiving a copy of any, please call Unitrode Marketing at 603-429-8725, or return the postcard in the Databook.

Publications by Unitrode Authors

1. "A High-Efficiency Boost Algorithm Optimizes a Lithium-Ion Battery Regulator"
   Portable-by-Design Conference, February 1995.
   - Bob Mammano and Mickey McClure

2. "A Study of MOSFET Performance in Processor Targeted Buck and Synchronous Rectifier Buck Converters"
   Power Systems World Conference, 1996. ***- Larry Spaziani***

3. "Analysis and Design of a 250kHz, 500W Power Factor Correction Circuit Employing Zero Voltage Transitions"
   High Frequency Power Conversion Conference, 1995.
   - Jim Noon

4. "Analysis of a Voltage Controlled Frequency Foldback Technique that Improves Short Circuit Protection for Buck Derived Converters"
   Intelec Conference, 1996. ***- Phil Cooke***

5. "Charging the New Batteries - IC Controllers Track New Technologies"
   IEEE Annual Battery Conference, January 1995. ***- Bob Mammano***

6. "Constant Input Power Modulation Technique for High Efficiency Boost Converter Optimized for Lithium-Ion Battery Applications"
   APEC 1996. ***- Mickey McClure and J. Scott Elder***

7. "Converter Optimization for Powering Low Voltage, High Performance Microprocessors"
   APEC 1996. ***- John O'Connor***

8. "Designing for Hot-Swap Requires Electronic Circuit Breakers"
Portable-by-Design Conference, February 1995.
- Bob Mammano and Dave Zendzian

9. "Designing PWM Power Supplies for High Efficiency at Micropower Levels"
Portable-by-Design Conference, 1997.
- Laszlo Balogh and Bob Mammano

10. "Monolithic Controller for Single Stage Power Factor Correction with Isolation and Soft-Switching"
High Frequency Power Conversion Conference, 1995.
- Jim Bazinet and Dhaval Dalal

11. "New Developments in High Power Factor Circuit Topologies"
Power Systems World Conference, September 1996.
- Bob Mammano

12. "Novel Control IC for Single-Ended Active Clamp Converters"
High Frequency Power Conversion Conference, 1995.
- Dhaval Dalal and Larry Wofford

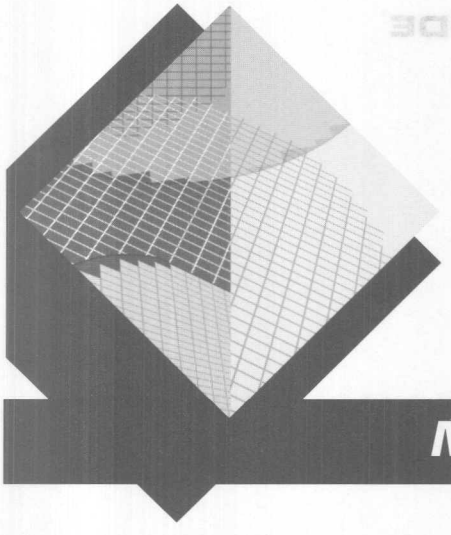
13. "The Performance of the Current Doubler Rectifier with Synchronous Rectification"
High Frequency Power Conversion Conference 1995.
- Laszlo Balogh

14. "Power Conversion Technique Optimizes Battery Lifetime and Provides Multiple Outputs from a Single Inductor"
Portable-by-Design Conference, 1997.
- Mark Jordan and Eddy Wells

15. "Practical Design Issues for PFC Circuits"
APEC 1997 *- Dhaval Dalal*

16. "System and Control Design for a DC Motor in a Force Feedback Application"
Incremental Motion Control Systems and Devices, 1997.
- Phil Cooke and Dave Zendzian

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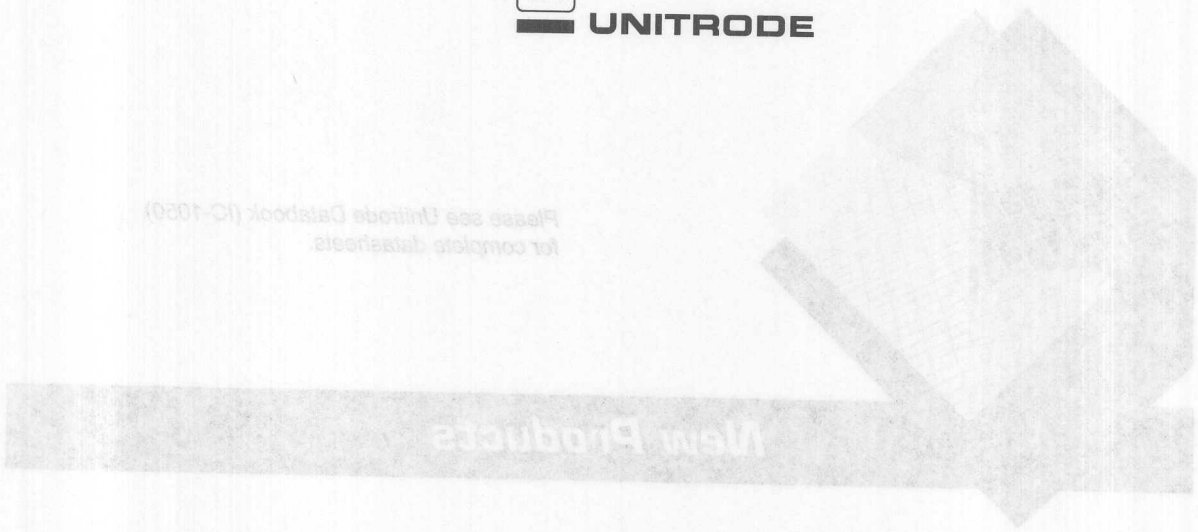


Please see Unitrode Databook (IC-1050) for complete datasheets.

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Pulse Width Modulators (cont'd)

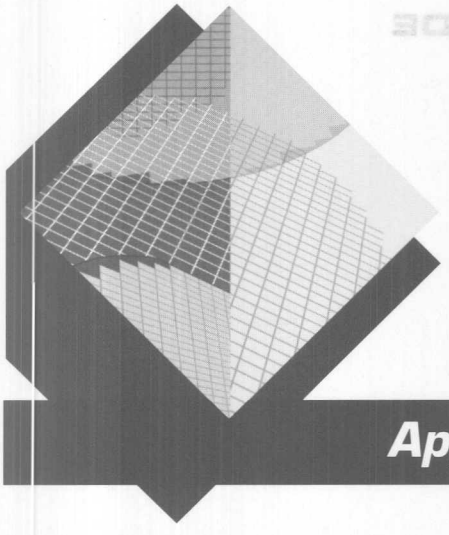
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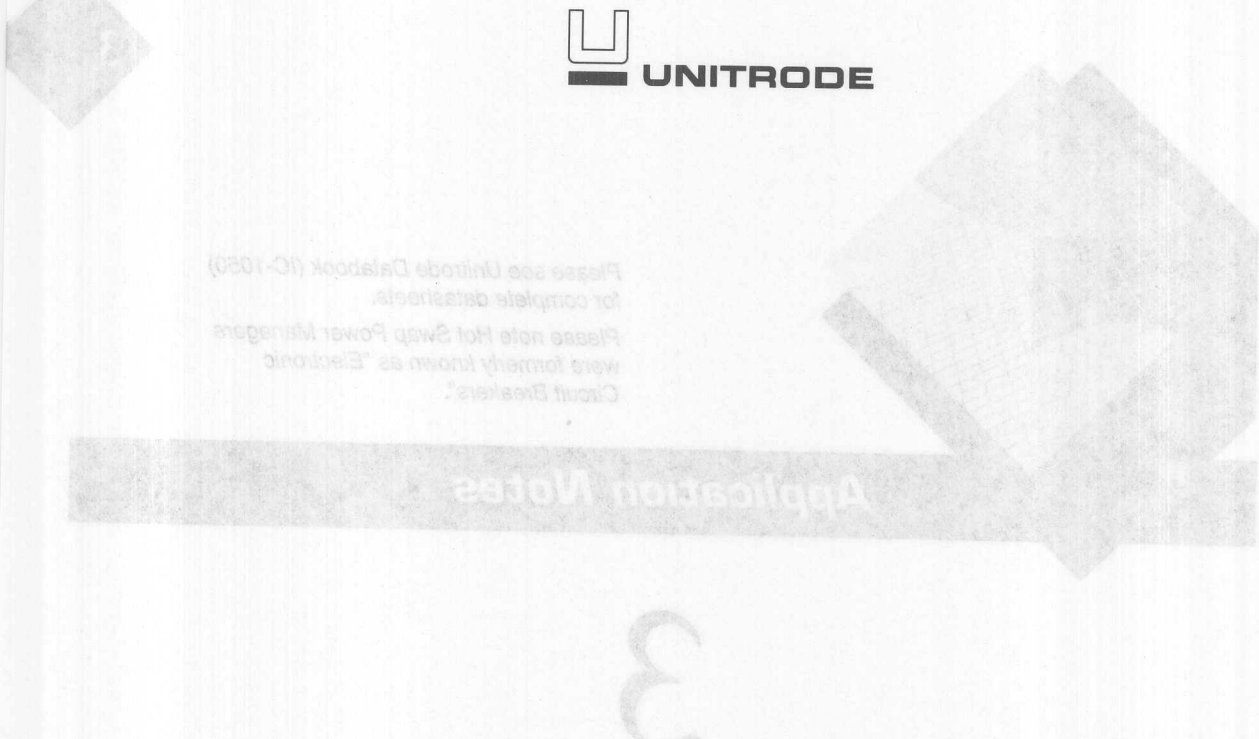


Please see Unitrode Databook (IC-1050) for complete datasheets.

Please note Hot Swap Power Managers were formerly known as "Electronic Circuit Breakers".

Application Notes

3


UNITRODE

A NEW INTEGRATED CIRCUIT FOR CURRENT MODE CONTROL

Abstract

The inherent advantages of current-mode control over conventional PWM approaches to switching power converters read like a wish list from a frustrated power supply design engineer. Features such as automatic feed forward, automatic symmetry correction, inherent current limiting, simple loop compensation, enhanced load response, and the capability for parallel operation all are characteristics of current-mode conversion. This paper introduces the first control integrated circuit specifically designed for this topology, defines its operation and describes practical examples illustrating its use and benefits.

1.0 Introduction

Over the past several years an increased interest in current-mode control of switching inverters has surfaced in the literature. Originally invented in the late 1960s, this scheme was not publicly reported until 1977[1] and has seen rapid development by many authors to date.[2-6] In short, current-mode control uses an inner or secondary loop to directly control peak inductor current with the error signal rather than controlling duty ratio of the pulse width modulator as in conventional converters. Practically, this means that instead of comparing the error voltage to a voltage ramp, it is compared to an analogue of the inductor current forcing the peak current to follow the error voltage.

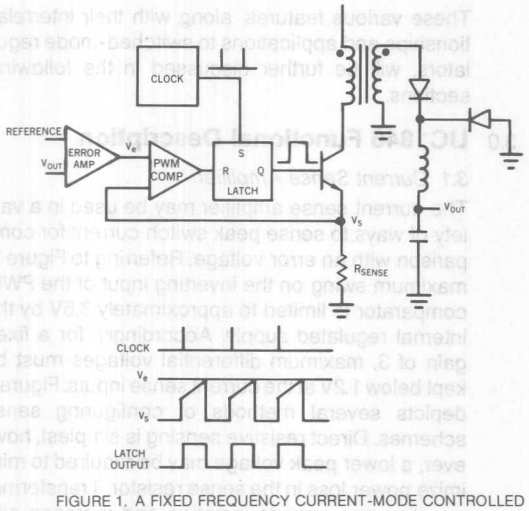


FIGURE 1. A FIXED FREQUENCY CURRENT-MODE CONTROLLED REGULATOR.

Figure 1 illustrates a simplified block diagram of a fixed frequency buck regulator employing current-mode control. As shown, the error signal, V_e, is controlling peak switch current which, to a good approximation, is proportional to average inductor current. Since the average inductor current can change only if the error signal changes, the inductor may be replaced by a current source, and the order of the system reduced by one. This results in a number of performance advantages including improved transient response, a simpler, more easily designed control loop, and line regulation comparable to conventional feed-forward schemes. Peak current sensing will automatically provide flux balancing thereby eliminating the need for complex balance schemes in push-pull systems. Additionally, by simply limiting the peak swing of the error voltage V_e, instantaneous peak current limiting is accomplished. Lastly, by feeding identical power stages with a common error signal, outputs may be paralleled while maintaining equal current sharing.

Although the advantages of current-mode control are abundant, wide acceptance of this technique has been hampered by a lack of suitable integrated circuits to perform the associated control functions. This paper introduces a new integrated circuit designed specifically for control of current-mode converters. Circuit function and features are described in detail, and a comparative design example is used to illustrate the numerous advantages of this approach.

2.0 UC1846 Chip Architecture

In addition to all the functions required of conventional PWM controllers, a current-mode controller

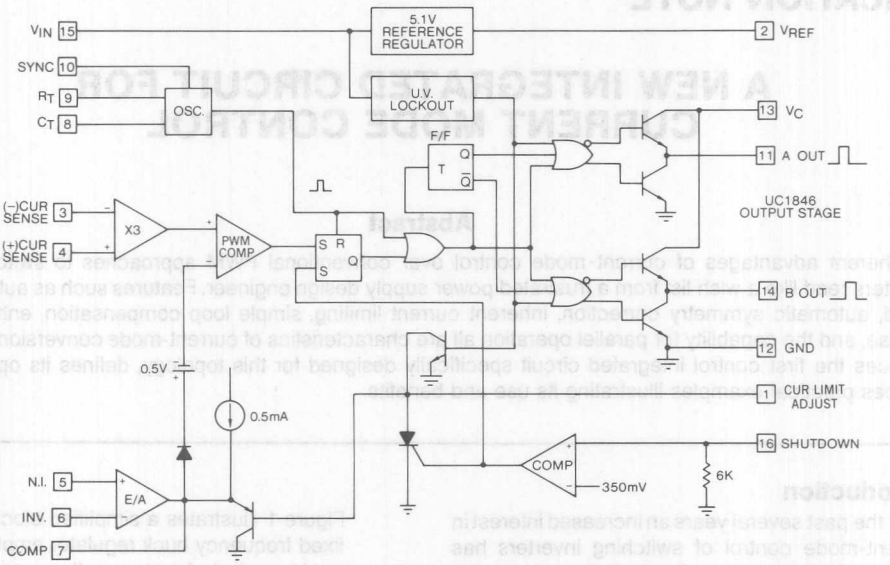


FIGURE 2. UC1846 BLOCK DIAGRAM

must be able to sense switch or inductor current and compare it on a pulse-by-pulse basis with the output of the error amplifier. As may be seen in the block diagram of Figure 2, this is accomplished in the UC1846 by using a differential current sense amplifier with a fixed gain of 3. The amplifier allows sensing of low level voltages while maintaining high noise immunity. A list of other features, while not unique to current-mode conversion, demonstrates the advanced, state-of-the-art architecture of the UC1846:

- A ± 1%, 5.1V trimmed bandgap reference used both as an external voltage reference and internal regulated power source to drive low level circuitry.
- A fixed frequency sawtooth oscillator with variable deadtime control and external synchronization capability. Circuitry features an all NPN design capable of producing low distortion waveforms well in excess of 1MHz .
- An error amplifier with common mode range from ground to V_{cc}-2V.
- Current limiting through clamping of the error signal at a user-programmed level.
- A shutdown function with built in 350mV threshold. May be used in either a latching, or non-latching mode. Also capable of initiating a "hiccup" mode of operation.
- Under-voltage lockout with hysteresis to guarantee outputs will stay "off" until reference is in regulation.
- Double pulse suppression logic to eliminate the possibility of consecutively pulsing either output.
- Totem pole output stages capable of sinking or sourcing 100mA continuous, 400mA peak currents.

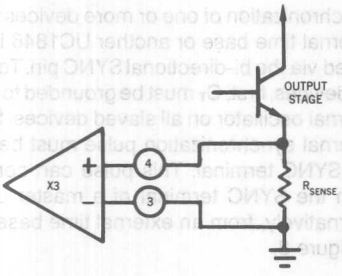
These various features, along with their interrelationships and applications to switched-mode regulators, will be further discussed in the following sections.

3.0 UC1846 Functional Description

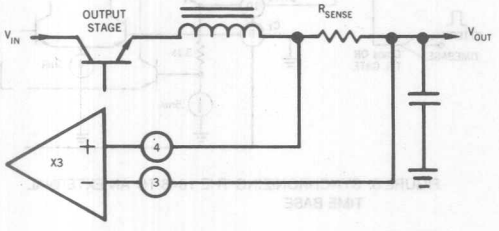
3.1 Current Sense Amplifier

The current sense amplifier may be used in a variety of ways to sense peak switch current for comparison with an error voltage. Referring to Figure 2, maximum swing on the inverting input of the PWM comparator is limited to approximately 3.5V by the internal regulated supply. Accordingly, for a fixed gain of 3, maximum differential voltages must be kept below 1.2V at the current sense inputs. Figure 3 depicts several methods of configuring sense schemes. Direct resistive sensing is simplest, however, a lower peak voltage may be required to minimize power loss in the sense resistor. Transformer coupling can provide isolation and increase effi-

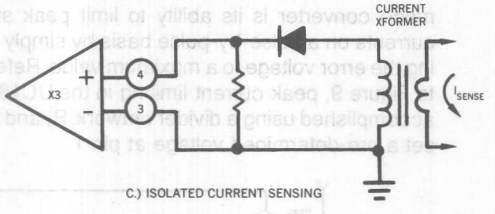
ciency at the cost of added complexity. Regardless of scheme, the largest sense voltage consistent with low power losses should be chosen for noise immunity. Typically, this will range from several hundred millivolts in some resistive sense circuits to the maximum of 1.2V in transformer coupled circuits.



A.) RESISTIVE SENSING WITH GROUND REFERENCE



B.) RESISTIVE SENSING ABOVE GROUND



C.) ISOLATED CURRENT SENSING

FIGURE 3. VARIOUS CURRENT SENSE SCHEMES

In addition, caution should be exercised when using a configuration that senses switch current (Figure 3A) instead of inductor current (Figure 3B). As the switch is turned on, a large instantaneous current spike can be generated in the sense resistor as the collector capacitance of the switch is discharged. This spike will often be of sufficient magnitude and duration to trip the current sense latch and result in erratic operation of the PWM circuit, particularly at lower duty cycles. A small RC filter (Figure 4) in series with the input is generally all that is required to reduce the spike to an acceptable level.

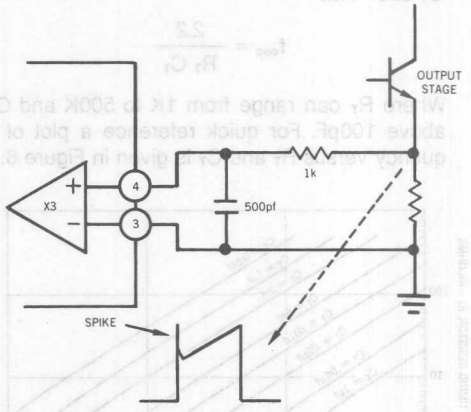


FIGURE 4. RC FILTER FOR REDUCING SWITCH TRANSIENTS

3.2 Oscillator

Although many data sheets tout 300 to 500kHz operation, virtually all PWM control chips suffer from both poor temperature characteristics and waveform distortions at these frequencies. Practical usage is generally limited to the 100 to 200kHz range. This is a direct consequence of having slow (f_t = 2MHz) PNP transistors in the oscillator signal path. By implementing the oscillator using all NPN transistors, the UC1846 achieves excellent temperature stability and waveform clarity at frequencies in excess of 1MHz.

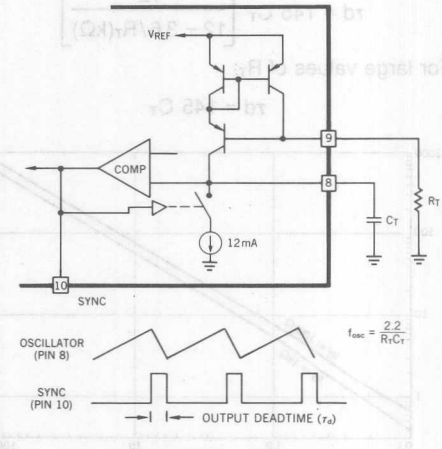


FIGURE 5. OSCILLATOR CIRCUIT

Referring to Figure 5, an external resistor R_T is used to generate a constant current into a capacitor C_T to

produce a linear sawtooth waveform. Oscillator frequency may be approximated by selecting R_T and C_T such that:

$$f_{osc} = \frac{2.2}{R_T C_T} \quad (1)$$

Where R_T can range from 1K to 500K and C_T is above 100pF. For quick reference a plot of frequency versus R_T and C_T is given in Figure 6.

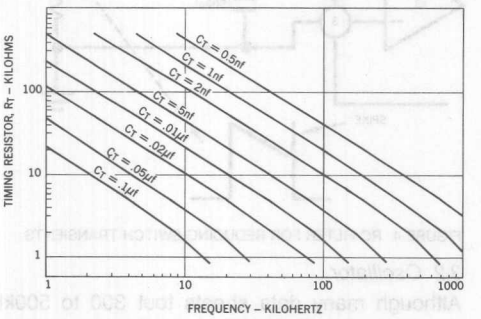


FIGURE 6. OSCILLATOR FREQUENCY AS A FUNCTION OF R_T AND C_T

Again referring to Figure 5, the oscillator generates an internal clock pulse used, among other things, to blank both outputs and prevent simultaneous cross conduction during switching transitions. This output "deadtime" is controlled by the oscillator fall time. Fall time, in turn, is controlled by C_T according to the formula:

$$\tau d = 145\ C_T \left[\frac{12}{12 - 3.6/R_T(k\Omega)}\right] \quad (2)$$

For large values of R_T:

$$\tau d = 145\ C_T \quad (3)$$

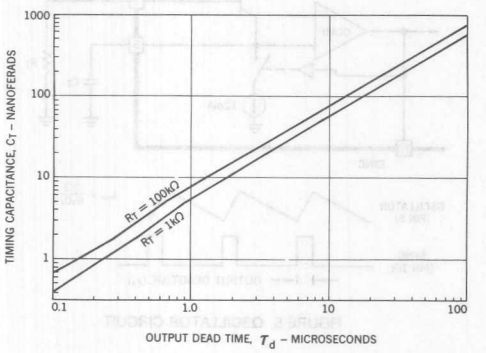


FIGURE 7. OUTPUT DEADTIME AS A FUNCTION OF TIMING CAPACITOR C_T

A plot of output deadtime versus C_T for two values of R_T is given in Figure 7.

Although timing capacitors as small as 100pF can be used successfully in low noise environments, it is generally recommended that C_T be kept above 1000pF to minimize noise effects on the oscillator frequency (see Section 4.0).

Synchronization of one or more devices to either an external time base or another UC1846 is accomplished via the bi-directional SYNC pin. To synchronize devices, first, C_T must be grounded to disable the internal oscillator on all slaved devices. Second, an external synchronization pulse must be applied to the SYNC terminal. This pulse can come directly from the SYNC terminal of a master UC1846 or, alternatively, from an external time base as shown in Figure 8.

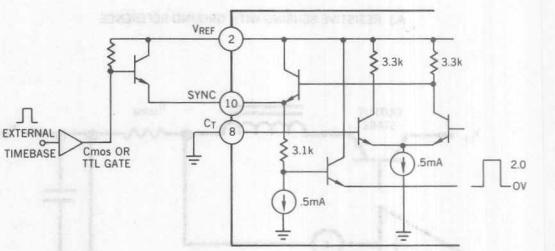


FIGURE 8. SYNCHRONIZING THE 1846 TO AN EXTERNAL TIME BASE

3.3 Current Limit

One of the most attractive features of a current-mode converter is its ability to limit peak switch currents on a pulse-by-pulse basis by simply limiting the error voltage to a maximum value. Referring to Figure 9, peak current limiting in the UC1846 is accomplished using a divider network, R_1 and R_2, to set a pre-determined voltage at pin 1.

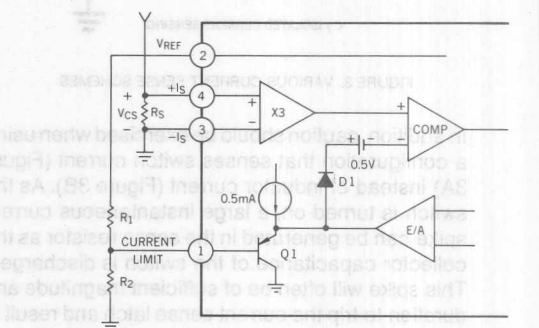


FIGURE 9. PEAK CURRENT LIMIT SET UP

This voltage, in conjunction with Q_1, acts to clamp the output of the error amplifier at a maximum value. Since the base emitter drop of Q_1 and the forward drop of diode D_1 very nearly cancel, the negative input of the comparator will be clamped at the value $V_{PIN\ 1}$ −0.5V. Following this through to the input of the current sense amplifier yields:

$$V_{cs} = \frac{V_{PIN\ 1} - 0.5}{3} \quad (4)$$

Where V_{cs} is the differential input voltage of the current sense amplifier. Using this relationship, a value for maximum switch current in terms of external programming resistors can be derived, resulting in:

$$I_{CL} = \frac{\frac{R_2\ (V_{REF})}{R_1 + R_2} - 0.5}{3R_S} \quad (5)$$

While still on the subject of resistor selection, it should be pointed out that R_1 also supplies holding current for the shutdown circuit, and therefore should be selected prior to selecting R_2 as outlined in the next section.

One last word on the current limit circuit. As may be seen from equation 5, any signal less than 0.5V at the current limit input will guarantee both outputs to be off, making pin 1 a convenient point for both shutting down and slow starting the PWM circuit. For example, both the under-voltage lockout and shutdown functions are connected internally to this point. If a capacitor is used to hold pin 1 low (Figure 10) then as the input voltage increases above the under-voltage lockout level, the capacitor will charge and gradually increase the PWM duty cycle to its operating point. In a similar manner if the shutdown amplifier is pulsed, the shutdown SCR will be fired and the capacitor discharged, guaranteeing a shutdown and soft restart cycle independent of input pulse width.

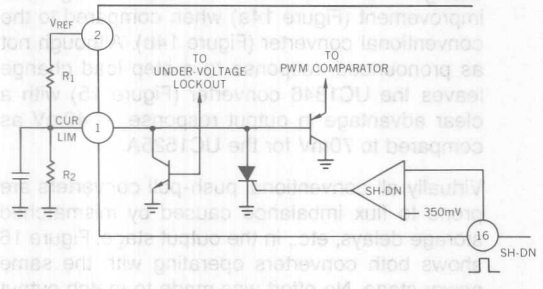


FIGURE 10. USING UNDER-VOLTAGE LOCKOUT AND SHUTDOWN TO INITIATE A SLOW START.

3.4 Shutdown

The shutdown circuit, shown in Figure 11, was designed to provide a fast acting general purpose shutdown port for use in implementing both protection circuitry and remote shutdown functions. The circuit may be divided into an input section consisting of a comparator with a 350mV temperature compensated offset, and an output section consisting of a three transistor latch. Shutdown is accomplished by applying a signal greater than 350mV to pin 16, causing the output latch to fire, and setting the PWM latch to provide an immediate signal to the outputs. At this point, several things can happen. Q_1 requires a minimum holding current, I_H, of approximately 1.5mA to remain in the latched state. Therefore, if R_1 is chosen greater than 5kΩ, Q_1 will discharge any capacitance, C_S, on pin 1 to ground and commutate the output latch, allowing C_S to recharge. If R_1 is chosen less than 2.5kΩ, Q_1 will discharge C_S and remain in the latched state until power is externally cycled off. In either case, C_S is required only if a soft-start or soft-restart function is desired.

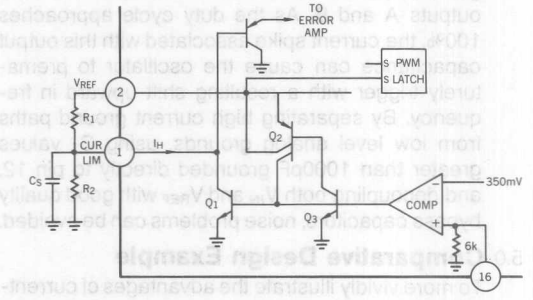


FIGURE 11. SHUTDOWN CIRCUITRY

For example, the shutdown circuit of Figure 12, operating in a nonlatched mode, will protect the supply from overcurrent fault conditions. Many times, if the output of a supply is shorted, circulating currents in the output inductor will build to dangerous levels. Pulse-by-pulse current limiting with its inherent time delay, will in general not be able to limit these currents to acceptable levels. Figure 12 details a circuit which will provide shutdown and soft-restart if the overcurrent threshold set by R_3 and R_4 is exceeded. This level should be greater than the peak current limit value determined by R_1 and R_2 (see equation 5). Sometimes called a "hiccup mode", this overcurrent function will limit both power and peak current in the output stages until the fault is removed.

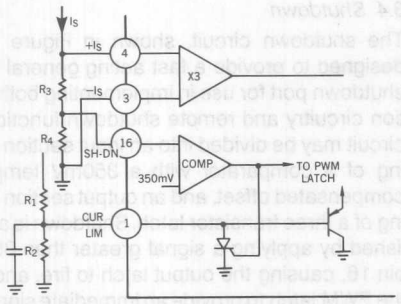


FIGURE 12. OVER CURRENT SENSING WITH THE SHUTDOWN CIRCUIT PRODUCES A SHUTDOWN — SOFT RESTART CYCLE TO PROTECT OUTPUT DRIVERS

4.0 Noise Immunity

As in all PWM circuits, some simple precautions should be observed to prevent switching noise from prematurely triggering the oscillator as it approaches its upper threshold. This is most evident when large capacitive loads — such as the gates of power FETS — are directly driven from outputs A and B. As the duty cycle approaches 100%, the current spike associated with this output capacitance can cause the oscillator to prematurely trigger with a resulting shift upward in frequency. By separating high current ground paths from low level analog grounds, using C_T values greater than 1000pF grounded directly to pin 12, and decoupling both V_{IN} and V_{REF} with good quality bypass capacitors, noise problems can be avoided.

5.0 Comparative Design Example

To more vividly illustrate the advantages of current-mode control, a relatively simple push-pull forward converter was designed using two interchangeable control sections, as shown in Figure 13. The control modules consist of (a) a UC1846 current-mode controller with associated circuitry, and (b) a conventional UC1525A PWM controller with its support circuitry. Loop compensation of the UC1525A was implemented by placing a zero in the feedback loop to cancel one of the poles in the output stage, resulting in a unity gain bandwidth of approximately 3kHz — a commonly used technique. Compensating the current-mode converter requires somewhat of a different approach. Since the output stage contains only a single pole, in theory closing the loop will produce a stable system with no additional compensation. In practice, however, it has been shown that subharmonic oscillation will result from excess gain at half the switching frequency[5]. Therefore, a pole-zero combination has been placed in the feedback loop to reduce high frequency gain and allow the output capacitor (low ESR) to roll off loop gain to 0dB at 3kHz.

While not demonstrated in Figure 13, fixed frequency current-mode converters are known to be unstable above 50% duty cycle without some form of slope compensation[4–6]. By injecting a small current from the sawtooth oscillator into the positive terminal of the current sense amplifier, slope compensation is accomplished, and the converter can be operated in excess of 50% duty cycle. An alternate, but just as effective, scheme would be to inject the signal into the negative terminal of the error amplifier.

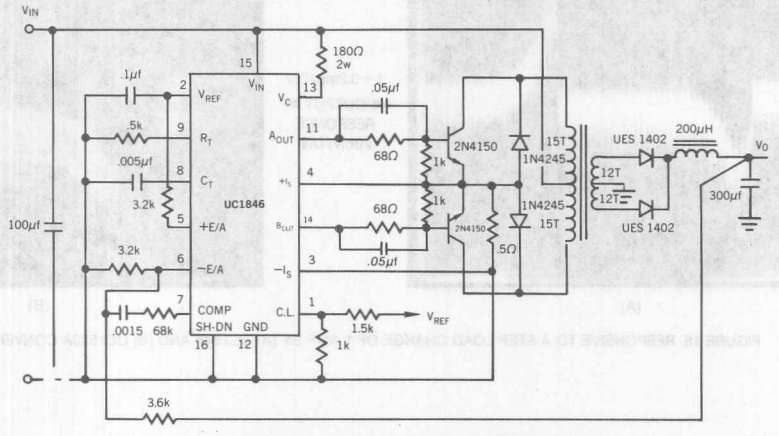
As may be seen, a similar parts count for both supplies was encountered. Topologically, using the UC1525A shutdown terminal provided only a crude current limit in contrast to the UC1846. Furthermore, internal double pulse suppression circuitry of the UC1846 gave an added level of protection against core saturation — important if your regulator is prone to subharmonic oscillations. Since both regulators were over-designed to withstand a short circuit on the output with resultant high peak currents, the shutdown-restart mode of the UC1846 was not used.

It should be pointed out at this time that one of the main features of a current-mode converter of this type is its ability to be paralleled with similar units. By disabling the oscillator and error amplifiers (C_T grounded, +E/A to V_{REF}, −E/A grounded) of one or more slave modules, and connecting SYNC and COMP pins of the slave(s) respectively, the outputs may be connected together to provide a modular approach to power supply design.

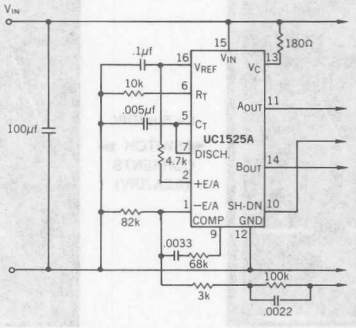
Starting with Figure 14, a comparison of line and load step responses is made between the two converters. As a result of the feed-forward effect of the current-mode converter, response to a step input change shows more than an order of magnitude improvement (Figure 14a) when compared to the conventional converter (Figure 14b). Although not as pronounced, response to a step load change leaves the UC1846 converter (Figure 15) with a clear advantage in output response — 40mV as compared to 70mV for the UC1525A.

Virtually all conventional push-pull converters are prone to flux imbalance caused by mismatched storage delays, etc., in the output stage. Figure 16 shows both converters operating with the same power stage. No effort was made to match output devices. As may be seen, there is little noticeable

difference between switch currents of the UC1846. However, the UC1525A — with identical output transistors — shows phase B driving the core close to saturation with 50% more current than phase A.

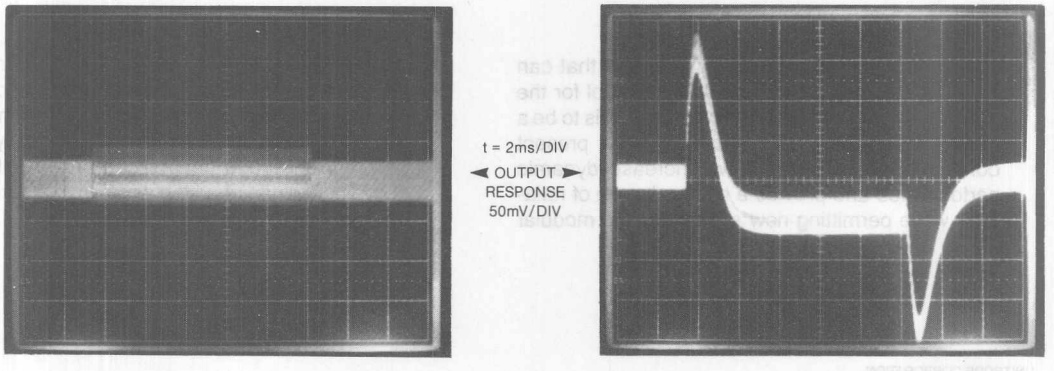


(A) UC1846 CURRENT-MODE CONTROLLED REGULATOR



(B) UC1525A VOLTAGE MODE CONTROLLER

FIGURE 13. PUSH-PULL FORWARD CONVERTER WITH (A) CURRENT-MODE CONTROL AND (B) VOLTAGE MODE CONTROL



(A) (B)

FIGURE 14. RESPONSE TO A STEP INPUT CHANGE OF 25 TO 35V BY (A) UC1846 and (B) UC1525A CONVERTERS

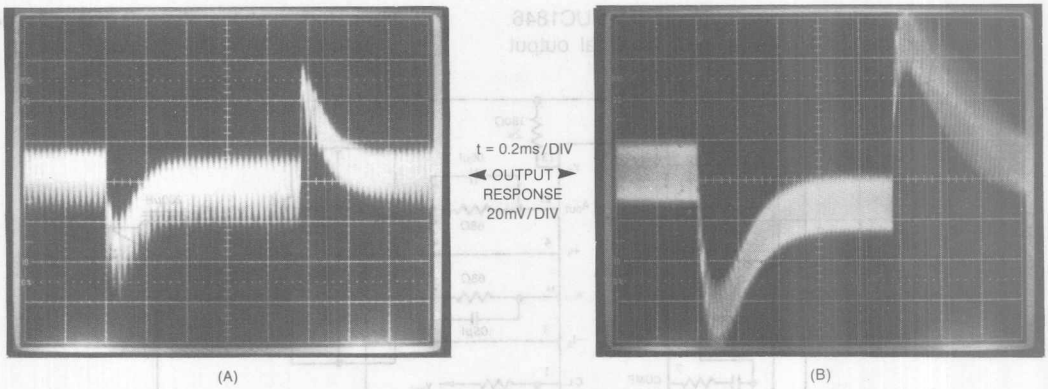


FIGURE 15. RESPONSIVE TO A STEP LOAD CHANGE OF 1 AMP BY (A) UC1846 AND (B) UC1525A CONVERTERS

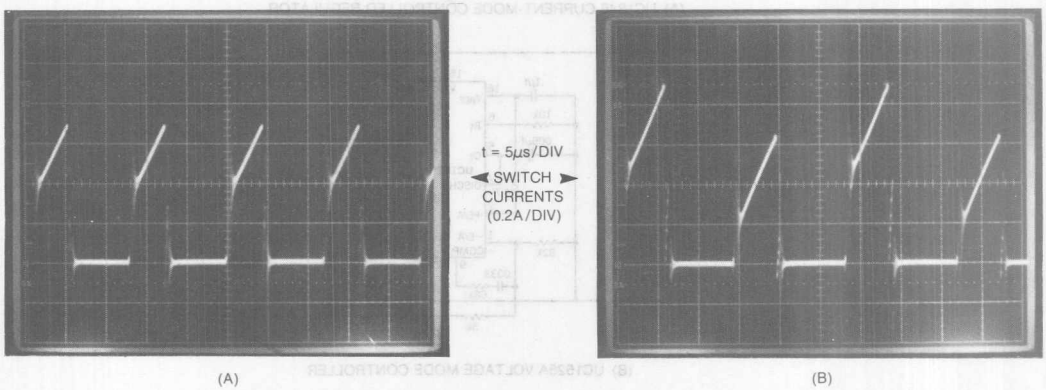


FIGURE 16. SWITCH CURRENTS SHOWING FLUX IMBALANCE IN (A) UC1846 AND (B) UC1525A CONVERTERS

6.0 Conclusion

Rarely do new design techniques evolve that can promise as much as current-mode control for the power supply engineer. We have shown this to be a simple technique easily extended from present converter topologies, that will increase dynamic performance and provide a higher degree of reliability while permitting new approaches to modular design. Until recently, current-mode converters could not compete with the economics of conventional converters designed with I.C. controllers. Now, with the UC1846 designed specifically for this task, current-mode control can provide all of the above performance advantages on a cost competitive basis.

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UNITRODE
APPLICATION NOTE

THE UC1901 SIMPLIFIES THE PROBLEM OF ISOLATED FEEDBACK IN SWITCHING REGULATORS

1. Introduction

The UC1901 simplifies the task of closing the feedback loop in isolated, primary-side control, switching regulators by combining a precision reference and error amplifier with a complete amplitude modulation system. Using the IC's amplitude modulated output, loop error signals can be transformer coupled across high voltage isolation boundaries, providing stable and repeatable closed-loop characteristics. Coupling across an isolation boundary is nothing new in transformer technology, and the UC1901's ability to generate carrier frequencies of up to 5MHz keeps the transformer size and cost at a minimum. With a secondary reference and accurate coupling path for the feedback signal, isolated off-line supplies can reliably achieve the tolerances, regulation, and transient performance of their non-isolated counter parts and still take advantage of the benefits of primary-side control.

Closing a feedback loop in a simple or complex system requires a thorough understanding of all of the loop elements. Worse case variations of each element must be taken into account when loop stability, dynamic response, and operating point are determined. Unpredictability in any of the loop components will affect the overall design by making it, necessarily, more conservative. The transient response of a control loop, for example, will usually suffer if a loop must be heavily compensated to guarantee stability with component variations.

To obtain high levels of load and line regulation, the output voltage of a power supply must be sensed and compared to an accurate reference voltage. Any error voltage must be amplified and fed back to the supply's control circuitry where the sensed error can be corrected. In an isolated supply, the control circuitry is frequently located on the primary, or line, side of the supply. As shown in Figure 1, the feedback signal in this type of supply must cross the isolation boundary. Coupling this signal requires an element that will withstand the isolation potentials and still transfer the loop error signal. Though some significant drawbacks to their use exist, optical couplers are widely used for this function due to their ability to couple DC signals. Primarily, optocouplers suffer from poor initial tolerance and stability. The gain, or current transfer ratio, through an opto-coupler is loosely specified and changes as a function of time and temperature. This variation will directly affect the overall loop gain of the system, making loop analysis more difficult and the resulting design more conservative. In addition, limited bandwidth capability prevents the use of optical couplers when an extended loop response is required.

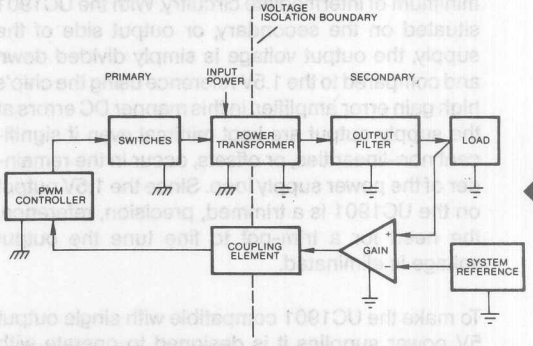


FIGURE 1: A Typical Closed-Loop Isolated Power Supply With Primary-Side Control.

With reliability firmly situated as an important aspect of electrical design, the benefits of primary-side control are increasingly attractive in off-line designs. The organization of an off-line switcher with primary-side control (See Figure 1) puts the control function on the same side of the isolation boundary as the switching elements. Not only does this simplify the interface between the controller and switches, it makes the protection of these switches much easier. Sensing of the switch currents and voltage can avoid failures and improve over-all supply performance. The argument for primary-side control has been further strengthened by the introduction of a new generation of control IC's. The controllers incorporate such features as low current start-up, high speed current sensing for pulse-by-pulse current limiting, and voltage feed-forward. Low current start-up alleviates the problem of efficiently supplying power to a line-side controller, while fast current limit circuitry and voltage feed-forward take advantage of the proximity of a primary-side controller to both the power switch(es) and the input supply voltage.

Combining all of the necessary functions to generate an AM feedback signal on the UC1901 make it the

first IC of its type. As will be seen, the UC1901 can be used in several modes to take full advantage of its functions. Recognizing the continuing evolution of power converter technology the UC1901 is intended to simplify the design of a new era of reliable and higher performance power converters.

2. The UC1901 Functions

The operation of the UC1901 is best undestood by considering a typical application. In Figure 2, the UC1901 is shown providing the feedback signal to close the loop in an isolated switching power supply. With any feedback system it is desirable to compare the system output to the system reference with a minimum of intermediate circuitry. With the UC1901 situated on the secondary, or output side of the supply, the output voltage is simply divided down and compared to the 1.5V reference using the chip's high gain error amplifier. In this manner DC errors at the supply output are kept minimal even if significant non-linearities, or offsets, occur in the remainder of the power supply loop. Since the 1.5V output on the UC1901 is a trimmed, precision, reference, the need for a trim-pot to fine tune the output voltage is eliminated.

To make the UC1901 compatible with single output 5V power supplies it is designed to operate with input voltages as low as 4.5V. This allows the part to be powered directly from a TTL compatible 5V output. A nominal supply current of only 5mA allows the part to be easily operated at its maximum input voltage rating of 40V without worry of excessive power dissipation.

The amplified error signal at the UC1901's compensation output is internally inverted and applied to the modulator. The other input to the modulator is the carrier signal from the oscillator. The modulator combines these two signals to produce a square wave output signal with an amplitude that is directly proportional to the error signal and whose frequency is that of the oscillator input. This output is buffered and applied to the coupling transformer. With the internal oscillator, carrier frequencies into the megahertz range can be generated. Operating at high frequencies can reduce both the size and cost of the coupling transformer. The secondary winding on the coupling transformer drives a diode-capacitor peak detector. With a simple resistive load to allow discharging of the holding capacitor an effective amplitude demodulator is formed. The small signal voltage gain from the error amplifier input to the detector output is a function of the feedback network around the error-amp, the modulator gain, the turns ratio of coupling transformer, and any loss in the demodulator.

In Figure 2 the relationship of the detector output to the sense supply voltage is non-inverting. This is necessary to guarantee start-up of the supply. Since the UC1901, as shown, is powered from the supply's output, the initial feedback signal back to the PWM controller will always be zero. The required 180° of DC phase shift is easily achieved by inverting the signal with the error amplifier that is present in most any PWM controller circuit.

In some applications it may be desirable to operate the carrier frequency of the UC1901 in synchroni-

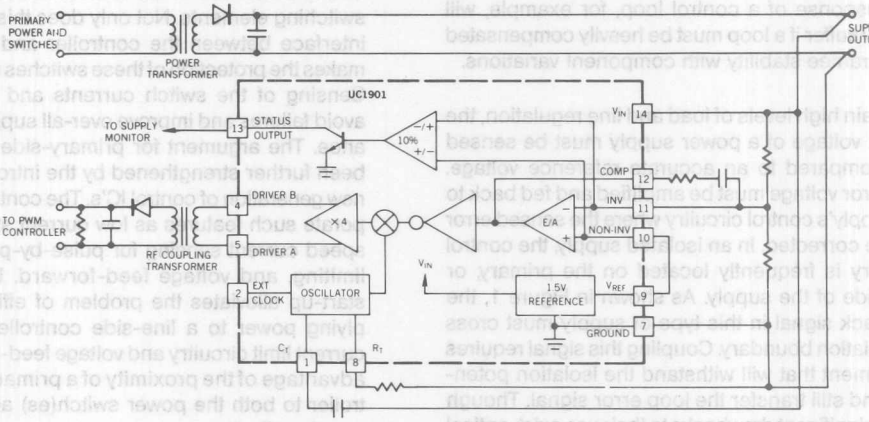


FIGURE 2: With a Precision Reference, and a Complete Amplitude Modulation System, the UC1901 Lets Isolated Feedback Loops be Closed Using a Small Signal Transformer.

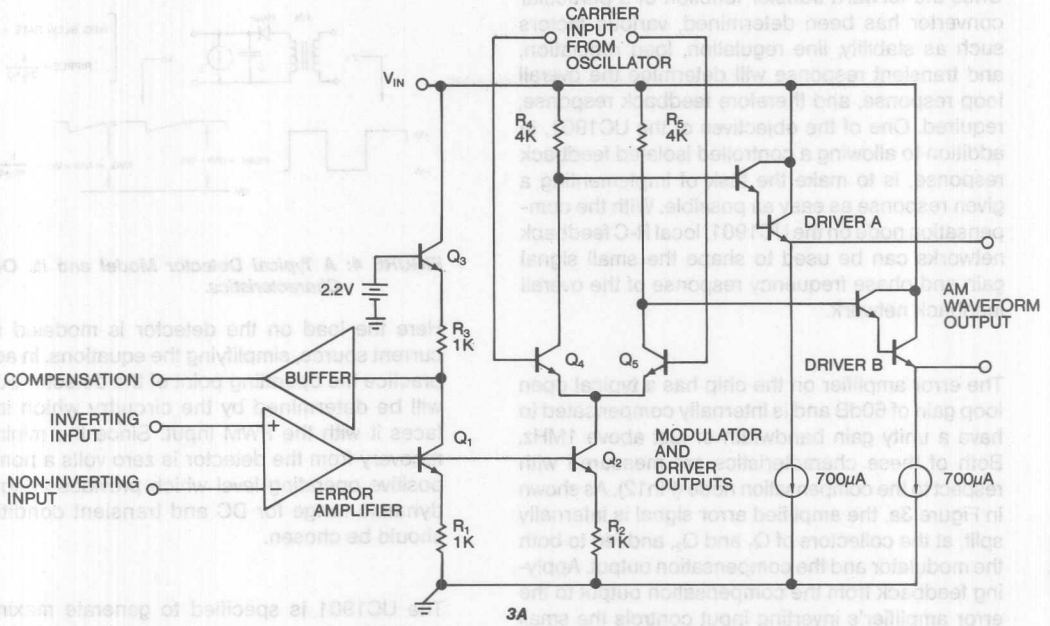


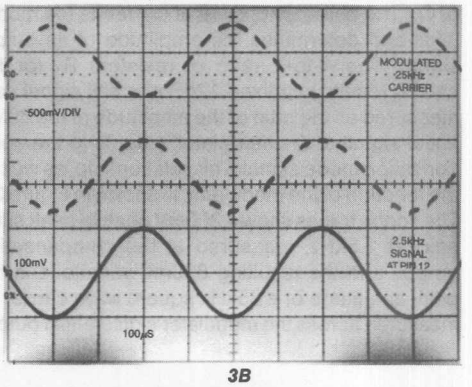
FIGURE 3: The Compensation Output on the UC1901 can be used to Accurately Control the AM Waveform Output. A Simplified Schematic, (a) Shows the internal Signal Split into the Modulator. Voltage Waveforms, (b) Across the Modulator Outputs, and at the Compensation Output show the Modulator Transfer Characteristic.

zation with a system clock, or reference frequency. In many situations, operation of the UC1901 at the switching frequency of the power supply can be beneficial. One such application is presented in this article. To accommodate this need the UC1901 has an external clock input.

One additional mode of operation is possible if the oscillator is left disabled and the external clock signal is kept low (or floated). In this condition the error amplifier can be used in a linear fashion with its output taken at the driver A output. The driver B output will be at a fixed DC voltage about 1.4V from the input supply voltage. If the external clock signal is tied high the roles of the two driver outputs are reversed. With 15mA of output current capacity, the two outputs can easily be combined to reference and drive an optical coupler. Although the instabilities of the coupler will still be present, the advantages of the UC1901's precision reference, high gain amplifier-driver, and 4.5V supply operation can be utilized.

3. A Controlled Feedback Response

There are many different topologies which can be used when implementing a switching power supply. For off-line supplies, fly-back and forward convert-



3B

ers are often designed. In the near future current-mode control versions of these may also be widely used. Each of these converter topologies has a different forward transfer characteristic and, within each type of converter, operating point, continuous or discontinuous inductor current, and voltage or current-mode duty cycle control are a few of the factors which can alter this characteristic. In short, the task of optimally designing a feedback network for one supply must usually be repeated when the next supply is designed.

Once the forward transfer function of a particular converter has been determined, various factors such as stability, line regulation, load regulation, and transient response will determine the overall loop response, and therefore feedback response, required. One of the objectives of the UC1901, in addition to allowing a controlled isolated feedback response, is to make the task of implementing a given response as easy as possible. With the compensation node on the UC1901, local R-C feedback networks can be used to shape the small signal gain and phase frequency response of the overall feedback network.

The error amplifier on the chip has a typical open loop gain of 60dB and is internally compensated to have a unity gain bandwidth of just above 1MHz. Both of these characteristics are measured with respect to the compensation node (Pin12). As shown in Figure 3a, the amplified error signal is internally split, at the collectors of Q_1 and Q_2, and fed to both the modulator and the compensation output. Applying feedback from the compensation output to the error amplifier's inverting input controls the small signal collector current through Q_1. Since Q_2 sees the same base voltage, and its emitter resistance is the same, its collector current will track that of Q_1. The collector current of Q_2 feeds the modulator and determines the amplitude of its output signal. The 4-to-1 ratio of resistors R_4 (or R_5) and R_2 results in a fixed 12dB of small signal gain measured as the ratio of the amplitude of the differential signal at the modulator outputs to the compensation mode signal. This relationship, as well as the function of the modulator, is shown in Figure 3b. The scope traces show a 200mV peak to peak sinusoid at 2.5kHz, measured at the compensation output, and the resulting 800mV variations in the peak amplitude of a 25kHz square wave carrier as measured across the modulator's differential output.

The remaining factors influencing the response of the feedback path are the signal gain through the transformer, the detector circuit, and the circuitry between the detector output and the supply's PWM. The signal gain through the transformer is simply the turns ratio of transformer. The small signal detector gain can usually be assumed to be unity as long as the AC load presented to the detector is kept small. Some load on the detector is necessary to allow its output to slew in a negative direction. Figure 4 summarizes the transfer and output characteristics of a typical transformer and detector.

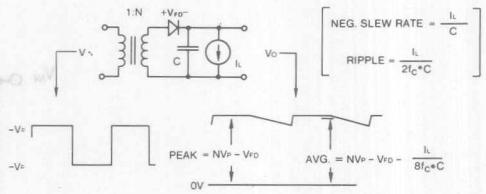


FIGURE 4: A Typical Detector Model and its Output Characteristics.

Here the load on the detector is modeled as a current source, simplifying the equations. In actual practice the operating point of the detector output will be determined by the circuitry which interfaces it with the PWM input. Since the minimum recovery from the detector is zero volts a nominal positive operating level which provides adequate dynamic range for DC and transient conditions should be chosen.

The UC1901 is specified to generate maximum carrier levels equal to or in excess of 1.6V peak. This indicates that a turns ratio of greater than one-to-one will be required for the coupling transformer if the detector output must exceed approximately 1V, (allowing for a detector diode drop of 0.6V). It should be noted that many switching power supplies now being designed include an integrated PWM control IC. A typical PWM IC includes a dedicated error amplifier which amplifies and buffers the input error voltage and applies it to the PWM ramp comparator. This amplifier can be readily used to fix a nominal detector operating point that is compatible with a one-to-one transformer. Additionally, the error amplifier on the UC1901 and the PWM's amplifier can be combined to achieve both large DC loop gains for improved load and line regulation, and the optimization of the loop gain and phase frequency response for improved transient and stability performance.

4. Transformer Requirements

The coupling transformer used with the UC1901 has two primary requirements. First, it must provide DC isolation. Secondly, it should transfer voltage information across the isolation boundary. Meeting the first requirement of DC isolation will depend on specific applications. In general, though, small signal transformers can be readily built to meet the isolation requirements of today's line-operated systems.

For the most stringent applications, E-type cores with bobbin carried windings are inexpensively available or built. Where small size is most important, a simple toroid core can be used.

The second requirement of the transformer primarily determines the amount of magnetizing inductance it must have. The magnetizing inductance of a transformer refers to the actual inductance formed by the windings around the core material. In many classical transformer examples, the magnetizing inductance is ignored. This is a valid approximation since, in these examples, the magnetizing current required is much less than the reflected load currents. In this case, the load currents are small and, as the transformer inductance is reduced, the magnetizing currents become dominant.

The driver outputs on the UC1901 are emitter followers which are biased at 700μA. Therefore, if the drivers are operated without additional bias current the peak current through the transformer's primary winding cannot exceed this value. Figure 5a illustrates the relationship of the magnetizing current to the voltage across the transformer's input. If the reflected load currents are neglected, it can be seen that the minimum magnetizing inductance required for linear transfer of the modulator square-wave is given by:

(1) $$L_M \geq \frac{V_P}{4f_c I_P}$$

Where: L_M = the magnetizing inductance,
V_P = the peak carrier voltage across transformer inputs,
f_C = the UC1901 operating frequency,
I_P = the bias current of the UC1901 drivers.

As an example, consider the case where Vp is equal to 2V, f_c is 100kHz, and the drivers are operating at their internal bias levels. Using equation 1, the inductance looking into the primary winding with no secondary load must be greater than 7.1mH. Alternatively, if the carrier frequency is raised to 1MHz and the bias levels of the UC1901 drivers are increased to 3.5mA, then L_M can be as low as 150μH. Using high permeability ferrite material, this level of magnetizing inductance can be realized with as little as 10 turns on a small toroid core.

Equation 1 sets a minimum limit on the magnetizing inductance for linear transfer of the carrier wave-

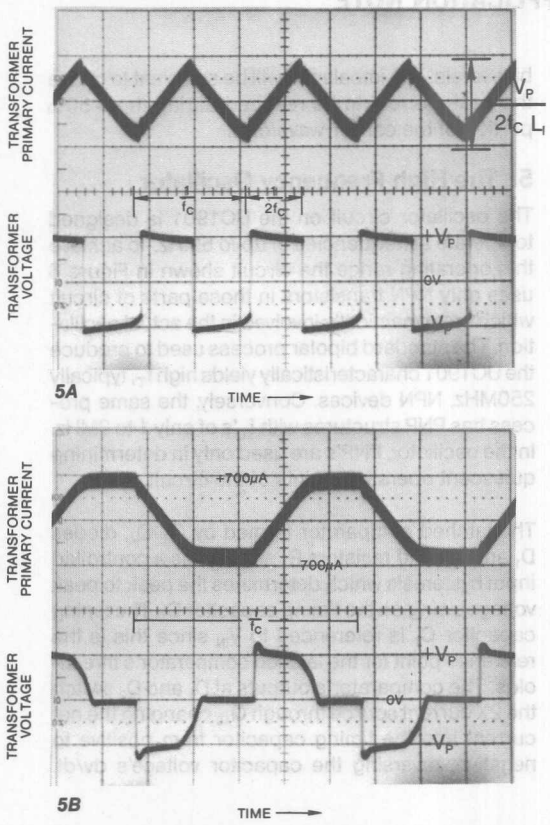


FIGURE 5: The UC1901 Driver Outputs Follow the Modulator Output Square Wave, (a.), Sourcing and Sinking Current Levels Dependent on Transformer Inductance, Carrier Frequency, and Voltage Level. When the Bias Level of the Driver Outputs, I_P, is Reached, (b.), a Tri-state Waveform is Coupled Across the Transformer, the Peak Voltage Level Though, Remains Approximately the Same. The Reflected Load Currents are Assumed Negligible.

form. Actually, the amplitude information is still coupled even when the inductance is less than this minimum. In this case, the UC1901 drivers will support the voltage across the coil until the peak current is reached. The result, illustrated in Figure 5b, is a tri-state waveform at the transformer's input and output. Peak detection of this waveform yields the same amplitude information as the linear transfer case, although detection ripple will increase. Another situation which results in a tri-state waveform exists when the carrier duty cycle is not 50%. In this case, the volt-seconds across the transformer will be balanced by an "imbalancing" of the driver

bias levels. The imbalance will be sufficient to cause the peak current to be reached during the > 50% portion of the carrier waveform.

5. The High Frequency Oscillator

The oscillator circuit on the UC1901 is designed to operate at frequencies of up to 5MHz. To achieve this operating range the circuit shown in Figure 6 uses only NPN transistors in those parts of circuit which are dynamically involved in the actual oscillation. The standard bipolar process used to produce the UC1901 characteristically yields high f_T, typically 250MHz, NPN devices. Conversely, the same process has PNP structures with f_T's of only 1 to 2MHz. In the oscillator, PNP's are used only in determining quiescent operating points of the circuit.

The latched comparator formed by Q_1-Q_4, diodes D_1 and D_2, and resistors R_1 and R_2 has a controlled input hysteresis which determines the peak to peak voltage swing on the timing capacitor C_T. The timing capacitor C_T is referenced to V_{IN} since this is the reference point for the latched comparator's thresholds. The comparator's outputs at D_1 and D_2 switch the 2X current source through Q_{10} changing the net current into the timing capacitor from positive to negative, reversing the capacitor voltage's dv/dt. When the resulting ramp reaches the comparator's lower threshold, the current is switched back to Q_{11} and the ramp reverses until the upper threshold is reached and the process begins again. This results in a triangle waveform at C_T and a squarewave signal at D_1 and D_2.

The magnitude of the charging current is controlled by the external resistor, R_T and the internally generated voltage across it. This voltage is compensated to track variations in the comparator hysteresis. The tracking characteristics of this voltage stabilize the oscillation frequency over temperature and enhance the initial frequency tolerance. Typically, repeatability and temperature stability of the operating frequency are both better than 5%.

The oscillator circuit has been optimized for a nominal R_T of 10kΩ. A desired operating frequency is obtained by choosing the correct value for C_T. As shown in Figure 7, the oscillator frequency is give by the relation:

$$(2) \qquad fosc. = \frac{1.24}{R_T C_T},$$

for frequencies below 500kHz. Above 500kHz, the solid line indicates appropriate C_T values. There is

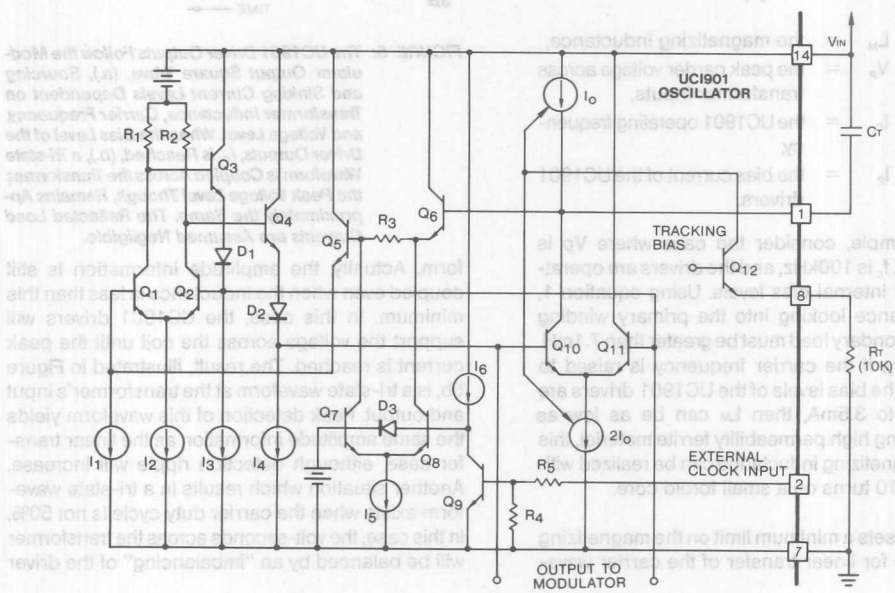


FIGURE 6: UC1901 High Frequency Oscillator Simplified Schematic.

no upper limit on the size of the capacitor used, thus allowing the oscillator to have an arbitrarily long period if desired.

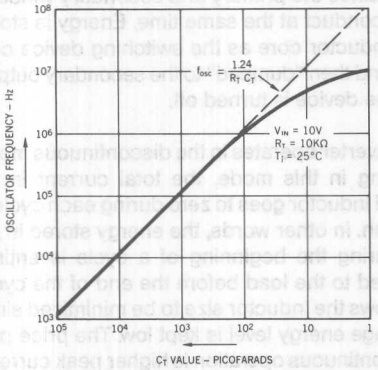


FIGURE 7: UC1901 Oscillator Frequency.

To allow operation of the modulator with a carrier frequency that is driven from a system operating frequency or clock, the oscillator can be over-ridden. Tying C_T to the input supply voltage disables the oscillator. The modulator circuit can now be switched in synchronization with a signal at the external clock input. Internally, the clock signal is applied to the latched comparator via the input device Q_9, and the differential pair Q_7 and Q_8. As the clock input goes high, Q_9 turns Q_8 off and Q_7 on, creating an offset across R_3 that is sufficient to switch the comparator. The comparator then, as before, drives the modulator. When the clock input returns low, the process is reversed. Using the external clock input, both the frequency and duty cycle of the modulator outputs are controlled.

6. A Status Output is More Than Just a Green Light

Many systems today require a monitoring function on the supply output. The status output on the UC1901 can fill this need, a green light function, and can also be used to fill some more "sophisticated" needs. The circuit in Figure 8 takes advantage of the status output in the start-up of an off-line forward converter. The UC1901 is being used in an application where the switching supply must be synchronized to a system clock. The clock signal is generated on the secondary or output side of the supply. To allow start-up, the PWM oscillator is free-running when the line voltage is applied. As the supply voltage rises, the UC1901's external clock input is driven at the switching frequency rate through resistors R_1 and R_2. When the supply output

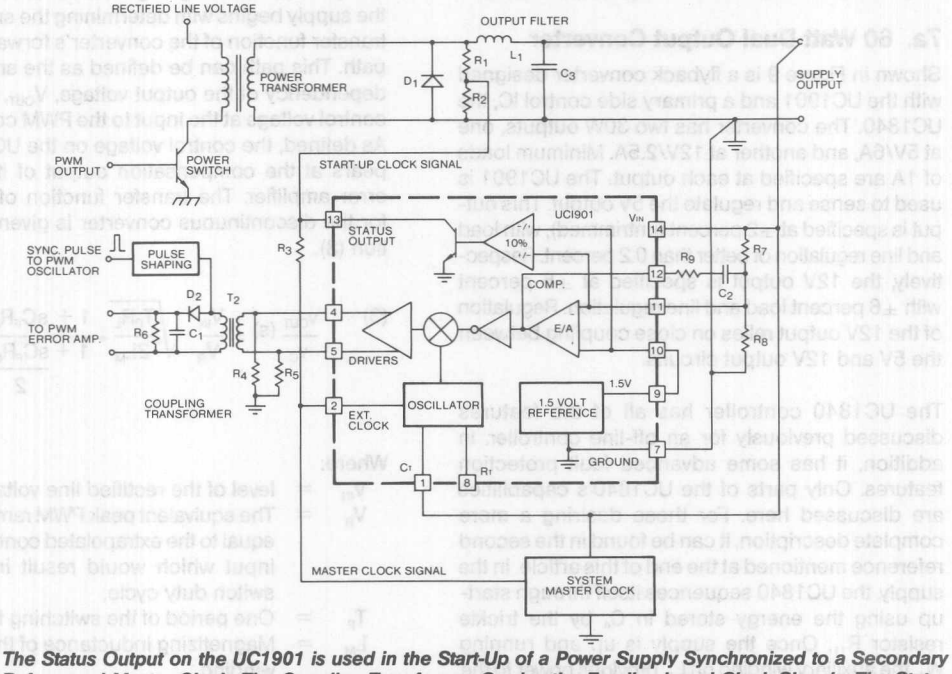


FIGURE 8: The Status Output on the UC1901 is used in the Start-Up of a Power Supply Synchronized to a Secondary Referenced Master Clock. The Coupling Transformer Carries the Feedback and Clock Signals. The Status Output is used to Sequence Clock Signals to the UC1901 External Clock Input During Start-Up.

reaches 90% of its operating level, the status output decouples the external clock input from the switcher and enables the UC1901's clock input to be driven from the now operational system clock.

On the primary side, the output of the coupling transformer is used before demodulation to provide a synchronization pulse to the PWM control oscillator. Under normal operation, the entire power supply, including the feedback system, will be synchronized to the system clock.

7. The UC1901 in an Off Line Flyback Converter

As alluded to previously, flyback converters see wide use in off-line applications. The flyback topology has some general cost benefits which have spurred its use in low cost, low power (<150W), off-line systems. Perhaps the two most significant of which are the need for only a single power magnetic element in the supply (no output filter inductor is required), and the ability to easily obtain multi-output systems by adding one additional winding to the coupling power inductor for each extra output. Also, the flyback topology, especially when used in the discontinuous mode, lends itself very well to the benefits of voltage feed-forward.

7a. 60 Watt Dual Output Converter

Shown in Figure 9 is a flyback converter designed with the UC1901 and a primary side control IC, the UC1840. The converter has two 30W outputs, one at 5V/6A, and another at 12V/2.5A. Minimum loads of 1A are specified at each output. The UC1901 is used to sense and regulate the 5V output. This output is specified at ±2 percent (untrimmed), with load and line regulation of better than 0.2 percent. Respectively, the 12V output is specified at ±5 percent with ±6 percent load and line regulation. Regulation of the 12V output relies on close coupling between the 5V and 12V output circuits.

The UC1840 controller has all of the features discussed previously for an off-line controller. In addition, it has some advanced fault protection features. Only parts of the UC1840's capabilities are discussed here. For those desiring a more complete description, it can be found in the second reference mentioned at the end of this article. In the supply, the UC1840 sequences itself through start-up using the energy stored in C_4 by the trickle resistor R_{11}. Once the supply is up and running W_4, the auxiliary winding on L_1, provides power to the controller and the switch drive circuitry. The primary winding on the coupled inductor, W_1 is applied across the rectified and filtered line voltage at a 60kHz rate via the FET switching device. L_1 is referred to as a coupled inductor, rather than as a transformer, since the primary and secondary windings do not conduct at the same time. Energy is stored in the inductor core as the switching device conducts, and then "dumped" to the secondary outputs when the device is turned off.

The converter operates in the discontinuous mode. Operating in this mode, the total current in the coupled inductor goes to zero during each cycle of operation. In other words, the energy stored in the core during the beginning of a cycle is entirely expended to the load before the end of the cycle. This allows the inductor size to be minimized since its average energy level is kept low. The price paid for discontinuous operation is higher peak currents in the switching and rectifying devices. Also, high ripple currents at the supply's output(s) make ESR, (equivalent series resistance), requirements on the output filter capacitors more stringent.

7b. Discontinuous Flyback's Forward Transfer Function

The process of designing a feedback network for the supply begins with determining the small signal transfer function of the converter's forward control path. This path can be defined as the small signal dependency of the output voltage, V_{OUT}, to, V_C, the control voltage at the input to the PWM comparator. As defined, the control voltage on the UC1840 appears at the compensation output of its internal error amplifier. The transfer function of this path for the discontinuous converter is given by equation (3).

$$(3)\quad \frac{v_{OUT}}{v_C}(s) = \frac{V_{IN}}{V_R}\sqrt{\frac{T_P R_L}{2L_M}} \cdot \frac{1 + sC_F R_S}{1 + \frac{sC_F R_L}{2}}$$

Where:

V_{IN} = level of the rectified line voltage,

V_R = The equivalent peak PWM ramp voltage-equal to the extrapolated control voltage input which would result in a 100% switch duty cycle,

T_P = One period of the switching frequency,

L_M = Magnetizing inductance of the primary winding,

C_F = A total effective output filter capacitor,

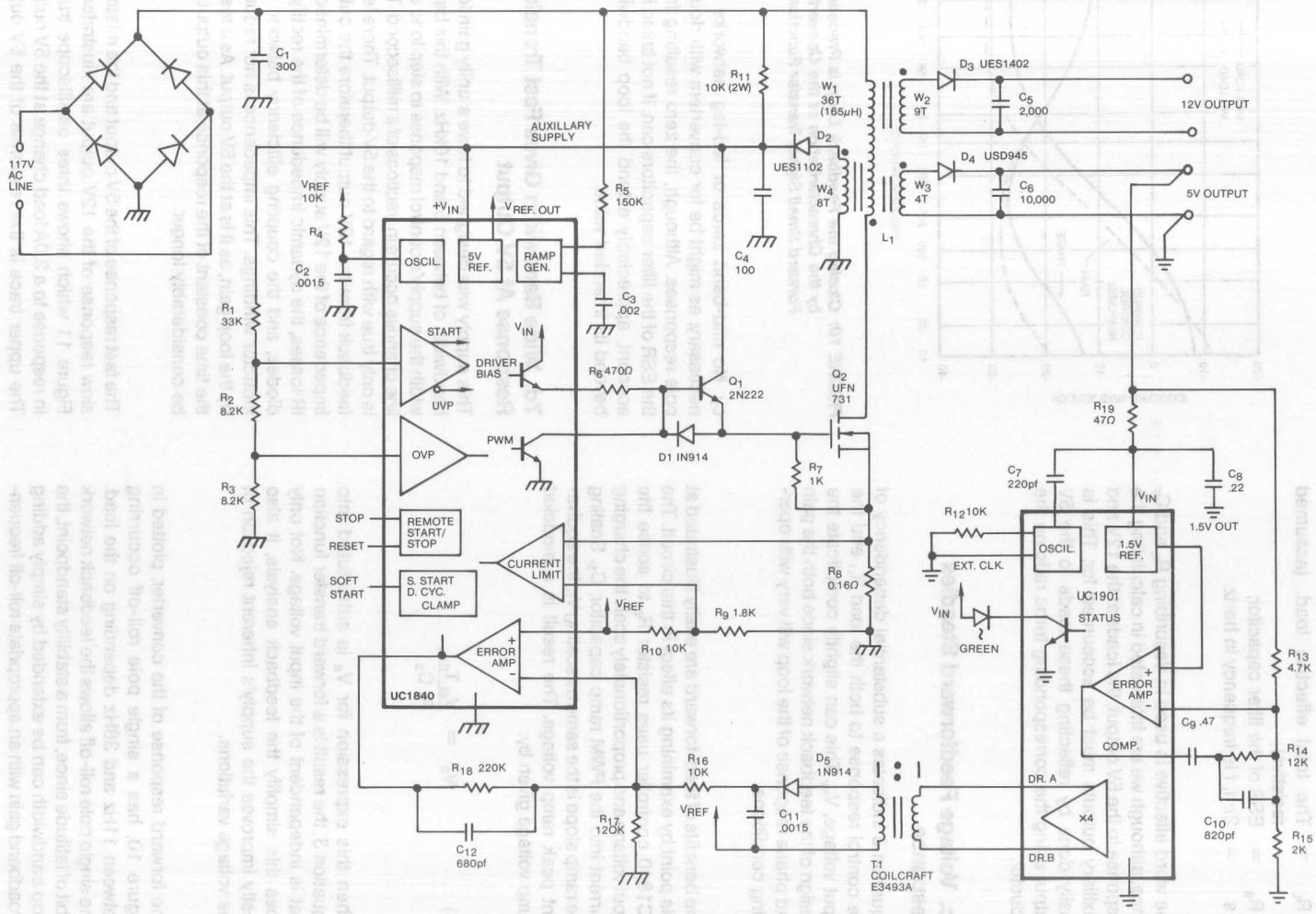


FIGURE 9: The UC1901 Combines With an Advanced PWM Controller in a 60W Off-Line Converter.

R_L = The total effective load, (assumed resistive),
R_S = ESR of the filter capacitor,
s = $2\pi jf$, f is frequency in hertz.

The word effective is used in describing R_L and C_F since, although we are interested in calculating the response to the 5V output, the loads at the 12V and auxiliary outputs must be accounted for. This is easily done by reflecting these loads to the 5V output using the corresponding turns ratio on the inductor.

7c. Voltage Feedforward Steadies Response

Equation 3 indicates a substantial dependency of the control response to both the load R_L, and the input voltage, V_{IN}. This can slightly complicate the design of the feedback network since both the gain and phase response of the loop will vary with operating conditions.

The benefits of feed-forward are easily illustrated at this point by examining its effect in this circuit. The UC1840 controller uses resistor R_5 to sense the input voltage and proportionately scale the charging current into the PWM ramp capacitor, C_3. Scaling the ramp slope is the same as scaling V_R, the equivalent peak ramp voltage. The result is a modeled ramp voltage given by:

$$(4) \qquad V_R = \frac{V_{IN}\, T_P}{R_5\, C_3}$$

When this expression for V_R is substituted into equation 3, the result is a forward transfer function that is independent of the input voltage. Not only does this simplify the feedback analysis, it also vastly improves the supply's inherent rejection of line voltage variations.

The forward response of the converter, plotted in Figure 10, has a single pole roll-off occurring between 11Hz and 38Hz depending on the load. The single pole roll-off allows the feedback network a bit of latitude since, from a stability standpoint, the loop bandwidth can be extended by simply adding broadband gain with an appropriate roll-off frequency. No mid-band zeros or led-lag networks are necessary, as might be for converters with double pole responses. Although, the zero resulting from the ESR of the filter capacitors can, if not taken into account, appreciably extend the loop bandwidth beyond its intended value.

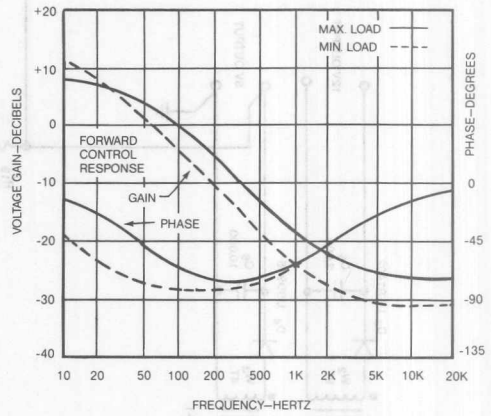


FIGURE 10: Closing the Feedback Loop is Preceeded by the Characterization of the Converter's Forward Small Signal Transfer Function.

7d. Wide Bandwidth Gives Fast Transient Response At 5V Output

This supply was designed to have a unity gain loop bandwidth of between 5 and 10kHz. With this bandwidth the supply's control response to step load and line changes occurs in fractions of a millisecond. This is only true with regard to the 5V output. There is no feedback from the 12V output therefore the output impedence of the 12V supply will be determined by IR losses, the dynamic impedence of the rectifying diodes, and the coupling efficiency between the inductor windings. This impedence is not reduced by the loop gain, as it is at the 5V output. As a result, the time constant of the response at this output will be considerably longer.

The fast response of the 5V output and the relatively slow response of the 12V output are illustrated in Figure 11 which shows three oscilliscope traces in response to a 3.0A load change at the 5V output. The upper trace is the response of the 5V output

which has been expanded and lowpass (< 15kHz) filtered slightly so the small signal loop characteristics can be seen. The trace below this is the 12V output's deviation due to cross-regulation limitations, the longer time constants involved are obvious. Both the fast response of the 5V loop, and the longer settling time of the 12V output are apparent in the third trace. This trace is the fed back correction signal at the UC1840's error amplifier output. From the middle trace the output impedence of the 12V supply can be estimated by noting the approximate 1ms time constant and dividing it by the 2000μF value of the 12V output filter capacitor. This gives a value of 0.5Ω for the output impedence. This agrees well with actual measurements of the 12V output's load regulation.

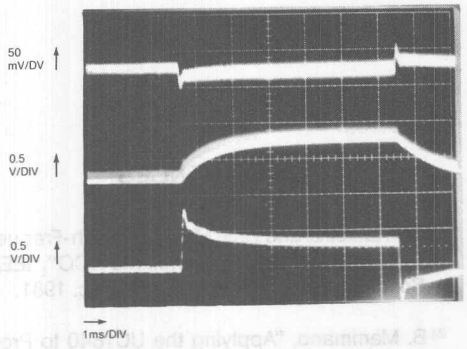


FIGURE 11: The Transient Response of the 5V Output (Top Trace), to a 3.0A Step Load Change Reflects the Extended Bandwidth of the 5V Loop. The Open-Loop 12V Output (Middle), Responds to the Effects of Cross Regulation. The Feedback Error Signal (Lower) Coupled Through the UC1901 is Measured at the UC1840 Error Amp. Output.

7e. The Feedback Response

Plotted in Figure 12 is the response of the feedback network. Also plotted are the asymptotic gain lines of the two contributing gain blocks, the UC1901 response (from 5V output to detector output) and the UC1840 error amp response (detector output to the PWM control voltage). The UC1901's error amplifier is run open loop at DC but is quickly rolled off to 8dB. With the 12dB of modulator gain, the UC1901 feedback system has a broadband gain of 20dB. A pole at 16kHz is added to reduce the gain through the UC1901 error amplifier at the 60kHz switching frequency. As mentioned earlier, excessive gain at the switching frequency can "use up" the dynamic range of the UC1901's AM output.

The UC1901 is operated with a carrier frequency of 500kHz. The coupling transformer, a Coilcraft E3493A, (double E core, bobbin wound construction), has a magnetizing inductance of 2.1mH. At 500kHz the peak current required to drive the primary winding is only 475μA per peak volt. The reflected load current is kept much smaller. This allows the transformer to be easily driven from the UC1901 driver outputs. The E3493A is widely used as a common mode line choke, and is rated for V.D.E. and U.L. isolation requirements. The transformer has a current rating of 2A, greatly exceeding the requirements of this application. Even though the device is larger than some alternatives, its availability and high volume pricing, as well as its isolation capability, make it a very suitable choice.

At the output of the transformer the diode-capacitor detector is referenced, along with the inverting input of the UC1840 error amplifier, to the UC1840's 5V reference. The operating point of the detector is fixed at 0.5V by the divider formed by R_{16} and R_{17} in Figure 9. This in turn sets the operating point of the carrier, with a detector diode drop of 0.5V, at about 1V peak. This level is reflected back through the one-to-one transformer to the UC1901 outputs. A 1V operating point is approximately at the center of the devices dynamic range.

The load current at the detector output is 50μA, set by the 0.5V operating level and R_{16}. The peak to peak detector ripple, at 500kHz, across the .0015μF holding capacitor is about 35mV. The gain through the UC1840 error amplifier at 500kHz is -26dB,

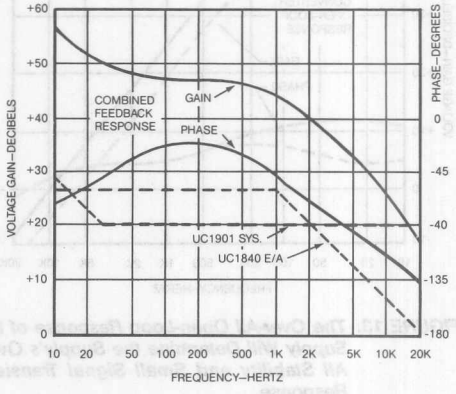


FIGURE 12: Local Feedback Around the UC1901 and 1840 Error Amplifiers is Used to Obtain the Desired Feedback Response.

attenuating the ripple to less than 2mV at the error amplifier output.

The response of the UC1840 error amplifier is flat out to 1kHz where the gain is rolled off to set the loop's 0db frequency. The DC gain is kept as high as possible, to fix the detector operating point, without actually having a series integrating capacitor in the feedback. If both the UC1901 and the UC1840 error amplifiers are run open loop at DC, with series R-C networks to set the AC gain, the total phase margin at low frequencies can become small or nonexistent. The result can be instability or, more likely, a peaked closed loop response that can increase the low frequency noise level of the supply.

The distribution of gain between the UC1901 and UC1840 error amplifiers is somewhat, although not entirely, arbitrary. Keeping the 500kHz ripple at the PWM comparator input below a certain level puts restrictions on the AC gain of the PWM's error amplifier. To much AC gain through the UC1901's amplifier can degrade the supply's transient response under large signal conditions. A suitable distribution for any application will, more than likely, be an iterative procedure. A simple computer or programmable calculator program can be a great tool when massaging these aspects of a design.

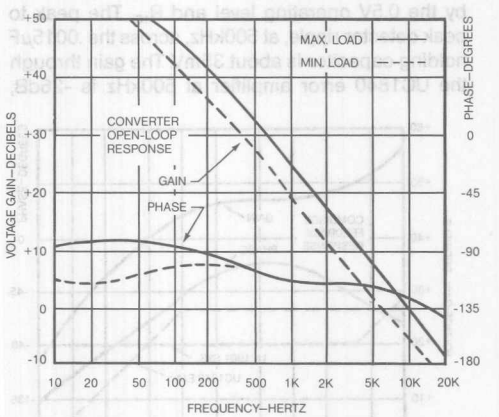


FIGURE 13: The Over-All Open-Loop Response of the Supply Will Determine the Supply's Over-All Stability and Small Signal Transient Response.

The overall open-loop responses, plotted in Figure 13, will not vary significantly except as indicated with load. The desired loop bandwidth has been achieved with an adequate phase margin of $> 50°$.

The result is a supply with very repeatable, as well as stable, operating characteristics. The same type of analysis for determining the required feedback response can be used in applying the UC1901 to any type of isolated closed loop supply. The choice of coupling transformer and carrier frequency used with the UC1901 should be based on individual system requirements.

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VERSATILE UC1834 OPTIMIZES LINEAR REGULATOR EFFICIENCY

Linear voltage regulators have long been an important resource to power supply designers. Three terminal, fixed-voltage linear regulators find extensive use as "spot" regulators and as post-regulation stages fed by switched-mode supplies. However, while inexpensive and simple to use, these devices have several performance limitations.

First, three terminal regulators are inefficient power converters. Power dissipation in a linear regulator is given by the relation:

$$P = I_O \cdot (V_{IN} - V_{OUT}).$$

Most monolithic regulators now available require an input-to-output voltage differential of at least 2 to 3V. This requirement can result in substantial inefficiency, particularly in low voltage supplies. As switched-mode power technology matures, power losses incurred in linear post-regulation stages are becoming more significant in terms of overall system efficiency.

Second, fixed-voltage regulators, with fixed maximum output currents, lack versatility. The use of these devices requires that OEMs maintain large, diverse inventories in order to support a broad range of power supply requirements.

Third, fixed three-terminal devices lack the capability of remote voltage sensing, and therefore can exhibit poor load regulation.

Finally, the most common failure mechanism for linear regulators is a shorted pass transistor. All critical loads, therefore, require over-voltage protection not provided by three-terminal regulators.

IMPROVED PERFORMANCE WITH UC1834

The UC1834 is a programmable linear regulator control IC which, with an external pass transistor, forms a complete linear power supply. This IC provides solutions to all the above-mentioned drawbacks of three-terminal devices.

Figure 1 shows the basic elements of positive and negative regulators implemented with the UC1834. An error amplifier monitors the output voltage and provides appropriate bias to the pass transistor (Q1) through a driver stage. This high-gain error amplifier (E/A) allows good dynamic regulation while allowing Q1 to operate near saturation in the common-emitter mode. The circuits can achieve high efficiency by maintaining output regulation with an input-to-output voltage differential as low as 0.5V (at 5A).

The UC1834 has both positive and negative reference voltage outputs, as well as a sink-or-source driver stage, as shown in Figure 1. These features allow implementation of either positive or negative regulators with this single IC, as shown. Output voltages from 1.5V to nearly 40V can be programmed by appropriate choice of remote sensing divider elements. Remote sensing also allows improved DC and dynamic load regulation.

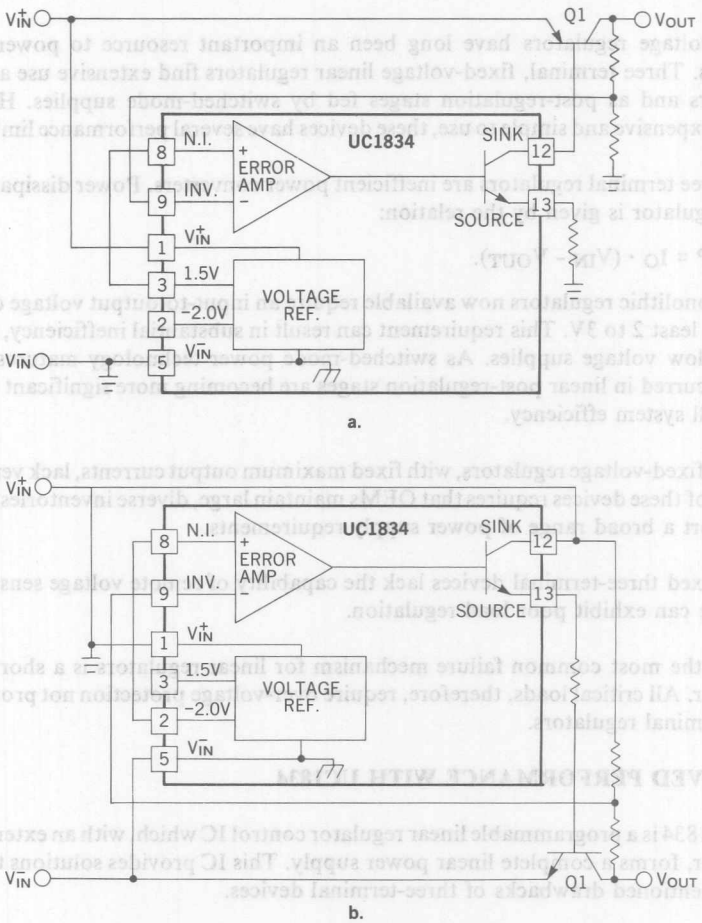


Figure 1. Basic Elements of (a.) Positive and (b.) Negative Regulators implemented with a UC1834

The UC1834 is intended to provide a complete linear regulation system. Therefore, many auxiliary features are included on this IC which eliminate the need for additional circuit elements. Figure 2 shows a more complete block diagram including on-chip provisions for current sensing, fault monitoring, remote voltage sensing, and thermal protection.

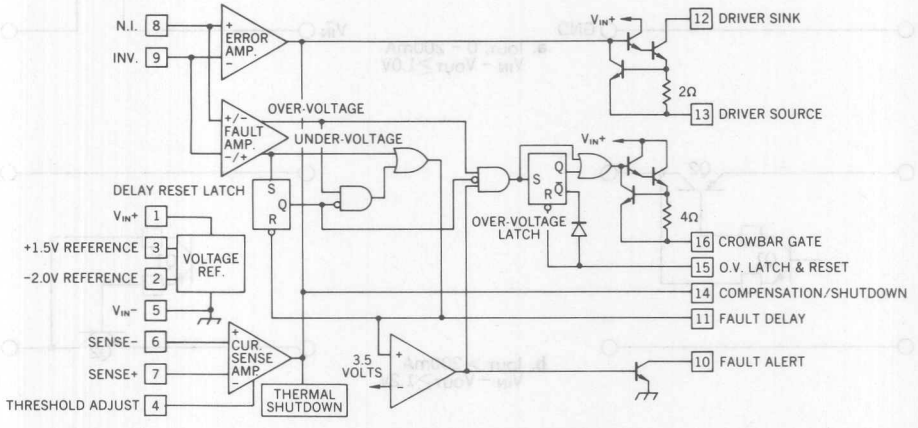


Figure 2. UC1834 Block Diagram

DRIVING THE PASS TRANSISTOR

Figure 3 shows suggested pass transistor configurations for implementing either positive or negative regulators with the UC1834. For those low current (≤200mA) applications in which efficiency is not extremely critical, the UC1834 output transistor can serve as the pass element, resulting in the simple configurations of Figure 3a. An external pass transistor is needed for output currents greater than 200mA. With the circuits of Figure 3c, the UC1834 can maintain regulation while operating the pass transistor near saturation. Operation at very high output currents (to ~30A) is possible with the Darlington pass elements of Figure 3d.

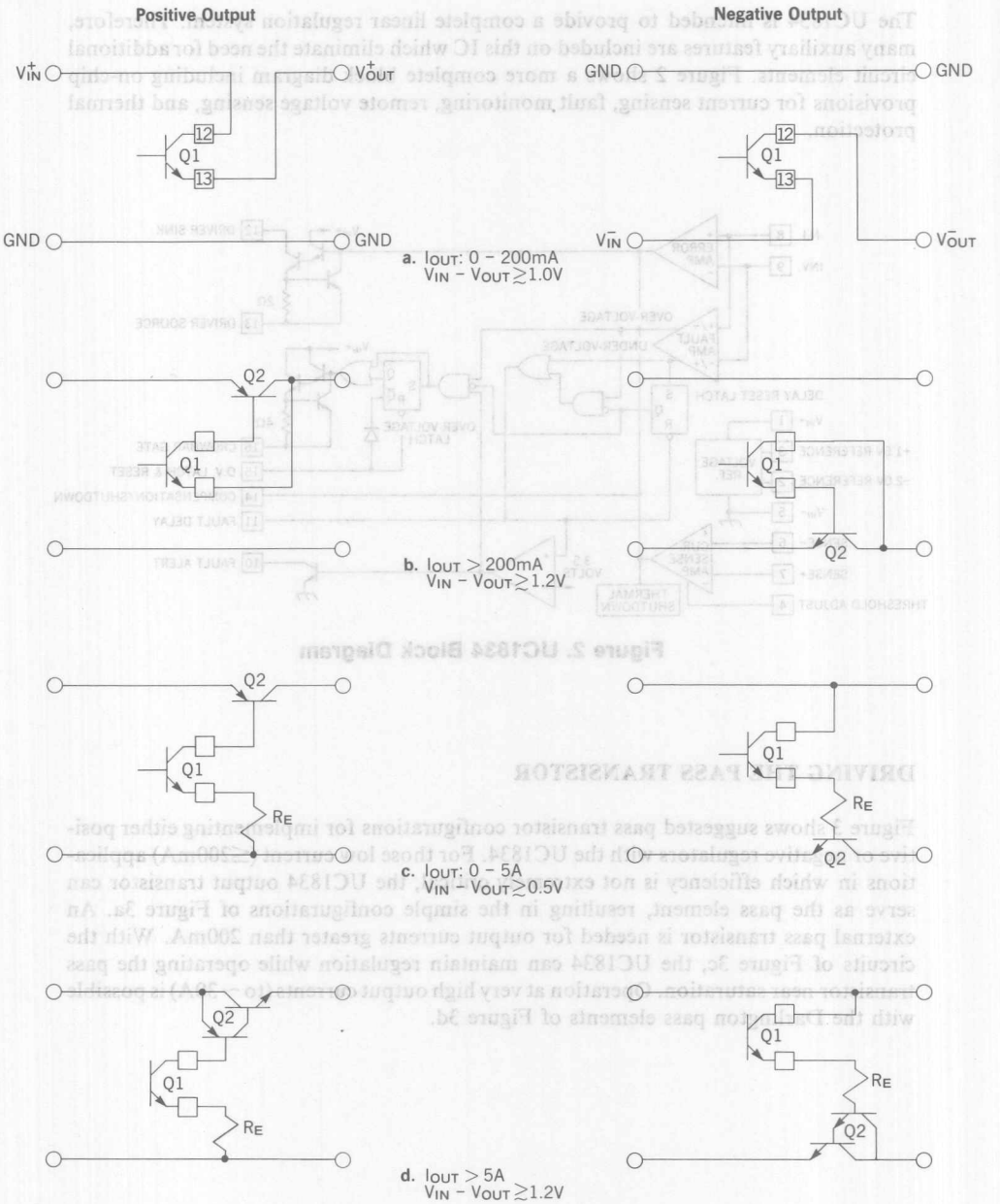


Figure 3. Pass Transistor Configurations

Current in the UC1834 output transistor is self-limiting, for improved reliability. This limiting is achieved by Q3 and R1 in Figure 4a. The resulting maximum output current is a function of temperature as shown in Figure 4b.

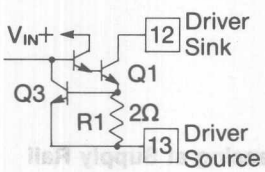
A resistor (R_E) is shown in series with the drive transistor in Figures 3c, d. This resistor shares base-drive power with the transistor, allowing cooler, more reliable operation of the IC. R_E should be as large as possible while still supporting adequate pass transistor base current under worst-case conditions of low input voltage and maximum output current:

$$V_{R_E(min)} = V_{IN(min)} - V_{BE(max)(Q2)} - V_{CE(sat)(max)(Q1)}$$
$$I_{B(max)(Q2)} = I_{O(max)} / \beta_{(min)(Q2)}$$
$$R_{E(opt)} = V_{R_E(min)} / I_{B(max)(Q2)}$$

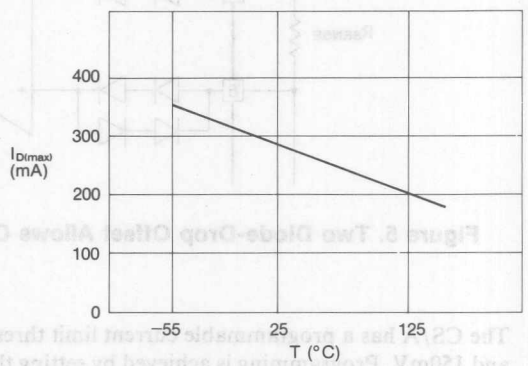
where: $V_{R_E(min)}$ is minimum voltage available to R_E
$I_{B(max)\ (Q2)}$ is maximum required base drive to Q2
$R_{E(opt)}$ is optimum value of R_E.

R_E also enhances stability by allowing operation of Q1 as an emitter-follower, thereby eliminating β_{Q1} from the loop transfer function:

$$I_{C(Q1)} \approx I_{E(Q1)} = (V_{E/A\ out} - V_{BE(Q1)} - V_{BE(Q2)}) / R_E \quad (\beta \text{ independent}).$$



a.



b.

Figure 4 a. Driver Current Limiting Circuit
b. Resulting Maximum Current vs Temperature

CURRENT SENSING

In order to protect the pass transistor from damage due to overheating, one must sense its emitter current (I_E) and then decrease the base drive if I_E is excessive. The UC1834 current sense amplifier (CS/A) accomplishes these tasks.

The UC1834 CS/A has a common mode range which includes both input supply "rails". This extended range is made possible by introducing matched voltage offsets in the differential input paths, as shown in Figure 5. Internal current sources bias the offset diodes in their appropriate direction. Which bias source (+ or -) is active is determined by whether the CS/A positive (+) input is greater or less than $V_{IN}/2$. Therefore, it is advisable to configure the sensing circuit such that the voltage at CS/A(+) will not cross $V_{IN}/2$ during operation. This precludes sensing in series with the load for most applications.

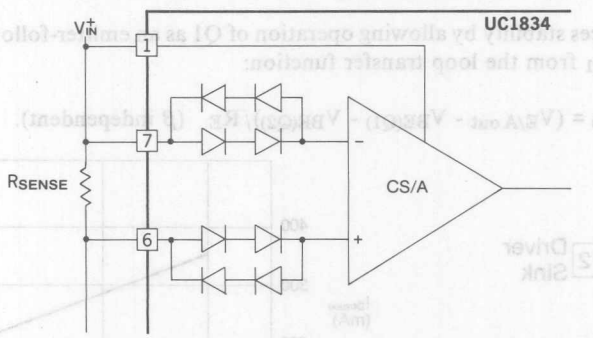


Figure 5. Two Diode-Drop Offset Allows Current Sensing at Supply Rail

The CS/A has a programmable current limit threshold which can be set between 0mV and 150mV. Programming is achieved by setting the voltage at the "Threshold Adjust" terminal (pin 4) to $10 \cdot V_{TH(desired)}$. The factor of 10 provides good noise immunity at pin 4 while allowing low power dissipation in the current sensing resistor. Figure 6 shows the guaranteed relationship between V_{PIN4} and the actual resulting threshold across the CS/A inputs. Note that the threshold is clamped at 150mV if pin 4 is open or if $V_{PIN4} > 1.5V$. The "Threshold Adjust" input is high impedance (bias current is less than $10\mu A$), allowing simple programming through a voltage divider from the 1.5V reference output. However, loading the 1.5V reference will affect the regulation of the -2.0V reference. Figure 7 shows how to compensate for this loading with a single resistor when the -2.0V reference is needed.

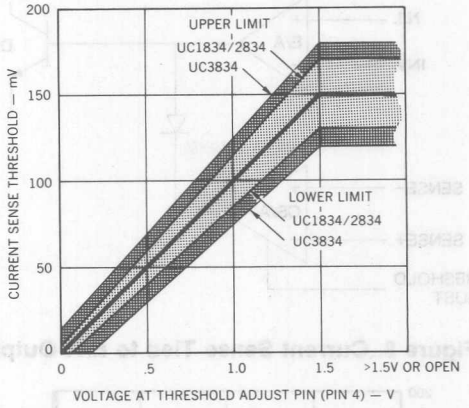


Figure 6. Guaranteed Tolerances on C/S Threshold Adjustment

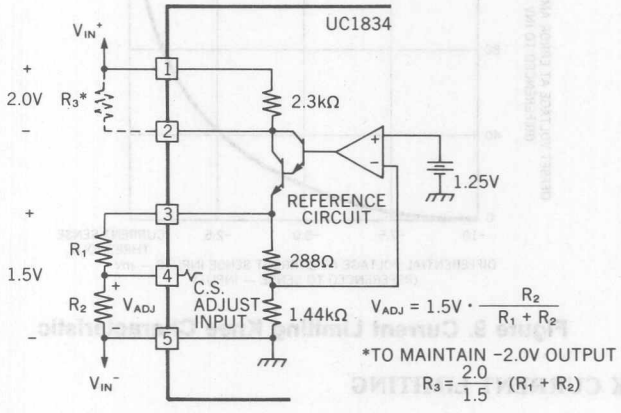


Figure 7. Setting the Current Threshold and Compensating the −2.0V Reference

The CS/A functions by pulling the E/A output low, turning off the output driver (Figure 8). As current approaches the threshold value, the E/A attempts to correct for the CS/A output, resulting in an E/A input offset voltage.The supply output voltage can decrease a proportional amount. When the CS/A input voltage differential reaches the current sense threshold, then the pass transistor is totally controlled by the CS/A. The combined CS/A and E/A gains and output configurations result in the current limit knee characteristic of Figure 9.

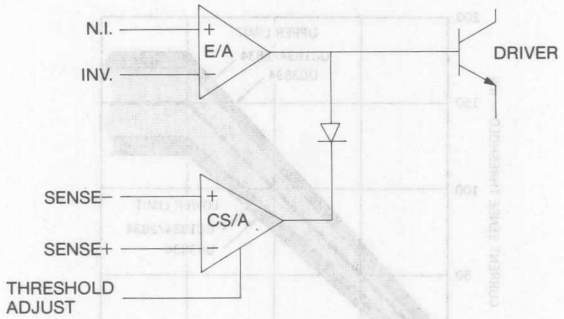


Figure 8. Current Sense Tied to E/A Output

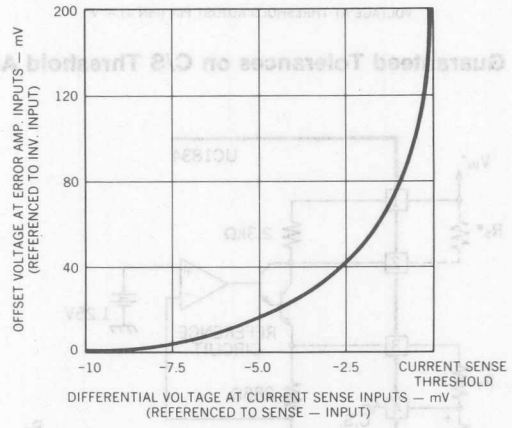


Figure 9. Current Limiting Knee Characteristic

FOLDBACK CURRENT LIMITING

It is desirable to put an upper limit on pass transistor power dissipation in order to protect that device. Ideally, for a constant power limit:

$I_{E(max)} \cdot V_{CE} \simeq K$ where K is a constant
or: $I_{E(max)} \simeq K/(V_{IN} - V_{OUT})$ (ignoring the sense resistor voltage drop).

As the input-to-out voltage differential increases, it is necessary to "fold back" the maximum allowable current. This ideal foldback characteristic is shown in Figure 10, along with a practical characteristic achievable with the circuit of Figure 11.

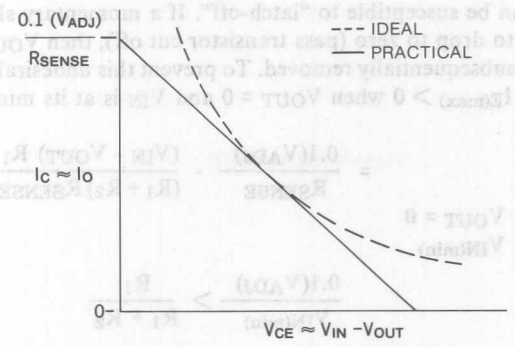


Figure 10. Ideal (Dashed Line) and Practical (Solid Line) Foldback Current Limiting Characteristics

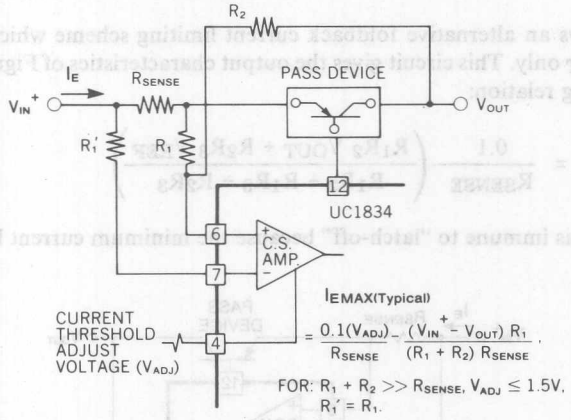


Figure 11. Foldback Current Limiting — Responds to Changes in V_{IN} or V_{OUT}

This circuit responds to changes in either V_{IN} or V_{OUT}. The voltage differential V_{IN} - V_{OUT} causes proportional current flow through R_1 and R_2. The additional drop across R_1 is interpreted by the CS/A as additional load current. The result is that the real current limit decreases linearly with V_{IN} - V_{OUT}:

$$I_{E(max)} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}}$$

for: $R_1 + R_2 \gg R_{SENSE}$
$V_{ADJ} \leq 1.5V$
$R_1' = R_1$.

This technique can be susceptible to "latch-off". If a momentary short at the supply output causes I_E to drop to zero (pass transistor cut off), then V_{OUT} cannot recover when the short is subsequentially removed. To prevent this undesirable operation, one must ensure that $I_{E(max)} > 0$ when $V_{OUT} = 0$ and V_{IN} is at its minimum:

$$I_{E(max)} \Big|_{\substack{V_{OUT}=0 \\ V_{IN(min)}}} = \frac{0.1(V_{ADJ})}{R_{SENSE}} - \frac{(V_{IN} - V_{OUT})\,R_1}{(R_1 + R_2)\,R_{SENSE}} > 0$$

$$\frac{0.1(V_{ADJ})}{V_{IN(min)}} > \frac{R_1}{R_1 + R_2}$$

$$R_2 > \frac{V_{IN(min)}\,R_1}{0.1\,(V_{ADJ})}\left(1 - \frac{0.1\,(V_{ADJ})}{V_{IN(min)}}\right)$$

Figure 12 shows an alternative foldback current limiting scheme which responds to decreased V_{OUT} only. This circuit gives the output characteristics of Figure 13, defined by the following relation:

$$I_{E(max)} = \frac{0.1}{R_{SENSE}} \cdot \left(\frac{R_1R_2\,V_{OUT} + R_2R_3\,V_{REF}}{R_1R_2 + R_1R_3 + R_2R_3}\right)$$

This technique is immune to "latch-off" because the minimum current limit is always non-zero.

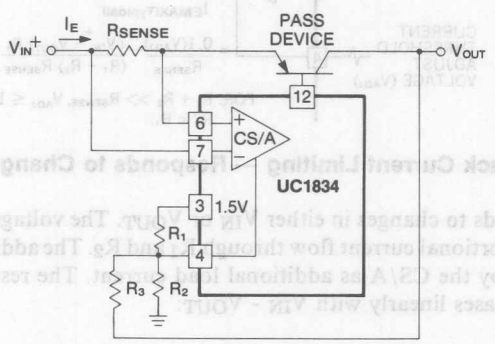


Figure 12. Foldback Current Limiting — Responds to Changes in V_{OUT} Only

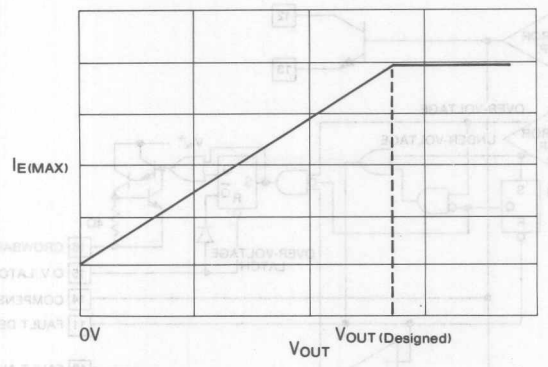


Figure 13. Foldback Current Limiting Characteristic

FAULT CIRCUITRY AND SYSTEM INTERFACING

In order to minimize the need for additional components, the UC1834 has on-chip provisions for fault detection and logic interfacing. These features are particularly useful when the linear regulator is part of a larger power supply system.

As shown in Figure 14, an internal comparator monitors the UC1834 E/A inputs. This comparator has two thresholds, for over- and under-voltage detection. Comparator thresholds are fixed at $|V_{N.I.} - V_{INV.}| = 150mV$. The resulting output voltage windows for non-fault operation are:

$$\frac{\pm .150V}{1.5V} = \pm 10\% \text{ for positive (+) supplies}$$

$$\frac{\pm .150V}{2V} = \pm 7.5\% \text{ for negative (-) supplies.}$$

A fault delay circuit prevents transient over- or under-voltage conditions (due to a rapidly changing load) being defined as faults. The delay time is programmable. An external capacitor at pin 11 is charged from an internal 75μA source. The delay period ends when the capacitor voltage reaches ~3.5V. The delay time is therefore ~47ms/μF. The fault alert output (pin 10) becomes an active low if an out-of-tolerance condition persists after the delay period. When no fault exists, this output is an open collector.

An over-voltage fault activates a 100mA crowbar gate drive output (pin 16) which can be used to switch on a shunt SCR. Such a fault also sets an over-voltage latch if the reset voltage (pin 15) is above the latch reset threshold (typically 0.4V). When the latch is set its $\overline{Q}$ output will pull pin 15 low through a series diode. As long as a nominal pull-up load exists, the series diode prevents $\overline{Q}$ from pulling pin 15 below the reset threshold. However, pin 15 is pulled low enough to disable the driver outputs if pins 15 and 14 are tied together. With pin 15 and 14 common, the regulator will latch off in response to an over-voltage fault. If the fault condition is cleared and pins 14 and 15 are momentarily pulled below the latch reset threshold, the driver outputs are re-enabled.

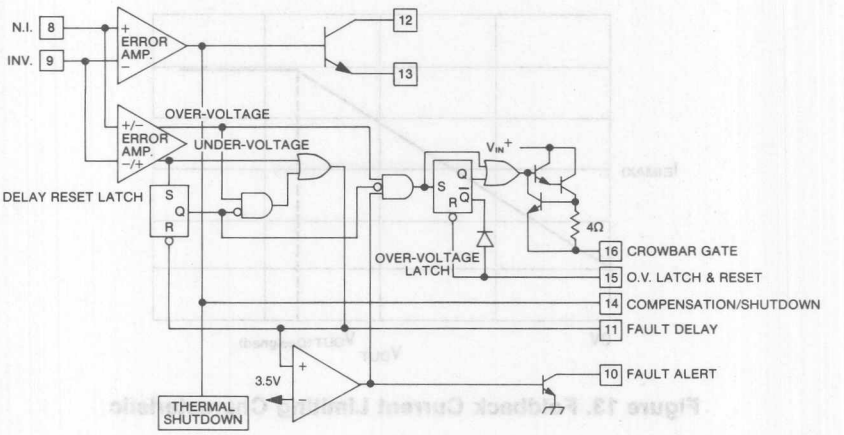


Figure 14. Fault Circuitry

An internal "delay reset latch" prevents crowbar turn-on when an under-voltage condition is immediately followed by a transient over-voltage condition. Such a situation could arise from a momentary short circuit at the supply output.

A thermal shutdown circuit pulls the E/A output low when junction temperatures reach 165°C, in order to protect the IC from excessive power dissipation in the drive transistor.

COMPENSATING THE FEEDBACK LOOP

A reliable design for any feedback system must yield a closed-loop frequency response which ensures unconditional stability. An optimum power supply response provides this stability while maximizing broadband gain for good dynamic voltage regulation with changing loads. Figure 15 illustrates such a response. The 0dB crossover frequency (f_c) should be as high as possible while maintaining phase margin above -360° at all lower frequencies (Nyquist stability criterion). In practice, this criterion dictates a single-pole response below f_c.

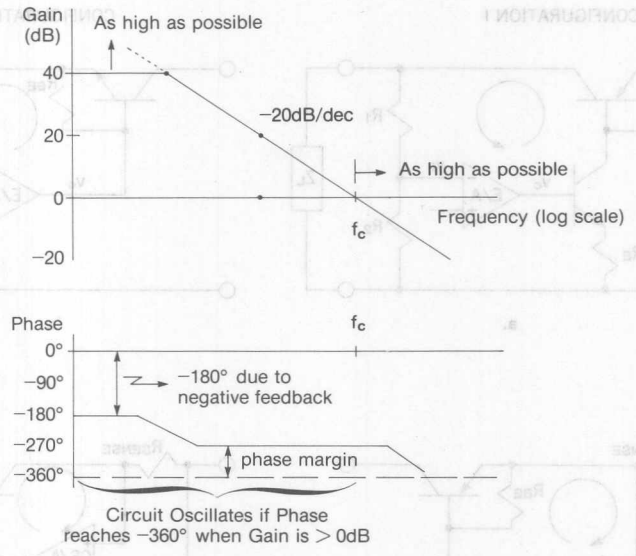


Figure 15. Desired Closed-Loop Response

Linear supplies using the UC1834 will usually have a current limiting loop in addition to the voltage control loop, as illustrated for two basic configurations* in Figure 16. Both loops must be stabilized for reliable operation. This is accomplished by appropriately compensating the E/A and CS/A at their common output (pin 14). Design of the compensation networks will often require an iterative procedure, since the compensation for one loop will affect the response of the other. A straightforward approach is outlined below:

1). Determine the frequency response of all voltage loop elements excluding the E/A. Appendix I offers guidelines for this step.

2). Design E/A compensation giving a frequency response which , when added to the response calculated in step 1, will yield a total loop characteristic consistent with the objectives outlined above. (Appendix II.)

3). Calculate the current loop response and determine whether it satisfies the Nyquist stability criterion. (Appendix III.) If not, add additional compensation and then recalculate the voltage loop response.

4). Iterate if necessary.

*All other configurations of Figure 3 are variants of these two, and can be treated in essentially the same ways.

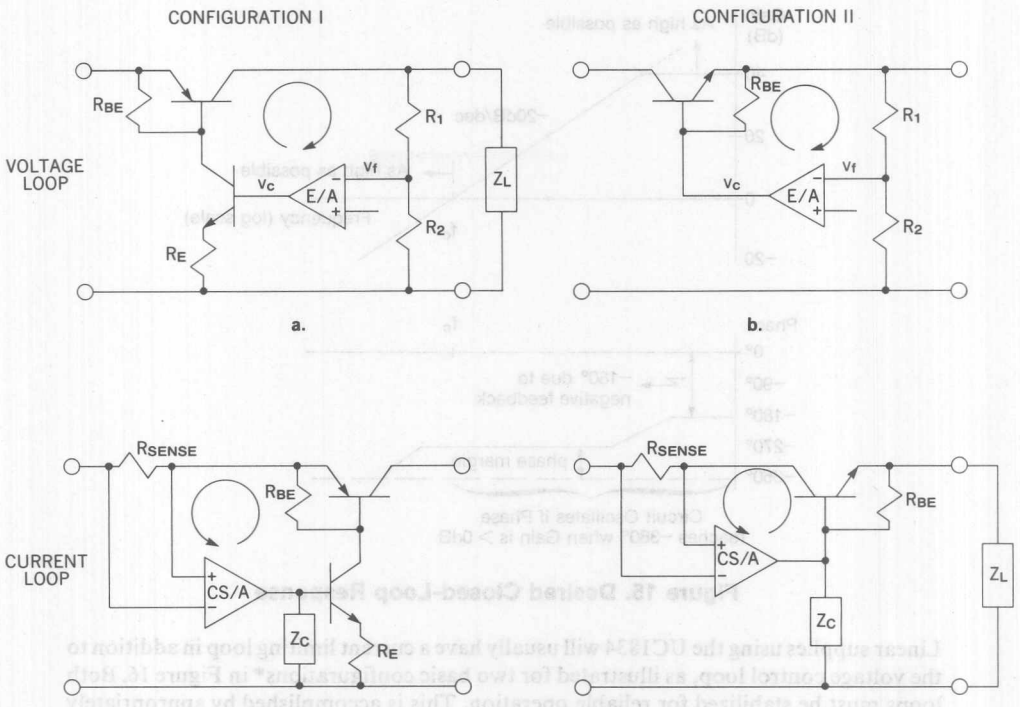


Figure 16. Voltage and Current Loops for Two Basic Configurations

EXAMPLE

Figure 17 shows a 5V, 5A (positive output) supply of the class shown in Figures 16a, c. This circuit tends toward instability when it is lightly loaded because of the high gain (β = 200) of the pass transistor at low currents. Output capacitor C_2 is needed to introduce a pole which rolls off the gain of the voltage loop to 0dB at 100kHz, avoiding instability due to the additional phase shift of a transistor pole at:

$$f = \frac{f_T}{\beta} = \frac{50MHz}{200} = 250kHz$$

Assuming a minimum load of 1A (R_L = 5Ω), the low frequency voltage loop gain, excluding the E/A, is (from Appendix I):

$$A_V = \frac{1}{15\Omega} \cdot 200 \cdot 5\Omega \cdot \frac{0.51k\Omega}{(1.7 + 0.51)\ k\Omega} = 20 = 26dB.$$

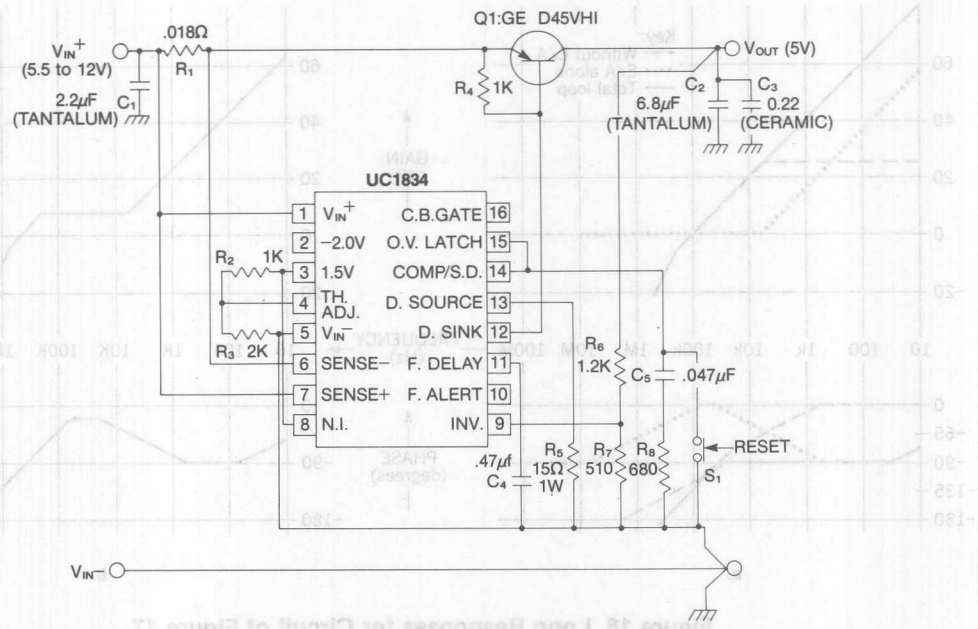


Figure 17. 0.5V Input-Output Differential 5A Positive Regulator

A pole at 5kHz is required in order to roll off from 26dB to 0dB at 100kHz. The required value of C_2 is therefore given by:

$$C_2 = \frac{1}{2\pi \cdot R_L \cdot f_p} = \frac{1}{2\pi \cdot 5\Omega \cdot 5kHz} = 6.4\mu F \text{ (6.8}\mu F \text{ used).}$$

The dashed curves of Figure 18a show the resulting voltage loop response, excluded the compensated E/A. Notice that the 5kHz pole (just added) itself introduces undesirable phase lag. This can be corrected by positioning the compensation zero (see Appendix II) at the same frequency. With $R_8 = 680\Omega$ (providing ~0dB E/A gain above 5kHz), then:

$$C_5 = \frac{1}{2\pi \cdot 680\Omega \cdot 5kHz} = .047\mu F.$$

The gain and phase of the compensated E/A (dotted lines) and complete voltage loop (solid lines) are also shown in Figure 18a.

The resulting current loop response (Figure 18b) is seen to meet the stability criterion. Gain above 5kHz is given by (from Appendix III):

$$A_I = \frac{1}{70\Omega} \cdot 680\Omega \cdot \frac{1}{15\Omega} \cdot 200 \cdot 0.018\Omega = 2.3 = 7.4dB.$$

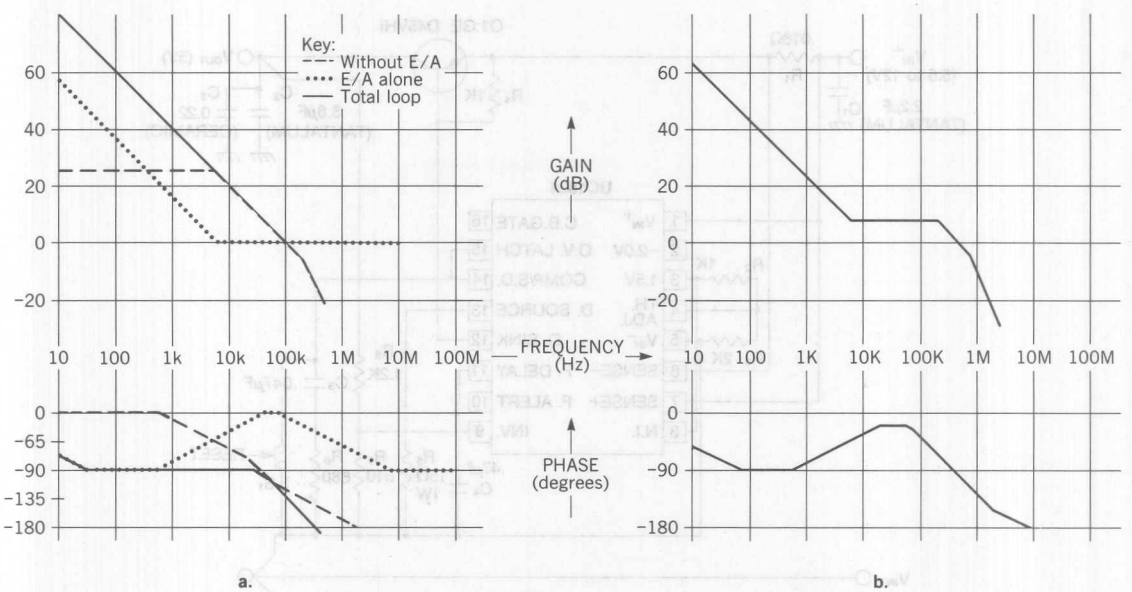


Figure 18. Loop Responses for Circuit of Figure 17
a. Voltage Loop
b. Current Loop

Reasonable phase margin (~40°) is maintained as the transistor and CS/A poles roll off this small gain to 0dB.

Figure 19 shows the UC1834 used to implement a negative output supply. A Darlington pass element provides adequate gain for operation at output current levels up to 10A.

CONCLUSION

Ever-increasing requirements for improved power supply economy and efficiency have produced a need for a versatile control IC capable of minimizing power losses in linear regulators. The UC1834 meets this need while also supporting all the auxilliary functions required of such supplies. This control circuit provides for optimized performance in a broad range of linear regulators, and in fact extends the range of applications for which such regulators are appropriate.

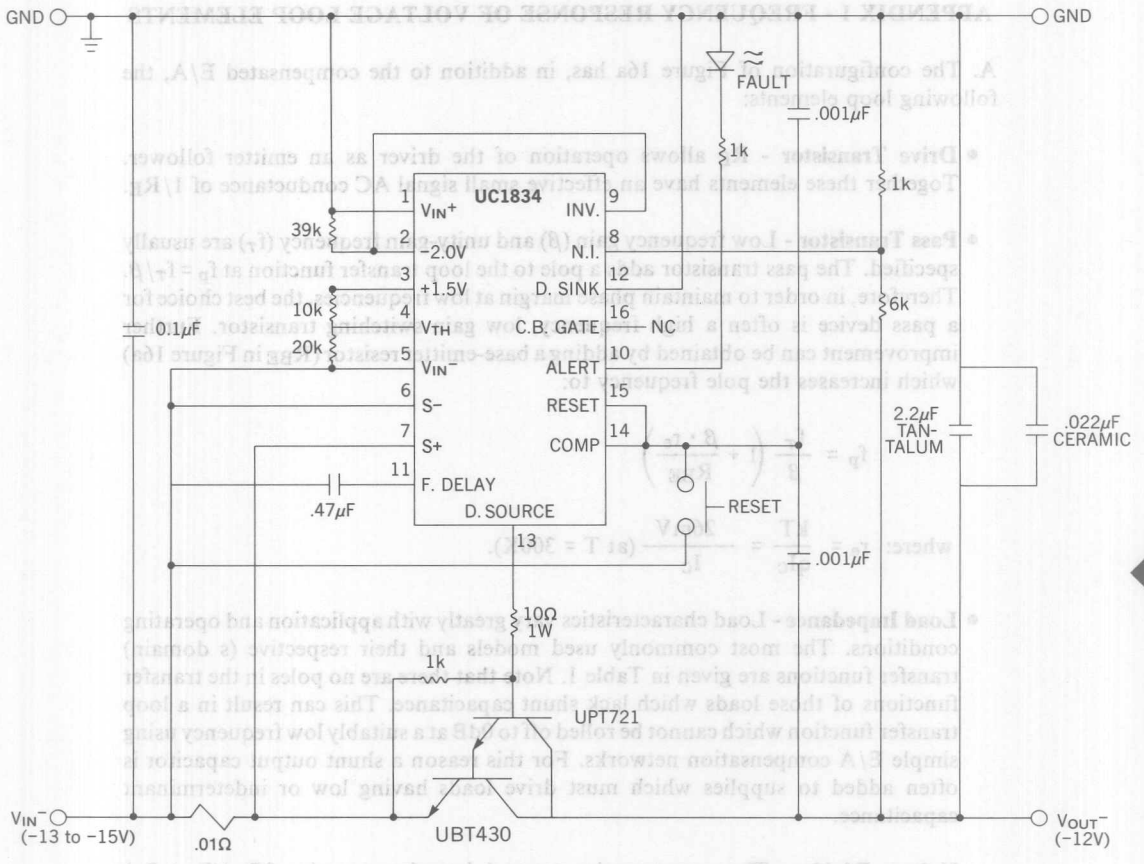


Figure 19. −12V, −10A Negative Regulator

APPENDIX I - FREQUENCY RESPONSE OF VOLTAGE LOOP ELEMENTS

A. The configuration of Figure 16a has, in addition to the compensated E/A, the following loop elements:

- **Drive Transistor** - R_E allows operation of the driver as an emitter follower. Together these elements have an effective small signal AC conductance of $1/R_E$.

- **Pass Transistor** - Low frequency gain (β) and unity-gain frequency (f_T) are usually specified. The pass transistor adds a pole to the loop transfer function at $f_p = f_T/\beta$. Therefore, in order to maintain phase margin at low frequencies, the best choice for a pass device is often a high frequency, low gain switching transistor. Further improvement can be obtained by adding a base-emitter resistor (R_{BE} in Figure 16a) which increases the pole frequency to:

$$f_p = \frac{f_T}{\beta}\left(1 + \frac{\beta \cdot r_e}{R_{BE}}\right)$$

where: $r_e = \frac{kT}{qI_C} = \frac{26mV}{I_C}$ (at T = 300K).

- **Load Impedance** - Load characteristics vary greatly with application and operating conditions. The most commonly used models and their respective (s domain) transfer functions are given in Table 1. Note that there are no poles in the transfer functions of those loads which lack shunt capacitance. This can result in a loop transfer function which cannot be rolled off to 0dB at a suitably low frequency using simple E/A compensation networks. For this reason a shunt output capacitor is often added to supplies which must drive loads having low or indeterminant capacitance.

- **Voltage Divider** - The output sensing network introduces a gain of $R_2/(R_1 + R_2)$.

- **Total Loop Gain,** excluding the E/A, is therefore given by:

$$A_V = \frac{v_c}{v_f} = \frac{1}{R_E} \cdot \beta_{PASS} \cdot Z_L \cdot \frac{R_2}{R_1 + R_2} \qquad \text{for } f < \frac{f_T}{\beta}\left(1 + \frac{\beta\, r_e}{R_{BE}}\right).$$

B. The circuit of Figure 16b has a more straightforward response, since the only element (other than the E/A) which introduces any gain is the voltage divider:

$$A_V = \frac{R_2}{R_1 + R_2}$$

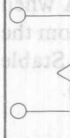
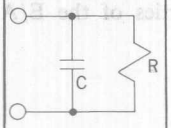
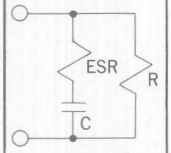
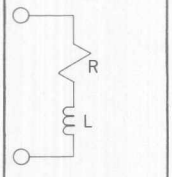
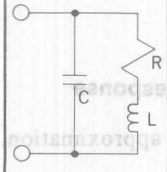
Load Model	Transfer Function	Poles @ f =	Zeros @ f =
	$Z_L(s) = R$	———	———
	$Z_L(s) = \frac{R}{1 + sRC}$	$\frac{1}{2\pi RC}$	———
	$Z_L(s) = \frac{R(1 + s(ESR)C)}{1 + s(R + ESR)C}$	$\frac{1}{2\pi(R + ESR)C}$	$\frac{1}{2\pi(ESR)C}$
	$Z_L(s) = R + sL$	———	$\frac{R}{2\pi L}$
	$Z_L(s) = \frac{s\left(s + \frac{R}{L}\right)}{s^2 + \frac{R}{L}s + \frac{1}{LC}}$	$\frac{-R/L \pm \sqrt{R^2/L^2 - 4/LC}}{4\pi}$	$0, \frac{R}{2\pi L}$

Table 1. Load Models and their Transfer Functions

APPENDIX II - ERROR AMPLIFIER RESPONSE

Figure 20 shows the open-loop gain and phase response of the UC1834 E/A when lightly loaded. The gain curve represents an upper limit on the gain available from the compensated amplifier. Note that a second-order pole occurs near 800kHz. Stable circuits will require a 0dB crossover well below this frequency ($f_c \leq$ 500kHz).

The E/A can be compensated with or without the use of local feedback. When operated without such feedback (Figure 21a) the transconductance properties of the E/A become evident; i.e. the voltage gain in given by:

$$A_{V(E/A)} = g_M Z_C \qquad (f \leq 500kHz)$$

where: $g_M \approx \frac{1}{700\Omega} = 1.4mS$

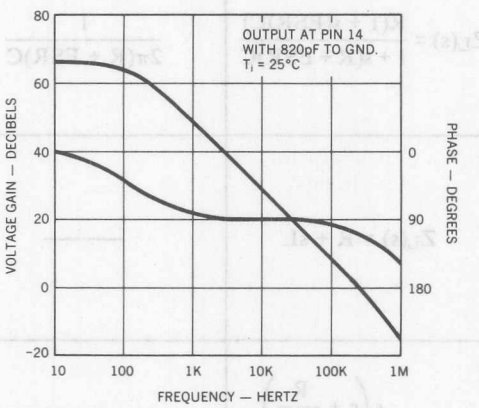


Figure 20. Error Amplifier Gain and Phase Frequency Response

When the E/A has local feedback (Figure 21b), its gain is, to a first approximation, independent of transconductance:

$$A_{V(E/A)} = \frac{Z_F}{Z_{IN}} \qquad (f \leq 500kHz)$$

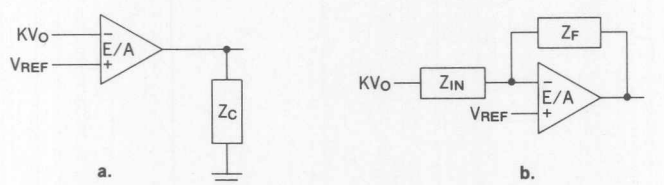


Figure 21. E/A Compensation (a.) Without and (b.) With Local Feedback

However, the use of local feedback creates an additional loop which must be independently stable. The UC1834 has no internal compensation to ensure this stability, so additional external compensation is usually required. An 820pF capacitor from the E/A output to ground will stabilize this inner voltage loop while also enhancing current loop stability.

An additional drawback to the use of local feedback is that Z_F places a DC load on the E/A output. With a transconductance amplifier this results in additional input offset voltage:

$$\Delta V_{IO} = \frac{I_{E/A\,OUT}}{g_M}$$

This offset results in degradation of DC regulation. The problem can be averted by taking local feedback from the emitter of the drive transistor if the driver is configured as an emitter-follower.

Whatever the compensation scheme, the UC1834 E/A output can sink or source a maximum of 100μA.

Table 2 shows two typical compensation schemes and the resulting E/A transfer functions. The first of these circuits is most widely used.

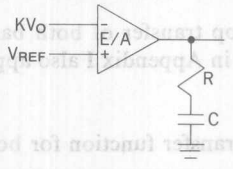
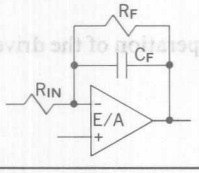
Compensation Circuit	E/A Gain ($A_{V(E/A)}(s)$)	Poles @ f =	Zeros @ f =
	$A_V = \frac{g_M(1 + sRC)}{sC}$	0	$\frac{1}{2\pi RC}$
	$A_V = \frac{R_F}{R_{IN}(1 + s R_F C_F)}$	$\frac{1}{2\pi R_F C_F}$	———

Table 2. E/A Compensation Circuits and Gain Response

APPENDIX III - FREQUENCY RESPONSE OF THE CURRENT LOOP

- **CS/A** - Figure 22 shows the open-loop gain and phase response of the UC1834 CS/A. This is also a transconductance amplifier, having $g_M \approx 1/70\Omega = 14mS$. The voltage gain is analogous to that of the E/A. The E/A compensation impedance (Z_C or $Z_{F(E/A)}$) is also seen by the CS/A output. For purposes of small signal AC analysis, the CS/A will always see this impedance as being returned to $V_{\overline{IN}}$ (as shown in Figures 16c, d) when the E/A is compensated by either of the methods shown in Table 2.

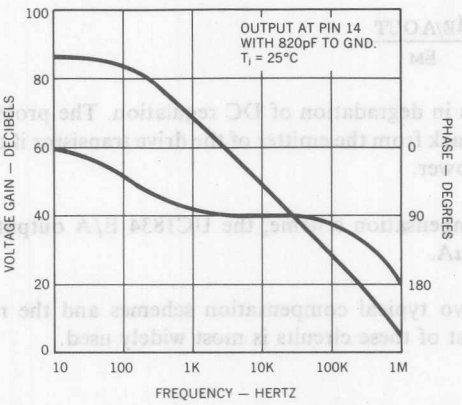


Figure 22. Current Sense Amplifier Gain and Phase Frequency Response

- **Pass Transistor** - Introduces current gain β to the loop transfer of both basic configurations (Figures 16c, d).Considerations outlined in Appendix I also apply here.

- **Sense Resistor** - Resistance value R_{SENSE} appears in transfer function for both configurations.

- **Drive Transistor** - In the circuit of Figure 16c, R_E allows operation of the driver as an emitter-follower. Effective conductance is $1/R_E$.

Closed-loop responses are given by the following:

for circuit of Figure 16c:

$$A_I = g_M \cdot Z_C \cdot \frac{1}{R_E} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_\tau}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

for circuit of Figure 16d:

$$A_I = g_M \cdot \frac{Z_C}{Z_C + \beta Z_L} \cdot \beta \cdot R_{SENSE} \qquad \left(f < 500kHz,\ f < \frac{f_\tau}{\beta}\left(1 + \frac{\beta r_e}{R_{BE}}\right)\right)$$

MODELLING, ANALYSIS AND COMPENSATION OF THE CURRENT-MODE CONVERTER

Abstract

As current-mode conversion increases in popularity, several peculiarities associated with fixed-frequency, peak-current detecting schemes have surfaced. These include instability above 50% duty cycle, a tendency towards subharmonic oscillation, non-ideal loop response, and an increased sensitivity to noise. This paper will attempt to show that the performance of any current-mode converter can be improved and at the same time all of the above problems reduced or eliminated by adding a fixed amount of "slope compensation" to the sensed current waveform.

1.0 INTRODUCTION

The recent introduction of integrated control circuits designed specifically for current mode control has led to a dramatic upswing in the application of this technique to new designs. Although the advantages of current-mode control over conventional voltage-mode control has been amply demonstrated[1-5], there still exist several drawbacks to a fixed frequency peak-sensing current mode converter. They are (1) open loop instability above 50% duty cycle, (2) less than ideal loop response caused by peak instead of average inductor current sensing, (3) tendency towards subharmonic oscillation, and (4) noise sensitivity, particularly when inductor ripple current is small. Although the benefits of current mode control will, in most cases, far out-weight these drawbacks, a simple solution does appear to be available. It has been shown by a number of authors that adding slope compensation to the current waveform (Figure 1) will stabilize a system above 50% duty cycle. If one is to look further, it becomes apparent that this same compensation technique can be used to minimize many of the drawbacks stated above. In fact, it will be shown that any practical converter will nearly always perform better with some slope compensation added to the current waveform.

The simplicity of adding slope compensation – usually a single resistor – adds to its attractiveness. However, this introduces a new problem – that of analyzing and predicting converter performance. Small signal AC models for both current and voltage-mode PWM's have been extensively developed in the literature. However, the slope compensated or "dual control" converter possesses properties of both with an equivalent circuit different from, yet containing elements of each. Although this has been addressed in part by several authors[1, 2], there still exists a need for a simple circuit model that can provide both qualitative and quantitative results for the power supply designer.

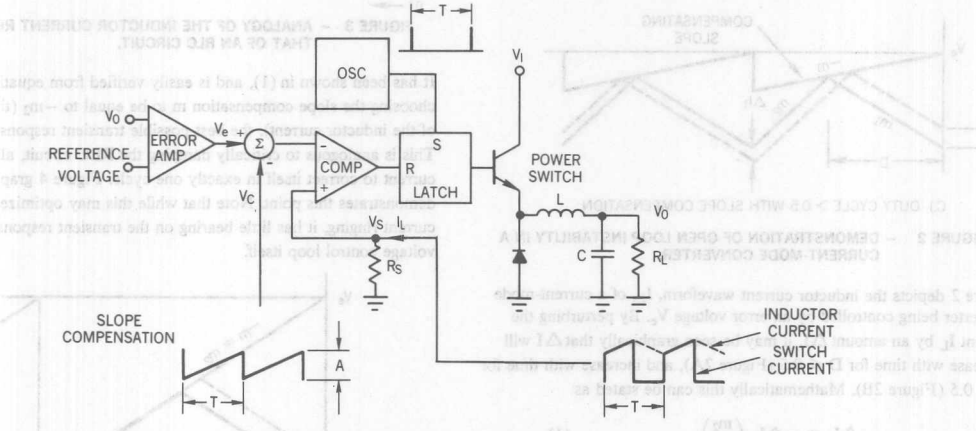


FIGURE 1 – A CURRENT-MODE CONTROLLED BUCK REGULATOR WITH SLOPE COMPENSATION.

The first objective of this paper is to familiarize the reader with the peculiarities of a peak-current control converter and at the same time demonstrate the ability of slope compensation to reduce or eliminate many problem areas. This is done in section 2. Second, in section 3, a circuit model for a slope compensated buck converter in continuous conduction will be developed using the state-space averaging technique outlined in(1). This will provide the analytical basis for section 4 where the practical implementation of slope compensation is discussed.

2.1 OPEN LOOP INSTABILITY

An unconditional instability of the inner current loop exists for any fixed frequency current-mode converter operating above 50% duty cycle – regardless of the state of the voltage feedback loop. While some topologies (most notably two transistor forward converters) cannot operate above 50% duty cycle, many others would suffer serious input limitations if greater duty cycle could not be achieved. By injecting a small amount of slope compensation into the inner loop, stability will result for all values of duty cycle. Following is a brief review of this technique.

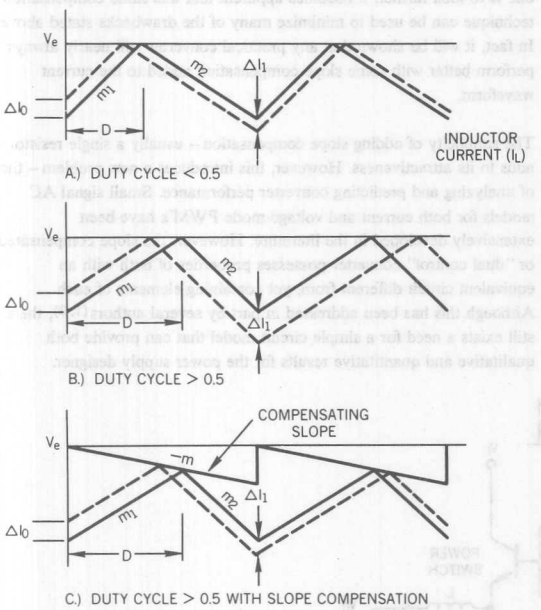


FIGURE 2 – DEMONSTRATION OF OPEN LOOP INSTABILITY IN A CURRENT-MODE CONVERTER.

Figure 2 depicts the inductor current waveform, I_L, of a current-mode converter being controlled by an error voltage V_e. By perturbing the current I_L by an amount ΔI, it may be seen graphically that ΔI will decrease with time for $D < 0.5$ (Figure 2A), and increase with time for $D > 0.5$ (Figure 2B). Mathematically this can be stated as

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2}{m_1}\right) \qquad (1)$$

Carrying this a step further, we can introduce a linear ramp of slope $-m$ as shown in Figure 2C. Note that this slope may either be added to the current waveform, or subtracted from the error voltage. This then gives

$$\Delta I_1 = -\Delta I_0 \left(\frac{m_2 + m}{m_1 + m}\right) \qquad (2)$$

Solving for m at 100% duty cycle gives

$$m > -\tfrac{1}{2} m_2 \qquad (3)$$

Therefore, to guarantee current loop stability, the slope of the compensation ramp must be greater than one-half of the down slope of the current waveform. For the buck regulator of Figure 1, m_2 is a constant equal to $\frac{V_0}{L} R_S$, therefore, the amplitude A of the compensating waveform should be chosen such that

$$A > T R_S \frac{V_0}{L} \qquad (4)$$

to guarantee stability above 50% duty cycle.

2.2 RINGING INDUCTOR CURRENT

Looking closer at the inductor current waveform reveals two additional phenomenon related to the previous instability. If we generalize equation 2 and plot I_n vs nT for all n as in Figure 3, we observe a damped sinusoidal response at one-half the switching frequency, similar to that of an RLC circuit. This ring-out is undesirable in that it (a) produces a ringing response of the inductor current to line and load transients, and (b) peaks the control loop gain at ½ the switching frequency, producing a marked tendency towards instability.

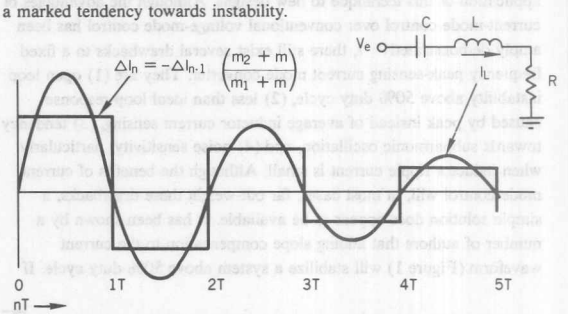


FIGURE 3 – ANALOGY OF THE INDUCTOR CURRENT RESPONSE TO THAT OF AN RLC CIRCUIT.

It has been shown in (1), and is easily verified from equation 2, that by choosing the slope compensation m to be equal to $-m_2$ (the down slope of the inductor current), the best possible transient response is obtained. This is analogous to critically damping the RLC circuit, allowing the current to correct itself in exactly one cycle. Figure 4 graphically demonstrates this point. Note that while this may optimize inductor current ringing, it has little bearing on the transient response of the voltage control loop itself.

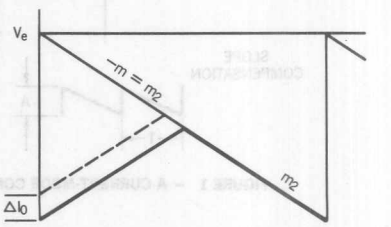


FIGURE 4 – FOR THE CASE OF $m = -m_2$, A CURRENT PERTURBATION WILL DAMP OUT IN EXACTLY ONE CYCLE.

2.3 SUBHARMONIC OSCILLATION

Gain peaking by the inner current loop can be one of the most significant problems associated with current-mode controllers. This peaking occurs at one-half the switching frequency, and – because of excess phase shift in the modulator – can cause the voltage feedback loop to break into oscillation at one-half the switching frequency. This instability, sometimes called subharmonic oscillation, is easily detected as duty cycle asymmetry between consecutive drive pulses in the power stage. Figure 5 shows the inductor current of a current-mode controller in subharmonic oscillation (dotted waveforms with period 2T).

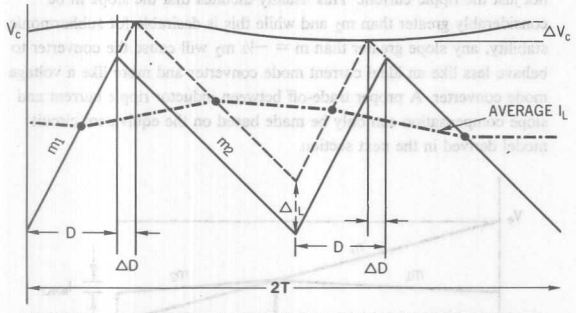


FIGURE 5 – CURRENT WAVE FORM (DOTTED) OF A CURRENT-MODE CONVERTER IN SUBHARMONIC OSCILLATION.

To determine the bounds of stability, it is first necessary to develop an expression for the gain of the inner loop at one-half the switching frequency. The technique used in (2) will be paralleled for a buck converter with the addition of terms to include slope compensation.

2.3.1 LOOP GAIN CALCULATION AT ½f_s

Referring to figures 5 and 6, we want to relate the input stimulus, ΔV_e, to an output current, ΔI_L. From figure 5, two equations may be written

$$\Delta I_L = \Delta D\, m_1\, T - \Delta D\, m_2\, T \quad (4)$$

$$\Delta V_C = \Delta D\, m_1\, T + \Delta D\, m_2\, T \quad (5)$$

Adding slope compensation as in figure 6 gives another equation

$$\Delta V_e = \Delta V_C + 2\Delta D\, m\, T \quad (6)$$

Using (5) to eliminate ΔV_C from (6) and solving for $\Delta I_L/\Delta V_e$ yields

$$\frac{\Delta I_L}{\Delta V_e} = \frac{m_1 - m_2}{m_1 + m_2 + m} \quad (7)$$

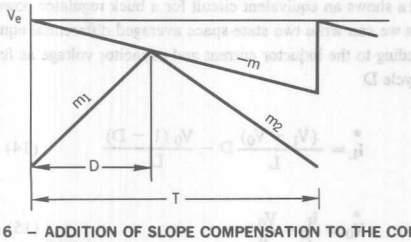


FIGURE 6 – ADDITION OF SLOPE COMPENSATION TO THE CONTROL SIGNAL

For steady state condition we can write

$$D\, m_1\, T = (1 - D)\, m_2\, T \quad (8)$$

or

$$D = \frac{-m_2}{m_1 - m_2} \quad (9)$$

By using (9) to reduce (7), we obtain

$$\frac{\Delta I_L}{\Delta V_e} = \frac{1}{1 - 2D\,(1 + m/m_2)} \quad (10)$$

Now by recognizing that ΔI_L is simply a square wave of period 2T, we can relate the first harmonic amplitude to ΔI_L by the factor $4/\pi$ and write the small signal gain at $f = \frac{1}{2}f_S$ as

$$\frac{i_L}{v_e} = \frac{4\pi}{1 - 2D\,(1 + m/m_2)} \quad (11)$$

If we assume a capacitive load of C at the output and an error amplifier gain of A, then finally, the expression for loop gain at $f = \frac{1}{2}f_S$ is

$$\text{Loop gain} = \frac{\frac{4TA}{\pi^2 C}}{1 - 2D\,(1 + m/m_2)} \quad (12)$$

2.3.2 USING SLOPE COMPENSATION TO ELIMINATE SUBHARMONIC OSCILLATION

From equation 12, we can write an expression for maximum error amplifier gain at $f = \frac{1}{2}f_S$ to guarantee stability as

$$A_{max} = \frac{1 - 2D\,(1 + m/m_2)}{\frac{4T}{\pi^2 C}} \quad (13)$$

This equation clearly shows that the maximum allowable error amplifier gain, A_{max}, is a function of both duty cycle and slope compensation. A normalized plot of A_{max} versus duty cycle for several values of slope compensation is shown in figure 7. Assuming the amplifier gain cannot be reduced to zero at $f = \frac{1}{2}f_S$, then for the case of $m = 0$ (no compensation) we see the same instability previously discussed at 50% duty cycle. As the compensation is increased to $m = -\frac{1}{2}m_2$, the point of instability moves out to a duty cycle of 1.0, however in any practical

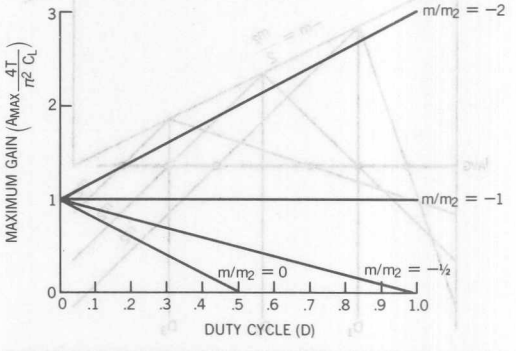


FIGURE 7 – MAXIMUM ERROR AMPLIFIER GAIN AT ½ f_s (NORMALIZED) V.S. DUTY CYCLE FOR VARYING AMOUNTS OF SLOPE COMPENSATION. REFER TO EQUATION 13.

system, the finite value of A_{max} will drive the feedback loop into subharmonic oscillation well before full duty cycle is reached. If we continue to increase m, we reach a point, $m = -m_2$, where the maximum gain becomes independent of duty cycle. This is the point of critical damping as discussed earlier, and increasing m above this value will do little to improve stability for a regulator operating over the full duty cycle range.

2.4 PEAK CURRENT SENSING VERSUS AVERAGE CURRENT SENSING

True current-mode conversion, by definition, should force the average inductor current to follow an error voltage – in effect replacing the inductor with a current source and reducing the order of the system by one. As shown in Figure 8, however, peak current detecting schemes are generally used which allow the average inductor current to vary with duty cycle while producing less than perfect input to output – or feedforward characteristics. If we choose to add slope compensation equal to $m = -\frac{1}{2} m_2$ as shown in Figure 9, we can convert a peak current detecting scheme into an average current detector, again allowing for perfect current mode control. As mentioned in the last section, however, one must be careful of subharmonic oscillations as a duty cycle of 1 is approached when using $m = -\frac{1}{2} m_2$.

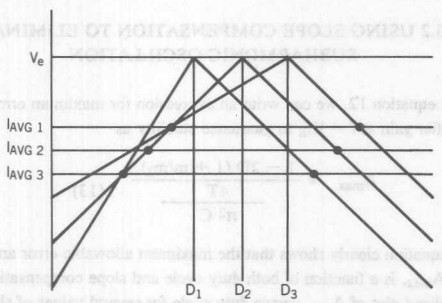


FIGURE 8 – PEAK CURRENT SENSING WITHOUT SLOPE COMPENSATION ALLOWS AVERAGE INDUCTOR CURRENT TO VARY WITH DUTY CYCLE

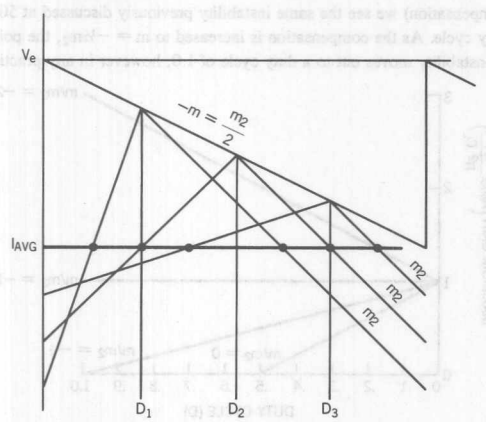


FIGURE 9 – AVERAGE INDUCTOR CURRENT IS INDEPENDENT OF DUTY CYCLE AND INPUT VOLTAGE VARIATION FOR A SLOPE COMPENSATION OF $m = -\frac{1}{2} m_2$.

2.5 SMALL RIPPLE CURRENT

From a systems standpoint, small inductor ripple currents are desirable for a number of reasons – reduced output capacitor requirements, continuous current operation with light loads, less output ripple, etc. However, because of the shallow slope presented to the current sense circuit, a small ripple current can, in many cases, lead to pulse width jitter caused by both random and synchronous noise (Figure 10). Again, if we add slope compensation to the current waveform, a more stable switchpoint will be generated. To be of benefit, the amount of slope added needs to be significant compared to the total inductor current – not just the ripple current. This usually dictates that the slope m be considerably greater than m_2 and while this is desirable for subharmonic stability, any slope greater than $m = -\frac{1}{2} m_2$ will cause the converter to behave less like an ideal current mode converter and more like a voltage mode converter. A proper trade-off between inductor ripple current and slope compensation can only be made based on the equivalent circuit model derived in the next section.

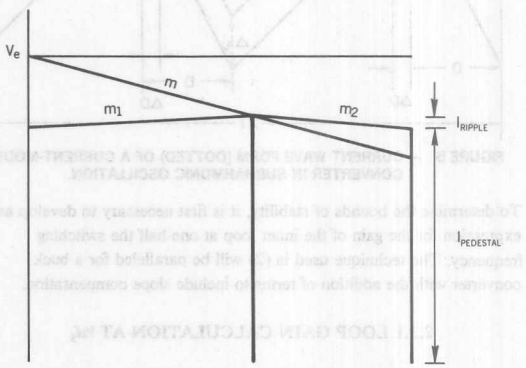


FIGURE 10 – A LARGE PEDESTAL TO RIPPLE CURRENT RATIO.

3.0 SMALL SIGNAL A.C. MODEL

As we have seen, many drawbacks associated with current-mode control can be reduced or eliminated by adding slope compensation in varying degrees to the current waveform. In an attempt to determine the full effects of this same compensation on the closed loop response, a small signal equivalent circuit model for a buck regulator will now be developed using the state-space averaging technique developed in (1).

3.1 A.C. MODEL DERIVATION

Figure 11a shows an equivalent circuit for a buck regulator power stage. From this we can write two state-space averaged differential equations corresponding to the inductor current and capacitor voltage as functions of duty cycle D

$$\dot{I}_L = \frac{(V_I - V_0)}{L} D - \frac{V_0 (1 - D)}{L} \qquad (14)$$

$$\dot{V}_0 = \frac{I_L}{C} - \frac{V_0}{R} \qquad (15)$$

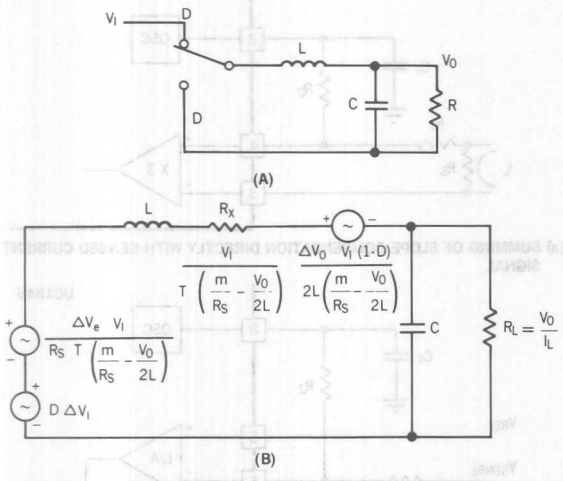


FIGURE 11 – BASIC BUCK CONVERTER (A) AND ITS SMALL SIGNAL EQUIVALENT CIRCUIT MODEL (B).

If we now perturb these equations – that in substitute $V_I + \Delta V_I$, $V_O + \Delta V_O$, $D + \Delta D$ and $I_L + \Delta I_L$ for their respective variables – and ignore second order terms, we obtain the small signal averaged equations

$$\Delta \dot{I}_L = \frac{D\Delta I_L}{L} - \frac{\Delta V_O}{L} + \frac{V_I \Delta D}{L} \qquad (16)$$

$$\Delta \dot{V}_O = \frac{\Delta I_L}{C} - \frac{\Delta V_O}{CR} \qquad (17)$$

A third equation – the control equation – relating error voltage, V_e, to duty cycle may be written from Figure 6 as

$$I_L R_S = V_e - mDT - \frac{(1-D)\, V_O\, T\, R_S}{2L} \qquad (18)$$

Perturbing this equation as before gives

$$\Delta I_L = \frac{\Delta V_e}{R_S} - \Delta D T\left(\frac{m}{R_S} - \frac{V_O}{2L}\right) - \frac{T}{2L}(1-D)\,\Delta V_O \qquad (19)$$

By using 19 to eliminate ΔD from 16 and 17 we arrive at the state-space equations

$$\Delta \dot{I}_L = \frac{D}{L}\Delta V_I + \frac{\Delta V_e \, V_I}{R_S \, LT\left(\frac{m}{R_S} - \frac{V_O}{2L}\right)} - \frac{\Delta V_O \, V_I \,(1-D)}{2L^2\left(\frac{m}{R_S} - \frac{V_O}{2L}\right)} - \frac{\Delta I_L V_I}{LT\left(\frac{m}{R_S} - \frac{V_O}{2L}\right)} \qquad (20)$$

$$\Delta \dot{V}_O = \frac{\Delta I_L}{C} - \frac{\Delta V_O}{CR} \qquad (21)$$

An equivalent circuit model for these equations is shown in Figure 11B and discussed in the next section.

3.2 A.C. MODEL DISCUSSION

The model of Figure 11B can be used to verify and expand upon our previous observations. Key to understanding this model is the interaction between R_X and L as the slope compensation, m is changed. In most cases, the dependent source between R_X and C can be ignored.

If R_X is much greater than L, as is the case for little or no compensation ($m = 0$), the converter will have a single pole response and act as a true current mode converter. If R_X is small compared to $L\left(m \gg \frac{R_S\, V_O}{2L}\right)$, then a double pole response will be formed by the LRC output filter similar to any voltage-mode converter. By appropriately adjusting m, any condition between these two extremes can be generated.

Of particular interest is the case when $m = \frac{R_S\, V_O}{2L}$. Since the down slope of the inductor current (m_2 from Figure 6) is equal to $\frac{R_S\, V_O}{L}$, we can write $m = -\frac{1}{2}m_2$. At this point, R_X goes to infinity, resulting in an ideal current mode converter. This is the same point, discussed in section 2.4, where the average inductor current exactly follows the error voltage. Note that although this compensation is ideal for line rejection and loop response, maximum error amp gain limitations as higher duty cycles are approached (section 2.3) may necessitate using more compensation.

Having derived an equivalent circuit model, we may now proceed in its application to more specific design examples. Figure 12 plots open loop ripple rejection ($\Delta V_O/\Delta V_I$) at 120Hz versus slope compensation for a typical 12 volt buck regulator operating under the following conditions:

V_O	=	12V
V_I	=	25V
L	=	200μH
C	=	300μf
T	=	20μS
R_S	=	.5Ω
R_L	=	1Ω, 12$\dot{\Omega}$

Again, as the slope compensation approaches $-\frac{1}{2}m_2$, the theoretical ripple rejection is seen to become infinite. As larger values of m are introduced, ripple rejection slowly degrades to that of a voltage-mode converter (−6.4dB for this example).

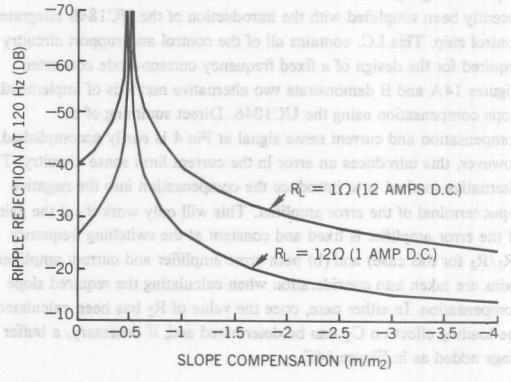


FIGURE 12 – RIPPLE REJECTION AT 120Hz V.S. SLOPE COMPENSATION FOR 1AMP AND 12AMP LOADS.

If a small ripple to D.C. current ratio is used, as is the case for R_L = 1ohm in the example, proportionally larger values of slope compensation may be injected while still maintaining a high ripple rejection ratio. In other words, to obtain a given ripple rejection ratio, the allowable slope compensation varies proportionally to the average D.C. current, not the ripple current. This is an important concept when attempting to minimize noise jitter on a low ripple converter.

Figure 13 shows the small signal loop response ($\Delta V_0/\Delta V_e$) versus frequency for the same example of Figure 12. The gains have all been normalized to zero dB at low frequency to reflect the actual difference in frequency response as slope compensation m is varied. At m = $-\frac{1}{2}$ m_2, an ideal single-pole roll-off at 6dB/octave is obtained. As higher ratios are used, the response approaches that of a double-pole with a 12dB/octave roll-off and associated 180° phase shift.

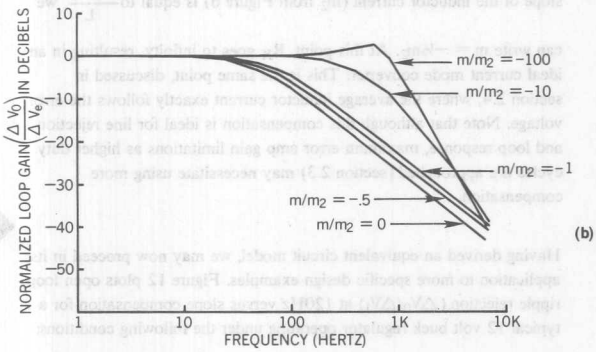
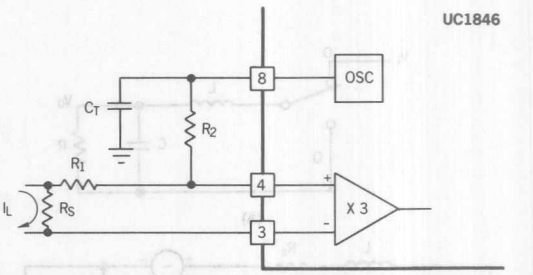


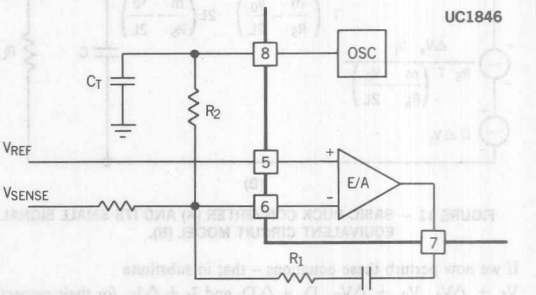
FIGURE 13 – NORMALIZED LOOP GAIN V.S. FREQUENCY FOR VARIOUS SLOPE COMPENSATION RATIO'S.

4.0 SLOPE COMPENSATING THE UC1846 CONTROL I.C.

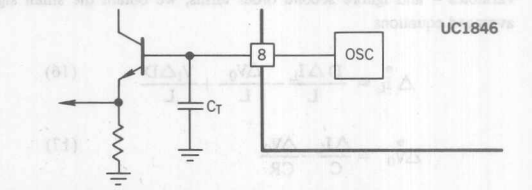
Implementing a practical, cost effective current-mode converter has recently been simplified with the introduction of the UC1846 integrated control chip. This I.C. contains all of the control and support circuitry required for the design of a fixed frequency current-mode converter. Figures 14A and B demonstrate two alternative methods of implementing slope compensation using the UC1846. Direct summing of the compensation and current sense signal at Pin 4 is easily accomplished, however, this introduces an error in the current limit sense circuitry. The alternative method is to introduce the compensation into the negative input terminal of the error amplifier. This will only work if (a) the gain of the error amplifier is fixed and constant at the switching frequency (R_1/R_2 for this case) and (b) both error amplifier and current amplifier gains are taken into consideration when calculating the required slope compensation. In either case, once the value of R_2 has been calculated, the loading effect on C_T can be determined and, if necessary, a buffer stage added as in Figure 14C.



(a) SUMMING OF SLOPE COMPENSATION DIRECTLY WITH SENSED CURRENT SIGNAL



(b) SUMMING OF SLOPE COMPENSATION WITH ERROR SIGNAL



(c) EMITTER FOLLOWER USED TO LOWER OUTPUT IMPEDANCE OF OSCILLATOR.

FIGURE 14 – ALTERNATIVE METHODS OF IMPLEMENTING SLOPE COMPENSATION WITH THE UC1846 CURRENT-MODE CONTROLLER.

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(4) W. Burns, A. Ohri, "Improving Off-Line Converter Performance with Current-Mode Control," Powercon 10 Proceedings, Paper B-2, 1983.

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UC3717 and L-C Filter Reduce EMI and Chopping Losses in Step Motor

A chopper drive which uses the inductance of the motor as the controlling element causes a temperature rise in the motor due to hysteresis and eddy current losses. For most motors, especially solid rotor constructions, this extra heat can force the designer to go to a larger motor and then derate it, or to a more expensive laminated construction in order to produce enough output torque for the job. Regardless of the motor type, *any* extra heat generated within a system will have to be removed or else other system components will be stressed unnecessarily. This could mean using a fan where convection cooling might otherwise have sufficed. In addition, the EMI generated from both the motor and its leads is of serious concern to the designer in view of ever-increasing EMI regulations.

These problems can be virtually eliminated by borrowing a simple technique from switching power supply designs, i.e., by placing a properly designed low-pass L-C filter across the output and using *this* L to control the UC3717. This removes the high frequency AC chopping losses in the motor by providing it with almost pure DC current. It also confines the EMI-causing, high frequency AC components to within the driver where they are easier to handle. This could allow increased wire lengths and possibly free up some design constraints, but remember that even though DC emits no EMI, the driver will still commutate the windings and can produce some components of frequency as high as 10 kHZ. The design of the L-C filter is straight-forward and its small additional cost can be recovered easily. The Unitrode UC3717, a complete chopper drive for one phase winding on a monolithic IC, makes the design job simple. The end result, a cooler running and EMI quieter step motor, can be achieved with just a few additional passive components.

Preliminary Considerations

For our analysis, we will use a "23" frame, bipolar motor with a solid rotor and the following specifications:

P_{max} =	9.0 Watts	= Maximum power dissipation at 25°C
V_{max} =	3.75 Volts	= Maximum voltage per motor phase at 25°C
I_{max} =	1.25 Amps	= Maximum current per motor phase at 25°C
R_m =	3.0 Ohms	= Resistance of one phase at 25°C
*L_m =	8.4 mH	= Inductance of one phase winding

*It should be noted that L_m, as given in a manufacturer's data sheet, is not always *true average* inductance as seen at high current in a circuit, but rather the inductance reading you would obtain from a low current inductance bridge. This value can differ from in-circuit inductance by a factor of 2 or more! The in-circuit inductance for this motor is 5.0 mH.

We begin by calculating the electrical time constant of one phase winding using the resistance value given above and the *actual* motor inductance:

$$\tau_m = \frac{L_m}{R_m} = \frac{5.0\ mH}{3.0\ Ohms} = 1.67\ msec \qquad (1)$$

If one were using a standard voltage drive then it would take approximately τ_m or 1.67 msec to reach the current level required for proper operation. This places a severe restriction on motor speed. Increasing the drive voltage will allow the motor to run faster but will cause it to draw too much current and overheat. Maximum motor speed may be increased by decreasing the time constant. Since L_m is fixed, the only parameter we can change is the effective value of R_m by placing a resistor in series with it. If we place a resistor 4 times R_m in series such that total R is 5 times R_m and increase the drive voltage by a factor of 5 then we will have reduced the time constant by a factor of 5 to 330 μsec and also increased both the maximum motor speed and maximum power output by a factor of 5 each. Unfortunately, we will have increased wasted power by a factor of 5 also.

The Chopper Drive

Using a chopper drive enables one to run at a higher voltage and thus reach proper operating current faster while still protecting the motor from excessive current that would otherwise flow due to the higher voltage. The high voltage is first applied across the motor winding and then, when I_{max} is reached, it is switched off. (If it were not switched off then the maximum current rating of the motor would be quickly exceeded.) The current is then allowed to circulate in a loop within the driver and motor for a fixed time period (t_{off}) after which the voltage is re-applied to the motor. The operating frequency, which is determined by both the motor inductance and t_{off} should be high enough that the resulting current ripple is small compared to the average DC current. Power efficiency is relatively high because there is no external resistor used.

Nothing is free in the world of physics, however, and the price one pays for the extra power output capability is an increase in wasted heat due to hysteresis and eddy current losses *within* the motor instead of in an external resistor. Being within the motor, it can now cause overheating as well as reliability problems. Since the excess heat increases rapidly with the overdrive ratio, this means that at low overdrive ratios (less than 5-to-1) there will be almost negligible heating, but at higher overdrive ratios (more than 10-to-1) the induced motor losses can beome as great as, or actually *exceed*, the I^2R losses! By placing a low-pass L-C filter in the circuit these induced losses can once again become negligible. The L and C components selected should be capable of operating at frequencies of 25 kHz or higher without heating effects in the inductor core or inductive effects in the capacitor.

UC3717 and L-C Filter

Designing with the UC3717

Using a supply voltage (v_s) of 40 volts (approximately a 10/1 overdrive), the turn-on rise-time becomes:

$$t_{rise} = -\tau_m \times \text{Ln}\,(1 - V_m/V_s) = -1.67 \times 10^{-3} \times \text{Ln}\,(1 - 3.75 / 40)$$
$$= 164\ \mu\text{sec} \qquad (2)$$

or *an improvement of approximately 10-to-1 in speed capability*.

Using an off-time (t_{off}) of 30 μsec as suggested on the UC3717 data sheet and limiting current (I_w) to 850 mA establishes a voltage across the resistive component of the winding ($V_{w\text{-}on}$) during the "on" time of:

$$V_{w\text{-}on} = I_w \times R_w = .85 \times 3.0 = 2.55 \text{ Volts} \qquad (3)$$

and during the "off" time (due to a 2.6 volt drop across the upper transistor, as shown in the data sheet, and a 0.4 volt drop across the Schottky "catch" diode) of:

$$V_{w\text{-}off} = V_{transistor} + V_{diode} = 2.6 + 0.4 = 3.0 \text{ Volts} \qquad (4)$$

Since the voltage and current changes are small, we can substitute a resistance (R_e) equivalent to $V_{w\text{-}off}/I_w$ in series with R_w to adjust the time constant and allow us to calculate the approximate current ripple (ΔI_w) during t_{off}:

$$\Delta I_w = I_w \left(1 - \exp\left[\frac{-t_{off}(R_w + R_e)}{L_m}\right]\right)$$
$$= .85 \times \left(1 - \exp\left[\frac{-30\text{x}10^{-6} \times (3.0 + 3.5)}{5\text{x}10^{-3}}\right]\right)$$
$$= 33 \text{ mA p-p} \qquad (5)$$

Knowing ΔI_w, we can now calculate the on-time (t_{on}):

$$t_{on} = \frac{\Delta I_w \times L_m}{V_s - V_{w\text{-}on}} = \frac{33\text{x}10^{-3} \times 5\text{x}10^{-3}}{40 - 2.55} = 4.4\ \mu\text{sec} \qquad (6)$$

and can also find our operating frequency (f) by:

$$f = 1 / (t_{on} + t_{off}) = 1 / (4.4 + 30) \times 10^{-6} = 29.1 \text{ kHz} \qquad (7)$$

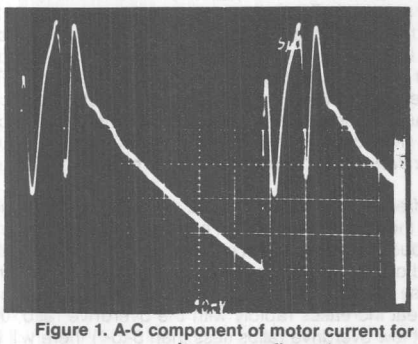


Figure 1. A-C component of motor current for standard chopper configuration.

Since this frequency is well above audible ranges, it will not cause any objectionable sound, but there are still the problems of EMI and excess motor heating to deal with. It is possible to generate EMI due to the current switching that occurs in the motor leads because they carry not only the primary frequency, but also many higher harmonics as well, so they require careful routing, shielding, or both. We can put in a low pass L-C filter to remove these high frequencies and still pass normal commutation currents without any significant loss of motor performance.

Design of the L-C Filter

Figure 2 is a block diagram of a motor connected to 2 UC3717s with the low-pass L-C filters in place.

Again we will use a current of 850 mA in each winding, an off-time of 30 μsec, and an on-time of 4.4 μsec but now we will use an

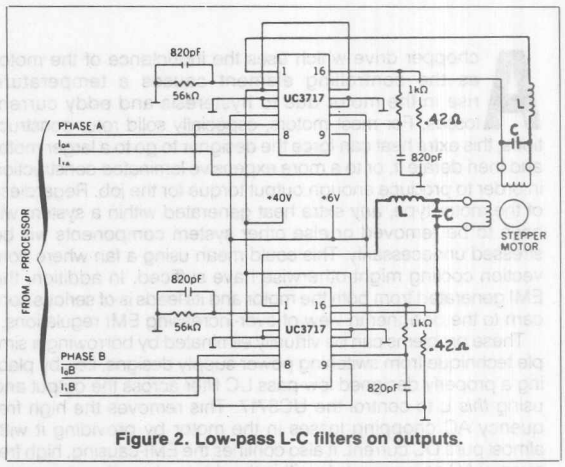


Figure 2. Low-pass L-C filters on outputs.

external inductance (L) to control the chopping. V_{drop} is the sum of the source (V_{so}) and sink (V_{si}) voltage drops at 850 mA:

$$V_{drop} = V_{so} + V_{si} + V_{sense} = (2.6 + 1.9 + 0.36)$$
$$= 4.9 \text{ volts} \qquad (8)$$

In order to minimize the effects of L on the motor current risetime we will make it 10 times smaller than L_m or 500 μH. In order to keep the peak current in the UC3717 below 1 amp we will use a 0.42 ohm sense resistor and also limit $_{\Delta}I_L$ to 300 mA. Using a variation of equation (6) we can check that:

$$L = \frac{(V_s - V_{drop}) \times t_{on}}{{}_{\Delta}I_L} = \frac{(40 - 4.9) \times 4.4\text{x}10^{-6}}{300\text{x}10^{-3}} = 515\ \mu\text{H} \qquad (9)$$

is in keeping with the constraints outlined above.

Similarly, we would like to find a value for the capacitor (C) such that it will have less than 1/10 the impedance of L at 29.1 kHz:

$$C = \frac{10}{(2 \times \pi \times f)^2 \times L} = \frac{10}{(2 \times 3.14 \times 29100)^2 \times 500\text{x}10^{-6}} \qquad (10)$$
$$= 0.6\ \mu\text{F}$$

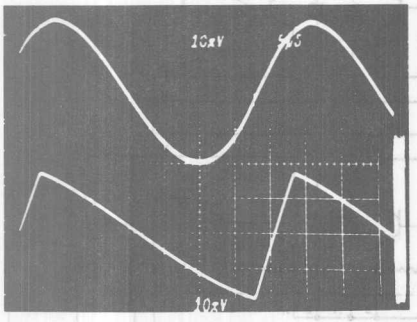
The test motor and driver, operated unloaded (nothing connected to the output shaft) and in the configuration of *Figure 2*, used values of 500 μH for the inductor and 0.47 μF for the capacitor. *Figure 1* and *Figures 3* through *6* are waveforms obtained from that motor.

The lower trace of *Figure 3* (*Figure 3b*) shows the 330 mA current sawtooth in the inductor, while the upper trace (*Figure 3a*) shows an 8 mA p-p current ripple in the motor winding. While this may seem to indicate only a 12 dB reduction in EMI over *Figure 1*, comparing the *sinusoidal* waveform of *Figure 3a* to the "noisy" *sawtooth* waveform of *Figure 1* will quickly point out sources of

UC3717 and L-C Filter

EMI. In *Figure 1*, the oscillations immediately following each switch of the driver are due to the motor's distributed capacitance resonating with its inductance and are a possible source of EMI. In addition, sharp current spikes are allowed to pass along the motor leads and through the motor's distributed capacitance unhindered, thus creating high frequency EMI. EMI spikes were virtually eliminated from *Figure 3a* by using a low ESR capacitor and connecting the motor leads close to the body of the capacitor.

Figure 4 shows motor current superimposed over the inductor current. Just to the left of the center graticle line a ringing occurs in the inductor current that also appears in the motor current, although attenuated. This ringing occurs at a frequency of:



a) VERT = 2 mA / DIV A-C component of Motor Current with L-C filter.

b) VERT = 100 mA / DIV A-C component of inductor current with L-C filter.

HORIZ = 5 µS / DIV

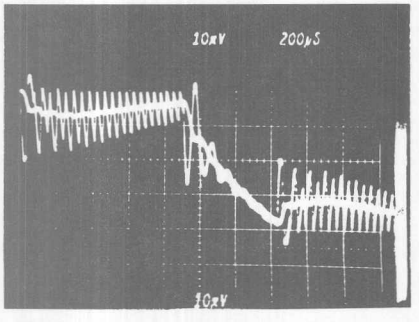
Figure 3. Motor and inductor current waveforms.

$$f_{res} = 1 / 2\pi\sqrt{L \times C} = 1 / 6.28 \times \sqrt{500\times10^{-6} \times 0.47\times10^{-6}} = 10.4 \text{ kHz} \quad (11)$$

which is the resonant frequency of the L-C filter. This frequency can be lowered by increasing the value of either L or C, although at a cost of reducing the high speed performance of the motor.

The high frequency sawtooth waveforms at the upper, flat portion of the motor current waveform are the 29.1 kHz chopping currents in the inductor. They cause a small corresponding ripple in the motor current but, because the chopping frequency is more than twice the break frequency of the 2-pole L-C filter, we would expect, and can see, an attenuation greater than 12 dB.

In a 2 phase step motor (sometimes referred to as a 4 phase step motor because of the 4 windings used in the unipolar version) the STEP RATE, in full steps per second (FSPS), is 4 times the primary frequency of the motor current waveform. The two phases of the step motor are operated in quadrature and thus will generate 4 distinct states in the 2 phases which correspond to 4 mechanical steps for each electrical cycle.



VERT = 500 mA / DIV

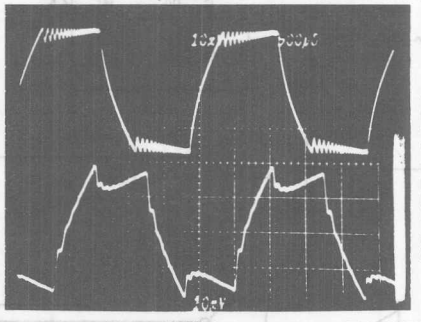
HORIZ = 200 mS / DIV

Figure 4. Filter current waveform superimposed over motor current waveform.

FSPS = 4 x frequency (for a 2 or "4" phase step motor) (12)

It is important to note at this time that 10.4 kHz is the highest *frequency* that can be passed to this motor without attenuation using the selected components, but that this corresponds to a *step rate* of 41,600 FSPS! The test motor was able to run at 17,000 full steps per second with the L-C filter in place, which is high enough for most situations.

Figures 5 and *6* are current waveforms for the motor running at 1600 FSPS and 16,000 FSPS respectively. The motor was operated with the L-C filter on only the lower trace winding so that the waveforms could be compared easily. Looking at *Figure 5*, one can see that the leading edges of both waveforms have the same risetimes, although the filtered one has more suscepibility toward ringing. From *Figure 6*, one can see that torque is down only 3 dB at 16,000 FSPS and that there are "glitches" in the unfiltered waveform that do not appear in the filtered waveforms.

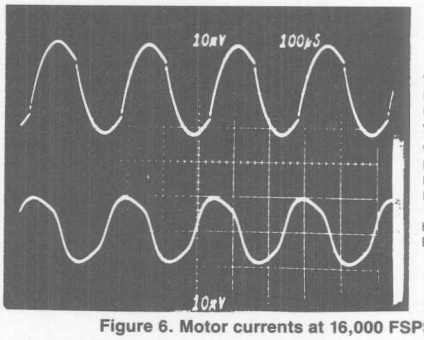


VERT = 500mA / DIV
Motor current without L-C filter.

VERT = 500mA / DIV
Motor current with L-C filter.

HORIZ = 500µS / DIV

Figure 5. Motor currents at 1600 FSPS.



VERT = 500mA / DIV
Motor current without L-C filter.

VERT = 500 mA / DIV
Motor current with L-C filter.

HORIZ = 100 mS / DIV

Figure 6. Motor currents at 16,000 FSPS.

Conclusions

The use of a low-pass filter can be an effective heat and EMI reduction mechanism when used with a step motor chopper driver such as the UC3717. The price one pays for a "clean" EMI environment is a *small* loss in very high speed performance. The technique may be applied equally well to non-IC chopper drivers but the peak currents must be accounted for and the minimum value of L adjusted accordingly. 500 µH is the smallest practical L that should be used with the UC3717 since we do not want the

UC3717 and L-C Filter

peak of the ripple to exceed 1.0 amps. This limits the usefulness of the technique to motors with inductances of 2 mH or more. At average currents less than 300 mA, the value of L may have to be larger in order to maintain continuous current in the inductor, but the physical size may be decreased. If an average current in excess of 850 mA is required, then a power amplifier may be added as shown in *Figure 7*. This will extend the peak current capabilities of the chopper drive to higher current and will also allow the value of L to be decreased.

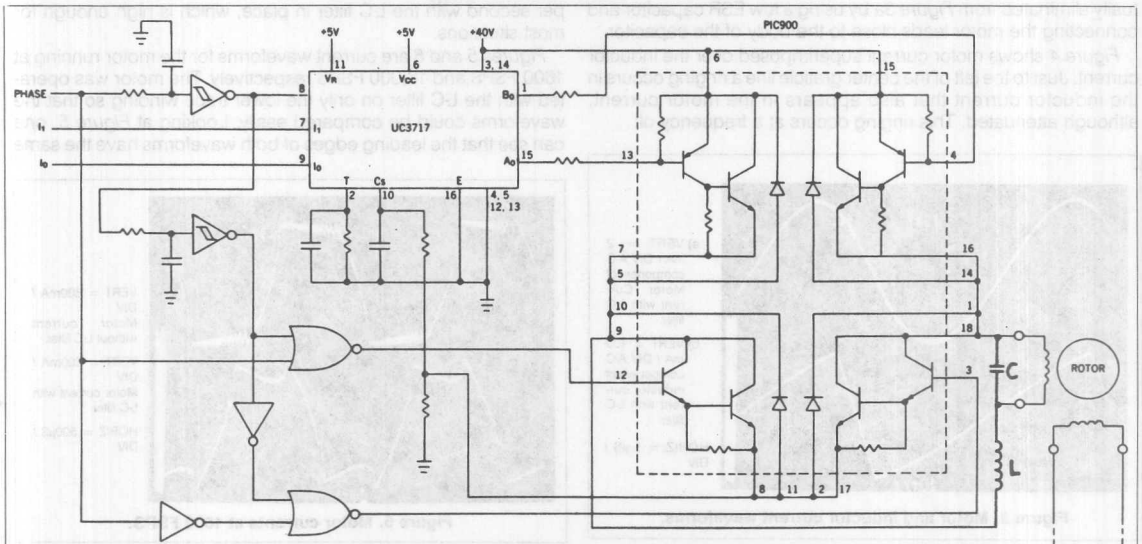


Figure 7. UC3717 chopper drive with PIC900B Power Amplifier on one phase of step motor.

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APPLICATION NOTE

UC3842/3/4/5 PROVIDES LOW-COST CURRENT-MODE CONTROL

INTRODUCTION

The fundamental challenge of power supply design is to simultaneously realize two conflicting objectives: good electrical performance and low cost. The UC3842/3/4/5 is an integrated pulse width modulator (PWM) designed with both these objectives in mind. This IC provides designers an inexpensive controller with which they can obtain all the performance advantages of current mode operation. In addition, the UC3842 series is optimized for efficient power sequencing of off-line converters, DC to DC regulators and for driving power MOSFETs or transistors.

This application note provides a functional description of the UC3842 family and highlights the features of each individual member, the UC3842, UC3843, UC3844 and UC3845. Throughout the text, the UC3842 part number will be referenced, however the generalized circuits and performance characteristics apply to each member of the UC3842 series unless otherwise noted. A review of current mode control and its benefits is included and methods of avoiding common pitfalls are mentioned. The final section presents designs of power supplies utilizing UC3842 control.

CURRENT-MODE CONTROL

Figure 1 shows the two-loop current-mode control system in a typical buck regulator application. A clock signal initiates power pulses at a fixed frequency. The termination of each pulse occurs when an analog of the inductor current reaches a threshold established by the error signal. In this way the error signal actually controls peak inductor current. This contrasts with conventional schemes in which the error signal directly controls pulse width without regard to inductor current.

Several performance advantages result from the use of current-mode control. First, an input voltage feed-forward characteristic is achieved; i.e., the control circuit instantaneously corrects for input voltage variations without using up any of the error amplifier's dynamic range. Therefore, line regulation is excellent and the error amplifier can be dedicated to correcting for load variations exclusively.

For converters in which inductor current is continuous, controlling peak current is nearly equivalent to controlling average current. Therefore, when such converters employ current-mode control, the inductor can be treated as an

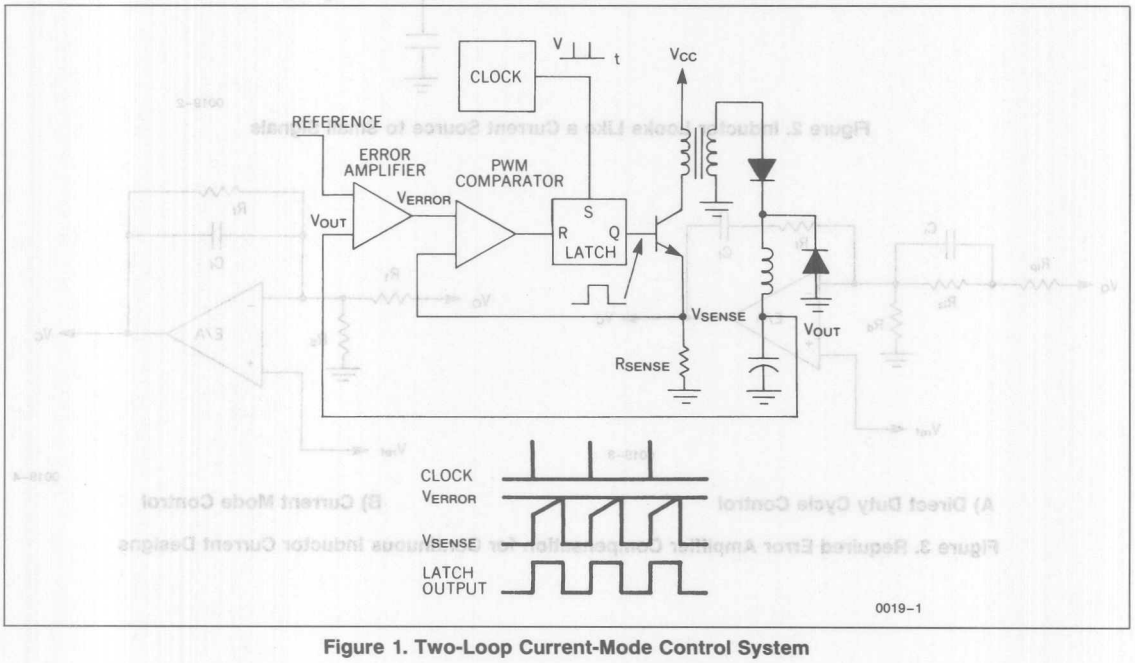


Figure 1. Two-Loop Current-Mode Control System

error-voltage-controlled-current-source for the purposes of small-signal analysis. This is illustrated by Figure 2. The two-pole control-to-output frequency response of these converters is reduced to a single-pole (filter capacitor in parallel with load) response. One result is that the error amplifier compensation can be designed to yield a stable closed-loop converter response with greater gainbandwidth than would be possible with pulse-width control, giving the supply improved small-signal dynamic response to changing loads. A second result is that the error amplifier compensation circuit becomes simpler, as illustated in Figure 3. Capacitor C_i and resistor R_{iz} in Figure 3a add a low frequency zero which cancels one of the two control-to-output poles of non-current-mode converters. For large-signal load changes, in which converter response is limited by inductor slew rate, the error amplifier will saturate while the inductor is catching up with the load. During this time, C_i will charge to an abnormal level. When the inductor current reaches its required level, the voltage on C_i causes a corresponding error in supply output voltage. The recovery time is $R_{iz}C_i$, which may be quite long. However, the compensation network of Figure 3b can be used where current-mode control has eliminated the inductor pole. Large-signal dynamic response is then greatly improved due to the absence of C_i.

Current limiting is greatly simplified with current-mode control. Pulse-by-pulse limiting is, of course, inherent in the control scheme. Furthermore, an upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

Finally, current-mode controlled power stages can be operated in parallel with equal current sharing. This opens the possibility of a modular approach to power supply design.

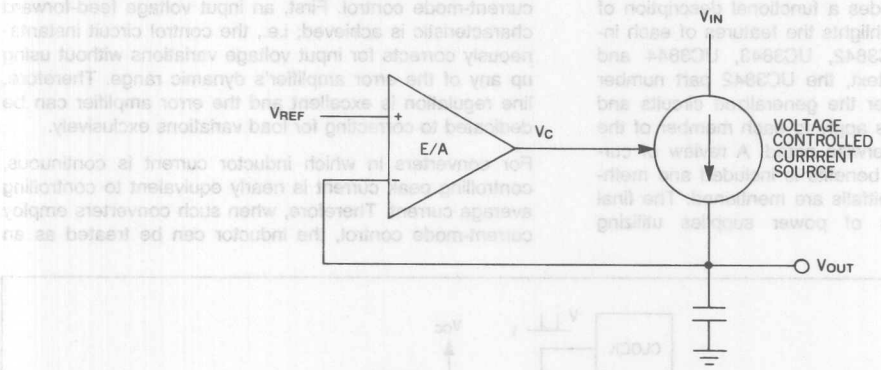
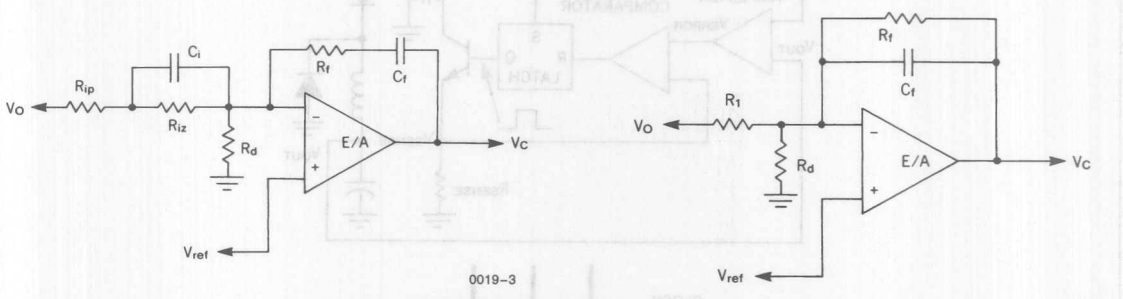


Figure 2. Inductor Looks Like a Current Source to Small Signals



A) Direct Duty Cycle Control **B) Current Mode Control**

Figure 3. Required Error Amplifier Compensation for Continuous Inductor Current Designs

THE UC3842/3/4/5 SERIES OF CURRENT-MODE PWM IC'S

DESCRIPTION

The UC1842/3/4/5 family of control ICs provides the necessary features to implement off-line or DC to DC fixed frequency current mode control schemes with a minimal external parts count. Internally implemented circuits include under-voltage lockout featuring start up current less than 1 mA, a precision reference trimmed for accuracy at the error amp input, logic to insure latched operation, a PWM comparator which also provides current limit control, and a totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving either N Channel MOSFETs or bipolar transistor switches, is low in the off state.

Differences between members of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC1842 and UC1844 have UVLO thresholds of 16V (on) and 10V (off), ideally suited to off-line applications. The corresponding thresholds for the UC1843 and UC1845 are 8.5V and 7.9V. The UC1842 and UC1843 can operate to duty cycles approaching 100%. A range of zero to <50% is obtained by the UC1844 and UC1845 by the addition of an internal toggle flip flip which blanks the output off every other clock cycle.

FEATURES

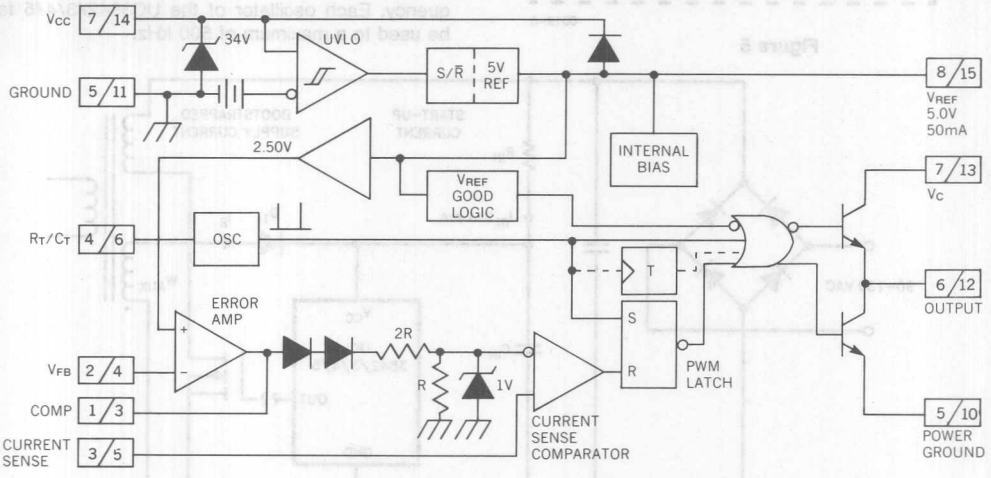
- Optimized for Off-Line and DC to DC Converters
- Low Start Up Current (<1 mA)
- Automatic Feed Forward Compensation
- Pulse-By-Pulse Current Limiting
- Enhanced Load Response Characteristics
- Under-Voltage Lockout with Hysteresis
- Double Pulse Suppression
- High Current Totem Pole Output
- Internally Trimmed Bandgap Reference
- 500 kHz Operation
- Low R_O Error Amp

IC SELECTION GUIDE

UVLO START	MAXIMUM DUTY CYCLE	
	<50%	<100%
8.5V	UC3845	UC3843
16V	UC3844	UC3842

RECOMMENDED USAGE

APPLICATION (CIRCUIT)	POWER SUPPLY INPUT (V)	
	HIGH (OFFLINE)	LOW (DC/DC)
FLYBACK	UC3844	UC3845
FORWARD	UC3844/2	UC3845/3
BUCK/BOOST	UC3842/4	UC3843/5



Note: 1. A/B A = DIL-8 Pin Number. B = SO-16 Pin Number.
2. Toggle flip flop used only in 1844A and 1845A.

Figure 4

3 APPLICATION NOTES

UNDER-VOLTAGE LOCKOUT

The UVLO circuit insures that V_{CC} is adequate to make the UC3842/3/4/5 fully operational before enabling the output stage. Figure 5 shows that the UVLO turn-on and turn-off thresholds are fixed internally at 16V and 10V respectively. The 6V hysteresis prevents V_{CC} oscillations during power sequencing. Figure 6 shows supply current requirements. Start-up current is less than 1 mA for efficient bootstrapping from the rectified input of an off-line converter, as illustrated by Figure 6. During normal circuit operation, V_{CC} is developed from auxiliary winding W_{AUX} with D_1 and C_{IN}. At start-up, however, C_{IN} must be charged to 16V through R_{IN}. With a start-up current of 1 mA, R_{IN} can be as large as 100 kΩ and still charge C_{IN} when V_{AC} = 90V RMS (low line). Power dissipation in R_{IN} would then be less than 350 mW even under high line (V_{AC} = 130V RMS) conditions.

During UVLO; the output driver is in a low state. While it doesn't exhibit the same saturation characteristics as normal operation, it can easily sink 1 milliamp, enough to insure the MOSFET is held off.

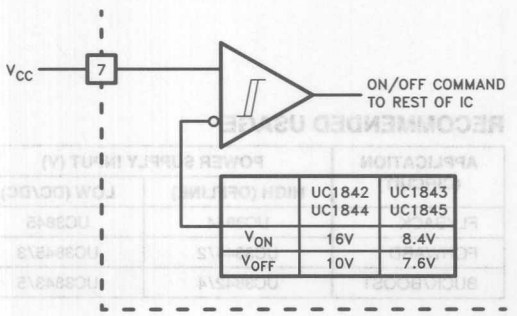


Figure 5

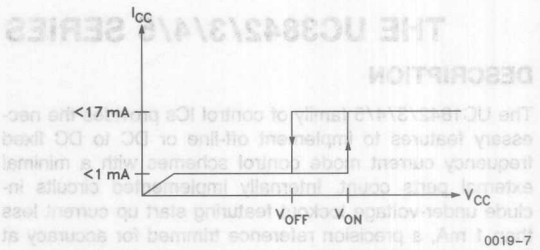


Figure 6. During Under-Voltage Lockout, the output driver is biased to sink minor amounts of current.

OSCILLATOR

The UC3842 oscillator is programmed as shown in Figure 8. Timing capacitor C_T is charged from V_{REF} (5V) through the timing resistor R_T, and discharged by an internal current source.

The first step in selecting the oscillator components is to determine the required circuit deadtime. Once obtained, Figure 9 is used to pinpoint the nearest standard value of C_T for a given deadtime. Next, the appropriate R_T value is interpolated using the parameters for C_T and oscillator frequency. Figure 10 illustrates the R_T/C_T combinations versus oscillator frequency. The timing resistor can be calculated from the following formula.

$$F_{OSC}\ (kHz) = 1.72 / (R_T\ (k) \times C_T\ (\mu f))$$

The UC3844 and UC3845 have an internal divide-by-two flip-flop driven by the oscillator for a 50% maximum duty cycle. Therefore, their oscillators must be set to run at twice the desired power supply switching frequency. The UC3842 and UC3843 oscillator runs AT the switching frequency. Each oscillator of the UC3842/3/4/5 family can be used to a maximum of 500 kHz.

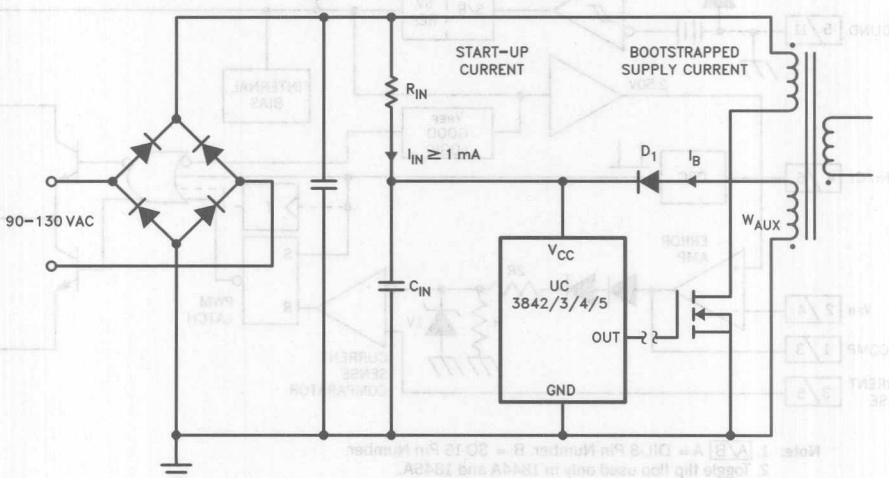


Figure 7. Providing Power to the UC3842/3/4/5

MAXIMUM DUTY CYCLE

The UC3842 and UC3843 have a maximum duty cycle of approximately 100%, whereas the UC3844 and UC3845 are clamped to 50% maximum by an internal toggle flip flop. This duty cycle clamp is advantageous in most flyback and forward converters. For optimum IC performance the deadtime should not exceed 15% of the oscillator clock period.

During the discharge, or "dead" time, the internal clock signal blanks the output to the low state. This limits the maximum duty cycle D_{MAX} to:

$D_{MAX} = 1 - (t_{DEAD} / t_{PERIOD})$ UC3842/3

$D_{MAX} = 1 - (t_{DEAD} / 2 \times t_{PERIOD})$ UC3844/5

where $T_{PERIOD} = 1 / F$ oscillator

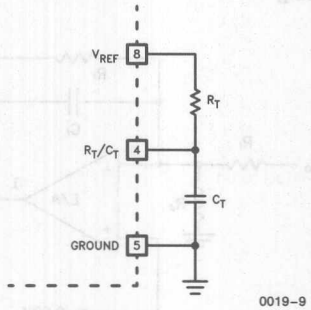


Figure 8

Deadtime vs C_T (R_T > 5k)

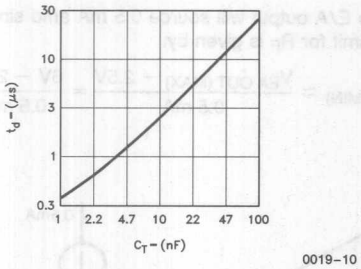


Figure 9

Timing Resistance vs Frequency

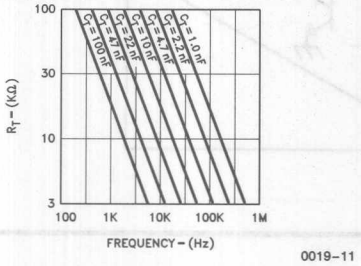


Figure 10

CURRENT SENSING AND LIMITING

The UC3842 current sense input is configured as shown in Figure 12. Current-to-voltage conversion is done externally with ground-referenced resistor R_S. Under normal operation the peak voltage across R_S is controlled by the E/A according to the following relation:

$$I_P = \frac{V_C - 1.4V}{3\,R_S}$$

where V_C = control voltage = E/A output voltage.

R_S can be connected to the power circuit directly or through a current transformer, as **Figure 11** illustrates. While a direct connection is simpler, a transformer can reduce power dissipation in R_S, reduce errors caused by the base current, and provide level shifting to eliminate the restraint of ground-referenced sensing. The relation between V_C and peak current in the power stage is given by:

$$i_{(pk)} = N\left(\frac{V_{RS(pk)}}{R_S}\right) = \frac{N}{3\,R_S}\left(V_C - 1.4V\right)$$

where: N = current sense transformer turns ratio
= 1 when transformer not used.

For purposes of small-signal analysis, the control-to-sensed-current gain is:

$$\frac{i_{(pk)}}{V_C} = \frac{N}{3\,R_S}$$

When sensing current in series with the power transistor, as shown in Figure 11, the current waveform will often have a large spike at its leading edge. This is due to rectifier recovery and/or inter-winding capacitance in the power transformer. If unattenuated, this transient can prematurely terminate the output pulse. As shown, a simple RC filter is usually adequate to suppress this spike. The RC time constant should be approximately equal to the current spike duration (usually a few hundred nanoseconds).

The inverting input to the UC3842 current-sense comparator is internally clamped to 1V (Figure 12). Current limiting occurs if the voltage at pin 3 reaches this threshold value, i.e., the current limit is defined by:

$$i_{max} = \frac{N \times 1V}{R_s}$$

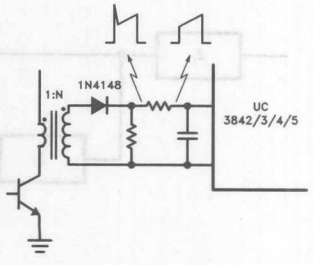


Figure 11. Transformer-Coupled Current Sensing

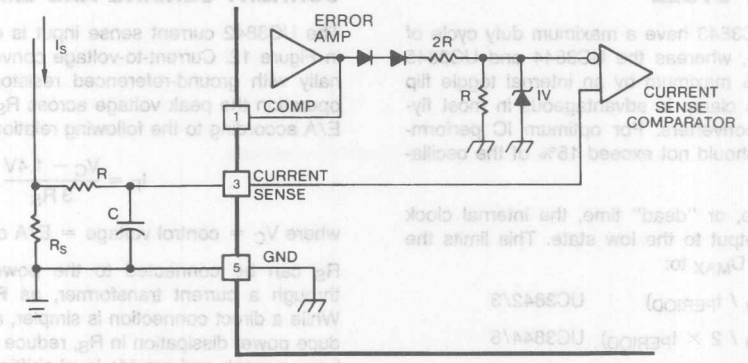


Figure 12. Current Sensing

ERROR AMPLIFIER

The error amplifier (E/A) configuration is shown in Figure 13. The non-inverting input is not brought out to a pin, but is internally biased to 2.5V ± 2%. The E/A output is available at pin 1 for external compensation, allowing the user to control the converter's closed-loop frequency response.

Figure 14 shows an E/A compensation circuit suitable for stabilizing any current-mode controlled topology except for flyback and boost converters operating with inductor current. The feedback components add a pole to the loop transfer function at $f_P = 1/2\pi\ R_F,C_F$. R_F and C_F are chosen so that this pole cancels the zero of the output filter capacitor ESR in the power circuit. R_I and R_F fix the low-frequency gain. They are chosen to provide as much gain as possible while still allowing the pole formed by the output filter capacitor and load to roll off the loop gain to unity (0 dB) at $f \approx f_{SWITCHING}/4$. This technique insures converter stability while providing good dynamic response.

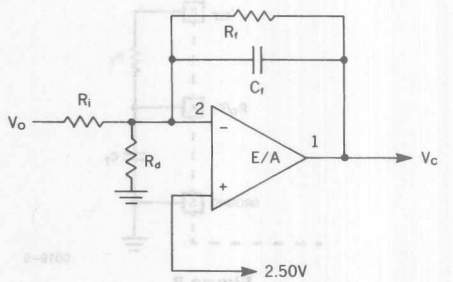


Figure 14. Compensation

The E/A output will source 0.5 mA amd sink 2 mA. A lower limit for R_F is given by:

$$R_{F(MIN)} \approx \frac{V_{EA\ OUT\ (MAX)} - 2.5V}{0.5\ mA} = \frac{6V - 2.5V}{0.5\ mA} = 7\ k\Omega.$$

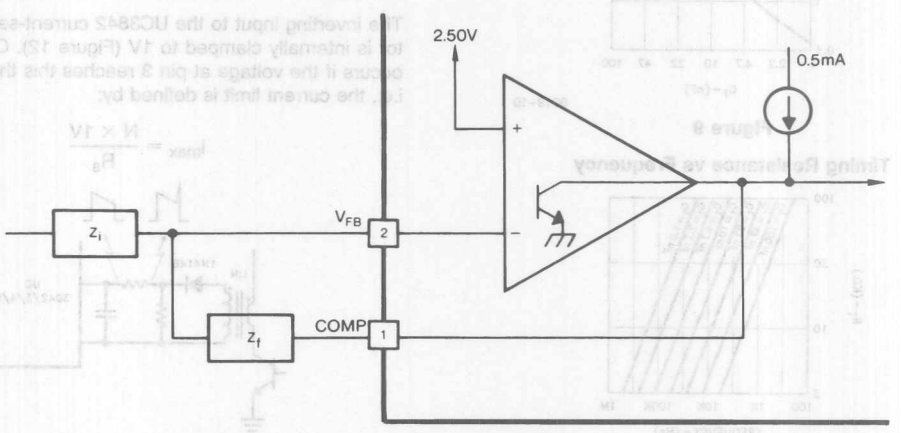


Figure 13. E/A Configuration

E/A input bias curret (2 μA max) flows through R_I, resulting in a DC error in output voltage (V_O) given by:

$\Delta V_{O(MAX)} = (2\ \mu A)\ R_I$,

It is therefore desirable to keep the value of R_I, as low as possible.

Figure 15 shows the open-loop frequency response of the UC3842 E/A. The gain represents an upper limit on the gain of the compensated E/A. Phase lag increases rapidly as frequency exceeds 1 MHz due to second-order poles at ~10 MHz and above.

Continuous-inductor-current boost and flyback converters each have a right-half-plane zero in their transfer function. An additional compensation pole is needed to roll off loop gain at a frequency less than that of the RHP zero. R_P and C_P in the circuit of Figure 16 provide this pole.

TOTEM-POLE OUTPUT

The UC3842 PWM has a single totem-pole output which can be operated to ±1 amp peak for driving MOSFET gates, and a ±200 mA average current for bipolar power transistors. Cross conduction between the output transistors is minimal, the average added power with V_{IN} = 30V is only 80 mW at 200 kHz.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage V_C by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole switching and the FET gate capacitance.

The use of a Schottky diode from the PWM output to ground will prevent the output voltage from going excessively below ground, causing instabilities within the IC. To be effective, the diode selected should have a forward drop of less than 0.3V at 200 mA. Most 1- to 3-amp Schottky diodes exhibit these traits above room temperature. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Implementation of the complete drive scheme is shown in the following diagrams. Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circum-

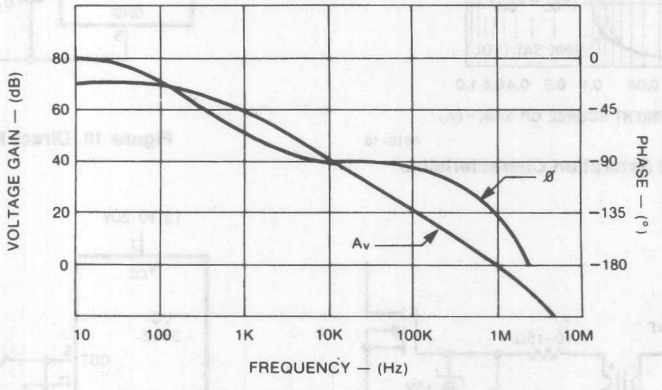


Figure 15. Error Amplifier Open-Loop Frequency Response

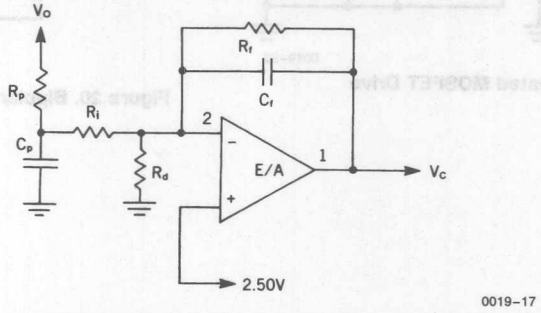


Figure 16. E/A Compensation Circuit for Continuous Boost and Flyback Topologies

stances from occurring on the PWM output. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Figures 18, 19 and 20 show suggested circuits for driving MOSFETs and bipolar transistors with the UC3842 output. The simple circuit of Figure 18 can be used when the control IC is not electrically isolated from the MOSFET turn-on and turn-off to ±1 amp. It also provides damping for a parasitic tank circuit formed by the FET input capacitance and series wiring inductance. Schottky diode D1 prevents the output of the IC from going far below ground during turn-off.

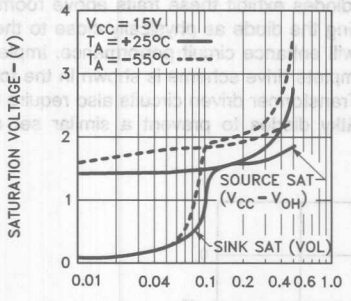


Figure 17. Output Saturation Characteristics

Figure 19 shows an isolated MOSFET drive circuit which is appropriate when the drive signal must be level shifted or transmitted across an isolation boundary. Bipolar transistors can be driven efficiently with the circuit of Figure 20. Resistors R_1 and R_2 fix the on-state base current while capacitor C_1 provides a negative base current pulse to remove stored charge at turn-off.

Since the UC3842 series has only a single output, an interface circuit is needed to control push-pull half or full bridge topologies. The UC3706 dual output driver with internal toggle flip-flop performs this function. A circuit example at the end of this paper illustrates a typical application for these two ICs. Increased drive capability for driving numerous FETs in parallel, or other loads can be accomplished using one of the UC3705/6/7 driver ICs.

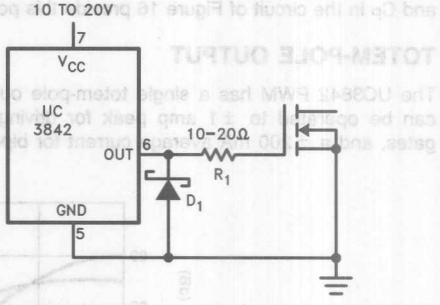


Figure 18. Direct MOSFET Drive

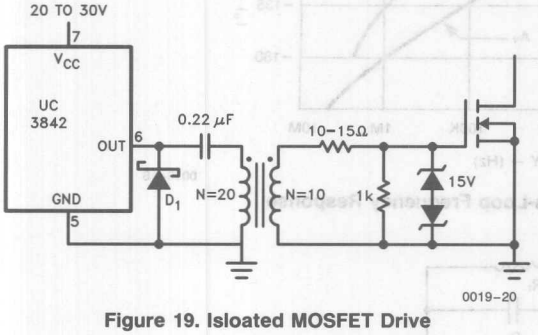


Figure 19. Isloated MOSFET Drive

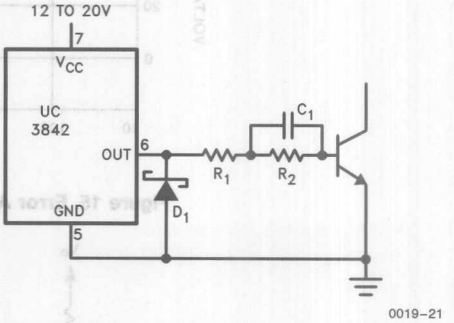


Figure 20. Bipolar Drive with Negative Turn-Off Bias

NOISE

As mentioned earlier, noise on the current sense or control signals can cause significant pulse-width jitter, particularly with continuous-inductor-current designs. While slope compensation helps alleviate this problem, a better solution is to minimize the amount of noise. In general, noise immunity improves as impedances decrease at critical points in a circuit.

One such point for a switching supply is the ground line. Small wiring inductances between various ground points on a PC board can support common-mode noise with sufficient amplitude to interfere with correct operation of the modulating IC. A copper ground plane and separate return lines for high-current paths greatly reduce common-mode noise. Note that the UC3842 has a single ground pin. High sink currents in the output therefore cannot be returned separately.

Ceramic monolythic bypass capacitors (0.1 μF) from V_{CC} and V_{REF} to ground will provide low-impedance paths for high frequency transients at those points. The input to the error amplifier, however, is a high-impedance point which cannot be bypassed without affecting the dynamic response of the power supply. Therefore, care should be taken to lay out the board in such a way that the feedback path is far removed from noise generating components such as the power transistor(s).

Figure 21 illustrates another common noise-induced problem. When the power transistor turns off, a noise spike is coupled to the oscillator R_T/C_T terminal. At high duty cycles the voltage at R_T/C_T is approaching its threshold level (~2.7V, established by the internal oscillator circuit) when this spike occurs. A spike of sufficient amplitude will prematurely trip the oscillator as shown by the dashed lines. In order to minimize the noise spike, choose C_T as large as possible, remembering that deadtime increases with C_T. It is recommended that C_T never be less than ~1000 pF. Often the noise which causes this problem is caused by the output (pin 6) being pulled below ground at turn-off by external parasitics. This is particularly true when driving MOSFETs. A Schottky diode clamp from ground to pin 6 will prevent such output noise from feeding to the oscillator. If these measures fail to correct the probelm, the oscillator frequency can always be stabilized with an external clock. Using the circuit of Figure 31 results in an R_T/C_T waveform like that of Figure 21B. Here the oscillator is much more immune to noise because the ramp voltage never closely approaches the internal threshold.

SYNCHRONIZATION

The simplest method to force synchronization utilizes the timing capacitor (C_T) in near standard configuration. Rather than bring C_T to ground directly, a small resistor is placed in series with C_T to ground. This resistor serves as the input for the sync pulse which raises the C_T voltage above the oscillator's internal upper threshold. The PWM is allowed to run at the frequency set by R_T and C_T until the sync pulse appears. This scheme offers several advantages including having the local ramp available for slope compensation. The UC3842/3/4/5 oscillator

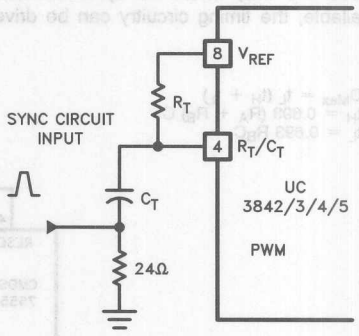


Figure 22. Sync Circuit Implementation

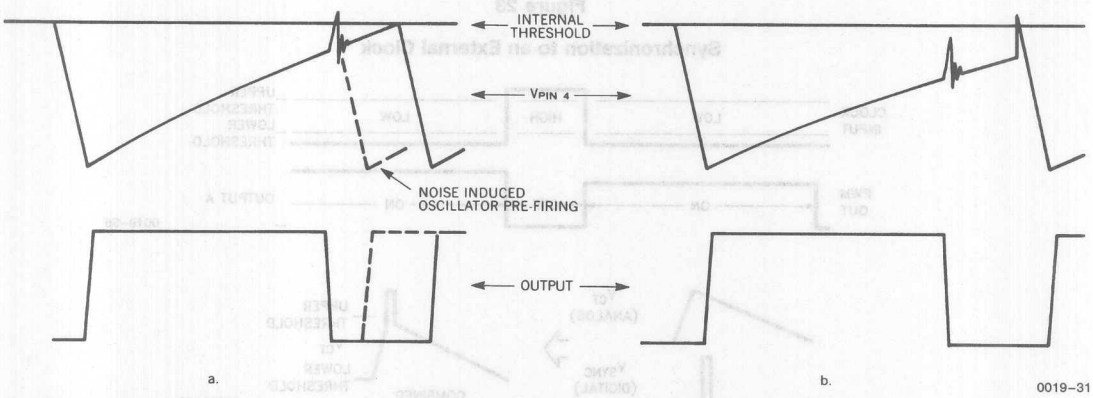


Figure 21. (a.) Noise on Pin 4 can cause oscillator to pre-trigger.
(b.) With external sync., noise does not approach threshold level.

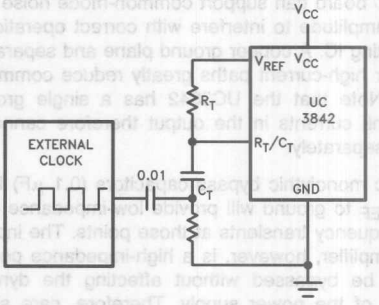
must be set to a lower frequency than the sync pulse stream, typically 20 percent with a 0.5V pulse applied across the resistor. Further information on synchronization can be found in "Practical Considerations in Current Mode Power Supplies" listed in the reference appendix.

The UC3842 can also be synchronized to an external clock source through the R_T/C_T terminal (Pin 4) as shown in Figure 23.

In normal operation, the timing capacitor C_T is charged between two thresholds, the upper and lower comparator limits. As C_T begins its charge cycle, the output of the PWM is initiated and turns on. The timing capacitor continues to charge until it reaches the upper threshold of the internal comparator. Once intersected, the discharge circuitry activates and discharges C_T until the lower threshold is reached. During this discharge time the PWM output is disabled, thus insuring a "dead" or off time for the output.

A digital representation of the oscillator charge/discharge status can be utilized as an input to the R_T/C_T terminal. In instances like this, where no synchronization port is easily available, the timing circuitry can be driven from a digital logic input rather than the conventional analog mode. The primary considerations of on-time, dead-time, duty cycle and frequency can be encompassed in the digital pulse train input.

A LOW logic level input determines the PWM maximum ON time. Conversely, a HIGH input governs the OFF, or dead time. Critical constraints of frequency, duty cycle or dead time can be acurately controlled by anything from a 555 timer to an elaborate microprocessor controlled software routine.



$D_{Max} = t_L (t_H + t_L)$
$t_H = 0.693 (R_A + R_B) C$
$t_L = 0.693 R_B C$

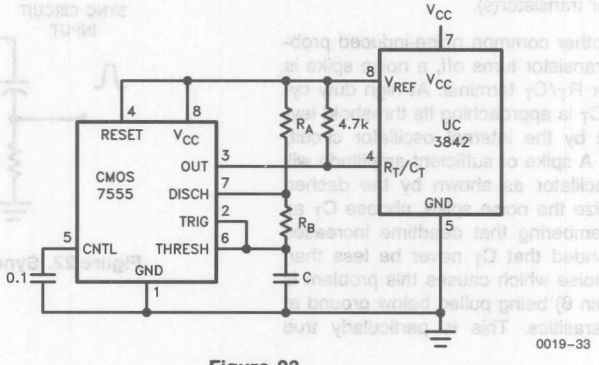


Figure 23

Synchronization to an External Clock

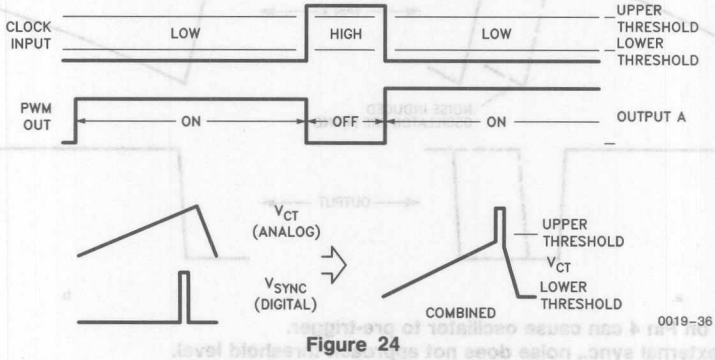


Figure 24

SYNC PULSE GENERATOR

The UC3842/3/4/5 oscillator can be used to generate sync pulses with a minimum of external components. This simple circuit shown in Figure 25 triggers on the falling edge of the C_T waveform, and generates the sync pulse required for the previously mentioned synchronization scheme. Triggered by the master's deadtime, this circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave(s). The photos shown in Figures 26 and 27 depict the circuit waveforms of interest.

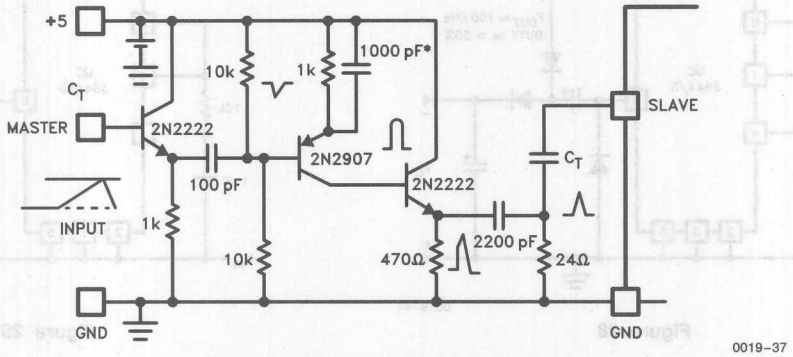
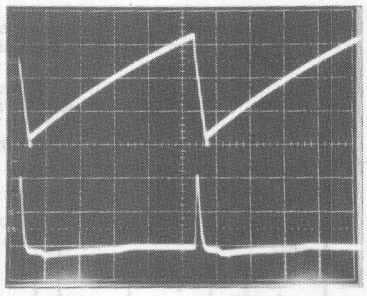


Figure 25. Sync Pulse Generator Circuit



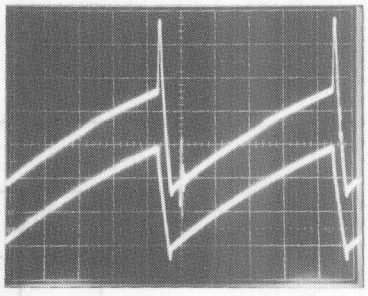
Top Trace:
Circuit Input

Bottom Trace:
Circuit Output
Across 24 Ohms

Vertical: 0.5V/CM Both
Horizontal: 0.5μS/CM

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Figure 26. Operating Waveforms at 500 kHz



Top Trace:
Slave C_T

Bottom Trace:
Master C_T

Vertical: 0.5V/CM Both
Horizontal: 0.5μS/CM

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Figure 27. Master/Slave Sync Waveforms at C_T

CHARGE PUMP CIRCUITS
LOW POWER DC/DC CONVERSION

Step Up

$V_O \approx 2 \times V_{IN}$

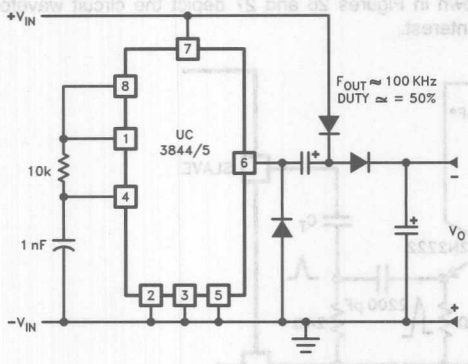


Figure 28

Inverting

$V_O \approx -V_{IN}$

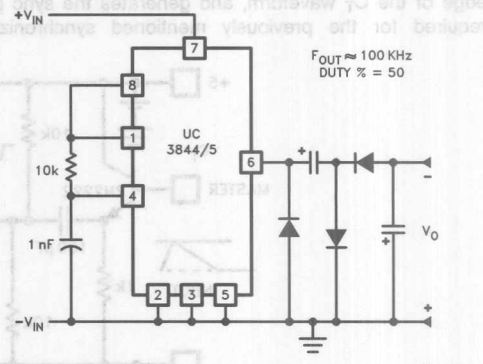


Figure 29

Low Power Buck Regulator—Voltage Mode

The basic buck regulator is described in the UNITRODE Applications Handbook.

*Consult UNITRODE Power Supply Design Seminar Book for compensation details; see "Closing The Feedback Loop", Buck Topology.

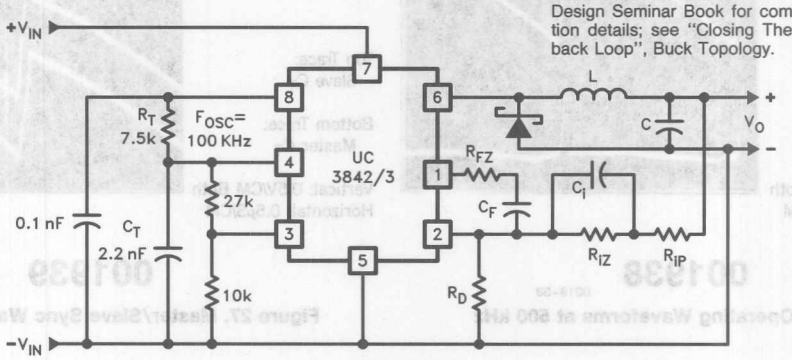


Figure 30

CIRCUIT EXAMPLES

1. Off-Line Flyback

Figure 31 shows a 25W multiple-output off-line flyback regulator controlled with the UC3844. This regulator is low in cost because it uses only two magnetic elements, a primary-side voltage sensing technique, and an inexpensive control circuit. Specifications are listed below.

Also consult UNITRODE application note U-96 in the applications handbook.

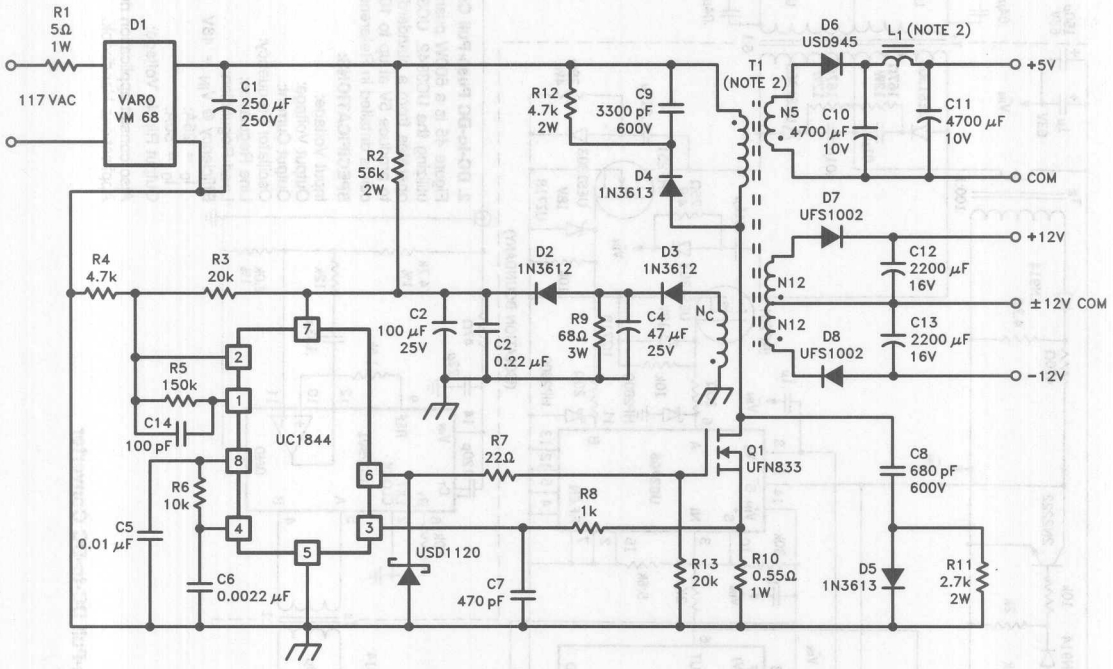


Figure 31

Power Supply Specifications

1. Input Voltage: 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation: 3750V
3. Switching Frequency: 40 kHz
4. Efficiency @ Full Load: 70%
5. Output Voltage:
   - A. +5V, ±5%: 1A to 4A load
     Ripple voltage: 50 mV P-P Max.
   - B. +12V, ±3% 0.1A to 0.3A load
     Ripple voltage: 100 mV P-P Max.
   - C. −12V ±3%, 0.1A to 0.3A load
     Ripple voltage: 100 mV P-P Max.

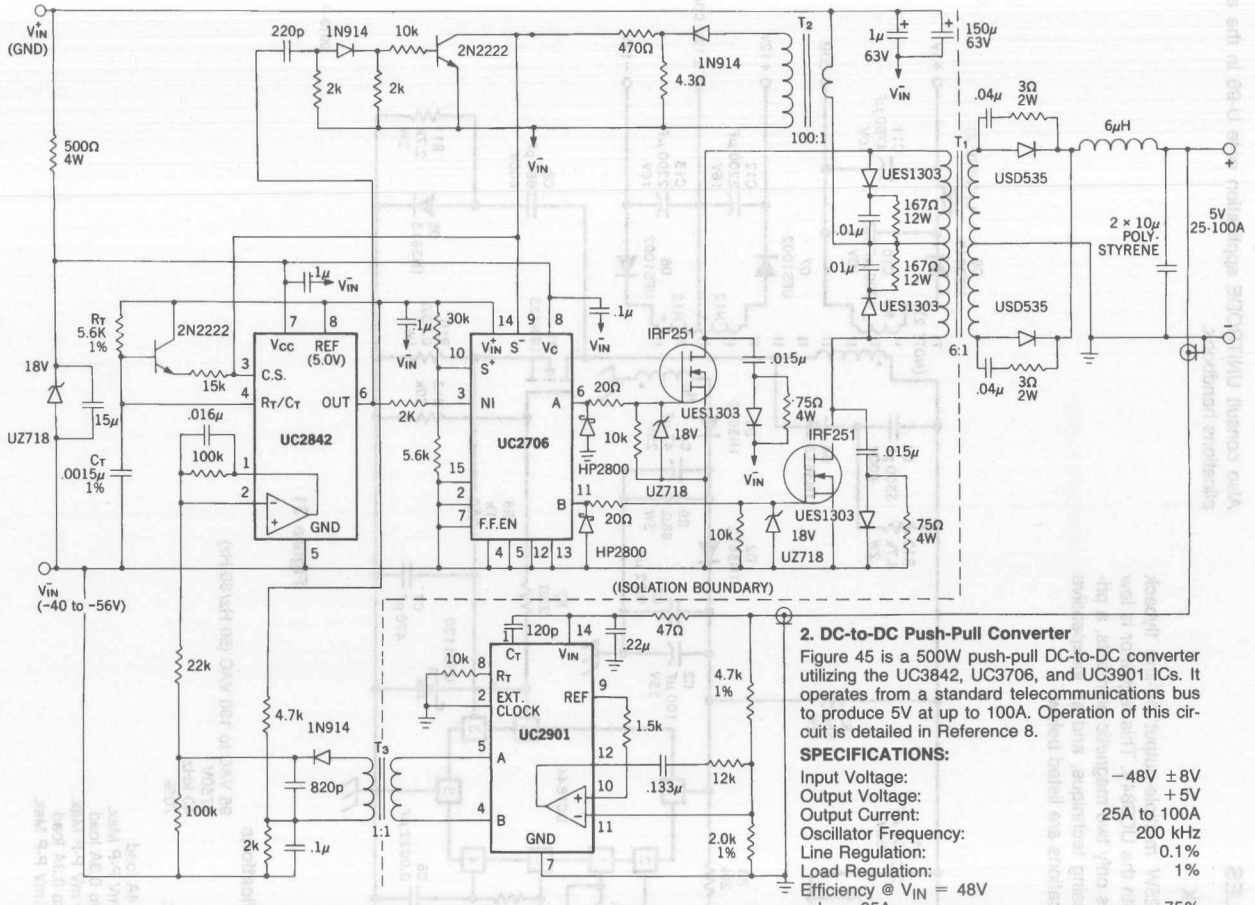


Figure 32. 500W Push-Pull DC-to-DC Converter

2. DC-to-DC Push-Pull Converter

Figure 45 is a 500W push-pull DC-to-DC converter utilizing the UC3842, UC3706, and UC3901 ICs. It operates from a standard telecommunications bus to produce 5V at up to 100A. Operation of this circuit is detailed in Reference 8.

SPECIFICATIONS:

Input Voltage:	−48V ±8V
Output Voltage:	+5V
Output Current:	25A to 100A
Oscillator Frequency:	200 kHz
Line Regulation:	0.1%
Load Regulation:	1%
Efficiency @ V_{IN} = 48V	
I_O = 25A:	75%
I_O = 50A:	80%
Output Ripple Voltage:	200 mV P-P

Also consult application note U-101 in the Unitrode Applications Handbook.

0019-48

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UNITRODE
APPLICATION NOTE

UC1637/2637/3637
SWITCHED MODE CONTROLLER FOR DC MOTOR DRIVE

INTRODUCTION

There is an increasing demand today for motor control circuits, as a result of the incredible proliferation of automated position control equipment, which is itself made possible by recent developments in the field of digital computation.

The UC1637 Switched Mode Controller for DC motors is one of several integrated circuits offered by Unitrode for motor controls. This Application Note presents the general principles of its operation and the circuit details that optimize its use. As an illustration we will carry out an actual design, which will involve not only the UC1637, but also a power H-bridge using MOSFET transistors, and a modern DC motor tachometer. Using the tach output and UC1637's error amplifier, we will close the velocity control loop after a brief analysis of the factors that affect the feedback loop stability.

To achieve high efficiency power amplification, the UC1637 uses pulse width modulation, or PWM. This technique is employed today in many different circuits where power losses must be minimized, and is most suitable in applications involving inductive loads such as motors, voice coils, etc.

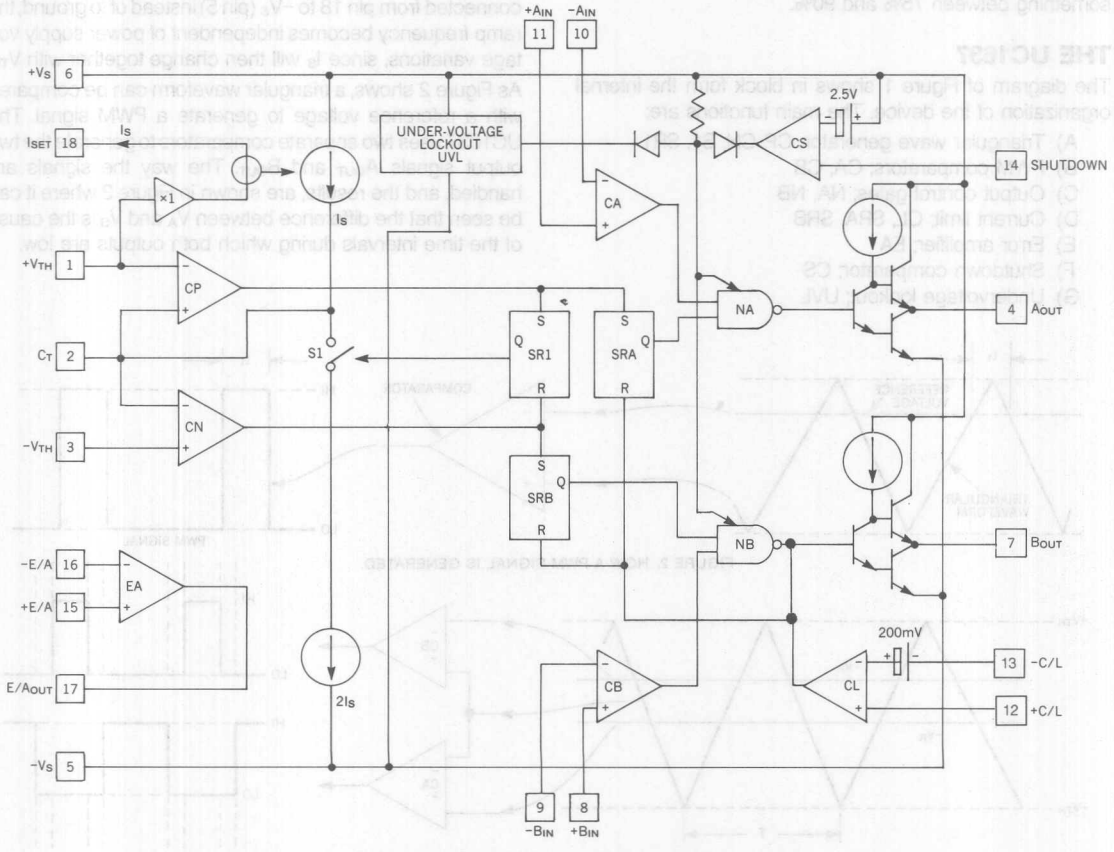


FIGURE 1. BLOCK DIAGRAM OF UC1637.

PULSE WIDTH MODULATION (PWM)

The function of a power amplifier is to regulate the flow of energy from a power supply to a load, under the control of an input signal. A linear amplifier does this by interposing a controlled voltage drop in series with the load, while carrying the full load current. The product of this voltage and current represents the amount of power that must be dissipated by the amplifier itself, and it is easy to see that the method is not very efficient. In fact, its usefulness diminishes rapidly as the amount of power to be controlled increases and, at some point, a more efficient method becomes imperative.

PWM is a switching technique in which the supply voltage is fully applied (switched) to the load and then removed, the "on" and "off" times being precisely controlled. The effect on the load is the same as if some lower voltage were continuously applied whose value depended on the duty-cycle, that is, the ratio of "on" time to the full switching period. Since supply current only flows during the "on" times, it is apparent that the efficiency should be much higher than in the linear amplifier, as in fact it is. Still, switching transistors have small but finite "on" voltages and transition times, all of which introduce losses, which limit practical PWM efficiencies to something between 75% and 90%.

THE UC1637

The diagram of Figure 1 shows in block form the internal organization of the device. The main functions are:

A) Triangular wave generator; CP, CN, S1, SR1
B) PWM comparators; CA, CB
C) Output control gates; NA, NB
D) Current limit; CL, SRA, SRB
E) Error amplifier; EA
F) Shutdown comparator; CS
G) Undervoltage lockout; UVL

The two output lines, A_{OUT} and B_{OUT}, are meant to drive the two legs of an H-bridge power amplifier, with the load driven in bipolar fashion. The A_{OUT} and B_{OUT} outputs themselves are rated at 500mA peak and 100mA continuous, which makes it easy to interface the device with most amplifiers.

In order to generate two PWM output signals, we first produce a triangular waveform, or linear ramp. This is done by charging a capacitor C_T (pin 2) with constant current I_S until the comparator CP, with a fixed threshold voltage of $+V_{TH}$, delivers a pulse to "set" the SR1 latch circuit. This forces Q high, which closes the switch S1 and adds a negative current, $2\times I_S$, to the node of pin 2. As a result, a net current equal to I_S now flows out of C_T, discharging it linearly until the comparator CN resets SR1, and the cycle restarts. Thus, the voltage at pin 2 ramps continuously between $-V_{TH}$ and $+V_{TH}$ at a frequency that depends on these two threshold voltages, on C_T, and on I_S.

The current I_S is programmed by means of a resistor connected to pin 18. The voltage at this pin is equal to $+V_{TH}$ and an internal current mirror forces the charging current I_S to be equal to the current flowing out of pin 18. If a resistor R_S is connected from pin 18 to $-V_S$ (pin 5) instead of to ground, the ramp frequency becomes independent of power supply voltage variations, since I_S will then change together with V_{TH}.

As Figure 2 shows, a triangular waveform can be compared with a reference voltage to generate a PWM signal. The UC1637 uses two separate comparators to generate the two output signals A_{OUT} and B_{OUT}. The way the signals are handled, and the results, are shown in Figure 3 where it can be seen that the difference between V_A and V_B is the cause of the time intervals during which both outputs are low.

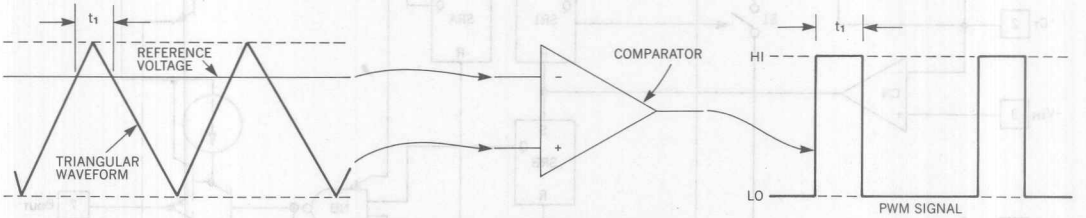


FIGURE 2. HOW A PWM SIGNAL IS GENERATED.

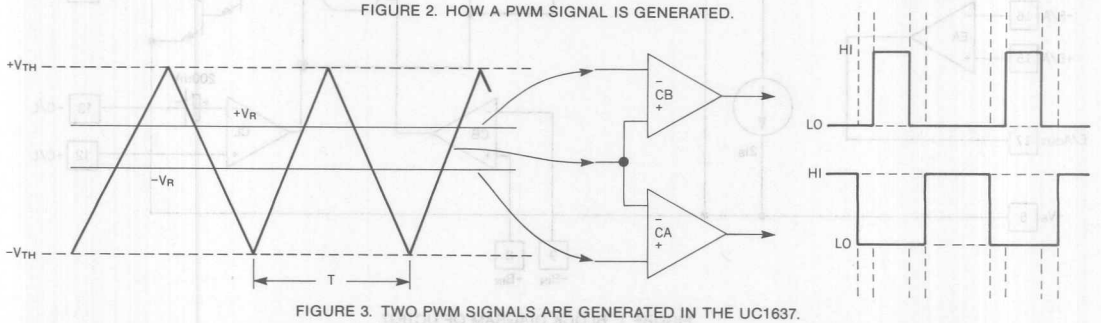


FIGURE 3. TWO PWM SIGNALS ARE GENERATED IN THE UC1637.

The two nand gates, NA and NB, will be enabled if the following two conditions are met:

A) supply voltage $+V_S$ is greater than +4.15 volts (typ)
B) the shut-down input line (pin 14) is at least 2.5 volts (typ) negative with respect to $+V_S$.

If these are satisfied, the A_{OUT} output line will be high if the CA output *and* Q of SRA are both high. Since SRA is set at each positive peak of the oscillator ramp, the output A_{OUT} can be controlled by CA singly — as long as a current-limit pulse from CL does not occur. The operation of the NB gate is similar.

The timing diagrams of Fig. 4 show the sequence of events before and after a current limit pulse occurs. Before time t_1 the PWM action is smoothly controlled by the ramp comparisons with V_A and V_B. The pulse from CL at time t_1 resets both SRA and SRB; the output lines are now disabled until SRA is set (at time t_2) and SRB is set (at time t_3).

The current limit comparator CL provides a means to protect both driver and motor from the consequences of very high currents. If the current delivered by the driver to the motor is made to flow through a low value resistor (for example, see R_S in Figure 7) the voltage drop across this resistor will be a measure of motor current. This voltage is applied between pins 12 and 13 of the UC1637, with pin 12 positive. A 200mV threshold is provided internally (see Figure 1) so that when the R_S voltage is equal to 200mV, the output of CA goes high, resetting both SRA and SRB and, consequently, terminating any active output pulse. This pulse-by-pulse method of current limiting is very fast and provides effective protection, not only for the driver components, but also for the motor, where the possibility of demagnetization due to excessive current is a matter of serious concern.

Finally, the UC1637 contains also an operational amplifier, EA, that can be used to provide gain and phase compensation, as will be seen later.

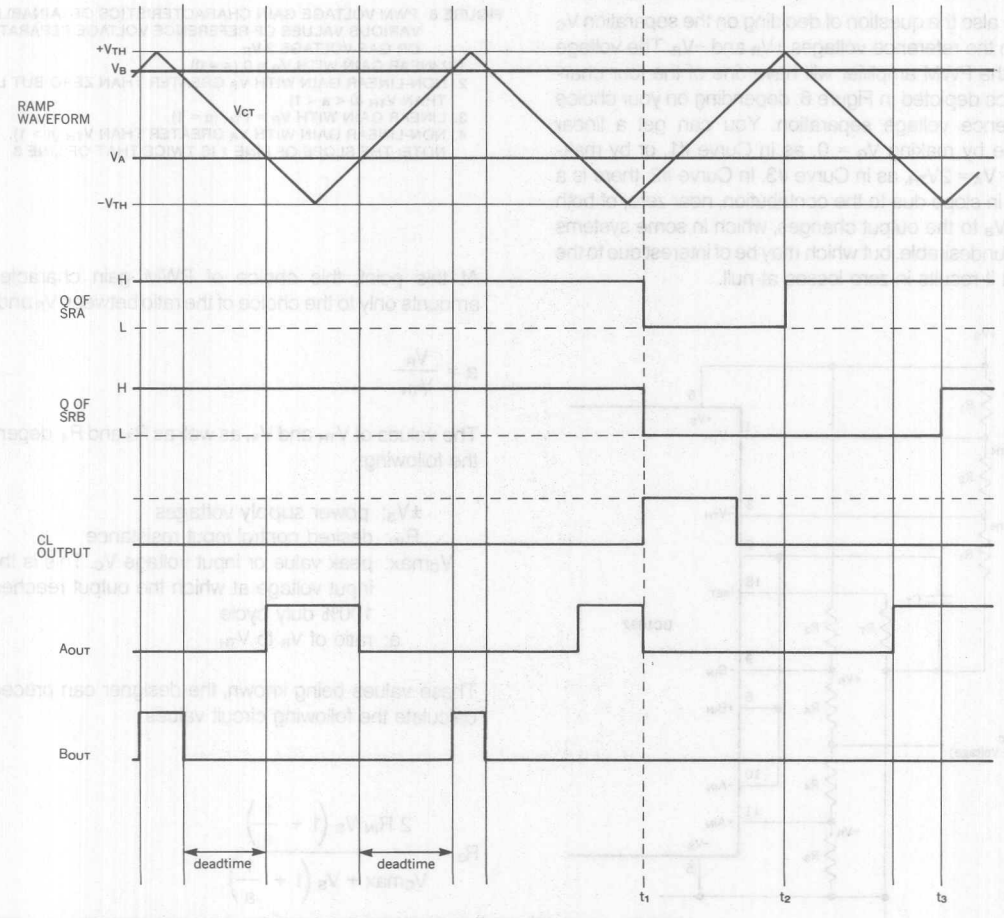


FIGURE 4. TIMING DIAGRAM SHOWING THE GENERATION OF PWM PULSES AT A_{OUT} AND B_{OUT}. BEFORE TIME t_1, THE Q OUTPUTS OF SRA AND SRB ARE BOTH HIGH AND THE OUTPUT PULSES ARE CONTROLLED BY THE RAMP INTERSECTIONS WITH V_A AND V_B. AT TIME t_1, THE CURRENT LIMIT COMPARATOR HAS SENSED EXCESS CURRENT AND THE CL OUTPUT HAS GONE HIGH, RESETTING BOTH SRA AND SRB. THIS TERMINATES THE A_{OUT} PULSE THAT WAS ACTIVE AT THE TIME. A_{OUT} CAN RESUME ONLY AFTER SRA IS SET AT t_2; B_{OUT} CAN RESUME ONLY AFTER SRB IS SET AT t_3.

Figure 5 shows the connections needed to get the ramp generator and the two comparators ready to go. There is no great difficulty in calculating values for the various resistors, which are no more than two simple voltage dividers. Still, certain things should be considered before proceeding.

The input impedance R_{IN}, seen by the control voltage V_C will be

$$R_{IN} = \frac{R_3 + R_4}{2} \quad (1)$$

and this value may be specified or determined in advance. Also, it would be economical to have a minimum number of different values of resistors. If we make

$$R_1 = R_3 \quad (2)$$

we will have four resistors of equal value in the final circuit.

There is also the question of deciding on the separation V_G between the reference voltages $+V_R$ and $-V_R$. The voltage gain of the PWM amplifier will have one of the four characteristics depicted in Figure 6, depending on your choice of reference voltage separation. You can get a linear response by making $V_G = 0$, as in Curve #1, or by making $V_B - V_A = 2V_{TH}$, as in Curve #3. In Curve #2, there is a change in slope due to the contribution, near zero, of both V_A and V_B to the output changes, which in some systems may be undesirable, but which may be of interest due to the fact that it results in zero losses at null.

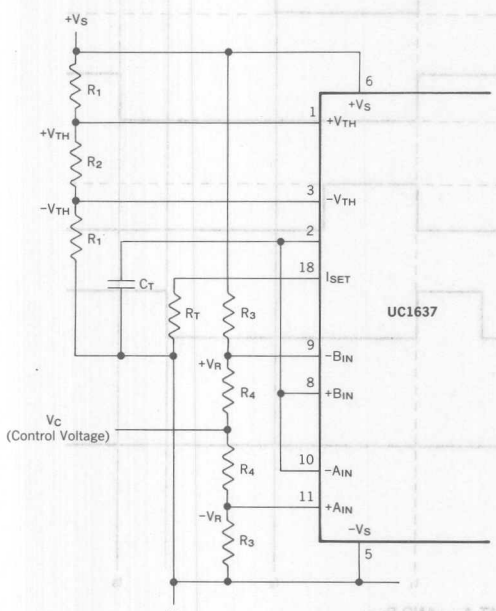
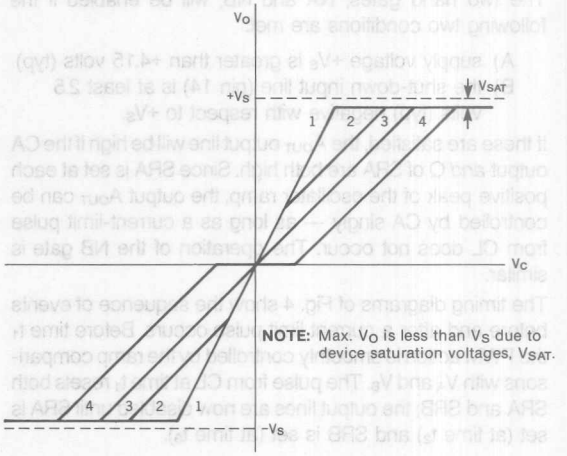


FIGURE 5. SETTING UP THE A AND B COMPARATOR INPUTS.



NOTE: Max. V_O is less than V_S due to device saturation voltages, V_{SAT}.

FIGURE 6. PWM VOLTAGE GAIN CHARACTERISTICS OBTAINABLE WITH VARIOUS VALUES OF REFERENCE VOLTAGE SEPARATION, OR GAP VOLTAGE 2 V_R.

1. LINEAR GAIN WITH $V_R = 0$ ($a = 0$).
2. NON-LINEAR GAIN WITH V_R GREATER THAN ZERO BUT LESS THAN V_{TH} ($0 < a < 1$).
3. LINEAR GAIN WITH $V_R = V_{TH}$ ($a = 1$).
4. NON-LINEAR GAIN WITH V_R GREATER THAN V_{TH} ($a > 1$).

NOTE: THE SLOPE OF LINE 1 IS TWICE THAT OF LINE 3.

At this point, this choice of PWM gain characteristic amounts only to the choice of the ratio between V_R and V_{TH}:

$$a = \frac{V_R}{V_{TH}} \quad (3)$$

The values of V_{TH} and V_R, as well as R_3 and R_4, depend on the following:

$\pm V_S$: power supply voltages
R_{IN}: desired control input resistance
$V_C$max: peak value or input voltage V_C. This is the input voltage at which the output reaches 100% duty cycle
a: ratio of V_R to V_{TH}

These values being known, the designer can proceed to calculate the following circuit values:

$$R_3 = \frac{2\,R_{IN}\,V_S\left(1 + \frac{1}{a}\right)}{V_C\text{max} + V_S\left(1 + \frac{1}{a}\right)} \quad (4)$$

$$R_4 = 2\,R_{IN} - R_3 \quad (5)$$

$$V_A = \frac{V_S R_4}{2 R_{IN}} \quad (6)$$

$$V_{TH} = \frac{V_R}{a} \quad (7)$$

$$R_2 = 2 R_3 \frac{V_{TH}}{V_S - V_{TH}} \quad (8)$$

and, from Eq. (2), $R_1 = R_3$.

Having chosen a frequency f_T for the PWM timing circuit, you can now calculate C_T and R_T. A suitable starting value for the charging current I_S is 0.5mA which gives

$$R_T = \frac{V_S + V_{TH}}{.0005} \quad (9)$$

$$C_T = \frac{.0005}{4 f_T V_{TH}} \quad (10)$$

You will probably need to make an adjustment here, so as to get a standard value for capacitor C_T, and it is best to keep I_S in the range from 0.3mA to 0.5mA when you do this.

It may be desirable, or even necessary in some conditions, to bypass the $+V_{TH}$ and $-V_{TH}$ inputs to ground, and for this, ceramic capacitors of 0.1μf should be adequate. Remember also that terminal 14, the shut-down line, must be held "low" (at least 2.5V below the positive rail) in order to enable the drive. With an external switch to ground, or to $-V_S$, and a pull-up resistor to $+V_S$, this line can be used to enable (low), and disable (high), the output. Both A_{OUT} and B_{OUT} will be low when the shut-down line is high.

The next step is to connect the UC1637 to a suitable power amplifier, and the amplifier to the motor. The UC1637 has provisions for current limiting, as discussed earlier, and you must make arrangements to develop a voltage proportional to motor current at the driver side. This can be done by adding to an H-bridge a low value resistor in series with rail connections. The current limit comparator has a common mode range that reaches all the way down to the negative rail (on the positive side the limit is 3V below the positive rail). A resistor R_S is then added at the bottom of the bridge, and its value is selected so as to give a voltage drop to 200mV when the desired limit current flows.

$$R_S = \frac{.2}{I_{MAX}} \text{ (ohms)} \quad (11)$$

where I_{MAX} is the maximum desired motor current in amperes. In a breadboard, a twisted pair of wires should be used to make the connection from this resistor to pins 12 and 13, and an RC filter should be added, as shown in Figure 7.

On a PC board, it is a good idea to keep R_S close to the UC1637 to minimize the length of the connecting traces. The RC filter should still be used.

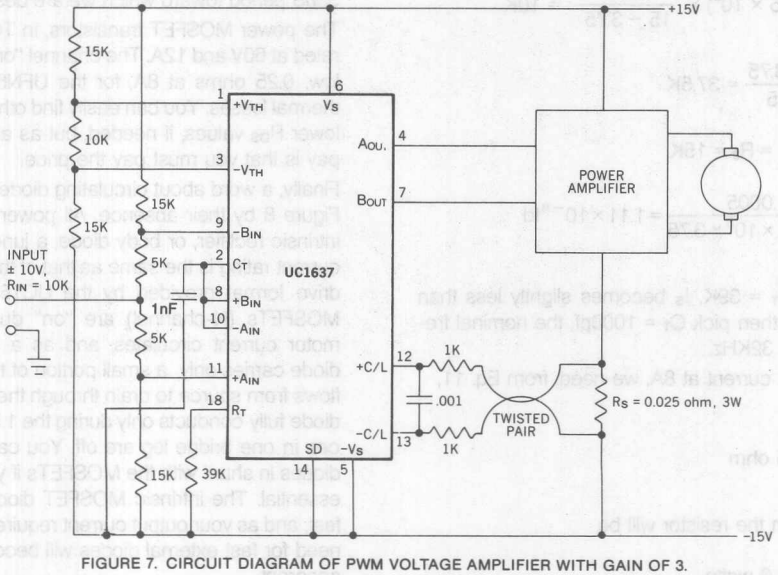


FIGURE 7. CIRCUIT DIAGRAM OF PWM VOLTAGE AMPLIFIER WITH GAIN OF 3.

AN EXAMPLE

We are ready now to design a current limited, PWM voltage amplifier to drive a small DC servomotor. Here are the requirements:

Supply voltages: ±15V
Input: ±10V max.; 10K input res.
PWM frequency: 30KHz
Motor current limited at 8A
Minimum power losses at idle

We have:
$V_S = 15V$
$V_C max = 10V$
$R_{IN} = 10^4$ ohm
$f_T = 3 \times 10^4$ Hz
and $I_{MAX} = 8A$

and also, from the last requirement, a = 1.

FROM EQUATIONS

(4) $$R_3 = \frac{2 \times 10^4 \times 15 \times 2}{10 + 15 \times 2} = 15K$$

(5) $$R_4 = 2 \times 10^4 - 15 \times 10^3 = 5K$$

(6) $$V_R = \frac{15 \times 5 \times 10^3}{2 \times 10^4} = 3.75V$$

(7) $$V_{TH} = 3.75V$$

(8) $$R_2 = (2 \times 15 \times 10^3) \times \frac{3.75}{15 - 3.75} = 10K$$

(9) $$R_T = \frac{15 + 3.75}{.0005} = 37.5K$$

and of course, $R_1 = R_3 = 15K$.

(10) $$C_T = \frac{.0005}{4 \times 30 \times 10^3 \times 3.75} = 1.11 \times 10^{-9} fd$$

If we settle for R_T = 39K, I_S becomes slightly less than 0.5mA and if we then pick C_T = 1000pf, the nominal frequency becomes 32KHz.

To limit the motor current at 8A, we need, from Eq. 11,

$$R_S = \frac{.2}{8} = 0.025 \text{ ohm}$$

The peak power in the resistor will be

$P_S = 8^2 \times .025 = 1.6$ watts.

Incidentally, the voltage gain of the amplifier can be determined from the fact that a 10V change at the input results in a 30V change at the output; therefore, the gain from input to motor terminals is 3. The above circuit is shown in Figure 7.

THE POWER AMPLIFIER

Where space is tight and motor current is less than five amperes, the Unitrode PIC900 offers a perfect solution to your power bridge design. This device comes in a DIL-18 package, requires only 5mA of input drive current, and is rated at 5A absolute maximum output current. It contains all you need for the output H-bridge — including the circulating diodes — and with only a few added parts, you are ready to go. A circuit diagram showing a velocity feedback loop using one UC1637 and one PIC900 appears in the UC1637 data sheet.

For higher currents, you will have to design your own amplifier, and for the purposes of this application note, a sample design is shown in Figure 8. Referring to that circuit, note that with $+V_S$ and $-V_S$ applied, if the inputs are left open, the power MOSFETs are all "off". If Drive A, for example, is driven to within 3.6V of either power rail, then the corresponding output is switched to that rail. Note that since the PNP and NPN junction transistors are by nature faster switching "on" than "off", while the MOSFETs are much faster than the junction transistors driving them, this connection provides a simple guarantee against cross-conduction. Also working toward this goal is the fact that the junction transistor can discharge the MOSFET's input capacitance faster than the 1K, 1W resistor can charge it. The arrangement shown in Figure 8 results in a transition time of about 1.5μS during which both MOSFETs in a given leg are off. This amount of time is a very small portion of the 33μS period toward which we are designing our example.

The power MOSFET transistors, in TO-220 package, are rated at 60V and 12A. The channel "on" resistance is quite low, 0.25 ohms at 8A, for the UFN533, resulting in low thermal losses. You can easily find other devices with even lower R_{DS} values, if needed, but as always, the price you pay is that you must pay the price.

Finally, a word about circulating diodes — conspicuous in Figure 8 by their absence. All power MOSFETs have an intrinsic rectifier, or body diode, a junction rectifier whose current rating is the same as that of the transistor. With the drive format provided by the UC1637, the two bottom MOSFETs (N-channel) are "on" during the time when motor current circulates, and as a result, the reversed diode carries only a small portion of the current; most of it flows from source to drain through the channel. In fact, the diode fully conducts only during the 1.5μS when both devices in one bridge leg are off. You can add fast recovery diodes in shunt with the MOSFETs if you find that they are essential. The intrinsic MOSFET diode is not particularly fast, and as your output current requirements increase, the need for fast external diodes will become more and more apparent.

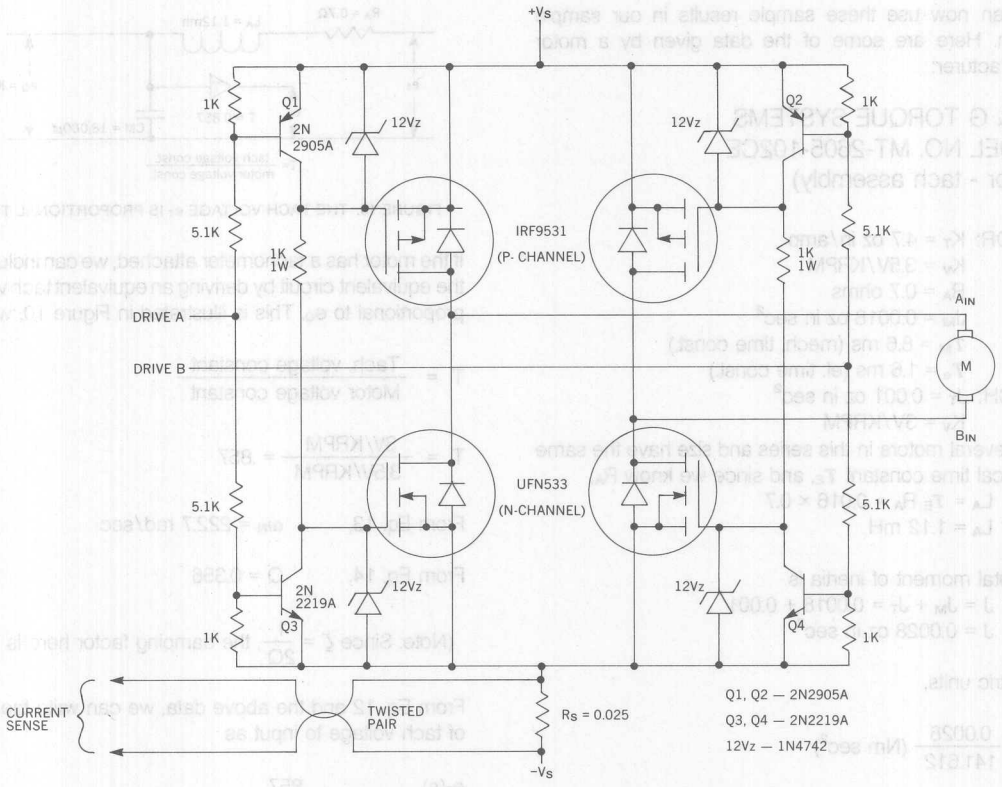


FIGURE 8. THIS 8A POWER AMPLIFIER IS SUITABLE FOR 30KHz OPERATION.

THE SERVOMOTOR

It is convenient to represent the DC servomotor by a simple equivalent circuit, and one such circuit is shown in Figure 9. Note that by expressing the moment of inertia J and the motor constant K in metric units (Nm sec^2 and Nm/A respectively), we avoid the need to include a multiplying constant in the expressions for C_M and e_o. Also, the motor constant K, in metric units, defines both the voltage constant in volt-sec/rad, and the torque constant in Nm/A, as one and the same number.

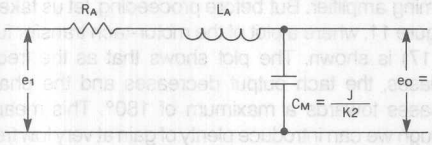


FIGURE 9. EQUIVALENT CIRCUIT OF MOTOR, WHERE J IS THE TOTAL MOMENT OF INERTIA OF ROTOR PLUS LOAD.

R_A = armature resistance; ohms.
L_A = armature inductance; henrys.
C_M = equivalent capacitance; farads.
J = total moment of inertia; Nm sec^2.
K = motor constant; volt sec/rad, or Nm/A.
ω = rotor angular velocity; rad/sec.

TO CONVERT FROM	TO	MULTIPLY BY
oz in sec^2	Nm sec^2	7.06×10^{-3}
volts/KRPM	volt sec/rad	9.55×10^{-3}

The ratio J/K^2 has the dimensions of capacitance, with a value runnng to several thousand microfarads. The voltage across this capacitor is equal to $K\omega$ where ω is the angular velocity of the rotor in rad/sec. Consequently, this voltage is the analog of shaft velocity.

Our equivalent circuit, then, is a simple series connection of R_A, the armature resistance; L_A, the armature inductance; and C_M, the equivalent capacitance, equal to J/K^2. It should come as no surprise that such a circuit will have a natural resonant frequency ω_N, and a resonant Q as well. This is indeed the case, and we have for its transfer function,

$$\frac{e_o(s)}{e_{1(s)}} = \frac{1}{(s/\omega_N)^2 + s/Q\omega_N + 1} \quad (12)$$

where $$\omega_N = \frac{K}{\sqrt{L_A J}} \quad (13)$$

and $$Q = \frac{K}{R_A}\sqrt{\frac{L_A}{J}} \quad (14)$$

We can now use these sample results in our sample design. Here are some of the data given by a motor manufacturer:

EG & G TORQUE SYSTEMS
MODEL NO. MT-2605-102CE
(motor - tach assembly)

MOTOR: K_T = 4.7 oz in/amp
K_V = 3.5V/KRPM
R_A = 0.7 ohms
J_M = 0.0018 oz in sec^2
τ_M = 8.6 ms (mech. time const.)
τ_e = 1.6 ms (el. time const.)
TACH: J_T = 0.001 oz in sec^2
K_V = 3V/KRPM

The several motors in this series and size have the same electrical time constant τ_E, and since we know R_A,

$L_A = \tau_E R_A = 0.016 \times 0.7$
L_A = 1.12 mH

The total moment of inertia is

$J = J_M + J_T = 0.0018 + 0.001$
J = 0.0028 oz in sec^2

In metric units,

$$J = \frac{0.0028}{141.612} \text{ (Nm sec}^2\text{)}$$

Putting K_T in metric units,

$$K = \frac{4.7}{141.612} \text{ (Nm/amp)}$$

The equivalent capacitance is

$$C_M = \frac{J}{K^2} = \frac{141.612 \times 0.0028}{(4.7)^2} = 18{,}000\mu f$$

For the equivalent circuit, then, the values are

R_A = 0.7 ohms
L_A = 1.12 mH
C_M = 18,000μf

The angular velocity will be proportional to the voltage e_o across C_M;

$$\omega = \frac{e_o}{K}$$

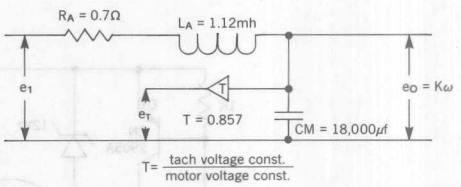


FIGURE 10. THE TACH VOLTAGE e_T IS PROPORTIONAL TO ω.

If the motor has a tachometer attached, we can include it in the equivalent circuit by deriving an equivalent tach voltage proportional to e_o. This is illustrated in Figure 10, where

$$T = \frac{\text{Tach. voltage constant}}{\text{Motor voltage constant}}$$

$$T = \frac{3\text{V/KRPM}}{3.5\text{V/KRPM}} = .857$$

From Eq. 13, ω_N = 222.7 rad/sec

From Eq. 14, Q = 0.356

(Note: Since $\zeta = \frac{1}{2Q}$, the damping factor here is 1.4)

From Eq. 12 and the above data, we can write the ratio of tach voltage to input as

$$\frac{e_T(s)}{e_1(s)} = \frac{.857}{\left(\frac{s}{222.7}\right)^2 + \frac{s}{79.3} + 1} \qquad (15)$$

THE VELOCITY LOOP

Our objective is to put together a feedback loop using our UC1637, H-bridge, and motor: the controlled variable is ω, the motor shaft's angular velocity. For high accuracy, we need a high loop gain, so that small velocity errors are magnified and corrected. The UC1637 internal ERROR amplifier is appropriate for this purpose, and will be used as a summing amplifier. But before proceeding, let us take a look at Figure 11, where a plot of the motor-tach transfer function (Eq. 17) is shown. The plot shows that as the frequency increases, the tach output decreases and the phase lag increases towards a maximum of 180°. This means that although we can introduce plenty of gain at very low frequencies, where the phase lag is low, the added gain must be reduced at the higher frequencies, where the 180° phase lag tends to make our loop a regenerative one. If we want the closed loop response to be "snappy", that is, if we want a bandwidth of several tens of hertz, then the loop gain must be

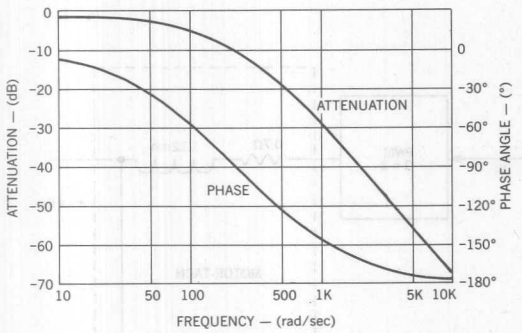
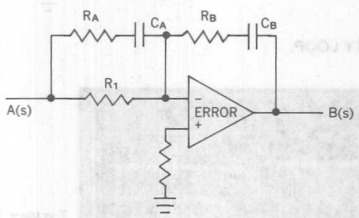


FIGURE 11. PLOT OF MAGNITUDE AND ANGLE OF EQ. 15, WHICH DESCRIBES PERFORMANCE OF OUR TEST MOTOR.

fairly high at all frequencies in the band; yet, for flat response and fast step response with no overshoot we must make certain that the overall phase shift is less than 180° at any frequency at which the gain is greater than unity.



$$\frac{A(s)}{B(s)} = \frac{(1 + sR_BC_B)\,[1 + s(R_1 + R_A)\,C_A]}{sR_1C_B\,(1 + sR_AC_A)}$$

FIGURE 12. ERROR AMPLIFIER WITH ITS FREQUENCY COMPENSATION NETWORK.
THE MAGNITUDE AND ARGUMENT OF THE TRANSFER FUNCTION CAN BE EASILY PLOTTED WITH THE AID OF A PROGRAMMABLE CALCULATOR.

The high gain ERROR amplifier of the UC1637, together with a few external components, is shown in Figure 12. Without R_A and C_A, the phase response of the circuit would go from −90° at low frequencies to 0° at high frequencies. This amount of phase correction is inadequate if we want a tight loop with good transient response. With R_A and C_A shunting R_1, it becomes possible to have a leading phase angle somewhere at midrange, even though the high frequency asymptote is still at zero degrees (R_A and C_A introduce both a zero and a pole). The transfer function of the circuit shown in Figure 12 is plotted in Figure 13 for the following component values:

R_1 = 9.1K
R_A = 1K
C_A = .22μf
R_B = 470K
C_B = .0047μf

The break frequencies are:

$$\frac{1}{R_BC_B} = \frac{1}{(R_1 + R_A)\,C_A} = 450 \text{ rad/sec}$$

$$\frac{1}{R_1C_B} = 23{,}400 \text{ rad/sec}$$

$$\frac{1}{R_AC_A} = 4{,}500 \text{ rad/sec}$$

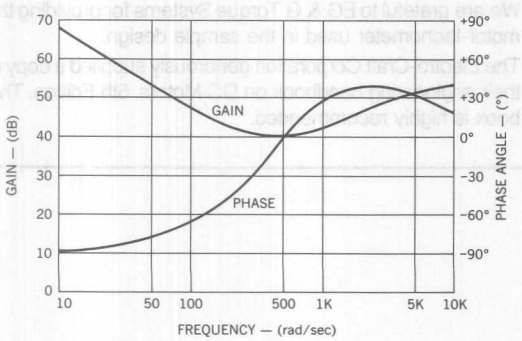


FIGURE 13. MAGNITUDE AND ANGLE OF COMPENSATION AMPLIFIER OF FIGURE 12.

The plot shown in Figure 14 shows the result of cascading the compensation amplifier, PWM amplifier, and motor-tach. All gain contributions have been simply added together, and all phase contributions have also been added. The result, shown in Figure 14, shows the open loop frequency response of the complete velocity control system.

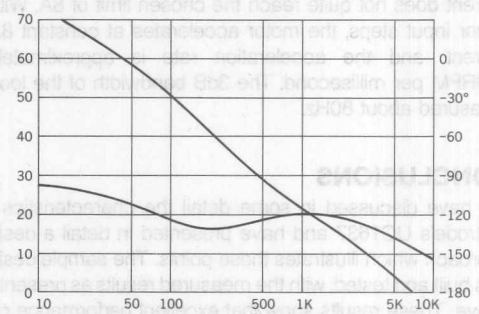


FIGURE 14. OVERALL OPEN-LOOP RESPONSE, INCLUDING +8dB DUE TO PWM AMPLIFIER GAIN AND MOTOR-TACH DC GAIN.

The inclusion of the ERROR amplifier with its compensation components has had the effect of introducing a large amount of gain at the lower frequencies, and also of reducing the phase lag at the higher frequencies. The loop gain is 0dB at about 7KHz, and the phase margin is about 40°.

Moreover, since the phase never exceeds 180°, we have the needed indication of *relative stability*, and can proceed to close the loop as shown in Figure 15 and make measurements. Note that a noise filter has neen added at the output of the tachometer. Such a filter is usually necessary, especially in PWM control loops of relatively wide bandwidth, because of the inevitable AC coupling between the motor signal and the tach output. In our filter, the 3dB cut-off point is at 21KHz, which is high enough not to affect the loop behavior.

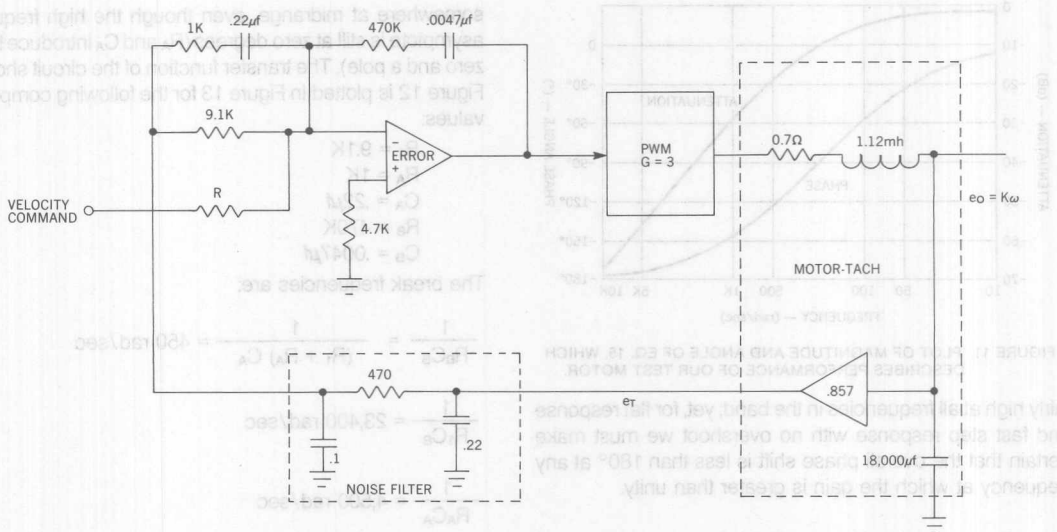
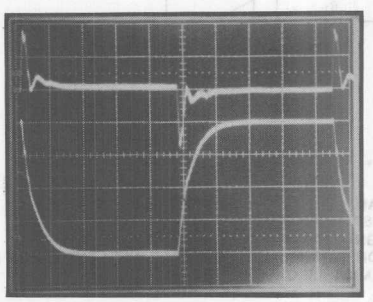


FIGURE 15. THE COMPLETE VELOCITY LOOP.

The oscilloscope trace shown in Figure 16 reveals that the step response of our loop is very well behaved. The motor shaft reaches full speed in less than 10mS, and there is no noticeable overshoot. The net velocity change in Figure 16 amounts to 133 RPM, and the current trace shows that the current does not quite reach the chosen limit of 8A. With larger input steps, the motor accelerates at constant 8A current, and the acceleration rate is approximately 100RPM per millisecond. The 3dB bandwidth of the loop measured about 80Hz.



Top trace: 5A/cm
Bottom trace: 100mV/cm
Horizontal: 5 msec/cm

FIGURE 16. STEP RESPONSE OF THE VELOCITY CONTROL LOOP OF FIGURE 15. THE UPPER TRACE SHOWS THE MOTOR CURRENT; THE LOWER TRACE SHOWS THE TACH OUTPUT VOLTAGE, I.E., MOTOR VELOCITY.

CONCLUSIONS

We have discussed in some detail the characteristics of Unitrode's UC1637 and have presented in detail a design approach which illustrates those points. The sample design was built and tested, with the measured results as presented above. These results show that excellent performance can be obtained with few components, and that the design technique is quite simple. Our velocity loop would perform well as an inner loop in a position control system, for example, although a different response might perhaps be desirable. However that may be, using the UC1637 a sizable portion to the job is completed beforehand.

See Figure 17.

ACKNOWLEDGMENTS

We are grateful to EG & G Torque Systems for providing the motor-tachometer used in the sample design.

The Electro-Craft Corporation generously supplied a copy of their engineering handbook on DC Motors, 5th Edition. This book is highly recommended.

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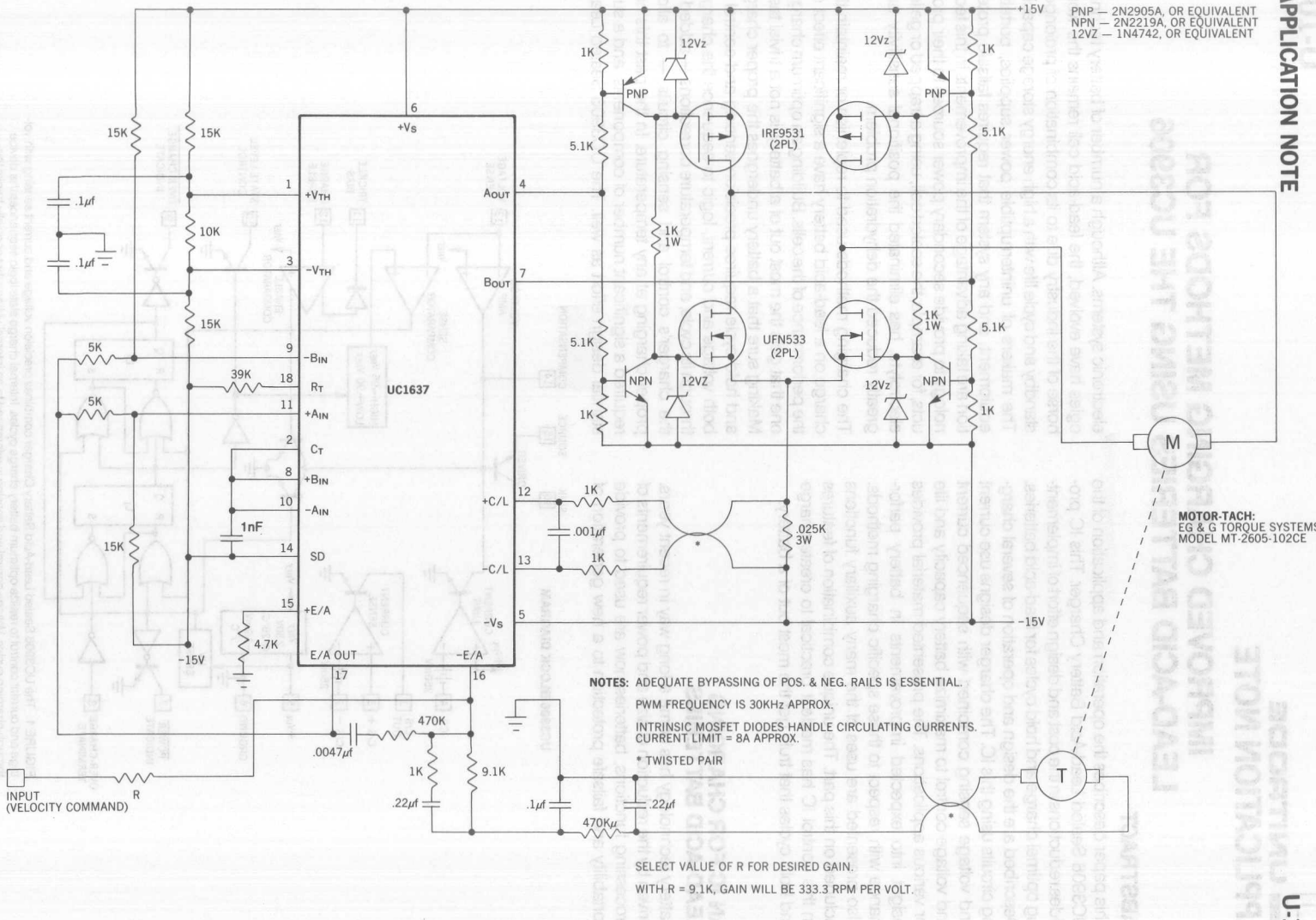


FIGURE 17. COMPLETE VELOCITY CONTROL LOOP OF SAMPLE DESIGN.

UNITRODE
APPLICATION NOTE

IMPROVED CHARGING METHODS FOR LEAD-ACID BATTERIES USING THE UC3906

ABSTRACT

This paper describes the operation and application of the UC3906 Sealed Lead-Acid Battery Charger. This IC provides reductions in the cost and design effort of implementing optimal charge and hold cycles for lead-acid batteries. Described are the design and operation of several charging circuits using this IC. The charger designs use current and voltage sensing combined with sequenced current and voltage control to maximize battery capacity and life for various applications. The presented material provides insight into expected improvements in battery performance with respect to these specific charging methods. Also presented are uses of the many auxiliary functions included on this part. The unique combination of features on this control IC has made it practical to create charge and hold cycles that truly get the most out of a battery.

AN IC FOR CHARGING LEAD-ACID BATTERIES

Battery technology has come a long way in recent years. Driven by the reduction of size and power requirements of processing functions, batteries now are used to provide portability and failsafe protection to a new generation of electronic systems. Although a number of battery technologies have evolved, the lead-acid cell remains the workhorse of the industry due to its combination of prolonged standby and cycle life with a high energy storage capacity. The makers of uninterruptible power supplies, portable equipment, and any system that requires failsafe protection are taking advantage of the improvements in this technology to provide secondary power sources to their products, for example, the sealed cell, using a trapped or gelled electrolyte, has eliminated the positional sensitivity and greatly reduced the dehydration problem.

The charging methods used to replenish or maintain the charge on a lead-acid battery have a significant effect on the performance of the cells. Building an optimum charger, one that gets the most out of a battery, is not a trivial task. Making sure that a battery undergoes the proper charge and hold cycle requires precision sensing and control of both voltage and current, logic to sequence the charger through its cycle, and temperature corrections — added to the charger's control and sensing circuits — to allow proper charging at any temperature. In the past this has required a significant number of components, and a substantial design effort as well. The UC3906 Sealed Lead-

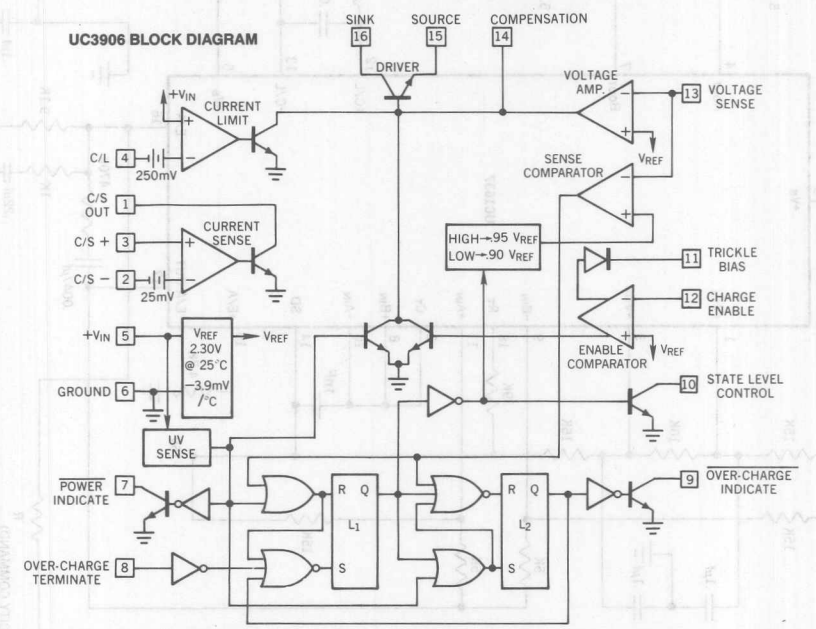


FIGURE 1. The UC3906 Sealed Lead-Acid Battery Charger combines precision voltage and current sensing with voltage and current control to realize optimum battery charge cycles. Internal charge state logic sequences the device through charging cycles. Voltage control and sensing is referenced to an internal voltage that specially tracks the temperature characteristics of lead-acid cells.

Acid Battery Charger has all the control and sensing functions necessary to optimize cell capacity and life in a wide range of battery applications.

The block diagram for the UC3906 is shown in figure 1. Separate voltage loop and current limit amplifiers regulate the output voltage and current levels in the charger by controlling the onboard driver. The driver will supply 25mA of base drive to an external pass element. Voltage and current sense comparators are used to sense the battery condition and respond with logic inputs to the charge state logic. The charge enable comparator on this IC can be used to remotely disable the charger. The comparator's 25mA trickle bias output is active high when the driver is disabled. These features can be combined to implement a low current turn-on mode in a charger, preventing high current charging during abnormal conditions such as a shorted or reversed battery.

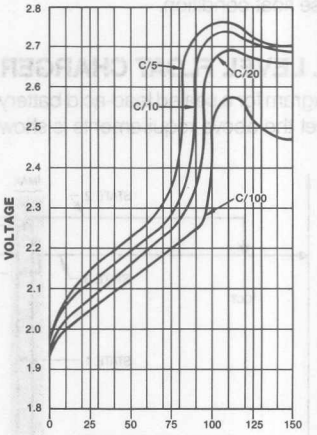
A very important feature of the UC3906 is its precision reference. The reference voltage is specially temperature compensated to track the temperature characteristics of lead-acid cells. The IC operates with very low supply current, only 1.7mA, minimizing on-chip dissipation and permitting the accurate sensing of the operating environmental temperature. In addition, the IC includes a supply under-voltage sensing circuit, used to initialize charging cycles at power on. This circuit also drives a logic output to indicate when input power is present. The UC3906 is specified for operation over the commercial temperature range of 0°C to 70°C. For operation over extended temperatures, –40°C to 70°C the UC2906 is available.

WHAT IS IMPORTANT IN A CHARGER?

Capacity and life are critical battery parameters that are strongly affected by charging methods. Capacity, C, refers to the number of ampere-hours that a charged battery is rated to supply at a given discharge rate. A battery's rated capacity is generally used as the unit for expressing charge and discharge current rates, i.e., a 2.5 amp-hour battery charging at 500mA is said to be charging at a C/5 rate. Battery life performance is measured in one of two ways; cycle life or stand-by life. Cycle life refers to the number of charge and discharge cycles that a battery can go through before its capacity is reduced to some threshold level. Standby life, or float life, is simply a measure of how long the battery can be maintained in a fully charged state and be able to provide proper service when called upon. The measure which actually indicates useful life expectancy in a given application will depend on the particulars of the application. In general, both aspects of battery life will be important.

During the charge cycle of a typical lead-acid cell, lead sulfate, $PbSO_4$, is converted to lead on the battery's negative plate and lead dioxide on the battery's positive plate. Once the majority of the lead sulfate has been converted, over-charge reactions begin. The typical result of over-charge is the generation of hydrogen and oxygen gas. In unsealed batteries this results in the immediate loss of water. In sealed cells, at moderate charge rates, the majority of the hydrogen and oxygen recombine before dehydration occurs. In either type of cell, prolonged charging rates significantly above C/500, will result in dehydration, accelerated grid corrosion, and reduced service life.

The onset of the over-charge reaction will depend on the rate of charge. At charge rates of >C/5, less than 80% of the cell's previously discharged capacity will be returned as the over-charge reaction begins. For over-charge to coincide with 100% return of capacity, charge rates must typically be reduced to less than C/100. Also, to accept higher rates the battery voltage must be allowed to increase as over-charge is approached. Figure 2 illustrates this phenomenon, showing cell voltage vs. percent return of previously discharged capacity for a variety of charge rates. The over-charge reaction begins at the point where the cell voltage rises sharply, and becomes excessive when the curves level out and start down again.



VOLTAGE CURVES FOR CELLS CHARGED AT VARIOUS CONSTANT (CURRENT) RATES AT ROOM TEMPERATURE

FIGURE 2. Depending on the charge rate, over-charge reactions begin, (indicated by the sharp rise in battery voltage), well below 100% return of capacity. (Reprinted with the permission of Gates Energy Products, Inc.)

Once a battery is fully charged, the best way to maintain the charge is to apply a constant voltage to the battery. This burdens the charging circuit with supplying the correct float charge level; large enough to compensate for self-discharge, and not too large to result in battery degradation from excessive overcharging. With the proper float charge, sealed lead-acid batteries are expected to give standby service for 6 to 10 years. Errors of just five percent in a float charger's characteristics can halve this expected life.

To compound the above concerns, the voltage characteristics of a lead-acid cell have a pronounced negative temperature dependence, approximately –4.0mV/°C per 2V cell. In other words, a charger that works perfectly at 25°C may not maintain or provide a full charge at 0°C and conversely may drastically over-charge a battery at +50°C. To function properly at temperature extremes a charger must have some form of compensation to track the battery temperature coefficient.

To provide reasonable re-charge times with a full 100% return of capacity, a charge cycle must adapt to the state of charge and the temperature of the battery. In sealed, or recombinate, cells, following a high current charge to return the bulk of the expended capacity, a controlled over-charge should take place. For unsealed cells the over-charge reaction must be minimized. After the over-charge, or at the onset of over-charge, the charger should convert to a precise float condition.

A DUAL LEVEL FLOAT CHARGER

A state diagram for a sealed lead-acid battery charger that would meet the above requirements is shown in figure 3.

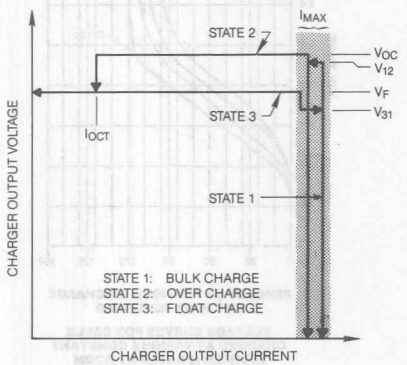


FIGURE 3. The dual level float charger has three charge states. A constant current bulk charge returns 70-90% of capacity to the battery with the remaining capacity returned during an elevated (constant) voltage over-charge. The float charge state maintains a precision voltage across the battery to optimize stand-by life.

This charger, called a dual level float charger, has three states, a high current bulk charge state, an over-charge state, and a float state. A charge cycle begins with the charger in the bulk charge state. In this state the charger acts like a current source providing a constant charge rate at I_{MAX}. The charger monitors the battery voltage and as it reaches a transition threshold, V_{12}, the charger begins its over-charge cycle. During the over-charge, the charger regulates the battery at an elevated voltage, V_{OC}, until the charge rate drops to a specified transition current, I_{OCT}. When the current tapers to I_{OCT}, with the battery at the elevated level, the capacity of the cell should be at nearly 100%. At this point the charger turns into a voltage regulator with a precisely defined output voltage, V_F. The output voltage of the charger in this third state sets the float level for the battery.

With the UC3906, this charge and hold cycle can be implemented with a minimum of external parts and design effort. A complete charger is shown in figure 4. Also shown are the design equations to be used to calculate the element values for a specific application. All of the programming of the voltage and current levels of the charger are determined by the appropriate selection the external resistors R_S, R_A, R_B, R_C.

Operation of this charger is best understood by tracing a charge cycle. The bulk charge state, the beginning, is initiated by either of two conditions. One is the cycling on of the input supply to the charger; the other is a low voltage condition on the battery that occurs while the charger is in the float state. The under-voltage sensing circuit on the UC3906 measures the input supply to the IC. When the input supply drops below about 4.5V the sensing circuit forces the two state logic latches (see figure 1) into the bulk charge condition (L1 reset and L2 set). This circuit also disables the driver output during the under-voltage condition. To enter the bulk charge state while power is on, the charger must first be in the float state (both latches set). The input to the charge state logic coming from the voltage sense comparator reports on the battery voltage. If the battery voltage goes low this input will reset L1 and the bulk charge state will be initiated.

With L1 reset, the state level output is always active low. While this pin is low the divider resistor, R_B is shunted by resistor R_C, raising the regulating level of the voltage loop. If we assume that the battery is in need of charge, the voltage amplifier will be in its stops trying to turn on the driver to force the battery voltage up. In this condition the voltage amplifier output will be over-ridden by the current limit amplifier. The current limit amplifier will control the driver, regulating the output current to a constant level. During this

time the voltage at the internal, non-inverting, input to the voltage sense comparator is equal to 0.95 times the internal reference voltage. As the battery is charged its voltage will rise; when the scaled battery voltage at PIN 13, the inverting input to the sense comparator, reaches 0.95Vref the sense comparator output will go low. This will reset the second latch and the over-charge state will be entered. At this time the over-charge indicator output will go low. Other than this there is no externally observable change in the charger. Internally, the starting of the over-charge state arms the set input of the first latch — assuming no reset signal is present — so that when the over-charge terminate input goes high, the charger can enter the float state.

In the over-charge state, the charger will continue to supply the maximum current. As the battery voltage reaches the elevated regulating level, V_{OC}, the voltage amplifier will take command of the driver, regulating the output voltage at a constant level. The voltage at PIN 13 will now be equal to the internal reference voltage. The battery is completing its charge cycle and the charge acceptance will start to taper off.

As configured in figure 4, the current sense comparator continuously monitors the charge rate by sensing the voltage across R_S. The output of the comparator is connected to the over-charge terminate input. Whenever the charge current is less than I_{OCT}, (25mV/R_S), the open collector output of the comparator will be off. When this transition current is reached, as the charge rate tapers in the over-charge state, the off condition of the comparator output will allow an internal 10μA pull-up current at PIN 8 to pull that point high. A capacitor can be added from ground to this point to provide a delay to the over-charge-terminate function, preventing the charger from prematurely entering the float state if the charging current temporarily drops due to system noise or whatever. When the voltage at PIN 8 reaches its 1V threshold, latch L1 will be set, setting L2 as well, and the charger will be in the float state. At this point the state level output will be off, effectively eliminating R_C from the divider and lowering the regulating level of the voltage loop to V_F.

In the float state the charger will maintain V_F across the battery, supplying currents of zero to I_{MAX} as required. In addition, the setting of L1 switches the voltage sense comparator's reference level from 0.95 to 0.90 times the internal reference. If the battery is now discharged to a voltage level 10% below the float level, the sense comparator output will reset L1 and the charge cycle will begin anew.

The float voltage V_F, as well as V_{OC} and the transition voltages, are proportional to the internal reference on the UC3906. This reference has a temperature coefficient of

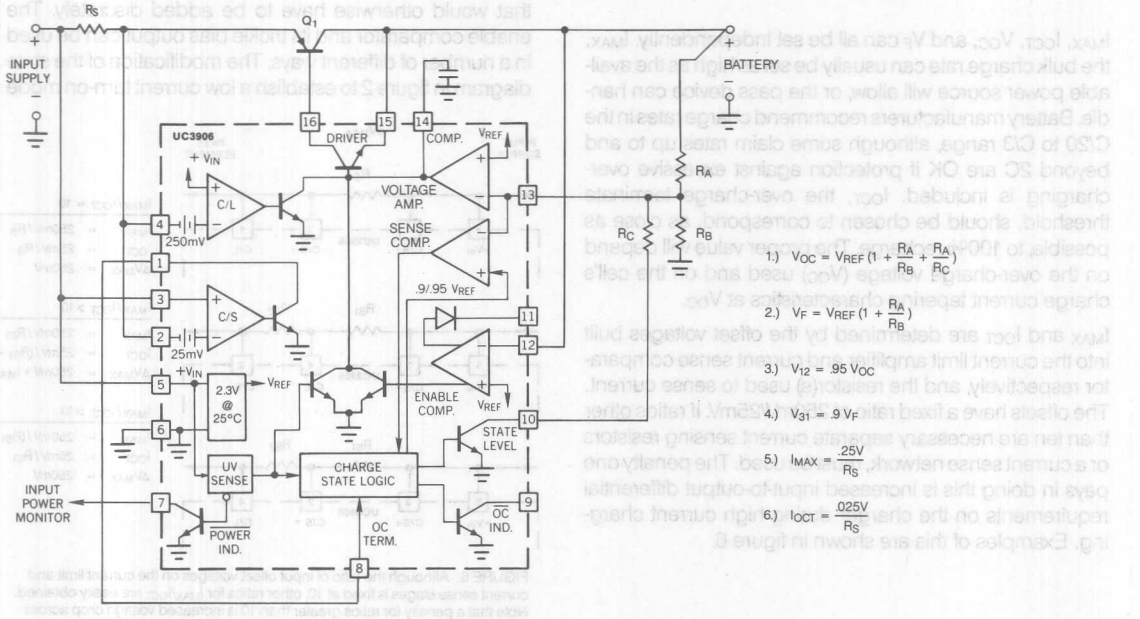


FIGURE 4. Using a few external parts and following simple design equations the UC3906 can be configured as a dual level float charger.

–3.9mV/°C. This temperature dependence matches the recommended compensation of most battery manufacturers. The importance of the control of the charger's voltage levels is reflected in the tight specification of the tolerance of the UC3906's reference and its change with temperature, as shown in figure 5.

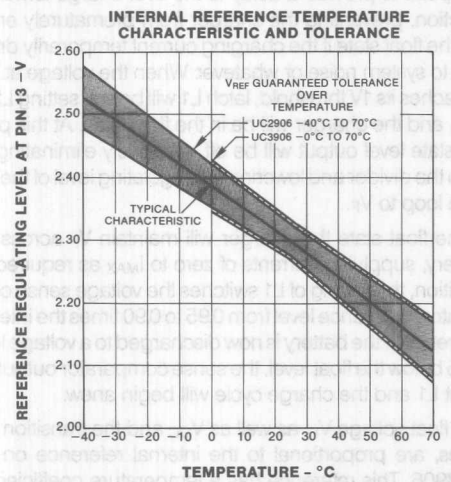


FIGURE 5. The specially temperature compensated reference on the UC3906 is tightly specified over 0 to 70°C, (–40 to 70°C for the UC2906), to allow proper charge and hold characteristics at all temperatures.

I_{MAX}, I_{OCT}, V_{OC}, and V_F can all be set independently. I_{MAX}, the bulk charge rate can usually be set as high as the available power source will allow, or the pass device can handle. Battery manufacturers recommend charge rates in the C/20 to C/3 range, although some claim rates up to and beyond 2C are OK if protection against excessive overcharging is included. I_{OCT}, the over-charge terminate threshold, should be chosen to correspond, as close as possible, to 100% recharge. The proper value will depend on the over-charge voltage (V_{OC}) used and on the cell's charge current tapering characteristics at V_{OC}.

I_{MAX} and I_{OCT} are determined by the offset voltages built into the current limit amplifier and current sense comparator respectively, and the resistor(s) used to sense current. The offsets have a fixed ratio of 250mV/25mV. If ratios other than ten are necessary separate current sensing resistors or a current sense network, must be used. The penalty one pays in doing this is increased input-to-output differential requirements on the charger during high current charging. Examples of this are shown in figure 6.

An alternative method for controlling the over-charge state is to use the over-charge indicate output, PIN 9, to initiate an external timer. At the onset of the over-charge cycle the over-charge indicate pin will go low. A timer triggered by this signal could then activate the over-charge terminate input, PIN 8, after a timed over-charge has taken place. This method is particularly attractive in systems with a centralized system controller where the controller can provide the timing function and automatically be aware of the state of charge of the battery.

The float, V_F, and over-charge, V_{OC}, voltages are set by the internal reference and the external resistor network, R_A, R_B, and R_C as shown in figure 4. For the dual level float charger the ranges at 25°C for V_F and V_{OC} are typically 2.3V-2.40V and 2.4V-2.7V, respectively. The float charge level will normally be specified very precisely by the battery manufacturer, little variation exists among most battery suppliers. The over-charge level, V_{OC}, is not as critical and will vary as a function of the charge rate used. The absolute value of the divider resistors can be made large, a divider current of 50μA will sacrifice less than 0.5% in accuracy due to input bias current offsets.

AUXILIARY CAPABILITIES OF THE CHARGER IC

Besides simply charging batteries, the UC3906 can be used to add many related auxiliary functions to the charger that would otherwise have to be added discretely. The enable comparator and its trickle bias output can be used in a number of different ways. The modification of the state diagram in figure 2 to establish a low current turn-on mode

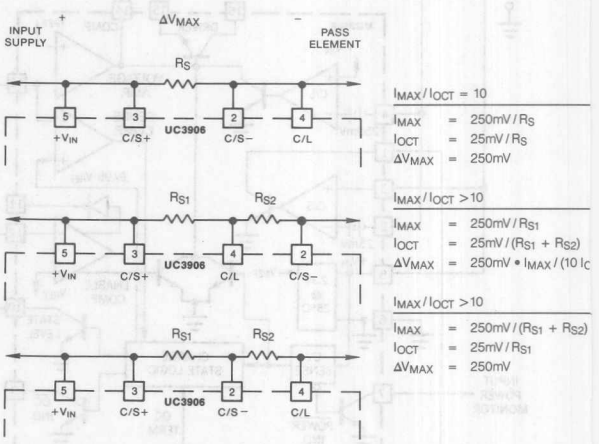


FIGURE 6. Although the ratio of input offset voltages on the current limit and current sense stages is fixed at 10, other ratios for I_{MAX}/I_{OCT} are easily obtained. Note that a penalty for ratios greater than 10 is increased voltage drop across the sensing network at I_{MAX}.

of the charger (see figure 7) is easily done. By reducing the output current of the charger when the battery voltage is below a programmable threshold, the charging system protects against: One, high current charging of a string with a shorted cell that could result in excessive outgassing from the remaining cells in the string. Two, dumping charge into a battery that has been hooked up backwards. Three, excessive power dissipation in the charger's pass element.

As shown in figure 7, the enable comparator input taps off the battery sensing divider. When the battery voltage is below the resulting threshold, V_T, the driver on the UC3906 is disabled and the trickle bias output goes high. A resistor, R_T, connected to the battery from this output can then be used to set a trickle current, ($\leq$25mA) to the battery to help the charger discriminate between severely discharged cells and damaged, or improperly connected, cells.

In applications where the charger is integral to the system, i.e. always connected to the battery, and the load currents on the battery are very small, it may be necessary to absolutely minimize the load on the battery presented by the charger when input power is removed. There are two simple precautions that, when taken, will remove essentially all reverse current into the charging circuit. In figure 8 the diode in series with the pass element will prevent any reverse current through this path. The sense divider should still be referenced directly to the battery to maintain accurate control of voltage. To eliminate this discharge path, the divider in the figure is referenced to the open collector power indicate output, PIN 7, instead of ground. Connected in this manner the divider string will be in series with essentially an open when input power is removed. When power is present, the open collector device will be on, holding the divider string end at nearly ground. The saturation voltage of the open collector output is specified to be less than 50mV with a load current of 50μA.

Figure 9 illustrates the use of the enable comparator and its output to build over-discharge protection into a charger. Over-discharging a lead-acid cell, like over-charging, can severely shorten the service life of the cell. The circuit monitors the discharging of the battery and disconnects all load from the battery when its voltage reaches a specified cutoff point. The load will remain disconnected from the battery until input power is returned and the battery recharged.

This scheme uses a relay between the battery and its load that is controlled by Q1 and the presence of voltage across the load. When primary power is available Q1 is on via D5. The battery is charging, or charged, and the trickle bias output at PIN 11 is off. When input power is removed, C2 provides enough hold-up time at the load to let Q1 turn off, and the relay to close as current flows through R1. The battery is now providing power to the load and, through D1, power to the charger. The charger current draw will typically be less than 2mA. As the battery discharges, the UC3906 will continue to monitor its voltage. When the vol-

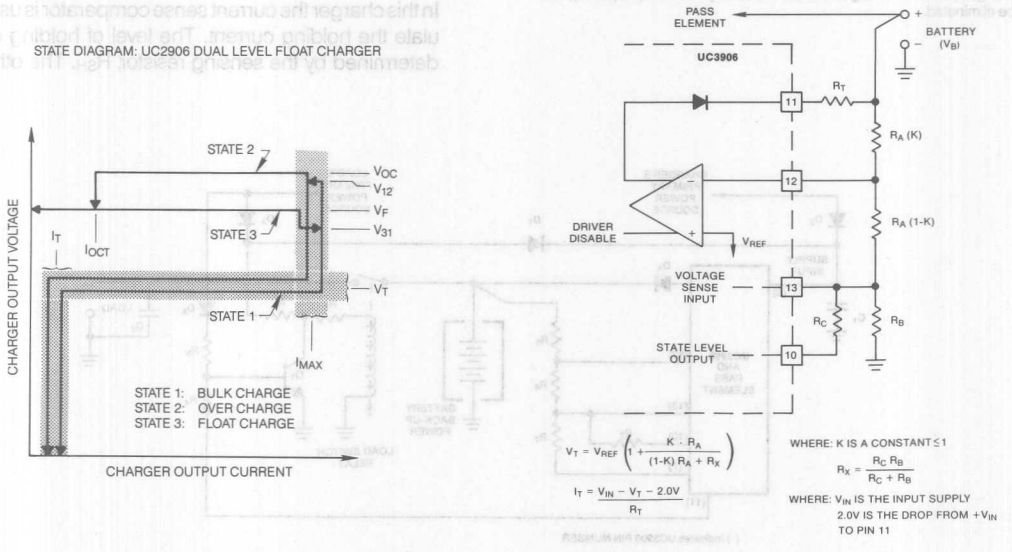


FIGURE 7. The charge enable comparator, with its trickle bias output, can be used to build protection into the charger. The current foldback at low battery voltages prevents high current charging of batteries with shorted cells, or improperly connected batteries, and also protects the pass element from excessive power dissipation.

tage reaches the cut-off level, set by the divider network, R5-R8, the trickle bias output, PIN 11, will go high. Q1 will turn back on and the relay current will collapse opening its contacts. As the load voltage drops, capacitor C1 supplies power to the UC3906 to keep Q1 on. Once the input to the charger has collapsed the power indicate pin, as shown in figure 8, will open the divider string. The battery will remain open-circuited until input power is returned. At that time the battery will begin to recharge.

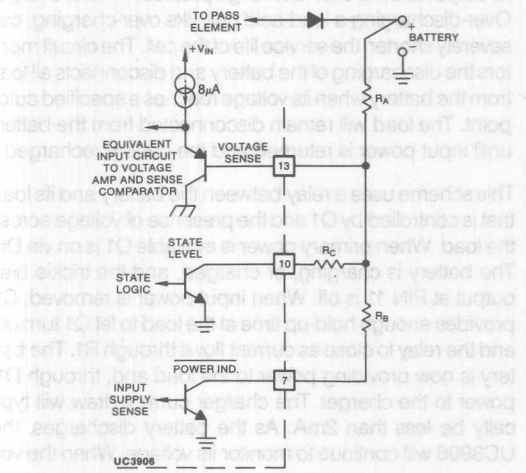


FIGURE 8. By using a diode in series with the pass element, and referencing the divider string to the power indicate pin, pin 7, reverse current into the charger, (when the charger is tied to the battery with no input power), can be eliminated.

CHARGING LARGE SERIES STRINGS OF LEAD-ACID CELLS

When large series strings of batteries are to be charged, a dual step current charger has certain advantages over the float charger of figures 3 and 4. A state diagram and circuit implementation of this type of charger is shown in figure 10. The voltage across a large series string is not as predictable as a common 3 or 6 cell string. In standby service varying self discharge rates can significantly alter the state of charge of individual cells in the string if a constant float voltage is used. The elevated voltage, low current holding state of the dual step current charger maintains full and equal charge on the cells. The holding, or trickle current, I_H, will typically be on the order of 0.005C to 0.0005C.

To give adequate and accurate recharge this charger has a bulk charge state with temperature compensated transition thresholds, V_{12}, and V_{21}. Instead of entering an elevated voltage over-charge, upon reaching V_{12} the charger switches to a constant current holding state. The holding current will maintain the battery voltage at a slightly elevated level but not high enough to cause significant overcharging. If the battery current increases, the charger will attempt to hold the battery at the V_F level as shown in the state diagram. This may happen if the battery temperature increases significantly, increasing the self-discharge rate beyond the holding current. Also, immediately following the transition from the bulk to float states, the battery will only be 80% to 90% charged and the battery voltage will drop to the V_F level for some period of time until full charging is achieved.

In this charger the current sense comparator is used to regulate the holding current. The level of holding current is determined by the sensing resistor, R_{SH}. The other series

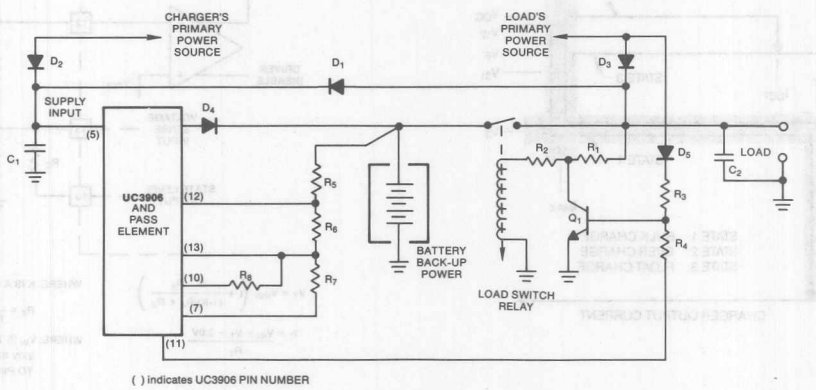


FIGURE 9. Using the enable comparator to monitor the battery voltage a precise discharge cut-off voltage can be set. When the battery reaches the cut-off threshold the trickle bial output switches off the load switch relay and the battery is left open circuited until input power is returned.

resistor, R_E, is necessary for the current sense comparator to regulate the holding current. Its value is selected by dividing the value of I_H into the minimum input to output differential that is expected between the battery and the input supply. If the supply variation is very large, or the holding current large, (>25mA), then an external buffering element may be required at the output of the current sense comparator.

The operating supply voltage into the UC3906 should be kept less than 45V. However, the IC can be adapted to charge a battery string of greater than 45V. To charge a large series string of cells with the dual step current charger the ground pin on the UC3906 can be referenced to a tap point on the battery string as shown in figure 11. Since the charger is regulating current into the batteries, the cells will all receive equal charge. The only offset results from the bias current of the UC3906 and the divider string current adding to the current charging the battery cells below the tap point. R_B can be added to subtract the bulk of this current improving the ability of the charger to control the low level currents. The voltage trip points using this technique will be based on the sum of the cell voltages on the high side of the tap.

PICKING A PASS ELEMENT AND COMPENSATING THE CHARGER

There are four factors to consider when choosing a pass device. These are:

1. The pass device must have sufficient current and power handling capability to accommodate the desired maximum charging rate at the maximum input to output differential.
2. The device must have a high enough current gain at the maximum charge rate to keep the drive current required to less than 25mA.
3. The type of device used, (PNP, NPN, or FET), and its configuration, may be dictated by the minimum input to output differential at which the charger must operate.
4. The open loop gain of both the voltage and the current control loops are dependent on the pass element and its configuration.

Figure 12 contains a number of possible driver configurations with some rough break points on applicable current ranges as well as the resulting minimum input to output differentials. Also included in this figure are equations for the dissipation that results on the UC3906 die, equations for a resistor, R_D, that can be added to minimize this dissipation, and expressions for the open loop gains of both the voltage and current loops.

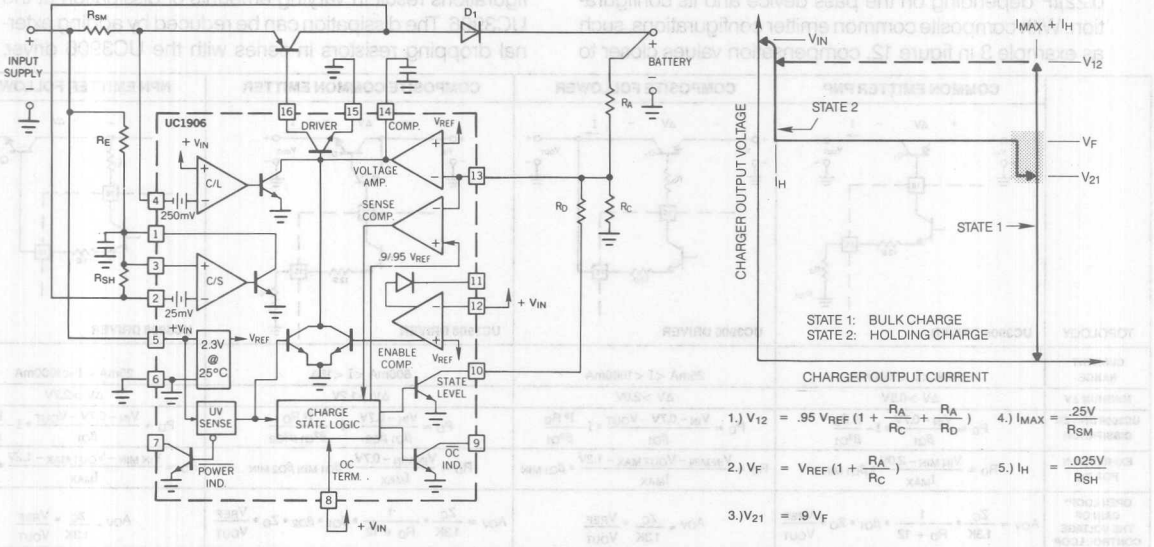


FIGURE 10. A dual step current charger has some advantages when large series strings must be charged. This type of charger maintains constant current during normal charging that results in equal charge distribution among battery cells.

As reflected in the gain expressions in figure 12, the open loop voltage gains of both the voltage and current control loops are dependent on the impedance, Z_C at the compensation pin. Both loops can be stabilized by adjusting the value of this impedance. Using the expressions given, one can go through a detailed analysis of the loops to predict respective gain and phase margins. In doing so one must not forget to account for all the poles in the open loop expressions. In the common emitter driver examples, 1 and 3, the equivalent load impedance at the output of the charger directly affects loop characteristics. In addition, a pole, or poles, will be added to the loop response due to the roll-off of the pass device's current gain, Beta. This effect will occur at approximately the rated unity gain frequency of the device divided by its low frequency current gain. The transconductance terms for the voltage and current limit amplifiers, (1/1.3K and 1/300 respectively), will start to roll off at about 500KHZ. As a rule of thumb, it is wise to kill the loop gain well below the point that any of these, not-so-predictable poles, enter the picture.

If you prefer not to go through a BODE analysis of the loops to pick a compensation value, and you recognize the fact that battery chargers do not require anything close to optimum dynamic response, then loop stability can be assured by simply oversizing the value of the capacitor used at the compensation pin. In some cases it may be necessary to add a resistor in series with the compensation capacitor to put a zero in the response. Typical values for the compensation capacitor will range from 1000pF to 0.22μF depending on the pass device and its configuration. With composite common emitter configurations, such as example 3 in figure 12, compensation values closer to

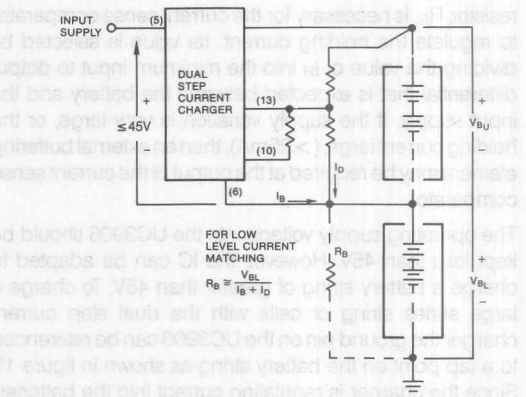
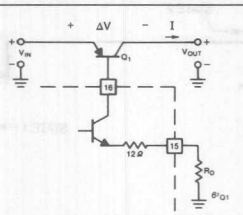
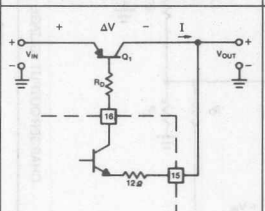
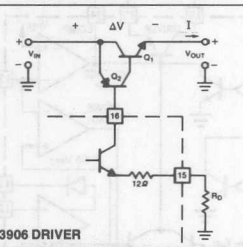
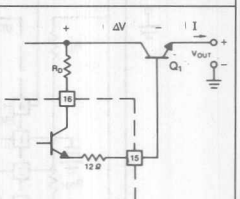


FIGURE 11. A dual step current charger can be configured to operate with input supplies of greater than 45V by using a tap on the battery to reference the UC3906. The charger uses the voltage across the upper portion of the battery to sense charging transition points. To minimize charging current offsets, R_B can be added to cancel the UC3906 bias and divider currents.

the 0.22μF value will be required to roll off the large open loop gain that results from the Beta squared term in the gain expression. Series resistance should be less than 1K, and may range as low as 100 ohms and still be effective.

The power dissipated by the UC3906 requires attention since the thermal resistance, (100°C/Watt) of the DIP package can result in significant differences in temperature between the UC3906 die and the surrounding air, (battery), temperature. Different driver/pass element configurations result in varying amounts of dissipation at the UC3906. The dissipation can be reduced by adding external dropping resistors in series with the UC3906 driver,

TOPOLOGY	COMMON EMITTER PNP	COMPOSITE FOLLOWER	COMPOSITE COMMON EMITTER	NPN EMITTER FOLLOWER
				
	UC3906 DRIVER	UC3906 DRIVER	UC3906 DRIVER	UC3906 DRIVER
CURRENT RANGE	25mA < I < 1000mA	25mA < I < 1000mA	600mA < I < 15A	25mA < I < 1000mA
MINIMUM ΔV	ΔV > 0.5V	ΔV > 2.0V	ΔV > 1.2V	ΔV > 2.7V
UC3906 DRIVER DISSIPATION	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}}$	$P_D \approx \frac{V_{IN} - 0.7V}{\beta_{Q1}\,\beta_{Q2}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}\,\beta^2_{Q2}}$	$P_D \approx \frac{V_{IN} - 0.7V - V_{OUT}}{\beta_{Q1}} \bullet I - \frac{I^2 R_D}{\beta^2_{Q1}}$
EXPRESSION FOR R_D	$R_D \approx \frac{V_{IN\,MIN} - 2.0V}{I_{MAX}} \bullet \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \bullet \beta_{Q1\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - 0.7V}{I_{MAX}} \bullet \beta_{Q1\,MIN}\,\beta_{Q2\,MIN}$	$R_D \approx \frac{V_{IN\,MIN} - V_{OUT\,MAX} - 1.2V}{I_{MAX}} \bullet \beta_{Q1\,MIN}$
OPEN LOOP* GAIN OF THE VOLTAGE CONTROL LOOP	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet Z_O \bullet \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet \beta_{Q2} \bullet Z_O \bullet \frac{V_{REF}}{V_{OUT}}$	$A_{OV} \approx \frac{Z_C}{1.3K} \bullet \frac{V_{REF}}{V_{OUT}}$
OPEN LOOP* GAIN OF THE CURRENT LIMIT LOOP	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet R_S$	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{12/\beta_{Q1} + Z_O} \bullet R_S$	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{R_D + 12} \bullet \beta_{Q1} \bullet \beta_{Q2} \bullet R_S$	$A_{OC} \approx \frac{Z_C}{300} \bullet \frac{1}{12/\beta_{Q1} + Z_O} \bullet R_S$

*Z_C = IMPEDANCE AT COMPENSATION PIN, PIN 14. = IMPEDANCE AT CHARGER OUTPUT.

FIGURE 12. There are a large number of possible driver/pass element configurations, a few are summarized here. The trade-offs are between current gain, input to output differential, and in some cases, power dissipation on the UC3906. When dissipation is a problem it can be reduced by adding a resistor in series with the UC3906 driver.

(see figure 12). These resistors will then share the power with the die. The charger parameters most affected by increased driver dissipation are the transition thresholds, (V_{12} and V_{21}), since the charger is, by design, supplying its maximum current at these points. The current levels will not be affected since the input offset voltages on the current amplifier and sense comparator have very little temperature dependence. Also, the stand-by float level on the charger will still track ambient temperature accurately since, normally, very little current is required of the charger during this condition.

To estimate the effects of dissipation on the charger's voltage levels, calculate the power dissipated by the IC at any given point, multiply this value by the thermal resistance of the package, and then multiply this product by –3.9mV/°C and the proper external divider ratio. In most cases, the effect can be ignored, while in others the charger design must be tweaked to account for die dissipation by adjusting charger parameters at critical points of the charge cycle.

SOME RESULTS WITH THE DUAL LEVEL FLOAT CHARGER

In figure 13 the schematic is shown for a dual level, float charger designed for use with a 6V, 2.5amp-hour, sealed lead-acid battery. The specifications, at 25°C, for this charger are listed below.

Input supply voltage	9.0V to 13V
Operating temperature range	0°C to 70°C
Start-up trickle current (I_T)	10mA (V_{IN} = 10V)
Start-up voltage (V_T)	5.1V
Bulk charge rate (I_{MAX})	500mA (C/5)
Bulk to OC transition voltage (V_{12})	7.125V
OC voltage (V_{OC})	7.5V
OC terminate current (I_{OCT})	50mA (C/50)
Float voltage (V_F)	7.0V
Float to Bulk transition voltage (V_{31})	6.3V
Temperature coefficient on voltage levels	–12mV/°C
Reverse current at charger output with the input supply at 0.0V	≤ 5μA

In order to achieve the low input to output differential, (1.5V), the charger was designed with a PNP pass device that can operate in its saturation region under low input supply conditions. The series diode, required to meet the reverse current specification, accounts for 1.0V of the 1.5V minimum differential. Keeping the reverse current under 5μA also requires the divider string to be disconnected when input power is removed. This is accomplished, as discussed earlier, by using the input power indicate pin to reference the divider string.

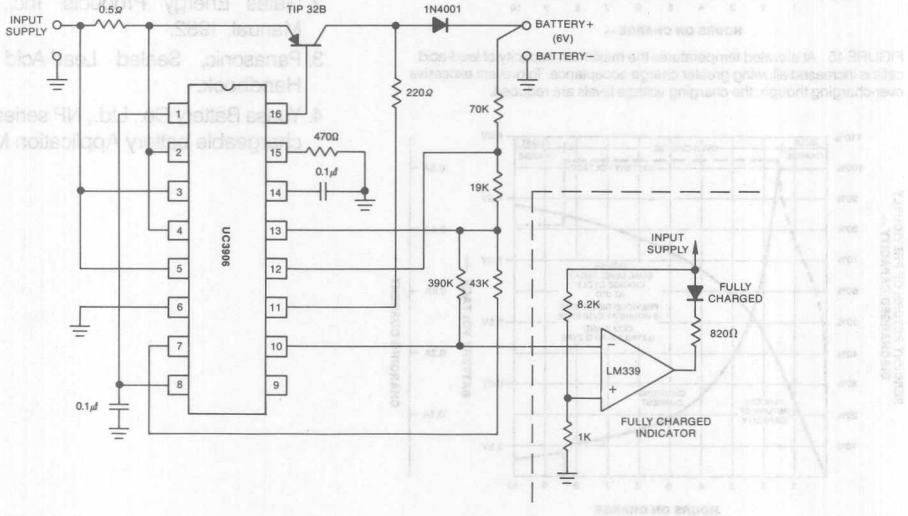


FIGURE 13. This dual level float charger was designed for a 6V (three 2V cells) 2.5AH battery. A separate "fully charged" indicator was added for visual indication of charge completion.

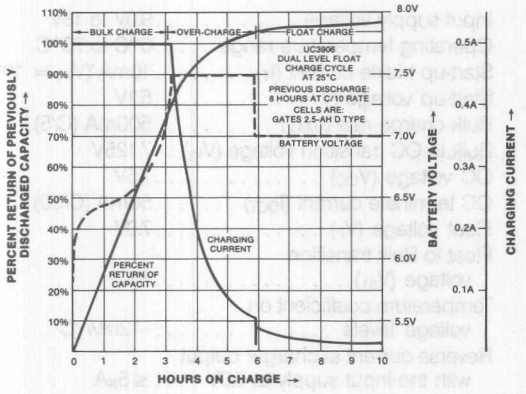


FIGURE 14. The nearly ideal characteristics of the dual level float charger are illustrated in these curves. The over-charge state is entered at about 80% return of capacity and float charging begins at just over 100% return.

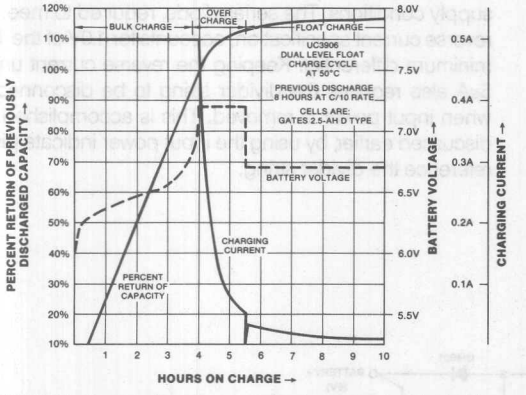


FIGURE 15. At elevated temperatures the maximum capacity of lead-acid cells is increased allowing greater charge acceptance. To prevent excessive over-charging though, the charging voltage levels are reduced.

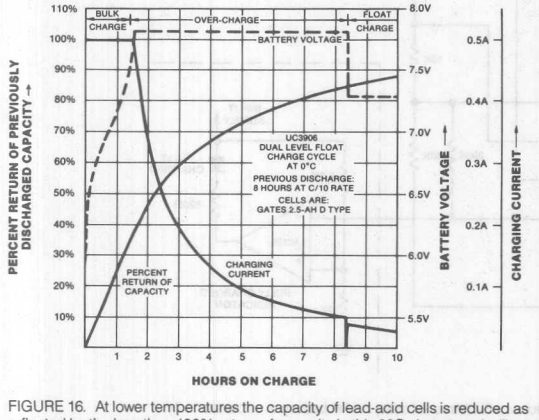


FIGURE 16. At lower temperatures the capacity of lead-acid cells is reduced as reflected by the less-than-100% return of capacity in this 0°C charge cycle, illustrating the need for elevated charging voltages to maximize returned capacity.

The driver on the UC3906 shunts the drive current from the pass device to ground. The 470ohm resistor added between PIN 15 and ground keeps the die dissipation to less than 100mW under worst case conditions, assuming a minimum forward current gain in the pass element of 35 at 500mA.

The charger in figure 13 includes a circuit to detect full charge and gives a visual indication of charge completion with an LED. This circuit turns on the LED when the battery enters the float state. Entering of the float state is detected by sensing when the state level output turns-off.

Figures 14-16 are plots of charge cycles of the circuit at three temperatures, 25°C, 50°C and 0°C. The plots show battery voltage, charge rate, and percent return of previously discharged capacity. This last parameter is the integral of the charge current over the time of the charge cycle, divided by the total charge volume removed since the last full charge. For all of these curves the previous discharge was an 80% discharge, (2amp-hours), at a C/10, (250mA), rate. The discharges were preceded by an over-night charge at 25°C.

The less than 100% return of capacity evident in the charge cycle at 0°C is the result of the battery's reduced capacity at this temperature. The tapering of the charge current in the over-charge state still indicates that the cells are being returned to a full state of charge.

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2. Gates Energy Products, Inc., Battery Application Manual, 1982.
3. Panasonic, Sealed Lead-Acid Batteries Technical Handbook.
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UC3620
BRUSHLESS DC MOTORS GET A CONTROLLER IC THAT REPLACES COMPLEX CIRCUITS

A COMMUTATOR AND DRIVER CHIP, COMPLETE WITH THERMAL AND UNDER-VOLTAGE PROTECTION AND TRANSIENT SUPPRESSION, RADICALLY SIMPLIFIES THE CONTROL OF BRUSHLESS DC MOTORS

INTRODUCTION

The popularity of the three-phase, brushless DC motor is on the rise for a number of good reasons: There are no brushes to wear out or to arc over, heat dissipation is better because the windings are on the stator, and good torque control is both possible and relatively easy to achieve with the availability of electronic circuits. The motor's main drawback has been the need to design and assemble a complex circuit consisting of six output power transistors with transient suppression diodes, a switching current control circuit, and a Hall logic decoder, plus loop control and protection circuitry.

The advent of the UC3620 controller chip greatly simplifies the designer's problem, for it integrates all these elements. This chip easily and safely controls motors requiring up to 2A of continuous current, and has a peak rating of 3A. The device has a maximum V_{CC} rating of 40V and is available in a 15-pin package rated at 25W. Only a half dozen external components are needed to get a motor running.

A three-phase brushless DC motor has two, four, or more permanent magnet poles mounted on its rotor. The required rotating field is produced by the stator's stationary windings, whose three phases must be commutated in the proper sequence. This sequence is governed by the rotor's angular position, and consequently, some means must be provided both to sense this position and to use that information to control the commutation sequence.

The sensing is accomplished by three Hall-effect devices mounted on the stator close to the rotor magnets, at the correct rotational angles. An electronic circuit decodes the Hall device signals and controls the direction of the currents applied to the three motor phases. This power switching is done by power transistors.

Another function must be added to the driving electronics, namely, that of controlling the motor current and maintaining it at the correct value. At high speed, the electric motor's back emf limits the phase currents. But at low speeds, the back emf is low (it is zero at stall), and therefore if the current is to be kept constant, the applied voltage must be reduced. This is done by sensing the motor current and using its value to regulate the duty cycle of the applied voltage, thereby controlling the average motor voltage. In this way, a constant-current source of motor power is obtained.

HOW IT WORKS

In the controller chip, each of the three output stages is a totem-pole pair (Figure 1) capable of sourcing and sinking the motor's full rated current. Inductive transients from the load are clamped to V_{CC} by Schottky diodes and to ground by the intrinsic substrate diodes, thus obviating the need for external clamping devices.

The power output stages have two functions. The first is to commutate the three motor phases in the proper sequence, producing unidirectional torque in the rotor. The second is to switch the applied motor voltage in the manner selected and programmed by the user, maintaining the output current at the desired level. This switching control of current is accomplished in a fixed-off-time, two-quadrant mode, providing the automatic peak current limiting and low ripple current essential to high electrical efficiency at the motor windings.

The emitters of the three bottom transistors of the totem-pole output stages are connected to Pin 1, through which all the motor current flows. If a low-value resistor is placed between this pin and ground, a usable voltage proportional to motor current is derived without appreciable I^2R losses.

This current-sensing voltage serves as a feedback signal for the switching current control loop. It is applied to the I_{SENSE} input through an RC filter, which prevents false triggering due to noise spikes in the current waveform.

An internal voltage comparator determines whether the voltage $V_{I\ SENSE}$ is equal to V_{REF}, a positive variable reference voltage dependent on the output of the chip's error amplifier. If Q of the monostable multivibrator (that follows the comparator) is high, the chip's output stages are enabled, the output current increases, and $V_{I\ SENSE}$ also increases until it becomes positive with respect to V_{REF}.

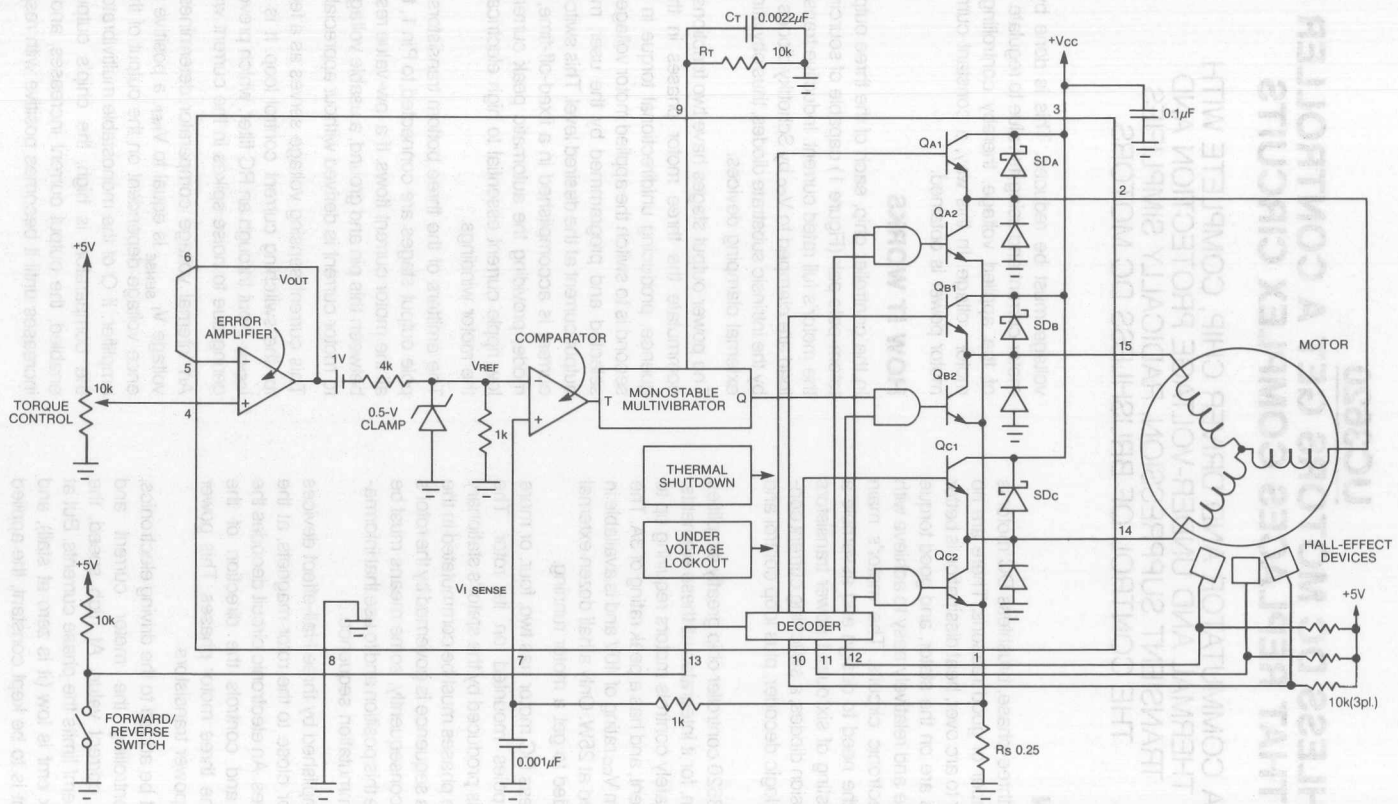


FIGURE 1. THE UC3620 CHIP PROVIDES FULL CONTROL OF MOTOR CURRENTS UP TO 2A, WITH ROTATION IN BOTH DIRECTIONS. HALL-EFFECT DEVICES INTERNAL TO THE MOTOR PROVIDE POSITION INFORMATION THROUGH A DECODER TO THREE TOTEM-POLE DRIVERS. COMPARING THE CHANGING VOLTAGE ACROSS R_S WITH THE ERROR AMPLIFIER OUTPUT HELPS KEEP THE CURRENT CONSTANT.

At this point the comparator resets the monostable, forcing Q low and disabling the output stages. The motor current now circulates through one of the Schottky diodes and the conducting upper transistor because of the stored inductive energy, until the monostable off-time has elapsed (Figure 2). Q then returns to the high state and the cycle is repeated.

The switching off-time is fixed, since it is determined by the user's choice of timing components R_T and C_T. At the start of the off-time, capacitor C_T is charged to +5V, and the monostable outputs are held in the off state until this voltage decays exponentially to a level of 2V. Since resistor R_T supplies the only path for the discharging current, it is possible to calculate the time required, t_{OFF}, in seconds:

$$\exp\left(\frac{-t_{OFF}}{R_T C_T}\right) = \frac{2}{5}$$

or:

$$\frac{-t_{OFF}}{R_T C_T} = \ln(2/5) = -0.916$$

$$t_{OFF} = 0.916 R_T C_T$$

When the 2 volt level is reached, the monostable is set again, and the cycle repeats.

The reference voltage, V_{REF}, then, is the controlling voltage of what is in effect a transconductance amplifier of which the controlled output is the motor current through resistor R_S. To repeat, the circuit controls the peak value of the current. If the switching frequency is high (low current ripple), the assumption may be made that the average value of motor current, I_M, is approximately equal to the peak, and so:

$$V_{REF} = I_M R_S$$

$$G_T = \frac{I_M}{V_{REF}} = \frac{1}{R_S} \text{ Siemens}$$

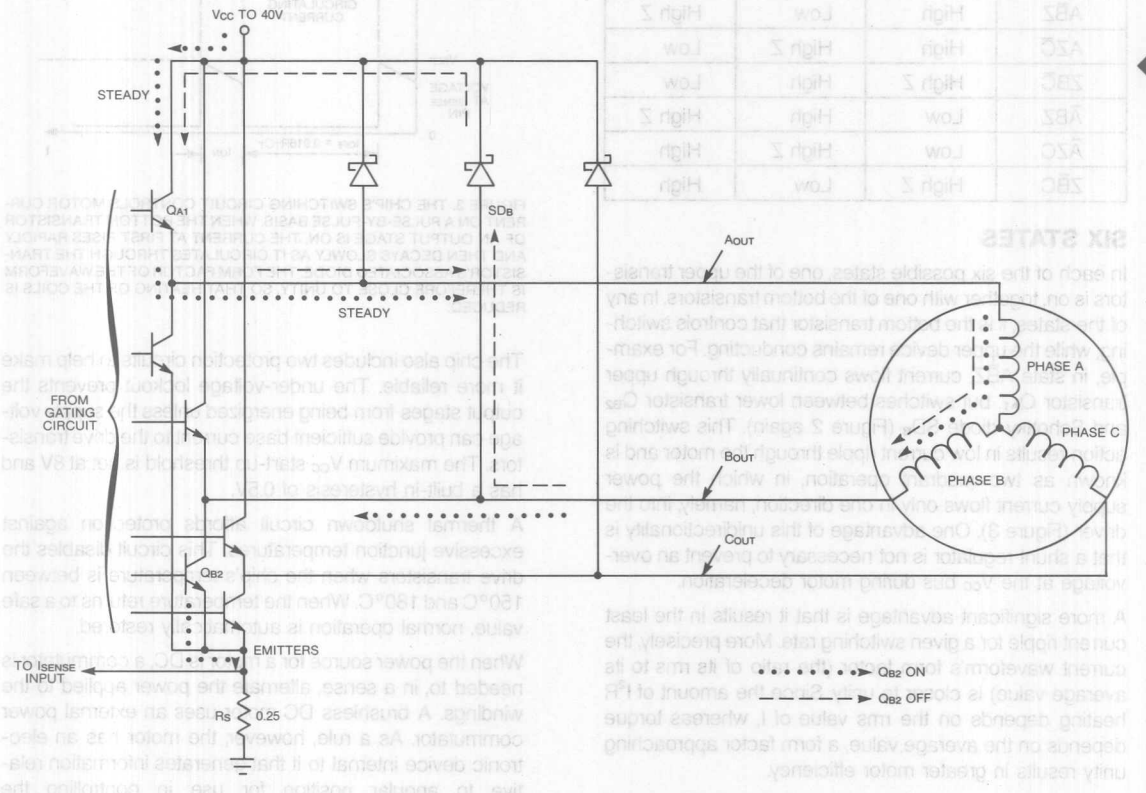


FIGURE 2. WHEN Q_{B2} IS ON, CURRENT FLOWS THROUGH Q_{A1} AND TWO MOTOR WINDINGS TO GROUND (DOTTED ARROWS). DURING THE TIME THAT Q_{B2} IS OFF, THE STORED ENERGY IN THE WINDING INDUCTANCE FLOWS THROUGH SCHOTTKY DIODE SD_B, TRANSISTOR Q_{A1}, AND BACK THROUGH THE WINDINGS (DASHED ARROWS).

The maximum value of V_{REF} is limited to 0.5V by a zener diode (Figure 1 again). This value sets a limit to the maximum motor current as well, since:

$$I_{MAX} = \frac{0.5}{R_S} \text{ amperes}$$

Consequently, the proper selection of R_S protects both the motor and the chip from excess current.

The motor is connected to the chip's three outputs A_{OUT}, B_{OUT}, and C_{OUT}. The motor windings are Y-connected, and the driver energizes two phases at a time, the third one being off. Thus each driver output will be in one of three states: high (V_{CC}), off (high impedance), or low (0V), generating six possible combinations (Table 1).

Table 1. Terminal Conditions for Different Driver Output States

OUTPUT STATE	TERMINAL A	TERMINAL B	TERMINAL C
$A\bar{B}Z$	High	Low	High Z
$AZ\bar{C}$	High	High Z	Low
$ZB\bar{C}$	High Z	High	Low
$\bar{A}BZ$	Low	High	High Z
$\bar{A}ZC$	Low	High Z	High
$Z\bar{B}C$	High Z	Low	High

SIX STATES

In each of the six possible states, one of the upper transistors is on, together with one of the bottom transistors. In any of the states, it is the bottom transistor that controls switching, while the upper device remains conducting. For example, in state $A\bar{B}Z$, current flows continually through upper transistor Q_{A1}, but switches between lower transistor Q_{B2} and Schottky diode SD_B (Figure 2 again). This switching action results in low current ripple through the motor and is known as two-quadrant operation, in which the power supply current flows only in one direction, namely, into the driver (Figure 3). One advantage of this unidirectionality is that a shunt regulator is not necessary to prevent an overvoltage at the V_{CC} bus during motor deceleration.

A more significant advantage is that it results in the least current ripple for a given switching rate. More precisely, the current waveform's form factor (the ratio of its rms to its average value) is closer to unity. Since the amount of I^2R heating depends on the rms value of I, whereas torque depends on the average value, a form factor approaching unity results in greater motor efficiency.

The current reference voltage V_{REF} at the inverting input of the chip's comparator depends on the output voltage, V_{OUT}, of the error amplifier. The relationship between the two is:

$$V_{REF} = \frac{V_{OUT} - 1}{5}$$

The offset of 1V between V_{OUT} and the 5:1 voltage divider ensures that the error amplifier can always achieve zero current at the motor. The amplifier itself has a high gain of 80dB minimum, an f_t of 0.8MHz; and is internally compensated for stable operation.

In a feedback speed control application, even with a reduction in gain of 14dB due to the 5:1 resistive attenuator between the amplifier and the comparator, there is still a minimum DC gain of 66dB, which is more than adequate for most requirements. The same consideration applies to the 1V offset, which is overshadowed by the high-gain loop as well.

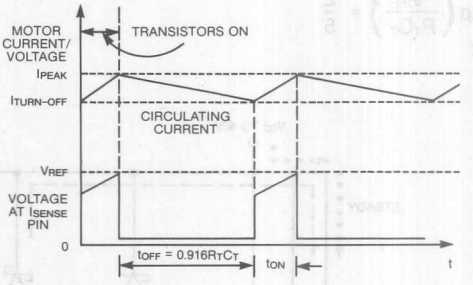


FIGURE 3. THE CHIP'S SWITCHING CIRCUIT CONTROLS MOTOR CURRENT ON A PULSE-BY-PULSE BASIS. WHEN THE BOTTOM TRANSISTOR OF AN OUTPUT STAGE IS ON, THE CURRENT AT FIRST RISES RAPIDLY AND THEN DECAYS SLOWLY AS IT CIRCULATES THROUGH THE TRANSISTOR'S ASSOCIATED DIODE. THE FORM FACTOR OF THE WAVEFORM IS THEREFORE CLOSE TO UNITY, SO THAT HEATING OF THE COILS IS REDUCED.

The chip also includes two protection circuits to help make it more reliable. The under-voltage lockout prevents the output stages from being energized unless the supply voltage can provide sufficient base current to the drive transistors. The maximum V_{CC} start-up threshold is set at 8V and has a built-in hysteresis of 0.5V.

A thermal shutdown circuit affords protection against excessive junction temperatures. This circuit disables the drive transistors when the chip's temperature is between 150°C and 180°C. When the temperature returns to a safe value, normal operation is automatically restored.

When the power source for a motor is DC, a commutator is needed to, in a sense, alternate the power applied to the windings. A brushless DC motor uses an external power commutator. As a rule, however, the motor has an electronic device internal to it that generates information relative to angular position for use in controlling the commutator.

CONTROLLING BRUSHLESS MOTORS TO 2A

The control chip was designed to drive any three-phase brushless DC motor of up to 2A and is particularly suited for motors with integral Hall-effect devices. H_A, H_B, and H_C (Figure 1 again) are TTL-compatible inputs that, together with the Forward-Reverse input (FWD/REV), determine the output states (Table 2).

The commutation logic built into the UC3620 is intended for use with motors with 120 electrical degree Hall codes. Motors that use the alternative 60 electrical degree code can be easily accomodated with the addition of an inverter to reverse polarity of one of the Hall signals.

When used as described, the device operates in a current feedback mode and acts as a current controller, or rather as a transconductance amplifier. This closed-loop circuit can be made part of another feedback loop to control the motor speed. Controlled speed loops are of interest in many applications, some of which require a very high degree of control accuracy. For example, a crystal-referenced phase-locked loop is needed to control the spindle speed of magnetic disk drives.

Table 2. Hall Device Logic Coding

HALL DEVICE INPUTS			FORWARD/ REVERSE LINE	DRIVER OUTPUT
H_A	H_B	H_C		
1	0	1	1	$A\bar{B}Z$
1	0	0	1	$AZ\bar{C}$
1	1	0	1	$ZB\bar{C}$
0	1	0	1	$\bar{A}BZ$
0	1	1	1	$\bar{A}ZC$
0	0	1	1	$Z\bar{B}C$

Note: A change of state in the Forward/Reverse line inverts the output states, thus reversing the direction.

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APPLICATION NOTE

1.5 MHZ CURRENT MODE IC CONTROLLED 50 WATT POWER SUPPLY

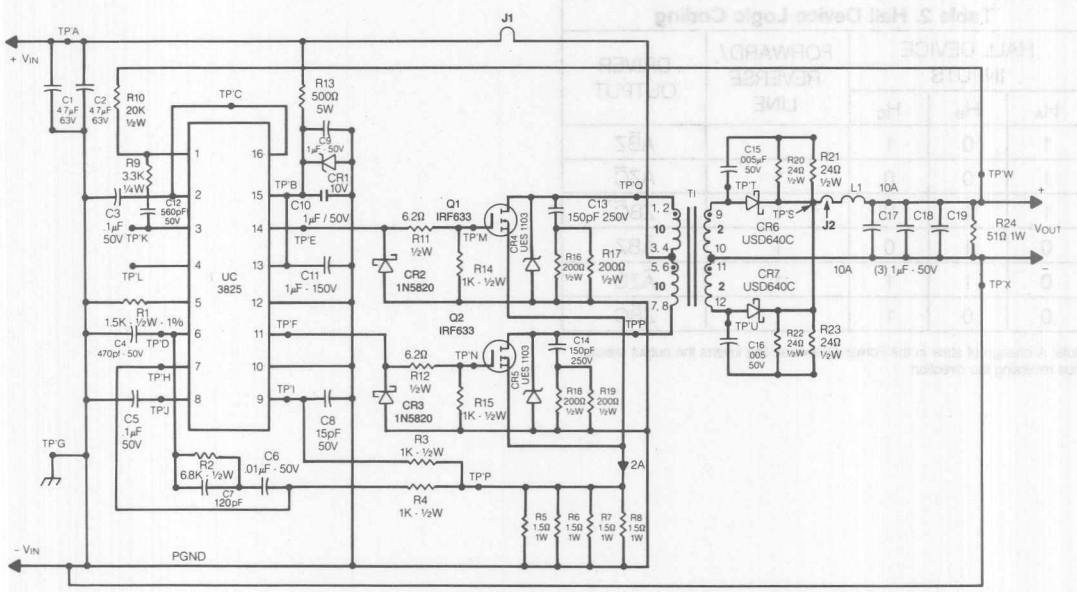
Abstract

This application note highlights the development of a 1.5 megahertz current mode IC controlled, 50 watt power supply. Push-pull topology is utilized for this DC to DC converter application of +48 volts input to +5 volts at 10 amps output. The beneficial increase in switching speed and dynamic performance is made possible by a new pulse width modulator, the Unitrode UC3825. Reductions in magnetic component sizes are realized and the selections of core geometry, ferrite material and flux density are discussed. The effects of power losses throughout the circuit on overall efficiency are also analyzed.

Introduction

The switching frequencies of power supplies have been steadily increasing since the advent of cost effective MOSFETS, used to replace the conventional bipolar devices. While the transition time in going from twenty to hundreds of kilohertz has been brief, few designers have ventured into, or beyond, the one megahertz benchmark. Until recently, those who have, had utilized discrete pulse width modulation designs due to the absence of an integrated circuit truely built for high speed. The 1.5 MHZ power supply shown schematically in figure 1 was designed to exemplify high frequency power conversion under the supervision of such an IC controller, the UC3825.[1]

Figure 1. Schematic Diagram



II. POWER SUPPLY SPECIFICATIONS

Input Voltage Range:	42 to 56 VDC
Switching Frequency:	1.5 MHz
Output Power:	51 Watts Max.
Output Voltage:	5.1 VDC Nom.
Output Current:	2–10 ADC
Line Regulation:	5 MV
Load Regulation:	15 MV
Output Ripple:	100 MV Typ.
Efficiency:	75% Typ.

III. OPERATING PRINCIPLES

Power can efficiently be converted using any of several standard topologies. Design tradeoffs of cost, size and performance will generally narrow the field to one that is most appropriate. For this demonstration application, the center-tapped push-pull configuration has been selected.

Current mode control provides numerous advantages over conventional duty cycle control, and has been implemented as the regulation method. In review, the error amplifier output (outer control loop) defines the level at which the primary current

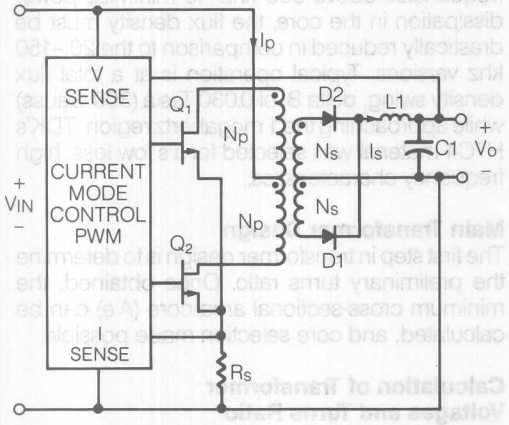


Figure 2. Basic Diagram — Push-Pull Converter Using Current Mode Control

(inner loop) will regulate the pulse width, and output voltage. Pulse-by-pulse symmetry correction (flux balancing) is inherent to current mode controllers, and essential for the push-pull topology to prevent core saturation.

A basic current mode controlled, mosfet switched push-pull converter is shown in figure 2. Transistor Q1 is turned on by a drive pulse from the PWM, causing primary current I_p to flow through the transformer primary, mosfet Q1 and sense resistor R_s. Simultaneously, diode D1 conducts current $I_p \times N_p/N_s$ in the secondary, storing energy in inductor L1 and delivering power to the output load. When Q1 receives a turn-off pulse from the PWM, it halts the current flow in the primary. Secondary current continues due to the filter inductor L1. Diodes D1 and D2 each conduct one-half the DC output current during these converter "off" times. This entire process is repeated on alternate cycles, as Q2 next is toggled on and off. The basic waveforms are shown in figure 3 for reference.

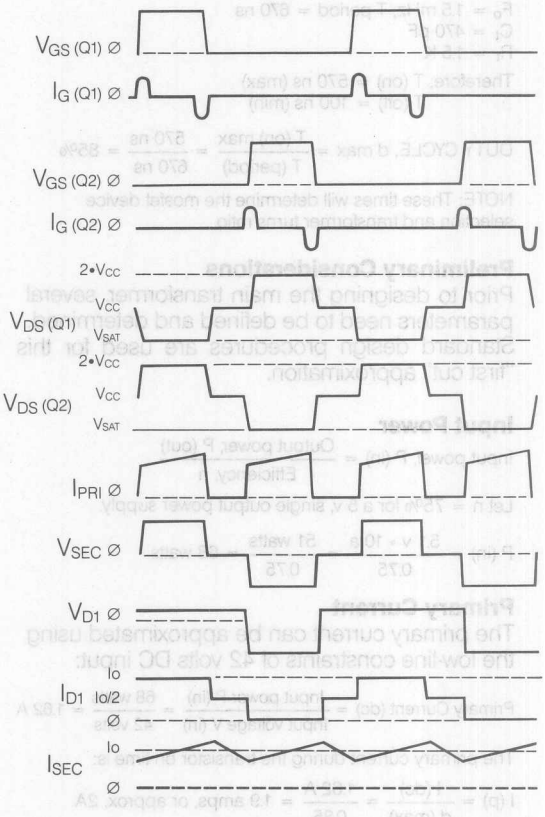


Figure 3. Basic Push-Pull Waveforms

IV. DESIGN CONSIDERATIONS

Auxiliary Supply Voltage

The 9.2 volt minimum requirement of the UC3825 and 20 volt gate-source maximum of the mosfets imply an approximate 10 thru 18 volt range of inputs. The 10 volt value was selected to supply both V_{CC} and V_C (totem pole outputs) while keeping power dissipation in the IC low. The circuit used is a simple resistor-zener dissipative network with ample bypassing capacitors located near the IC to reduce noise.

Oscillator Frequency

The oscillator frequency selected is 1.5 MHz, resulting in a 670 nanosecond period. From the UC3825 data sheet, oscillator frequency versus R_t, C_t, and deadtime curves:

F_o = 1.5 mHz; T period = 670 ns
C_t = 470 pF
R_t = 1.5 K

Therefore; T (on) = 570 ns (max)
T (off) = 100 ns (min)

$$\text{DUTY CYCLE, d max} = \frac{\text{T (on) max}}{\text{T (period)}} = \frac{570\text{ ns}}{670\text{ ns}} = 85\%$$

NOTE: These times will determine the mosfet device selection and transformer turns ratio.

Preliminary Considerations

Prior to designing the main transformer, several parameters need to be defined and determined. Standard design procedures are used for this "first cut" approximation.

Input Power

$$\text{Input power, P (in)} = \frac{\text{Output power, P (out)}}{\text{Efficiency, n}}$$

Let n = 75% for a 5 v, single output power supply.

$$\text{P (in)} = \frac{5.1\text{ v} \cdot 10\text{ a}}{0.75} = \frac{51\text{ watts}}{0.75} = 68\text{ watts}$$

Primary Current

The primary current can be approximated using the low-line constraints of 42 volts DC input:

$$\text{Primary Current (dc)} = \frac{\text{Input power P (in)}}{\text{Input voltage V (in)}} = \frac{68\text{ watts}}{42\text{ volts}} = 1.62\text{ A}$$

The primary current during the transistor on time is:

$$\text{I (p)} = \frac{\text{I (dc)}}{\text{d (max)}} = \frac{1.62\text{ A}}{0.85} = 1.9\text{ amps, or approx. 2A}$$

The RMS primary current is:

$$\text{Ip (rms)} = \text{Ip}\sqrt{\text{duty}} = 1.24\text{A (rms)}$$

Sense Resistor R (s)

Primary current is sensed and controlled in a current mode controller by first developing a voltage proportional to the primary current, used as an input to UC3825. This is accomplished by sense resistor R (s) with a calculated value of the I limit threshold value divided by the primary current at the desired current limit point, typically 120% I (max).

$$\text{R (s)} \leq \frac{\text{V th (pin 9)}}{120\% \cdot \text{I (pri)}} = \frac{1\text{ volt}}{1.2 \cdot 2\text{ amps}} = 0.42\text{ ohm}$$

Mosfet DC Losses

A high quality mosfet is used to keep both DC and switching losses low, with an R (ds) on max of 0.8 ohms. Calculation of the voltage drops across the device are required for the transformer design.

V ds (on) = Rds (max) • I (p) = 0.8 • 2 = 1.6 v

During an overload; V ds (max) = 0.8 • 2 • 1.20 = 1.92 v (2 v)

P dc = I dc² Rds max • duty
= 2² • 0.8 • 0.85/2 = 1.35 watts

Selection of Core Material

Few manufacturers provide core loss curves for frequencies above 500 khz. To minimize power dissipation in the core, the flux density must be drastically reduced in comparison to the 20 –150 khz versions. Typical operation is at a total flux density swing, delta B, of 0.030 Tesla (300 Gauss) while approaching the 1 megahertz region. TDK's H7C4 material was selected for it's low loss, high frequency characteristics.

Main Transformer Design

The first step in transformer design is to determine the preliminary turns ratio. Once obtained, the minimum cross-sectional area core (Ae) can be calculated, and core selection made possible.

Calculation of Transformer Voltages and Turns Ratio

V pri (min) = V in (min) – V xtor (max) – V (Rs) max
V p (min) = 42 v – 2.0 v – 1 v
= 39.0 v

V sec (min) = V out (max) + V diode (max)
+ V choke (dc) + V (losses)
V sec (min) = 5.1 + 0.65 + 0.1 + 0.05 (est) = 5.9 v

$$\text{Turns ratio N} = \frac{\text{V pri (min) Duty (max)}}{\text{V sec (min)}} = \frac{39.0 \cdot 0.85}{5.9} = 5.6{:}1$$

The secondary is designed for excellent coupling using copper foil, and the primary has been rounded to the nearest lower turns.

Turns ratio: N = N pri / N sec = 5:1

The actual number of both primary and secondary turns will be determined by the ferrite core characteristics as a function of operating frequency and Gauss level.

Minimum Core Size

The minimum cross-sectional area core that can be used is calculated with the following equation for core loss limited applications.

$$Ac\ (min) = \frac{V\ (pri)\ min \cdot Duty\ (max) \cdot 10^4}{2 \cdot Freq. \cdot N\ (p) \cdot \Delta B\ (Tesla)}\ (cm^2)$$

At first it would seem that the core area required for this 1.5 MHZ switcher would be ten times smaller than that of a 150 KHZ version. This would be true if the flux density, number of turns and core losses remained constant. However, losses are a function of both frequency and frequency squared[2] and as it increases, the flux density swing (ΔB) must be drastically reduced to provide a similar core loss, hence temperature rise. In this example, an acceptable figure was selected of one percent of the total output power, or one-half watt. Empirically, this translates to a temperature rise of 25°C, at 325 Gauss (0.0325 Tesla) for cores with a cross-sectional area of 0.70 sq. cm, a ballpark estimate of the true core size.

This formula can be rewritten as:

$$Ac \cdot Np = \frac{V\ pri \cdot D\ max \cdot 10^4}{2 \cdot F \cdot \Delta B}$$

This is a more convenient formula because the right hand side of the equation contains all constants. Input voltage, frequency of operation and flux density have already been determined. The selection of core size (cross-sectional area) is inversely proportional to the number of primary turns, and vice-versa. Based on the five-to-one turns ratio, an original assumption of five turns for the primary would result in a large core size for this 50 watt application. Alternatively, a ten turn primary is used to minimize core size.

Substituting previous values for high line operation at 0.0325 Tesla (325 Gauss) and a magnetic operating frequency of 750 kHz:

$$Ac\ (min) = \frac{39 \cdot 0.85 \cdot 10^4}{2 \cdot 750{,}000 \cdot 10 \cdot 0.0325} = 0.68\ cm^2$$

Core Loss Limited Conditions

As the switching frequencies are increased, generally a reduction of core size or minimum number of turns is realized. This is true, however, but only to the point at which the increasing core losses prevent a further reduction of either size or minimum turns. This crossover point occurs at different frequencies for each individual ferrite material based upon their losses and acceptable circuit losses, or temperature rise[3].

Core Geometry Selection

A variety of standard core shapes are available in the cross-sectional area range of 0.62 to 0.84 cm^2. Considerations of safety agency spacing requirements, physical dimensions, window area and relative cost of assembly must be evaluated.

Core Style	Description	AC (cm^2)	Weight (g)
PQ	PQ 20/20	0.62	15
POT CORE	P 22/13	0.63	13
LP	LP 22/13	0.68	21
TOROID	T 28/13	0.76	26
EE	EE 35/28	0.78	28

The LP 22/13 style was selected to easily terminate (breakout) the high current output windings. For a given cross-sectional area, it occupies less PC board space, and has good shielding characteristics.

Wire Size Selection

The single, most difficult task in high frequency magnetic design is to minimize the eddy current losses, or skin effects while optimizing wire sizes. Penetration depth refers to the thickness (or depth) into a copper conductor in which a wave will penetrate for a specific frequency. For copper at 100°C:

$$d\ pen = 7.5 / (frequency^{0.5})\ (cm)$$

At 750 kHz, this corresponds to $8.66 \cdot 10^3$ cm, or about the thickness of an AWG #39 wire. Larger size wire can be used, however the AC current flows only in the depth penetrated at the switching frequency. Consult the UNITRODE DESIGN SEMINAR SEM-400 book, appendix M2 for additional information on this subject.

For low current windings, several strands of thin wire can be paralleled, or twisted together forming a "bundle." Seven wires twisted around each other closely approximate a round conductor with a net diameter of three times the individual wire diameter. This twisting is commonly done at 10-12 turns per foot, and significantly reduces parasitics between wires at high frequencies.

Medium to high current windings require the use of Litz wire, a similar bundle of numerous conductors. Copper foil is also an excellent choice.

Industry practice is to operate at 450 amps (RMS) per centimeter squared, or $2.22 \cdot 10^{-3}$ cm²/A. This applies to windings operating at an acceptable temperature rise.

Area required = I rms / 450A / cm²

Primary area (Axp) = 1.24A / 450A / cm² = $2.75 \cdot 10^{-3}$ cm²

Calculate Secondary RMS Current.

$$\text{I rms (sec)} = \frac{\text{I sec}^2\,(\text{duty on}) + \frac{\text{I sec}^2\,(2 \cdot \text{duty off})}{2}}{2}$$

$$\text{I rms (sec)} = \frac{10^2\,(.425) + \frac{5^2\,(2 \cdot .075)}{2}}{2}$$

I rms (sec) = 4.81A

Secondary Area (Axs) = 4.81A / 450A / cm²
= $1.07 \cdot 10^{-2}$ cm²

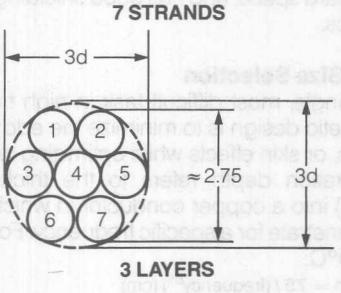


Figure 4.

For a given bundle of 7 conductors, the cross-sectional area of each conductor equals:

$$\frac{\text{Required area}}{\text{\# conductors}} = \frac{\text{Axp}}{7} = \frac{2.75 \cdot 10^{-3}}{7} = 3.93 \cdot 10^{-4}\ \text{cm}^2$$

The cross-sectional area of an AWG #36 wire is $1.32 \cdot 10^{-4}$, therefore, three bundles of seven conductors each should be used. Two bundles were utilized as a compromise between practical winding considerations and acceptable eddy current losses.

Copper foil is used for the secondary, with a required width slightly less than the bobbin width, and thickness determined by:

$$\frac{\text{Secondary area (Axs)}}{\text{Bobbin width}} = \frac{1.07 \cdot 10^{-2}\ \text{cm}}{1.40\ \text{cm}} = 7.64 \cdot 10^{-3}\ \text{cm}$$

This corresponds to 0.003″ thick foil, a standard value. In practice, slightly thicker foil (0.004″ to 0.005″) may be required to minimize power losses in the transformer.

Transformer Assembly

Standard practice to increase coupling between primary and secondary is position both as closely as possible to each other inside the transformer. In this design, the first layer wound is one primary, and the next layer is the corresponding secondary. This is again followed by the other secondary and primary. It is important to keep the secondaries in close proximity since both will be conducting simultaneously twice per period. The primaries do not conduct in this manner, so coupling from primary A to primary B is not critical, only primary A to secondary C, and primary B to secondary D.

Referring to the transformer schematic, primary A is wound closest to the bobbin. After insulation, secondaries C and D are wound bifilar and insulated. Primary B is wound last, then terminated so that primaries A and B are wired in series, likewise for secondaries C and D.

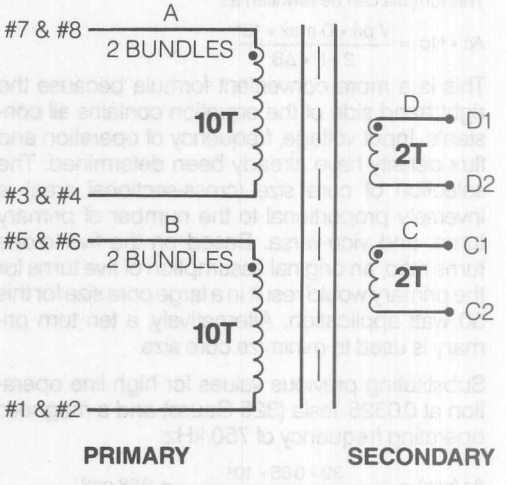


Figure 5. Transformer Schematic

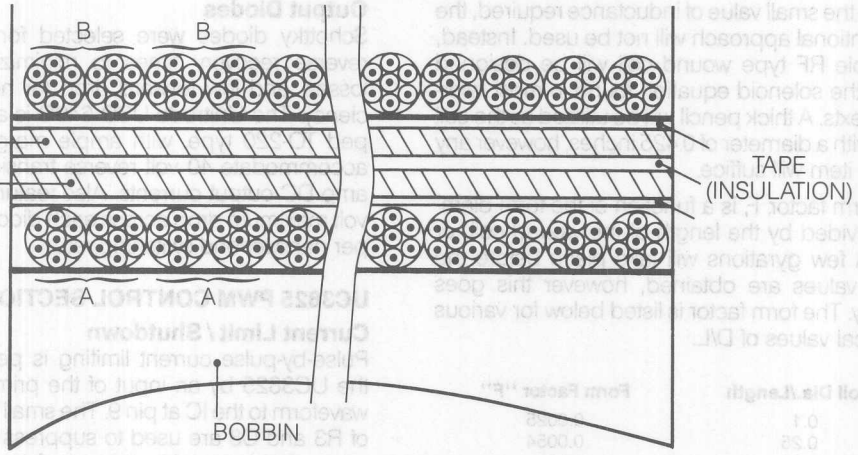


Figure 6. Transformer — Exploded View

Calculation of Winding Resistances and Losses

The mean length of turn for the bobbin can be determined from the specifications of O.D. and I.D., and for the BLP 22/13 a figure of 4.51 cm or 1.77 in. was obtained. AWG #36 wire has a resistance of $1.82 \cdot 10^{-2}$ ohms/cm at 100°C for the following:

Primary resistance can be calculated:

$$Rpri = \frac{R\ wire \cdot M.L.T. \cdot \#\ turns}{\#\ wires} = \frac{0.0182 \cdot 4.51 \cdot 10}{14} = 0.0586\ ohm$$

Voltage drop and power loss in each half winding can be also calculated:

$$V\ (R\ pri) = Ipri \cdot Rpri = 2.0 \cdot 0.58 = 0.116\ volt\ (negligible)$$

$$P\ (Rpri) = R\ pri \cdot I\ pri^2 \cdot duty = 0.0586 \cdot 4 \cdot 0.425 = 0.0996\ watts$$

The resistance of the secondary can be approximated by using the wire tables, and substituting the foil for wire of similar cross-sectional area. In this example, AWG #16 wire is used to obtain Rsec $= 1.58 \cdot 10^{-4}$ ohms/cm.

$$Rsec = R\ foil \cdot M.L.T. \cdot \#\ turns = 1.58 \cdot 10^{-4} \cdot 4.5 \cdot 2 = 0.00143\ ohm$$

$$V\ (Rsec) = 1.43 \cdot 10^{-3} \cdot 10 = 0.0143\ volt\ (negligible)$$

$$P\ (Rsec) = R\ sec\ ((Idc^2 \cdot D\ on) + ((Idc/2)^2 \cdot 2 \cdot D\ off))$$

$$P\ (Rsec) = 0.00143\ ((10^2 \cdot 0.425) + (5^2 \cdot 0.15) = 0.066\ watts$$

Transformer Power Losses

The total copper losses for two windings are then:

$$P\ cu = P\ (Rpri) + P\ (Rsec) = 2 \cdot (0.066 + 0.0996) = 0.332\ watts$$

Estimated eddy current losses are approximately 50% of the copper losses. Pcu ≈ 0.50 watts.

Given the core material type, geometry, frequency and operating Gauss level, the ferrite losses can be calculated. From the manufacturers information, the typical loss coefficient for H7C4 material operating at a flux density swing of 0.035 Tesla (350 Gauss) at 750 kHz is 0.15 watts per cubic centimeter of core volume, which is 3.327 cm^3 per LP 22/13 core set. Therefore:

$$P\ core = 3.327 \cdot 0.15 = 0.50\ watt$$

The total power lost is a summation of the copper and ferrite losses:

$$P\ xfmr = P\ cu + P\ core = 0.50 + 0.50 = 1.00\ watts$$

OUTPUT SECTION

Output Choke Calculations

Typically, the RMS output ripple current is less than 15% I dc, or 1.5 amps in this case. Delta I, the peak to peak ripple therefore is twice the RMS, or 3 amps.

$$V = \frac{L\ di}{dt} : L = \frac{V\ dt}{di} = \frac{5.9\ v\ (350)\ 10^{-9}\ s}{3.0\ A} = 690\ nanohenries$$

Due to the small value of inductance required, the conventional approach will not be used. Instead, a simple RF type wound coil will be designed using the solenoid equation found in most reference texts. A thick pencil will be utilized as the coil form with a diameter of 0.425 inches, however any similar item will suffice.

The form factor, F, is a function of the form diameter divided by the length of the wound coil, or D/L. A few gyrations will take place before the exact values are obtained, however this goes quickly. The form factor is listed below for various practical values of D/L.

Coil Dia./Length	Form Factor "F"
0.1	0.0025
0.25	0.0054
0.50	0.010
1.0	0.0173
2.0	0.026
5.0	0.040

$L\ (\mu H) = F \cdot N^2 \cdot D\ (in),\ N = (L/F \cdot D)^{1/2}$ (turns)

For D = 0.425, D/L = 1 (approx); F = 0.0173

$N = (0.690 / 0.0173 \cdot 0.425)^{1/2} = 9.76$ turns

Rounding off to the nearest next number of turns, the actual inductance for 10 turns can be calculated:

$L\ (\mu h) = 0.0173 \cdot 10^2 \cdot 0.425 = 744$ nanohenries

In an air core inductor the permeability "u" equals unity, therefore the flux density B equals the driving function H.

Output Capacitor

$$Q = \frac{I\ p\text{-}p}{2} \cdot \frac{T\ period}{2} \cdot \frac{I}{2},\ \text{Delta } Q = I\ p\text{-}p / 8 \cdot F$$

C = Q / dV where dV (output ripple) equals 0.100 volts.

$C = I\ p\text{-}p / 8 \cdot F \cdot dV = 3 / 8 \cdot 1.5 \cdot 10^6 \cdot 0.10 = 2.5\ \mu F$

Three 1 μf caps are used in parallel. With a typical ripple voltage of <50 mv due to ESR, the ESR each (at 1.5 mHz) must be approximately 150 milliohms. The Unitrode ceramic monolithic capacitor series was selected for their excellent high frequency characteristics.

Resonance, and its effect at these frequencies must be taken into account. In this case, the capacitor reaches resonance at 1.5 mHz, and the effective impedance is resistive.

Output Diodes

Schottky diodes were selected for their short reverse recovery times to minimize switching losses, and low forward drop for high DC efficiency. The Unitrode USD 640C is a center-tapped TO-220 type, with ample margin to safely accommodate 40 volt reverse transients and 10 amp DC output currents. Also featured is a 0.65 volt maximum drop across each diode and 1 volt per nanosecond switching rate.

UC3825 PWM CONTROL SECTION

Current Limit / Shutdown

Pulse-by-pulse current limiting is performed by the UC3825 by an input of the primary current waveform to the IC at pin 9. The small RC network of R3 and C8 are used to suppress the leading edge glitch caused by turn-on of the mosfet and transformer parasitics. The input must be below the 1 volt threshold or current limiting will occur. Once reached, an input above the threshold will narrow the pulse width accordingly. When this reaches a 1.4 volts amplitude, shutdown of the outputs will occur, and the UC3825 will initiate a soft start routine.

Ramp

The UC3825 offers the flexibility of both Current Mode Control or conventional duty cycle control via the RAMP input pin. When connected to the timing capacitor, the UC3825 operates as a duty cycle control IC. Connecting the RAMP input to the current waveform changes the control method to Current Mode. In this application, the ramp waveform is tied through a small RC filter network to the primary current waveform. This network is defined in the next section — slope compensation. The dynamic range of this input is 1-3 volts, and is generally used for introducing slope compensation to the PWM.

Slope Compensation

Slope compensation is required to compensate for the peak to average differences in primary current as a function of pulse width. Adding a minimum of 50% of the reflected downslope of the output current waveform to the primary current is required. See UNITRODE APPLICATION NOTE U-93 and U-97 for further information. Empirically, 60-75% should be used to accommodate circuit tolerances and increase stability[5]

Resistors R2 and R4 in this circuit form a voltage divider from the oscillator output to the RAMP input, superimposing the slope compensation on the primary current waveform. Capacitor C6 is an AC coupling capacitor, and allows the 1.8 volt swing of the oscillator to be used without adding offset circuitry. Capacitor C7 has a two-fold purpose. During turn on it filters the leading edge noise of the current waveform, and provides a negative going pulse across R4 to the ramp input at the end of each cycle. This overrides any parasitic capacitance at the ramp input, (pin 7), that would tend to hold it above zero volts. This insures the proper voltage input at the beginning of the next cycle.

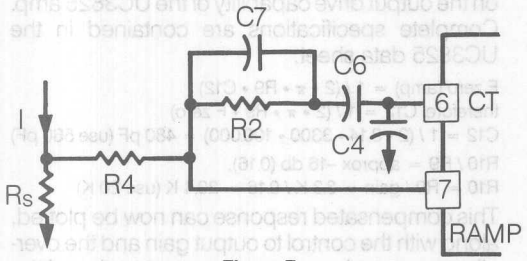


Figure 7.

For the purposes of determining the resistor values, capacitors C4 (timing), C6 (ac coupling) and C7 (filtering) can be removed from the circuit schematic. The simplified model represented in figure 8 is used for the calculations. These calculations can be applied to all Current Mode circuits using a similar scheme.

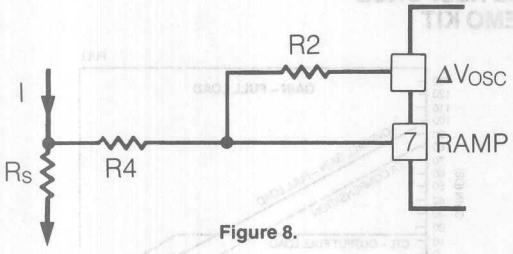


Figure 8.

STEP 1. Calculate Inductor Downslope

$S(L) = di/dt = V\,sec / L = 5.9\,V / .740\,\mu H = 8.0\,A/\mu s$ (1)

STEP 2. Calculate Reflected Downslope to Primary

$S(L)' = S(L) / N\,(turns\ ratio) = 8.0/5 = 1.6\,A/\mu S$ (2)

STEP 3. Calculate Equivalent Ramp Downslope Voltage

$V\,S(L)' = S(L)' \bullet Rsense = 1.6 \bullet 0.375 = 0.600\,V/\mu s$ (3)

STEP 4. Calculate Oscillator Slope

$V\,S\,(osc) = d\,(V\,osc) / T\,on = 1.8\,V / 570\,ns = 3.15\,V/\mu s$ (4)

STEP 5. Generate the Ramp Equations

Using superposition, the circuit can be configured as:

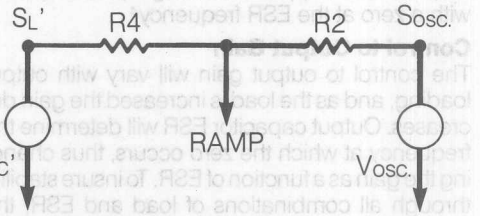


Figure 9.

$$V\,(ramp) = \frac{V\,S\,(L)' \bullet R2}{R2 + R4} = \frac{V\,S\,(osc) \bullet R4}{R2 + R4} \quad (5)$$

SUBSTITUTING,

$V\,(ramp) = V\,S\,(L)'' + V\,S\,(comp)$ (6)

WHERE

$$V\,S\,(comp) = \frac{V\,S\,(osc) \bullet R4}{R2 + R4}; \quad V\,S\,(L)'' = \frac{V\,S\,(L)' \bullet R2}{R2 + R4}$$

STEP 6. Calculate Slope Compensation

$V\,S\,(comp) = m \bullet S(L)''$ (7)

Where m equals the amount of inductor downslope to be introduced. In this example, let m = 75%, or 0.75.

$$\frac{V\,S\,(osc) \bullet R4}{R2 + R4} = \frac{m \bullet V\,S(L)' \bullet R2}{R2 + R4}$$

SOLVING FOR R2:

$$R2 = R4 \bullet \frac{V\,S\,(osc)}{V\,S\,(L)' \bullet m} = R4 \bullet \frac{3.15}{0.600 \bullet 0.75} \quad (9)$$

USING CIRCUIT VALUES,

$R2 = 7.05 \bullet R4$

For simplicity, let R4 equal 1 K ohms and R2 therefore equals 7.05 K. Using the nearest standard value resistor of 6.8 K, the exact amount of downslope is minimally affected. Important, however, is that the series combination of R2 and R4 is high enough in resistance not to load down the oscillator and cause frequency shifting.

CLOSING THE FEEDBACK LOOP

Error Amplifier

Compensation of the high gain error amplifier in the UC3825 is straight forward. There is a single-pole at approximately 5 hertz. A zero will be introduced in the compensation network to provide gain once the zero db threshold is crossed. Using Current Mode control greatly simplifies the compensation task as the output choke is controlled by the inner current loop, thus making the output section appear as a single pole response with a zero at the ESR frequency.[4]

Control to Output Gain

The control to output gain will vary with output loading, and as the load is increased the gain decreases. Output capacitor ESR will determine the frequency at which the zero occurs, thus changing the gain as a function of ESR. To insure stability through all combinations of load and ESR, the amplifier will be compensated to cross zero db at approximately one-fifth of the switching frequency with ample phase margin.

The output filter pole and zero occur at

$F_p = 1/2\ \pi\ R\ (load)\ C\ (output)$

$F_z = 1/2\ \pi\ R\ (esr)\ C\ (output)$

CIRCUIT PARAMETERS:

C (output) = 3 μF; ESR (each) = 0.050 min – 0.300 max

For three capacitors in parallel, ESR = 0.016 – 0.100 ohms

R (output) = 2.5 ohms at 2 A, 0.5 ohms at 10 A

Using the above equations;

F_p (2A) = $1 / (2 \cdot 3.14 \cdot 2.5 \cdot 3 \cdot 10^{-6}) = 21.2$ kHz

F_p (10A) = $1 / (2 \cdot 3.14 \cdot 0.5 \cdot 3 \cdot 10^{-6}) = 106.1$ kHz

F_z (high) = $1 / (2 \cdot 3.14 \cdot 0.016 \cdot 3 \cdot 10^{-6}) = 3.315$ mHz

F_z (low) = $1 / (2 \cdot 3.14 \cdot 0.100 \cdot 3 \cdot 10^{-6}) = 530.5$ kHz

GAIN

$$\frac{V\ (output)}{V\ (control)} = K \cdot R_o, \text{ where } K = \frac{Ipri \cdot N_p/N_s}{V\ (control)} = \frac{2 \cdot 5}{0.85} = 11.76$$

Therefore, at 2 amps and 10 amps,

$V_o/V_c = K \cdot ro = 11.76 \cdot 2.5 = 29.4$ db (2A)

$V_o/V_c = K \cdot ro + 11.76 \cdot 0.5 = 15.4$ db (10A)

Error Amplifier Compensation

The control to output gain can be plotted along with the desired zero db crossing point and an estimate of the error amplifier required compensation network can be made. The amp compensation should have a zero at approximately 100 kHz, and a gain of –16 db at this frequency. Resistor R9 has been selected to be 3.3 k ohms based on the output drive capability of the UC3825 amp. Complete specifications are contained in the UC3825 data sheet.

F zero (amp) = $1 / (2 \cdot \pi \cdot R9 \cdot C12)$

therefore, C12 = $1 / (2 \cdot \pi \cdot R9 \cdot F\ zero)$

C12 = $1 / (2 \cdot 3.14 \cdot 3300 \cdot 100.000) = 480$ pF (use 560 pF)

R10 / R9 = approx –16 db (0.16),

R10 = R9 / gain = 3.3 K / 0.16 = 20.4 K (use 20 K)

This compensated response can now be plotted, along with the control to output gain and the overall power supply response is a summation of the two curves, as seen in figures 11 and 12. Low frequency gains of 100 db at full load, and 115 db at light load are obtained, with a zero db crossing at approx. 100 kHz for both. Phase margin is generous with approx. 90 degrees for both light and 45 degrees at full load.

GAIN AND PHASE RESPONSE
UC3825 DEMO KIT

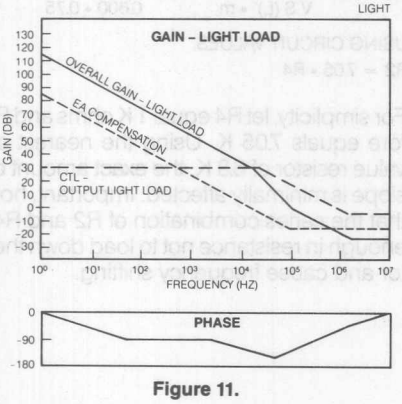


Figure 11.

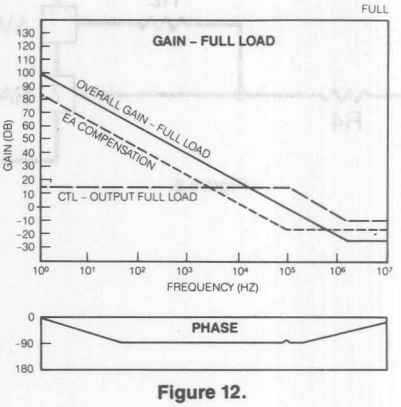


Figure 12.

LIST OF MATERIALS

REFERENCE	DESCRIPTION	
Capacitors		
C1, 2	4.7 μF, 63 VDC Electrolytic	
C3, 5	0.1 μF, 50 VDC Monolithic	
C4	470 pF, VDC Monolithic	
C6	0.01 μF, 50 VDC Monolithic	
C7	120 pF, 50 VDC Monolithic	
C8	15 pF, 50 VDC Monolithic	
C9-11, 17-19	1 μF, 50 VDC Monolithic	
C12	560 pF, 50 VDC Monolithic	
C13, 14	150 pF, 150 VDC Ceramic	
C15, 16	5000 pF, 50 VDC Ceramic	
Diodes		
CR1	1N4465	10 V, 1.5 Watt Zener
CR2, 3	USD1140	40 V, 1 Amp Schottky
CR4, 5	UES1105	150 V, 2.5 Amp Ultrafast
CR6, 7	USD640C	40 V, 12 Amp Schottky
Integrated Circuits		
U1	UC3825	Unitrode High Speed PWM
Transistors		
Q1, 2	UFN633	150 V, 8A Mosfet
Resistors		
R1	1.5 K, 1/2 W, 1%	
R2	6.8 K, 1/2 W, 5%	
R3, 4, 14, 15	1 K, 1/2 W, 5%	
R5-8	1.5 R, 1 W, 5%	
R9	3.3 K, 1/2 W, 5%	
R10	20 K, 1/2 W, 5%	
R11, 12	6.2 R, 1/2 W, 5%	
R13	500 R, 5 W, 10%	
R16-19	200 R, 1/2 W, 5%	
R20-23	24 R, 1/2 W, 5%	
R24	51 R, 1 W, 5%	
Magnetics		
L1	740 nH Wound Coil	
T1	AIE Magnetics Custom Transformer, 5:1 Turns Ratio	
Miscellaneous		
H1	Heatsink—Mosfets (AAALL #5786B)	
H2	Heatsink—Diodes (AAALL #5299B)	

Efficiency Measurements

V (In)	I (In)	P (In)	P (Loss)	Efficiency
42	1.707	71.7	20.2	71.8%
48	1.483	71.2	19.7	72.4%
56	1.331	73.2	21.7	70.4%

V (In) V	Vout (2A)	Vout (5A)	Vout (10A)	Load Reg. MV
42	5.110	5.102	5.093	17
48	5.108	5.101	5.092	16
56	5.108	5.102	5.089	19
Line	2 mv	1 mv	4 mv	

Dynamic Performance

The power supply was pulse loaded from 5 amps to 10 amps at a frequency of 100 kilohertz. Recovery to within 50 mv was less than 2 microseconds with a total excursion of less than 200 millivolts. High speed FETS were used to switch the load current with typical rise/fall times of 50 nanoseconds.

Short Circuit

The short circuit input current is approximately 0.75 amps, or an input power of 36 watts.

Circuit Power Losses

The total circuit losses are approximated using both the calculated and measured losses throughout the power supply.

Power Losses

Current Sense Circuit	1.2 W
Output Diodes	9.8 W
Switching Transistors	3.2 W
Dropping Resistor	3.0 W
Snubber Networks	1.0 W
Transformer Losses	1.0 W
Auxiliary Supply	0.8 W
Miscellaneous	0.2 W
TOTAL LOSSES	20.2 W

If a bootstrapped technique is utilized in the auxiliary supply to the IC and drive circuitry, the dropping resistor losses of three watts can be reduced to 0.1 watts in the bootstrap circuitry. In addition, the lossy resistive current sensing network can be replaced by a small current transformer, lowering the losses by a half-watt. Overall efficiency would then increase to 75%, fairly high for a five volt output application. Noteworthy is that the switching losses at this high of frequency can be minimized, and have little overall effect on circuit efficiency.

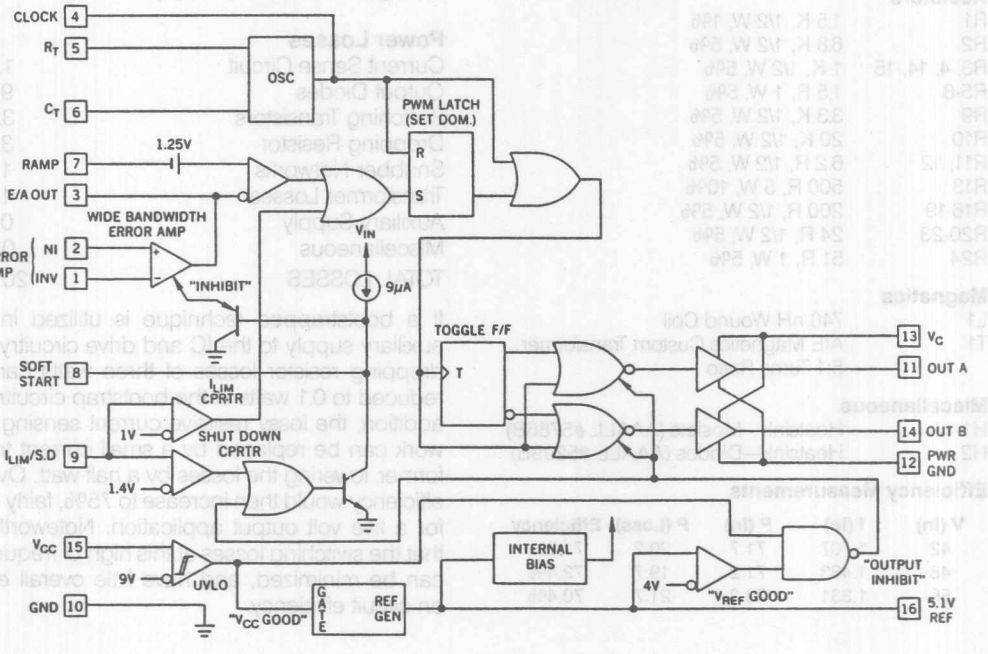
Summary

The demands of higher power densities will undoubtedly throttle many switch-mode power supply designs into and beyond the megahertz region in the near future. Designers will be facing the challenges of selecting switching devices, magnetic materials and IC controllers built exclusively for high efficiency at these frequencies. The thrust from contemporary hundreds of kilohertz designs to megahertz versions is rapidly making progress. This 1.5 MHZ current mode push-pull is an example of what can successfully be accomplished with existing high speed components and technology.

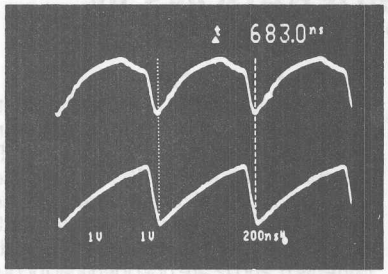
References

1. Woffard, Larry, — "New Pulse Width Modulator Chip Controls, MHZ Switchers" — U-107; Unitrode Applications Handbook 1987/88.
2. Dixon, Lloyd Jr. — "Eddy Current Losses" Section M2-4, Unitrode Power Supply Design Seminar Book, SEM-500.
3. Andreycak, Bill — "1.5 MHZ Current Mode IC Controlled 50 Watt Power Supply," Proceedings of the High Frequency Power Conversion Conference, 1986.
4. Dixon, Lloyd Jr. — "Closing the Feedback Loop" Section C1 — Unitrode Power Supply Design Seminar Book, SEM-500.
5. Andreycak, Bill "Practical Considerations in Current Mode Power Supplies" Topic 1 — Unitrode Power Supply Design Seminar Book, SEM-500.

UC3825 BLOCK DIAGRAM



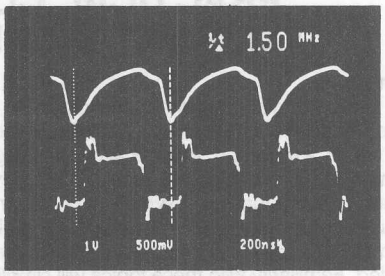
TIMING WAVEFORMS



Top Trace
Ramp Voltage
TP 'H', 1 v/cm

Bottom Trace
CT Waveform,
TP 'D', 1 v/cm

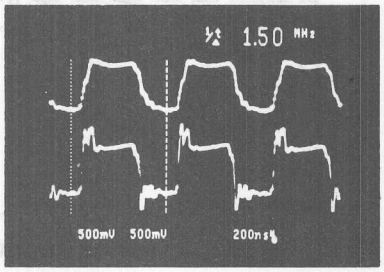
RAMP VOLTAGE



Top Trace
Filtered I_P with
Slope Compensation
TP 'H', 1 v/cm

Bottom Trace
Unfiltered I_P
TP 'P', .5 v/cm

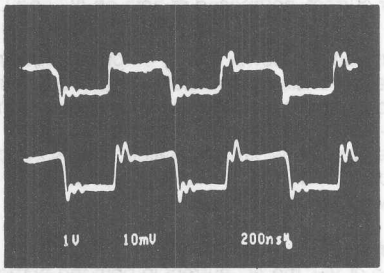
PRIMARY CURRENT



Top Trace
Filtered I_P
TP 'I', .5 v/cm

Bottom Trace
Unfiltered I_P
TP 'P', .5 v/cm

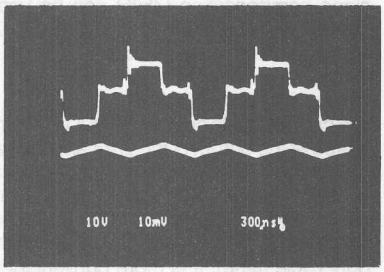
PRIMARY CURRENT



Top Trace
J1, 2 A/cm

Bottom Trace
TP 'P', 1 v/cm

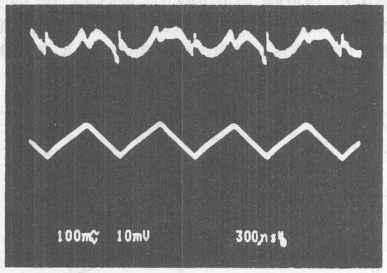
SECONDARY WAVEFORMS



Top Trace
Secondary Voltage
TP 'T', 10 v/cm

Bottom Trace
Secondary Current
J2, 5 A/cm

OUTPUT WAVEFORMS



Top Trace
Output Voltage
Ripple & Noise
TP 'W', 100 mv/cm

Bottom Trace
AC Output Current
J2, 2 A/cm

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PRACTICAL CONSIDERATIONS IN CURRENT MODE POWER SUPPLIES

Introduction

This detailed section contains an in-depth explanation of the numerous PWM functions, and how to maximize their usefulness. It covers a multitude of practical circuit design considerations, such as slope compensation, gate drive circuitry, external control functions, synchronization, and paralleling current mode controlled modules. Circuit diagrams and simplified equations for the above items of interest are included. Familiarity with these topics will simplify the design and debugging process, and will save a great deal of time for the power supply design engineer.

I. SLOPE COMPENSATION

Current mode control regulates the PEAK inductor current via the 'inner' or current control loop. In a continuous mode (buck) converter, however, the output current is the AVERAGE inductor current, composed of both an AC and DC component.

While in regulation, the power supply output voltage and inductance are constant. Therefore, V_{OUT} / L_{SEC} and dI/dT, the secondary ripple current, is also constant. In a constant volt-second system, dT varies as a function of V_{IN}, the basis of pulse width modulation. The AC ripple current component, dI, varies also as a function of dT in accordance with the constant V_{OUT} L_{SEC}.

Average Current

At high values of V_{IN}, the AC current in both the primary and the secondary is at its maximum. This is represented graphically by duty cycle D1, the corresponding average current I1, and the ripple current d(I1). As V_{IN} decreases to its minimum at duty cycle, the ripple current also is at its minimum amplitude. This occurs at duty cycle D2 of average current I2 and ripple current d(I2). Regulating the peak primary current (current mode control) will produce different AVERAGE output currents I1, and I2 for duty cycles D1 and D2. The average current INCREASES with duty cycle when the peak current is compared to a fixed error voltage.

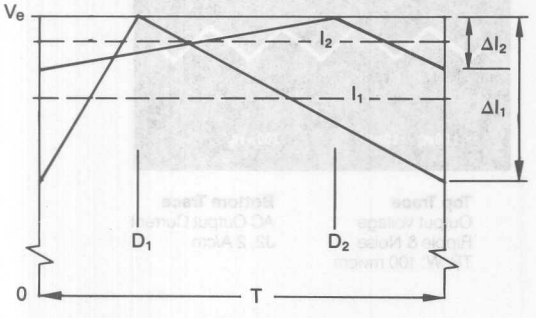


Figure 1. Average Current Error

Constant Output Current

To maintain a constant AVERAGE current, independent of duty cycle, a compensating ramp is required. Lowering the error voltage precisely as a function of T_{ON} will terminate the pulse width sooner. This narrows the duty cycle creating a CONSTANT output current independent of T_{ON}, or V_{IN}. This ramp simply compensates for the peak to average current differences as a function of duty cycle. Output currents I1 and I2 are now identical for duty cycles D1 and D2.

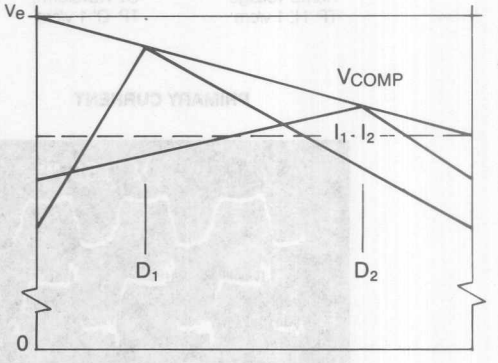


Figure 2. Constant Average Current

Determining the Ramp Slope

Mathematically, the slope of this compensating ramp must be equal to one-half (50%) the downslope of the output inductor as seen from the control side of the circuit. This is proven in detail in "Modelling, Analysis and Compensating of the Current Mode Controller," (Unitrode publication U-97 and its references). Empirically, slightly higher values of slope compensation (75%) can be used where the AC component is small in comparison to the DC pedestal, typical of a continuous converter.

Circuit Implementation

In a current mode control PWM IC, the error voltage is generated at the output of the error amplifier and compared to the primary current at the PWM comparator. At this node, subtracting the compensating ramp from the error voltage, or adding it to the primary current sense input will have the same effect: to decrease the pulse width as a function of duty cycle (time). It is more convenient to add the slope compensating ramp to the current input. A portion of the oscillator waveform available at the timing capacitor (C_T) will be resistively summed with the primary current. This is entered to the PWM comparator at the current sense input.

Parameters Required for Slope Compensation Calculations

Slope compensation can be calculated after specific parameters of the circuit are defined and calculated.

SECTION	PARAMETER
Control	T on (Max) Oscillator
	ΔV Oscillator (PK-PK Ramp Amplitude)
	I Sense Threshold (Max)
Output	V Secondary (Min)
	L Output
	I AC Secondary (Secondary Ripple Current)
General	R Sense (Current Sensing Resistor)
	M (Amount of Slope Compensation)
	N Turns Ratio (N_P / N_S)

Once obtained, the calculations for slope compensation are straightforward, using the following equations and diagrams.

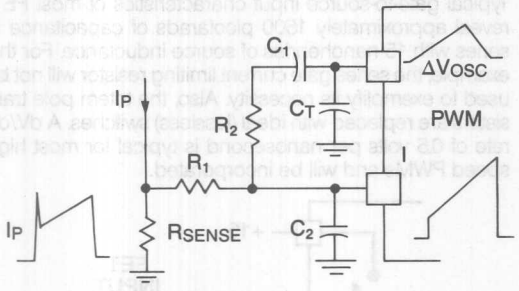


Figure 3. General Circuit

Resistors R1 and R2 form a voltage divider from the oscillator output to the current limit input, superimposing the slope compensation on the primary current waveform. Capacitor C1 is an AC coupling capacitor, and allows the AC voltage swing of the oscillator to be used without adding offset circuitry. Capacitor C2 forms an R-C filter with R1 to suppress the leading edge glitch of the primary current wave. The ratio of resistor R2 to R1 will determine the exact amount of slope compensation added.

For purposes of determining the resistor values, capacitors C_T (timing), C1 (coupling), and C2 (filtering) can be removed from the circuit schematic. The oscillator voltage (V_{OSC}) is the peak-to-peak amplitude of the sawtooth waveform. The simplified model is represented schematically in the following circuit.

These calculations can be applied to all current mode converters using a similar slope compensating scheme.

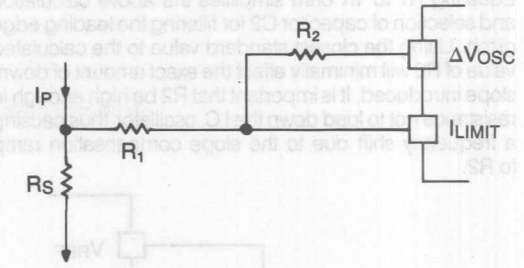


Figure 4. Simplified Circuit

Step 1. Calculate the Inductor Downslope
$S(L) = di/dt = V_{SEC}/L_{SEC}$ (Amps/Second)

Step 2. Calculate the Reflected Downslope to the Primary
$S(L)' = S(L)/N$ (Amps/Second)

Step 3. Calculate Equivalent Downslope Ramp
$V\,S(L)' = S(L)' \bullet R\ sense$ (Volts/Second)

Step 4. Calculate the Oscillator Charge Slope
$V\,S_{(OSC)} = d\,(V_{OSC}) / T\ on$ (Volts/Second)

Step 5. Generate the Ramp Equations
Using superposition, the circuit can be illustrated as:

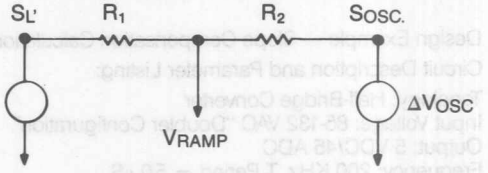


Figure 5. Superposition

$$V_{(RAMP)} = \frac{V\,S(L)' \bullet R2}{R1 + R2} + \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} \quad \text{simplifying,}$$

$$V_{(RAMP)} = V\,S(L)'' + V\,S_{(COMP)} \quad \text{where}$$

$$V\,S_{(COMP)} = \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2}\text{, and } V\,S(L)'' = \frac{V\,S(L)' \bullet R2}{R1 + R2}$$

Step 6. Calculate Slope Compensation
$V\,S(COMP) = M \bullet S(L)''$ where M is the amount of inductor downslope to be introduced.

$$\text{Equating } \frac{V\,S_{(OSC)} \bullet R1}{R1 + R2} = \frac{M \bullet V\,S(L)' \bullet R2}{R1 + R2}$$

, solving for R2

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M}$$

Equating R1 to 1K ohm simplifies the above calculation and selection of capacitor C2 for filtering the leading edge glitch. Using the closest standard value to the calculated value of R2 will minimally effect the exact amount of downslope introduced. It is important that R2 be high enough in resistance not to load down the I.C. oscillator, thus causing a frequency shift due to the slope compensation ramp to R2.

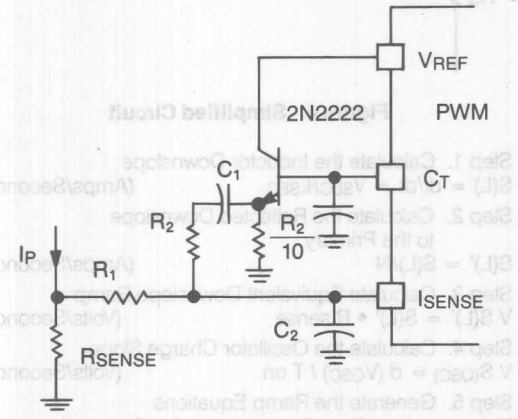


Figure 6. Emitter Follower Circuit

Design Example — Slope Compensation Calculations

Circuit Description and Parameter Listing:

Topology: Half-Bridge Converter
Input Voltage: 85-132 VAC "Doubler Configuration"
Output: 5 VDC/45 ADC
Frequency: 200 KHz, T Period = 5.0 μS
T Deadtime: 500 ns, T on Max = 4.5 μS
Turns Ratio: 15 / 1, (Np/Ns)
V Primary: 90 VDC Min, 186 Max
V Sec Min: 6 VDC
R Sense: 0.25 Ohm
I Sec Ac: 3.0 Amps (<10% I DC)
L Output: 5.16 μh

1. Calculate the Inductor Downslope on the Secondary Side
S (L) = di/dt = V_{SEC}/L_{SEC} = 6 v/5.16 μh = 1.16 A/μs
2. Calculate the Transformed Inductor Slope to the Primary Side
S (L)' = S (L) • Ns/Np = 1.16 • 1/15 = 0.0775 A/μS
3. Calculate the Transformed Slope Voltage at Sense Resistor
V S(L)' = S (L)' • Rsense = 7.72 • 10^{-2} • 0.250 = 1.94•10^{-2} V/μS
4. Calculate the Oscillator Slope at the Timing Capacitor
$S_{(OSC)}$ = d V osc/T on max = 1.8/4.5 = 0.400 V/μS
5. Let Amount of Slope Compensation (M) = 0.75 and R1 = 1K

$$R2 = R1 \bullet \frac{V\,S_{(OSC)}}{V\,S(L)' \bullet M} \; ; R2 = \frac{1K \bullet 0.400}{0.0192 \bullet 0.75}$$

= 27.4 K ohms

II. GATE DRIVE CIRCUITRY

The high current totem-pole outputs of most PWM ICs have greatly enhanced and simplified MOSFET gate drive circuits. Fast switching times of the high power FETs can be attained with nearly a "direct" drive from the PWM. Frequently overlooked, only two external components — a resistor and Schottky diode are required to insure proper operation of the PWM while delivering the high current drive pulses.

MOSFET Input Impedance

Typical gate-to-source input characteristics of most FETs reveal approximately 1500 picofarads of capacitance in series with 15 nanohenries of source inductance. For this example, the series gate current limiting resistor will not be used to exemplify its necessity. Also, the totem pole transistors are replaced with ideal (lossless) switches. A dV/dT rate of 0.5 volts per nanosecond is typical for most high speed PWMs and will be incorporated.

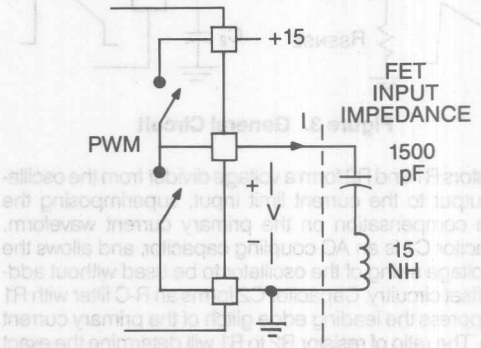


Figure 7. Ideal Circuit Gate Drive

Assuming no external circuit parasitics of R, L or C, the PWM is therefore driving an L-C resonant tank with no attenuation. The driving function is a 15 volt pulse derived from the auxiliary supply voltage. The resulting current waveform is shown in figure 8, having a peak current of approximately seven amps at a frequency of thirty-three megahertz.

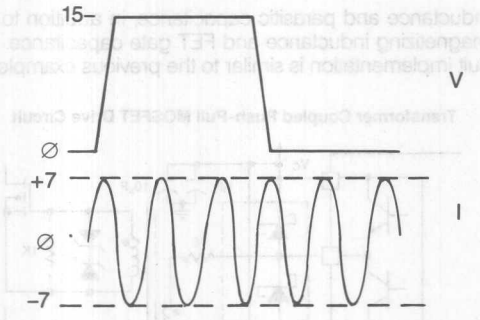


Figure 8. Voltage & Current Waveforms at Gate

In a practical application, the transistors and other circuit parameters, fortunately, are less than ideal. The results above are unlikely to happen in most designs, however they will occur at a reduced magnitude if not prevented.

Limiting the peak current through the IC is accomplished by placing a resistor between the totem-pole output and the gate of the MOSFET. The value is determined by dividing the totem-pole collector voltage (Vc) by the peak current rating of the IC's totem-pole. Without this resistor, the peak current is limited only by the dV/dT rate of the totem-pole and the FET gate capacitance.

For this example, a collector supply voltage of 10 volts is used, with an estimated totem-pole saturation voltage of approximately 2 volts. Limiting the peak gate current to 1.5 amps max requires a resistor of six ohms, and the nearest standard value of 6.2 ohms was used. Locating the resistor in series with the collector to the auxiliary voltage source will only limit the turn-on current. Therefore it must be placed between the PWM and gate to limit both turn-on and turn-off currents.

Actual circuit parasitics also play a key role in the drive behavior. The inductance of the FET source lead (15 nanohenries typical) is generally small in comparison to the layout inductance. To model this network, an approximation of 30 nanohenries per inch of PC trace can be used. In addition, the inductance between the pins of the IC and the die can be rounded off to 10 nanohenries per pin. It now becomes apparent that circuit inductances can quickly add up to 100 nanohenries, even with the best of PC layouts. For this example, an estimate of 60 nh was used to simulate the demonstration PC board. The equivalent circuit is shown in figure 10. A 10 volt pulse is applied to the network using 6.2 ohms as the current limiting resistance. Displayed is the resulting voltage and current waveform at the totem-pole output.

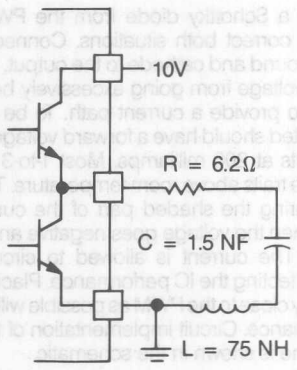


Figure 9. Circuit Parameters

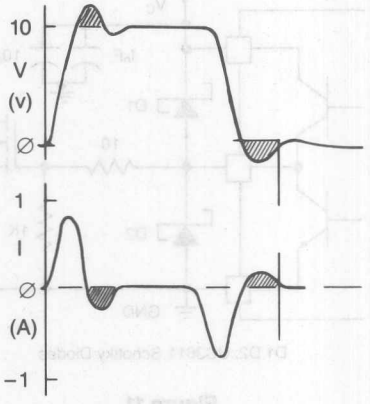


Figure 10. Circuit Response

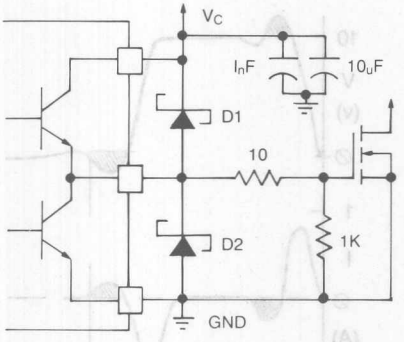
The shaded areas of each graph are of particular interest. During this time, the lower totem-pole transistor is saturated. The voltage at its collector is negative with respect to it's emitter (ground). In addition, a positive output current is being supplied to the RLC network thru this saturated NPN transistor's collector. The IC specifications indicate that neither of these two conditions are tolerable individually, nevermind simultaneously. One approach is to increase the limiting resistance to change the response from underdamped to slightly overdamped. This will occur when:

$$R\ (gate) \geq 2 \bullet \sqrt{L/C}$$

Unfortunately, this also reduces the peak drive current, thus increasing the switching times of the FETS — highly undesirable. The alternate solution is to limit the peak current, and alter the circuit to accept the underdamped network.

The use of a Schottky diode from the PWM output to ground will correct both situations. Connected with the anode to ground and cathode to the output, it will prevent the output voltage from going excessively below ground, and will also provide a current path. To be effective, the diode selected should have a forward voltage drop of less than 0.3 volts at 200 milliamps. Most 1-to-3 amp diodes exhibit these traits above room temperature. The diode will conduct during the shaded part of the curve shown in figure 10 when the voltage goes negative and the current is positive. The current is allowed to circulate without adversely effecting the IC performance. Placing the diode as physically close to the PWM as possible will enhance circuit performance. Circuit implementation of the complete drive scheme is shown in the schematic.

Power MOSFET Drive Circuit

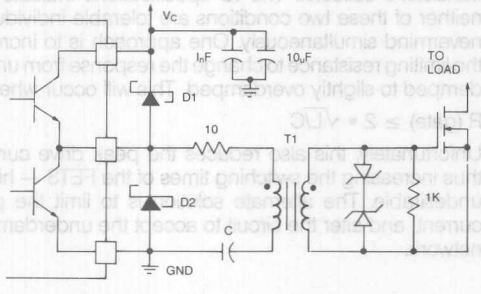


D1.D2: UC3611 Schottky Diodes

Figure 11.

Transformer driven circuits also require the use of the Schottky diodes to prevent a similar set of circumstances from occurring on the PWM outputs. The ringing below ground is greatly enhanced by the transformer leakage inductance and parasitic capacitance, in addition to the magnetizing inductance and FET gate capacitance. Circuit implementation is similar to the previous example.

Transformer Coupled MOSFET Drive Circuit



D1.D2: UC3611 Schottky Diode Array

Figure 12.

Transformer Coupled Push-Pull MOSFET Drive Circuit

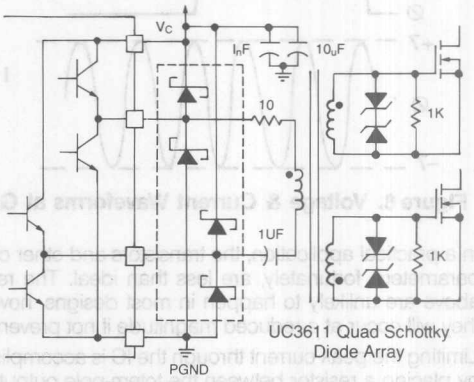


Figure 13.

Peak Gate Current and Rise Time Calculations

Several changes occur at the MOSFET gate during the turn-on period. As the gate threshold voltage is reached, the effective gate input capacitance goes up by about fifteen percent, and as the drain current flows, the capacitance will double. The gate-to-source voltage remains fairly constant while the drain voltage is decreasing. The peak gate current required to switch the MOSFET during a specified turn-on time can be approximated with the following equation.

$$I\,pk = \frac{2}{Ton}\left\{ Ciss\left[(2.5 \bullet Vgth) + \frac{Id}{gm} \right] + [Crss\,(VDD - Vgth)] \right\}$$

Several generalizations can be applied to simplify this equation. First, let Vgth, the gate turn-on threshold, equal 3 volts. Also, assume gm equals the drain current Id divided by the change in gate threshold voltage, dVgth. For most applications, dVgth is approximately 2.5 volts for utilization of the FET at 75% of its maximum current rating. In most off-line power supplies, the gate threshold voltage is a small percentage of the drain voltage and can be eliminated from the last part of the equation. The formulas to determine peak drive current and turn-on time using the FET parameters now simplify to:

$$I\,pk = \frac{2}{Ton} \bullet \{ (10 \bullet Ciss) + (Crss \bullet V\,drain) \}$$

$$Ton = \frac{2}{I\,pk} \bullet \{ (10 \bullet Ciss) + (Crss \bullet Vdrain) \}$$

Switching times in the order of 50 nanoseconds are attainable with a peak gate current of approximately 1.0 amps in many practical designs. Higher drive currents are obtainable using most Unitrode current mode PWMs which can source and sink up to 1.5 amps peak (UC1825). Driver ICs with similar output totem poles (UC1707) are recommended for paralleled MOSFET, high speed applications.

SEE APPLICATION NOTE U-118

III. SYNCHRONIZATION

Power supplies have historically been thought of as "black boxes," an off-the-shelf commodity by most end users. Their primary function is to generate a precise voltage, independent of load current or input voltage variations, at the lowest possible cost. In addition, end users allocate a minimal amount of system real estate in which it must fit. The major task facing design engineers is to overcome these constraints while exceeding the customers' expectations, attaining high power densities and avoiding thermal management problems. It is imperative, too, that the power supply harmonize and integrate with the system rather than cause catastrophic noise problems and last minute headaches. Products that had performed to satisfaction on the lab workbench powered by well filtered linear supplies may not fare as well when driven by a noisy switcher enclosed in a small cabinet.

Basic power supply design criteria such as the switching frequency may be designated by the system clock or CPU and thus may not be up to the power supply designer's discretion. This immediately impacts the physical size of the magnetic components, hence overall supply size, and may result in less-than-optimum power density. However, for the system to function properly, the power supply must be synchronized to the system clock.

There are numerous other reasons for synchronizing the power supply to the system. Most switching power noise has a high peak-to-average ratio of short duration, generally referred to as a spike. Common mode noise generated by these pulsating currents through stray capacitance may be difficult (if not impossible) to completely eliminate after the system design is complete. Ground loop noise may also be amplified due to the interaction of changing currents through parasitic inductances, resultng in crosstalk through the system. EMI filtering to the main input line is much simpler and more repeatable when power is processed at a fixed frequency.

In addition, multiple power stages require synchronization to reduce the differential noise generated between modules at turn-on. In unison, the converters begin their cycles at the same time, each contributing to common mode noise simultaneously, rather than randomly. This also simplifies peak power considerations and will result in predictable power distribution and losses. Compensation made for voltage drops along the bus bars, produced by both the AC and DC power current components, can be accomplished. Balancing of the loads and power bus losses also contributes to diminishing the differential noise and should be administered for optimum results.

Operation of the PWM Oscillator

In normal operation, the timing capacitor (Ct) is linearly charged and discharged between two thresholds, the upper and lower comparator thresholds. The charging current is determined by means of a fixed voltage across a user selected timing resistance (Rt). The resulting current is then mirrored internally to the timing capacitor Ct at the IC's Ct output. The discharge current is internally set in most PWM designs.

As Ct begins its charge cycle, the outputs of the PWM are initiated and turn on. The timing capacitor charges, and when its amplitude equals that of the error amplifier output, the PWM output is terminated and the outputs turn off. Ct continues to charge until it reaches the upper threshold of the timing comparator. Once intersected, the discharge circuitry activates and discharges Ct until the timing comparator lower threshold is reached. During this discharge time, the PWM outputs are disabled, thus insuring a "dead" time when each output is off.

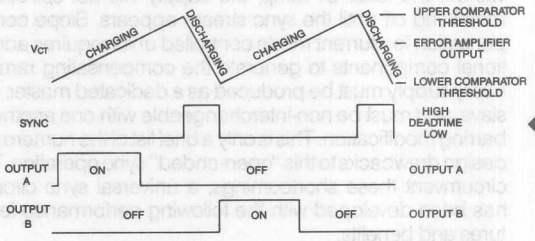


Figure 14. Voltage Mode Control – Normal Operation

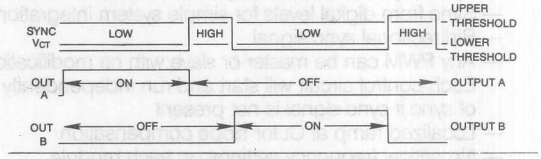


Figure 15.

The SYNC terminal provides a "digital" representation of the oscillator charge/discharge status and can be utilized as both an input or an output on most PWM's. In instances where no synchronization port is easily available, the timing circuitry (Ct) can be driven from a digital (0V, 5V) logic input rather than in the analog mode. The primary considerations of on-time, off-time, duty cycle and frequency can be encompassed in the digital pulse train. A LOW logic level input determines the PWM ON time. Conversely, a HIGH input governs the OFF time, or dead time. Critical constraints of frequency, duty cycle or dead time can be accurately controlled by a digital signal to the PWM timing cap (Ct) input. The command can be executed by anything from a simple 555 timer, to an elaborate microprocessor software controlled routine.

Not all PWM IC's have a direct synchronization input/output connection available to the internal oscillator. In these applications, the slave oscillator must be disabled and driven in a different fashion. This approach may also be required when using different PWMs amongst the slave modules with different sync characteristics, or anti-phase signals.

Unfortunately, there are several drawbacks to this method, depending on the implementation. First, the PWM error amplifier has no control over the pulse width in voltage mode control. The error amplifier output is compared to a digital signal instead of a sawtooth ramp, rendering its attempts fruitless. The conventional soft start technique of clamping the error amp output, thereby clamping the duty cycle will not function. With no local timing ramp available, the supply is completely under the direction of the sync pulse source. Should the pulse become latched or removed, the PWM outputs will either stay fully on, or fully off, depending on the sync level input (voltage mode). Also, without the local Ct ramp, the supply will not self-start, remaining off until the sync stream appears. Slope compensation for current mode controlled units requires additional components to generate the compensating ramp. Every supply must be produced as a dedicated master, or slave, and must be non-interchangeable with one another, barring modification. This is only a brief list of the numerous design drawbacks to this "open-ended" sync operation. To circumvent these shortcomings, a universal sync circuit has been developed with the following performance features and benefits:

— Sync any PWM to/from any other PWM
— Sync any PWM to/from any number of other PWMs
— Sync from digital levels for simple system integration
— Bidirectional sync signal
— Any PWM can be master or slave with no modifications
— Each control circuit will start and run independently of sync if sync signal is not present
— Localized ramp at Ct for slope compensation
— No critical frequency settings on each module
— High speed — minimum delays
— High noise immunity
— Low power requirements
— Remote off capability
— Minimal effect on frequency, duty cycle, and dead time
— Low cost and component count
— Small size

Sync Circuit Operating Principles

These optimal objectives can be obtained using a combination of both analog and digital signal inputs. The timing capacitor Ct input will be used as a summing junction for the analog sawtooth and digital sync input. The PWM is allowed to run independently using its own Rt and Ct components in standard configuration. When synchronization is required, a digital sync pulse will be superimposed on the Ct waveform.

When applied, the sync pulse quickly raises the voltage at Ct above the PWM comparator upper threshold. This forces a change in the oscillator charge/discharge status and operation. The oscillator then begins its normal discharge cycle synchronized to the sync signal. This digital sync pulse simply adds to the analog Ct waveform, forcing the Ct input voltage above the comparator upper threshold.

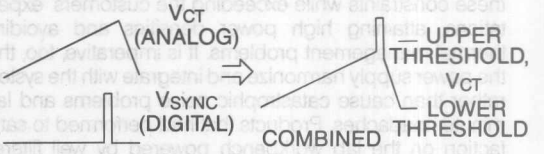


Figure 16.

In practice, this approach is best implemented by bringing Ct to ground through a small resistance, about 24 ohms. This low value was selected to have minimal offset and effects on the initial oscillator frequency. The sync pulse will be applied across the 24 ohm resistor. Since all PWMs utilize the timing capacitor in their oscillator section, it is both a convenient and universal node to work with.

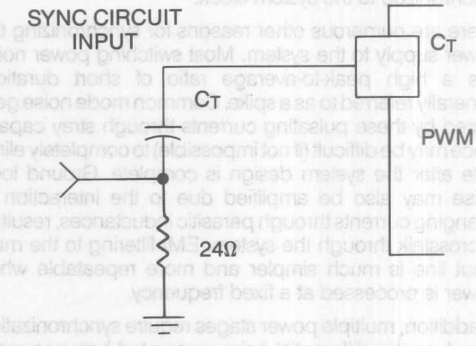


Figure 17. Sync Circuit Implementation

Oscillator Timing Equations

The oscillator timing components must be first selected to guarantee synchronization to the sync pulse. The sawtooth amplitude must be lower than the upper threshold voltage at the desired sync frequency. If not, the oscillator will run in its normal mode and cross the upper threshold first, before the sync pulse. This requirement dictates that the PWM oscillator frequency must be lower than the sync pulse frequency to trigger reliably. Typically, a ten percent reduction in free running frequency can be accommodated throughout the power supply. Adding the sync circuit will have minor effects on the PWM duty cycle, deadtime and ramp amplitude. (These will be examined in detail.)

The Timing Ramp

As mentioned, the timing ramp amplitude needs to be approximately ten percent lower in frequency than normal. Therefore, the MINIMUM sync pulse amplitude must fill the remaining ten percent of the peak-to-peak ramp amplitude to reach the upper threshold. Synchronization can be insured over a wide range of frequency inputs and component tolerances by supplying a slightly higher amplitude sync pulse.

Lowering the peak-to-peak charging amplitude also lowers the peak-to-peak discharge amplitude. This shortens the time required to discharge Ct since it begins at a lower potential. Consequently, this reduces the deadtime accordingly. However, the sync pulse width adds to the IC generated deadtime and increases the effective off, or deadtime due to discharge. This sync pulse width need only be wide enough to be sensed by the IC comparator, which is fairly fast. Additional sync pulse width increases deadtime which can be used to compensate for the 10% lower ramp, hence deadtime.

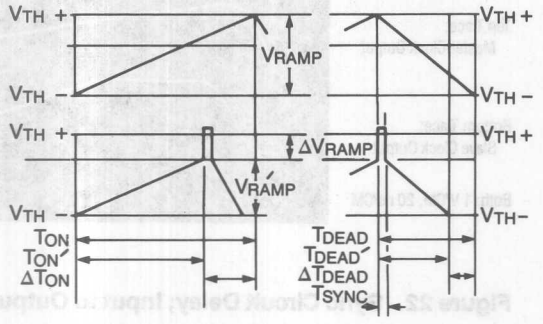


Figure 18. Oscillator Ramp Relationships

Oscillator Ramp Equations

The timing components required in the oscillator section are generally determined graphically from the manufacturers' data sheets for frequency and deadtime versus Rt and Ct. While fine for most applications, a careful examination of the equations is necessary to analyze the impacts of the additional sync circuit components on the timing relationships.

Oscillator Charging Ramp Equations

$$\Delta V\,osc = \frac{1}{Ct}\int I\,chg\,dT = \frac{I\,chg}{Ct}\Big]_0^t \quad T$$

$$T\,chg = \{\,\Delta V\,osc \bullet Ct\,\} / Ichg \quad \text{where } Ichg = Vchg / Rt$$

$$\Delta V\,osc = Vth\ upper - Vth\ lower$$

$$\Delta V\,osc' = \Delta V\,osc\,\frac{(tchg')}{t\,chg(o)} - V\ (24\ ohm)$$

$$V\ (24\ ohm) = I\,chg \bullet 24 = [Vchg / Rt] \bullet 24$$

These equations can be reduced if an approximation is made that the deadtime is very small in comparison to the total period. In this case, the entire effect of changing the ramp voltage is upon the charging time of the oscillator. Synchronizing to a higher frequency simply reduces the charging time of Ct, (Tchg). The new charging time (Tchg') is the original charge time multiplied by the change in frequency between F original and F sync. This relative change will be used in several equations; it is labelled P, for percentage of change.

$$\frac{T\,chg'}{T\,chg(o)} = \frac{T\,sync}{T\,orig} = \frac{F\,orig}{F\,sync} = P\ \text{"relative F change"}$$

For small values of charging current, or large values of Rt, the voltage drop across the 24 ohm resistor is negligible. A current of 2 milliamps will result in a 2.5% timing error with a 2 volt peak to peak oscillator ramp at Ct. It is also preferrable to free-run the IC oscillator at about a 15% lower frequency than the synchronization frequency, where "P" = 0.85.

$$\Delta Vosc'\ (sync) = \Delta Vosc(o) \bullet P = 0.85 \bullet \Delta[Vosc]\ orig.$$

$$T\,chg' = T\,chg(o) \bullet P = 0.85\ T\,chg(o)$$

$$V\ sync\ (minimum)\ amplitude = \Delta\,[Vosc] \bullet (1\text{-}P)$$
$$= 0.15 \bullet \Delta\,[Vosc(o)]$$

With an approximate 2 volt peak to peak oscillator amplitude, the minimum sync pulse amplitude is 0.30 volts for synchronization to occur with a 15% latitude in frequencies.

Oscillator Discharge Ramp Equations

Proper deadtime control in the switching power stage is required to safeguard against catastrophic failures. Adding the sync circuit to the oscillator reduces the discharge time of the timing capacitor Ct, hence reducing the deadtime of the PWM. There are two contributing factors. First, the peak amplitude at the timing capacitor is lowered by ΔV osc(o) – ΔVosc', and the capacitor begins its discharge from a lower potential. Second, the 24 ohm resistor adds an offset voltage, dependent on its current. Typical IC discharge currents range from approximately 6 to 12 milliamps. This offset due to charging current (1-2 ma) is low in comparison to that of the discharge current (6 to 12 ma). While negligible during the charge cycle, its tenfold effects must be taken into account during the discharge, or deadtime.

The discharge time (T dchg) can be calculated knowing the discharge current of the particular IC. More convenient is to use the manufacturers' published deadtime listing for a known value of Ct, and to calculate the effects of the sync circuit. The discharge current has been averaged to 8 milliamps for brevity.

$$\Delta V\,dschg' = [\Delta Vdchg(o) \bullet P] - V\ (24\ ohm)$$
$$= [0.85 \bullet \Delta Vosc(o)] - 0.2\ volts$$

$$T\,dchg' = T\,dchg(o) - T\,loss\ (24\ ohms)$$
where T dchg(o) = initial deadtime from curve
$$= T\,dchg(o) \bullet [\Delta V\,dchg' / \Delta Vosc(o)]$$

The actual deadtime is a summation of both the discharge time of Ct and the width of the sync pulse. While being applied, the sync pulse disables the PWM outputs and must be added to the discharge time. The sync pulse width can be used to compensate for the "lost" deadtime, or as a deadtime extension.

T dead' = T dchg' + T sync pulse width

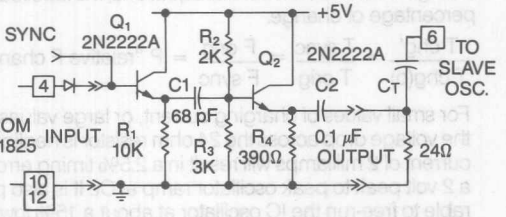


Figure 19. Sync Circuit Schematic

Operating Principles

A positive going signal is input to the base of transistor Q1 which operates as an emitter follower. The leading edge of the sync signal is coupled into the base of Q2 through capacitor C1, developing a voltage across R4 in phase with the sync input. This signal is driven through C2 to the slave timing capacitor and 24 ohm resistor network, forcing synchronization of the slave to the master. This high speed pulse amplifier circuit adds a minimum of delay (≈50 ns) between the master to slave timing relationship.

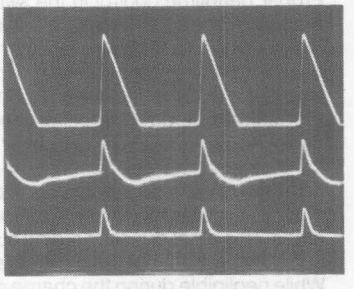


Figure 20. Sync Circuit Waveforms

This photo displays the waveforms of the sync circuit in operation at a clock frequency of 1 megahertz. The top trace is the circuit input, a 2.5 volt peak-to-peak clock output signal from the UC3825 PWM. Any of several other PWMs can be used as the source with similar results at lower frequencies. The center trace depicts the base to ground voltage waveform at transistor Q2, biased at 3 volts. The lower trace displays the output voltage across R4 while driving three slave modules, or about 8 ohms from the 5 volt reference.

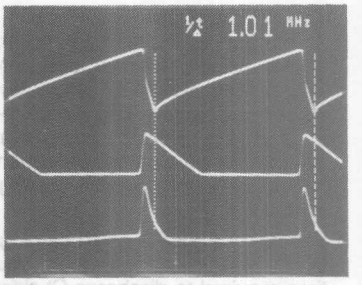


Figure 21. Circuit Timing Waveforms

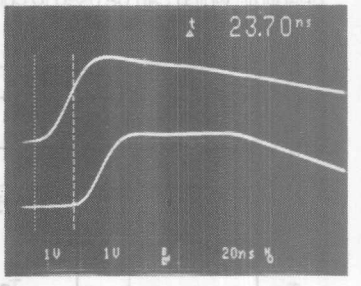


Figure 22. Sync Circuit Delay; Input to Output

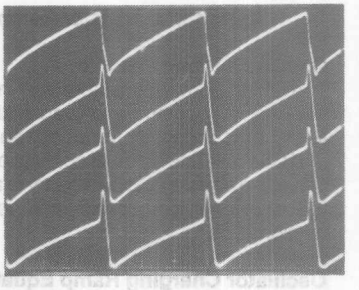


Figure 23. Oscillator Waveforms: Master and Slaves

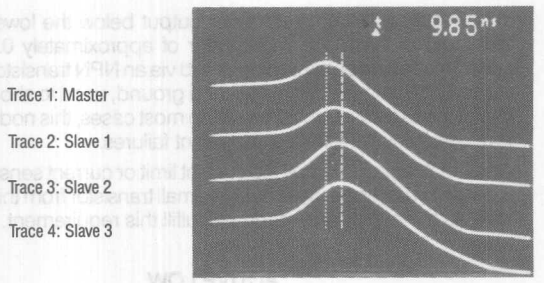


Figure 24. Typical Sync Delay at C_T: Master to Slaves

Synchronization ranges for the slaves were discussed in the previous text. The 1 volt sync pulse will accommodate most ranges in frequency due to manufacturers' tolerances. The following photo is included to display the outcome of trying to use the sync circuit on slaves with oscillator frequencies set beyond the sync circuit range. The upper trace is the master Ct waveform. The center trace is Ct of a slave free-running at approximately one half that of the master. The sync pulse alters the waveform, however does not bring it above the comparator's upper threshold to force synchronization. The lower trace shows a slave free running at approximately twice that of the master's oscillator. In this instance, the sync pulse forces synchronization at alternate cycles to the master.

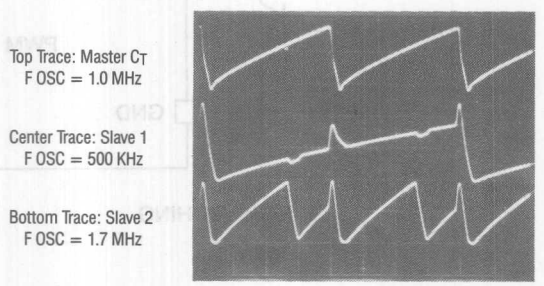


Figure 25. Nonsynchronous Operation

For voltage mode control, the free-running frequencies of the oscillator should be set as close to the master as tolerances will allow. One of the consequences of not doing so is the reduced amplitude of the Ct waveform, resulting in a lower dynamic range to compare against the error amplifier output. The top trace in the following photo shows that slave 1 has a much smaller ramp than slave 2, the lower trace. The amplitude should be made as large as possible to enhance circuit performance.

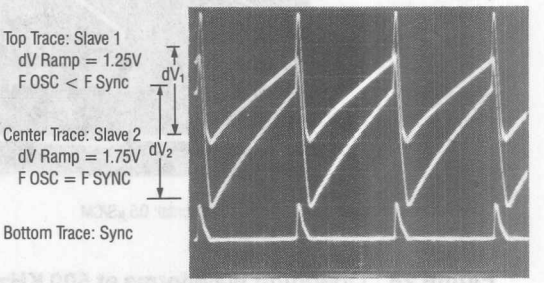


Figure 26. C_T Ramp Amplitude Waveforms

Sync Pulse Generation from the Oscillator Ct Waveform

Not every PWM IC is equipped with a sync output terminal from the oscillator. This is certainly the case with most low cost, mini-dip PWMs with a limited number of pin, like the UC1842/3/4/5. These ICs can provide a sync output with a minimum of external components.

Common to all PWMs of interest is the timing capacitor, Ct, used in the oscillator frequency generation. The universal sync circuit previously described triggers from the master deadtime, or Ct discharge time. A simple circuit will be described to detect this falling edge of the Ct waveform and generate the sync pulse required to the slave PWM(s).

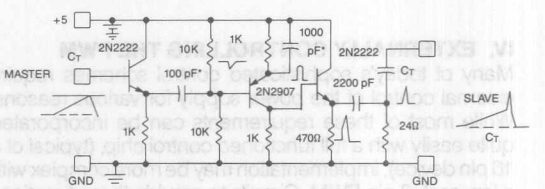


Figure 27. Sync Pulse Generator Circuit

Operating Principles

Transistor Q1 is an emitter follower to buffer the master oscillator circuit, and capacitively couples the falling edge of the timing waveform to the base of Q2. Since the rising edge of the waveform is typically ten or more times slower, it does not pass through to Q2, only the falling edge, or deadtime pulse is coupled. Transistor Q2 inverts this sync signal at its collector, which drives Q3, the power stage of this circuit. Similar to the universal sync circuit, the slave oscillator sections are driven from Q3's emitter. This circuit is useable to several hundred kilohertz with a minimum of delays between the master and slave synchronization relationship.

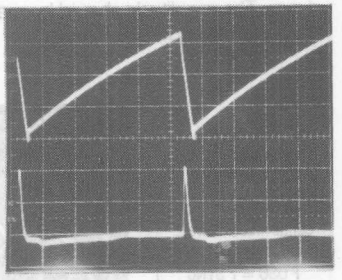


Figure 28. Operating Waveforms at 500 KHz

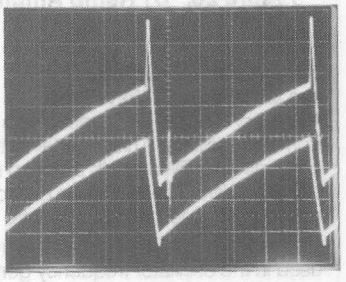


Figure 29. Master/Slave Sync Waveforms at C_T

IV. EXTERNALLY CONTROLLING THE PWM

Many of today's sophisticated control schemes require external control of the power supply for various reasons. While most of these requirements can be incorporated quite easily with a full functioned control chip, (typical of a 16 pin device), implementation may be more complex with a low cost, 8 pin PWM. Circuits to provide these functions with a minimum of external parts will be highlighted.

Shutdown

One of the most common requirements is to provide a complete shutdown of the power supply for certain situations like remote on/off, or sequencing. Typically, a TTL level input is used to disable the PWM outputs. Both voltage and current mode control ICs can perform this task by simply pulling the error amplifier output below the lower threshold of the PWM comparator of approximately 0.5 volts. This can be easily implemented via an NPN transistor placed between the E/A output and ground, used to short circuit the E/A output to zero volts. In most cases, this node is internally current limited to prevent failures.

Another scheme is to pull the current limit or current sense input above its upper threshold. A small transistor from this input to the reference voltage will fulfill this requirement.

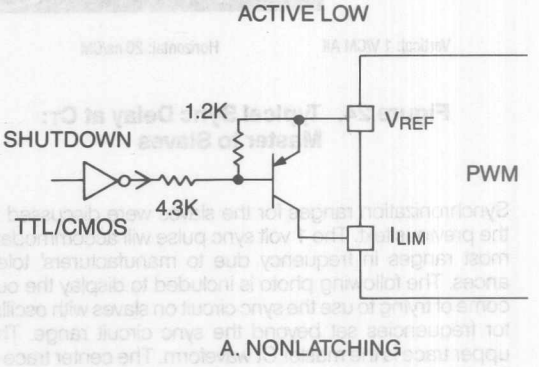
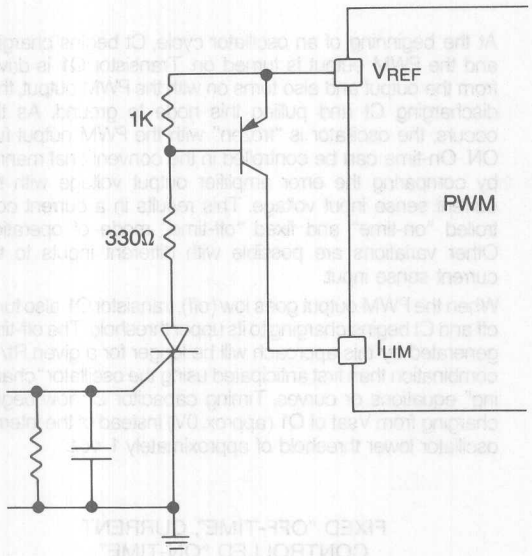


Figure 30. PWM Shutdown Circuits

Figure 31.

Latching Shutdown

For those applications which require a latching shutdown mechanism, an SCR can be used in conjunction with the above circuits, or in lieu of them. The SCR can also be placed from the PWM E/A output to ground, provided the PWM E/A minimum short circuit current is greater than the maximum holding current of the SCR, and the voltage drop at I(hold) is less than the lower PWM threshold.

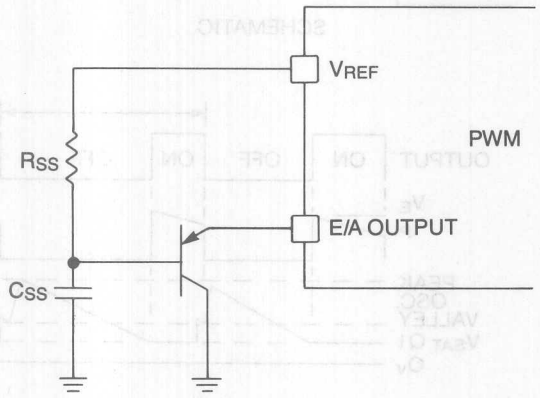


C. LATCHING

Figure 32.

Soft Start

Upon power-up, it is desirable to gradually widen the PWM pulse width starting at zero duty cycle. On PWMs without an internal soft start control, this can be implemented externally with three components. An R/C network is used to provide the time constant to control the I limit input or error amplifier output. A transistor is also used to isolate the components from the normal operation of either node. It also minimizes the loading effects on the R/C time constant by amplification through the transistors gain.



B. USING E/A

Figure 33.

Variable Frequency Operation

Certain topologies and control schemes require the use of a variable frequency oscillator in the controlling element. However, most PWMs are designed to operate in a fixed frequency mode of operation. A simple circuit is presented to disable the ICs internal oscillator between pulses, thus allowing variable frequency operation.

Internal at the ICs timing resistor (Rt) terminal is a current mirror. The current flowing through Rt is duplicated at the Ct terminal during the charge cycle, or "on" time. When the Rt terminal is raised to V ref (5 volts), the current mirror is turned off, and the oscillator is disabled. This is easily switched by a transistor and external logic as the control element, for example, a pulse generator. The PWM's timing resistor and capacitor should be selected for the maximum "ON" time and minimum "DEAD" time of the PWM output(s). The rate at which the PWM oscillator is disabled determines the frequency of the output(s).

The frequency can be varied in two distinct fashions depending on the desired control mode and trigger source. The "off" time of both outputs will occur on a pulse-by-pulse basis when the PWM outputs are OR'd to the trigger source. In this configuration either output initiates the "off" time, triggered by its falling edge. The PWM output A is activated, then both outputs A and B are low during the "off" time of the pulse generator. This is followed by output B being activated, then both outputs A and B low again during the next "off" time. This cycle repeats itself at a frequency determined by the pulse generator circuitry.

Another method is to introduce the "off" time after two (alternate A, then B) output pulses. Output A is activated, followed immediately by output B, then the desired "off" time. The pulse generator circuitry is triggered by the PWM's falling edge of output B. The specific control scheme utilized will depend on the power supply topology and control requirements.

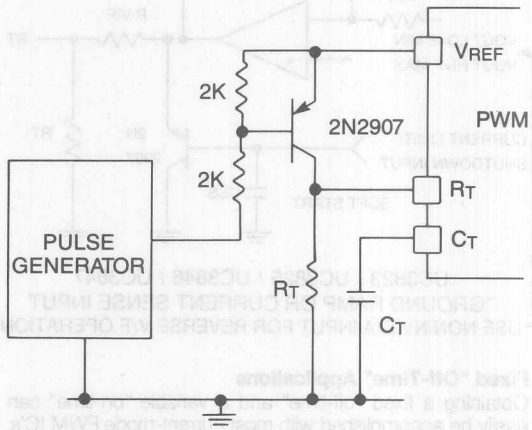
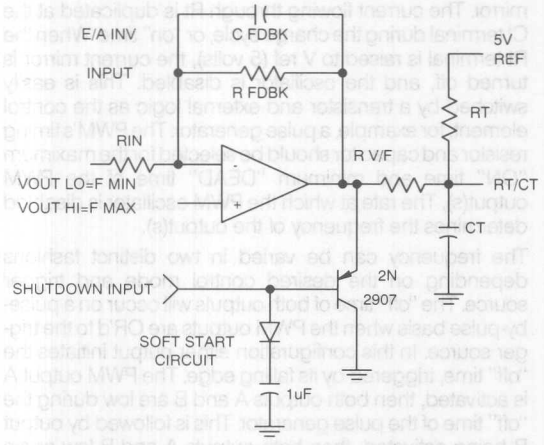


Figure 34. Oscillator Disable Circuit Variable Frequency Operation

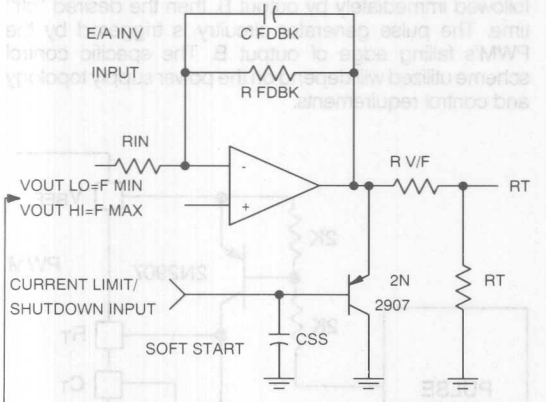
VOLTAGE CONTROLLED OSCILLATOR GENERAL CONFIGURATION

VARIABLE FREQUENCY OPERATION FIXED 50% DUTY CYCLE OSCILLATORS WITH SINGLE PIN PROGRAMMING



UC3851 / UC3844A / UC3845A
*GROUND RAMP OR CURRENT SENSE INPUT

OSCILLATORS WITH SEPARATE RT & CT PINS



UC3823 / UC3825 / UC3846 / UC3847
*GROUND RAMP OR CURRENT SENSE INPUT
USE NONINV E/A INPUT FOR REVERSE V/F OPERATION

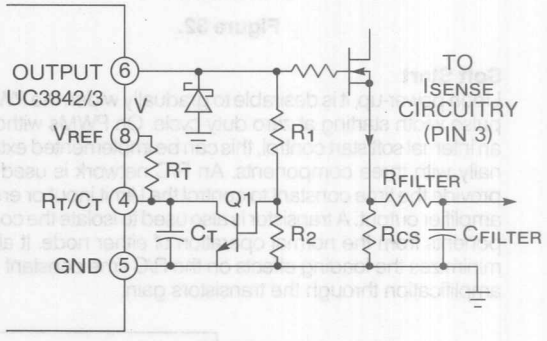
Fixed "Off-Time" Applications

Obtaining a fixed "off-time" and a variable "on-time" can easily be accomplished with most current-mode PWM IC's. In these applications, the Rt/Ct timing components are used to generate the "off-time" rather than the traditional "on-time." Implementation is shown schematically in Figure 3 along with the pertinent waveforms.

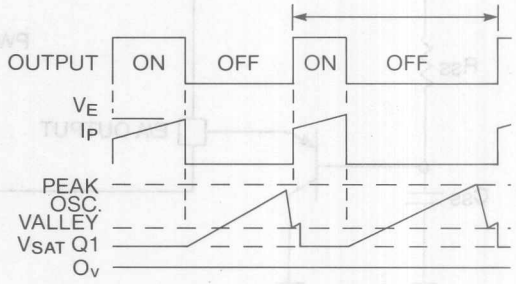
At the beginning of an oscillator cycle, Ct begins charging and the PWM output is turned on. Transistor Q1 is driven from the output and also turns on with the PWM output, thus discharging Ct and pulling this node to ground. As this occurs, the oscillator is "frozen" with the PWM output fully ON. On-time can be controlled in the conventional manner by comparing the error amplifier output voltage with the current sense input voltage. This results in a current controlled "on-time" and fixed "off-time" mode of operation. Other variations are possible with different inputs to the current sense input.

When the PWM output goes low (off), transistor Q1 also turns off and Ct begins charging to its upper threshold. The off-time generated by this approach will be longer for a given Rt/Ct combination than first anticipated using the oscillator "charging" equations or curves. Timing capacitor Ct now begins charging from Vsat of Q1 (approx. 0V) instead of the internal oscillator lower threshold of approximately 1 volt.

FIXED "OFF-TIME", CURRENT CONTROLLED "ON-TIME"



SCHEMATIC



WAVEFORMS

Figure 35.

Current Mode ICs Used in Voltage Mode

Most of today's current mode control ICs are second and third generation PWMs. Their features include high current output driver stages, reduced internal delays through their protection circuitry, and vast improvements in the reference voltage, oscillator and amplifier sections. In comparison to the first generation ICs (1524), numerous advantages can be obtained by incorporating a second or third generation IC (18XX) into an existing voltage mode design.

In duty cycle control (voltage mode), pulse width modulation is attained by comparing the error amplifier output to an artificial ramp. The oscillator timing capacitor Ct is used to generate a sawtooth waveform on both current or voltage mode ICs. To utilize a current mode chip in the voltage mode, this sawtooth waveform will be input to the current sense input for comparison to the error voltage at the PWM comparator. This sawtooth will be used to determine pulse width instead of the actual primary current in this method.

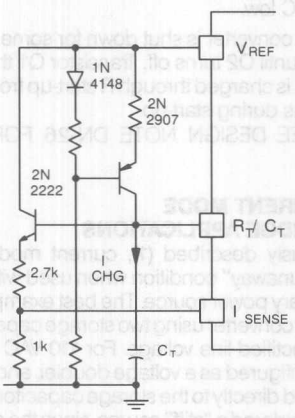


Figure 36. Current Mode PWM Used as a Voltage Mode PWM

Compensation of the loop is similar to that of voltage mode, however, subtle differences exist. Most of the earlier PWMs (15xx) incorporate a transconductance (current) type amplifier, and compensation is made from the E/A output to ground. Current mode PWMs use a low output resistance (voltage) amplifier and are compensated accordingly. For further reference on topologies and compensation, consult "Closing the Feedback Loop" listed in this appendix.

VI. FULL DUTY CYCLE (100%) APPLICATIONS

Many of the higher power (>500 watt) power supplies incorporate the use of a fan to provide cooling for the magnetic components and semiconductors. Other users locate fans throughout a computer mainframe, or other equipment to circulate the air and keep temperatures from skyrocketing. In either case, the power supply designer is usually responsible for providing the power and control.

The popularity of low voltage DC fans has increased throughout the industry due to the stringent agency safety requirements for high voltage sections of the overall circuit. In addition, it's much easier to satisfy dual AC inputs and frequency stipulations with a low cost DC fan, powered by a semi-regulated secondary output.

The most efficient way to regulate the fan motor speed (hence temperature) is with pulse width modulation. An error signal proportional to temperature can be used as the control voltage to the PWM error amplifier. While nearly full duty cycle can be easily attained, the circumstances may warrant full, or true 100% duty cycle.

This condition is highly undesirable in a switch-mode power supply, therefore most PWM IC designs have gone to great extent to prevent 100% duty cycle from occurring. There are simple ways to over-ride these safeguards, however. One method, presented below, "freezes" the oscillator and holds the PWM output in the ON, or high state when the circuit is activated. Feedback from the output is required to guarantee that the oscillator is stopped while the output is high. Without feedback, the oscillator can be nulled with the output in either state.

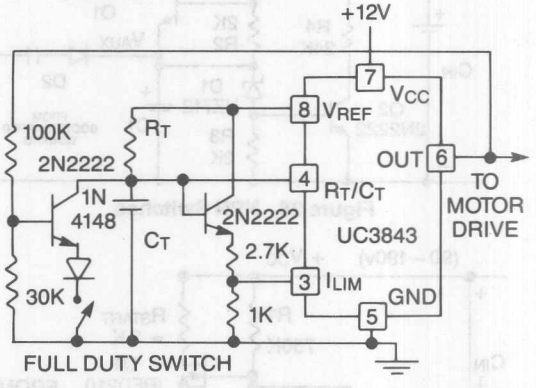


Figure 37. Full Duty Cycle Implementation

3

APPLICATION NOTES

VII. HIGH EFFICIENCY START-UP CIRCUITS FOR BOOTSTRAPPED POWER SUPPLIES

Many pulse width modulator I.C.s have been optimized for offline use by incorporating an under-voltage lockout circuit. Demanding only a milliamp or two until start-up, the auxiliary supply voltage (V aux) can be generated by a simple resistor/capacitor network from the high voltage dc rail (+V dc). Once start-up is reached, the auxiliary power is supplied by means of a "boostrap" winding on the main transformer.

While the start-up requirements are quite low, losses in the resistor to the high voltage DC can be significant in steady state operation. This is especially true for low power (<35 watt) applications and circuits with high voltage rails (400 volts DC, for example). Once the main converter is running, switching the start-up resistor out of circuit would increase efficiency substantially. Circuits have been developed to use either bipolar or MOSFET transistors as the switch to lower the start-up circuit power consumption, depending on the application. Selection can be based on optimizing circuit efficiency (MOSFET) or lowest component cost (bipolar). The overall improvement in power supply efficiency suggests this circuitry is a practical enhancement.

The high efficiency start-up circuit shown in figure 1 utilizes two NPN bipolar transistors to switch the start-up resistor in and out of circuit. It can be used in a variety of applications with minor modifications, and requires a minimum of components. Figure 2 displays a similar circuit utilizing N channel MOSFET devices to perform the switching.

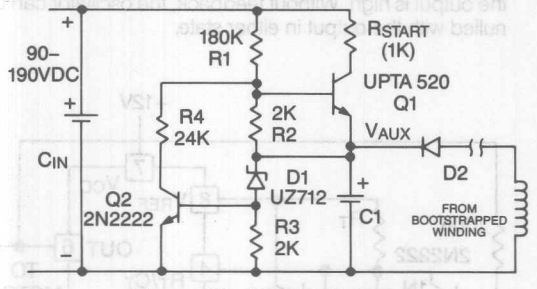


Figure 38. NPN Switches

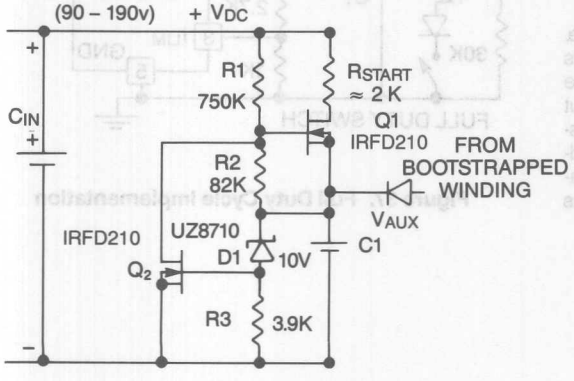


Figure 39.

Theory of Operation

Prior to applying the high voltage DC, capacitor C1 is discharged; switches Q1, Q2 and the main converter are off. As the input supply voltage (Vdc) rises, resistors R1 and R2 form a low current voltage divider. The voltage developed across R2 rises accordingly with +V dc until switch Q1 turns on, thus charging C1 thru R start-up from +V dc. This continues as the UV lockout threshold of the I.C. is reached and the main converter begins operation. Energy is delivered to C1 from the bootstrap winding in addition to that supplied through R start-up.

After several cycles, the auxiliary voltage rises with the main converters increasing pulse width, typical of a soft-start routine. Current flows through zener diode D1 and develops a voltage across the Q2's biasing resistor, R3. Transistor Q2 turns on when the auxiliary voltage reaches V zener plus Q2's turn on threshold. As this occurs, transistor Q1 is turned off, thus eliminating the start-up resistor from the circuit power losses. In most applications, the auxiliary voltage is optimized between 12 and 15 volts for driving the main power MOSFETs, while keeping power dissipation in the PWM IC low.

If the main converter is shut down for some reason, V aux will decay until Q2 turns off. Transistor Q1 then turns back on, and C1 is charged through R start-up from the high voltage DC, as during start-up.

NOTE: SEE DESIGN NOTE DN-26 FOR ADDITIONAL CIRCUITS.

VIII. CURRENT MODE HALF BRIDGE APPLICATIONS

As previously described (1), current mode control can cause a "runaway" condition when used with a "soft" centered primary power source. The best example of this is the half bridge converter using two storage capacitors in series from the rectified line voltage. For 110 VAC operation, the input is configured as a voltage doubler, and one of the AC inputs is tied directly to the storage capacitor's centerpoint. This is considered a "stiff" source, since the centerpoint will remain at one-half of the developed voltage between the upper and lower rail. However, during 220 VAC inputs, a bridge configuration is used for the input rectifiers, and the capacitors are placed in series with each other, across the bridge. Their centerpoint potential will vary when different amounts of charge are removed from the capacitors. This is generally caused by uneven storage times in the switching transistors Q1 and Q2.

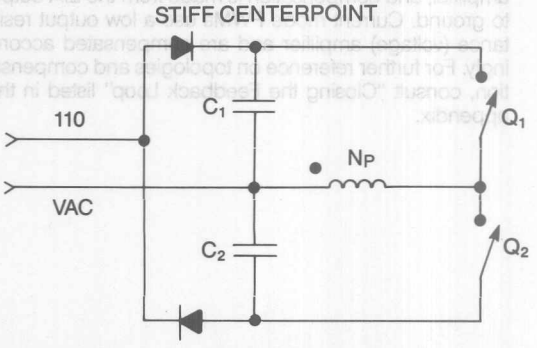


Figure 40.

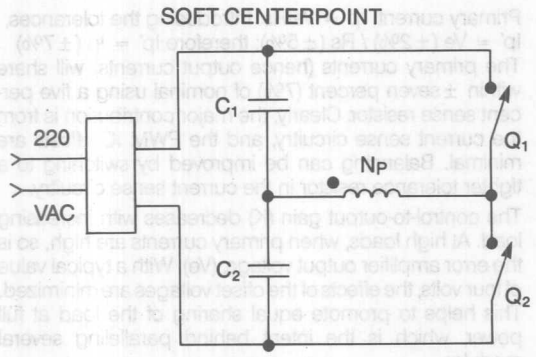


Figure 41.

The centerpoint voltage can be maintained at one-half +Vdc by the use of a balancing technique. In normal operation, transistor Q1 turns on, and the transformer primary is placed across one of the high voltage capacitors, C1 for example. On alternate cycles the transformer primary is across the other cap, C2. An additional balancing winding, equal in number in turns to the primary, is wound on the transformer. It is connected also to the capacitor centerpoint at one end and thru diodes to each supply rail at the other end. The phasing is such that it is in series with the primary winding through the ON time of either transistor Q1 or Q2.

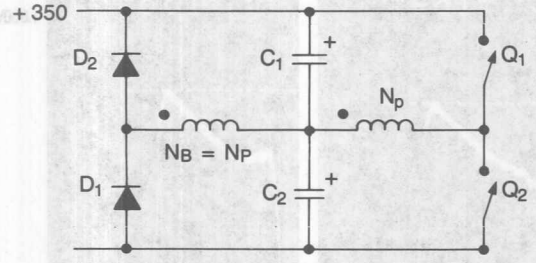


Figure 42. Schematic – Balancing Winding

In this configuration, the center point of the high voltage caps is forced to one-half of the input DC voltage by nature of the two series windings of identical turns. Should the midpoint begin to drift, current flows thru the balancing winding to compensate.

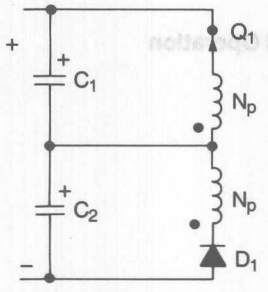


Figure 43. Transistor Q1 On

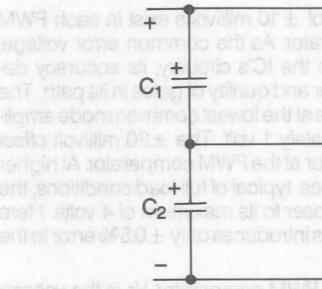


Figure 44. Transistor Q2 On

In most high frequency MOSFET designs, the FET mismatches are small, and the average current in the balancing winding is less than 50 milliamps. A small diameter wire can be wound next to the larger sized primary for the balancing winding with good results.

IX. PARALLELING CURRENT MODE MODULES

One of the numerous advantages of current mode control is the ability to easily parallel several power supplies for increased output power. This discussion is intended as a primer course to explore the basic implementation scheme and design considerations of paralleling the power modules. Redundant operation, failure modes and their considerations are not included in this text.

The prerequisites for parallel operation are few in number, but important to insure proper operation. First, each power supply module must be current mode controlled, and capable of supplying its share of the total output power. All modules must be synchronized together, and one unit can be designated as the master for the sake of simplicity. All remaining units will be configured as slaves.

The master will perform one function in addition to generating the operating frequency. It provides a common error voltage (Ve) to all modules as the input to the PWM comparator. This voltage is compared to the individual module's primary current at its PWM comparator. The slaves are utilized with their error amplifier configured in unity gain. Assume there are identical primary current sense resistors in each module, and no internal offsets in the ICs amplifiers or other circuit components. In this case, the output voltages and currents of each module would be identical, and the load would be shared equally among the modules.

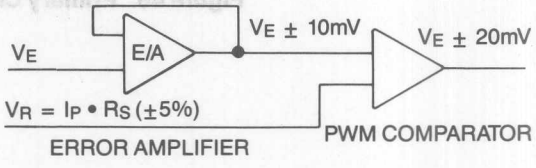


Figure 45. PWM Diagram

In reality, small offets of ±10 millivolts exist in each PWM amplifier and comparator. As the common error voltage, (Ve) traverses through the IC's circuitry, its accuracy decreases by the number and quality of gates in its path. The maximum error occurs at the lowest common mode amplifier voltage, approximately 1 volt. The ±20 millivolt offset represents a ±2% error at the PWM comparator. At higher common mode voltages, typical of full load conditions, the error voltage (Ve) is closer to its maximum of 4 volts. Here the same ±20 millivolts introduces only ±0.5% error to the signal.

The other input to the PWM comparator, Vr, is the voltage developed by the primary current flowing through the current sense resistor(s). In many applications, a 5% tolerance resistor is utilized resulting in a ±5% error at the PWM comparator's "current sense" or ramp input.

Pulse width is determined by comparing the error voltage (Ve) with the current sense voltage, (Vr). When equal, the primary current is therefore the error voltage divided by the current sense resistance; Ip = Ve/Rs. Output current is related to the primary current by the turns ratio (N) of the transformer. Sharing of the load, or total output current is directly proportional to the sharing of the total primary current. The previous equations and values can be used to determine the percentage of sharing between modules.

Primary current, Ip = Ve/Rs. Introducing the tolerances, Ip' = Ve (±2%) / Rs (±5%); therefore Ip' = Ip (±7%) The primary currents (hence output currents) will share within ±seven percent (7%) of nominal using a five percent sense resistor. Clearly, the major contribution is from the current sense circuitry, and the PWM IC offsets are minimal. Balancing can be improved by switching to a tighter tolerance resistor in the current sense circuitry.

The control-to-output gain (K) decreases with increasing load. At high loads, when primary currents are high, so is the error amplifier output voltage, (Ve). With a typical value of four volts, the effects of the offset voltages are minimized. This helps to promote equal sharing of the load at full power, which is the intent behind paralleling several modules.

For demonstration purposes, four current mode push-pull power supplies were run in parallel at full power. The primary current of each was measured (lower traces) and compared to a precision 1 volt reference (upper trace). The voltage differential between traces is displayed in the upper right hand corner of the photos. Using closely matched sense resistors, the peak primary currents varied from a low of 2.230A to 2.299 amps. Calculating a mean value of 2.270 amps, the individual primary currents shared within two percent, indicative of the sense resistor tolerances.

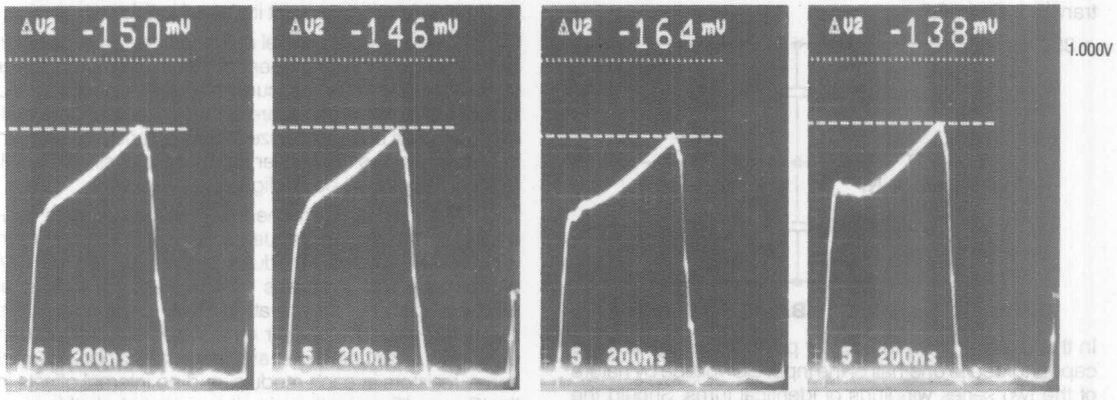
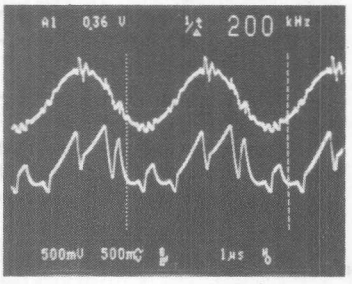


Figure 46. Primary Currents – Parallel Operation

Other factors contributing to mismatch of output power are the individual power supply diode voltage drops. The output choke inductance reflects back to the primary current sense, and any tolerances associated with it will alter the primary current slope, hence current. In the control section, the peak-to-peak voltage swing at the timing capacitor Ct effects the amount of slope compensation introduced, along with the tolerance of the summing resistor. These must all be accounted for to calculate the actual worst case current sharing capability of the circuit.



Top Trace:
V_E: Error Voltage with Noise

Lower Trace:
V_R: Primary Current

Figure 47. Noise Modulating V_E

Proper layout of all interconnecting wires is required to insure optimum performance. Shielded coax cable is recommended for distributing the error voltage among the modules. Any noise on this line will demonstrate its impact at the PWM comparator, resulting in poor load sharing, or jitter.

Cables should be of equal length, originating at the master and routed away from any noise sources, like the high voltage switching section. All input and output power leads should be exactly the same length and wire gauge, connected together at ONE single point. Leads should be treated as resistors in series with the load, and deviations in length will result in different currents delivered from each module.

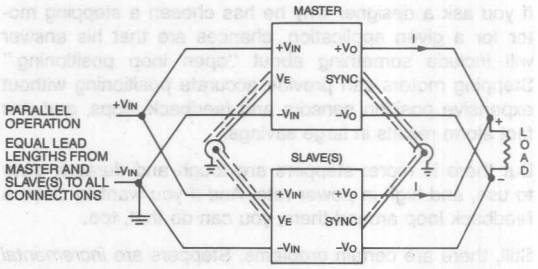


Figure 48.

UNITRODE
APPLICATION NOTE

A HIGH PRECISION PWM TRANSCONDUCTANCE AMPLIFIER FOR MICROSTEPPING USING UNITRODE'S UC3637

INTRODUCTION

If you ask a designer why he has chosen a stepping motor for a given application, chances are that his answer will include something about "open loop positioning." Stepping motors can provide accurate positioning without expensive position sensors and feedback loops, and this fact alone results in large savings.

But there is more: steppers are tough and durable, easy to use, and high in power rate. And if you want to close a feedback loop around them, you can do that, too.

Still, there are certain problems. Steppers are *incremental motion* machines, and as such they tend to be noisy and are prone to behave erratically under certain conditions; for example, when the stepping rate is such as to excite a mechnical or electro-mechanical resonant mode. Furthermore, although the angular increments may be small—especially when half-stepping is used—the positioning resolution is restricted to a finite number of discrete points.

Therefore, this question arises: "Is there a method of driving stepping motors such that the resulting movement is smooth and quiet—that is, essentially continuous, as opposed to incremental? And would this result in improved positioning resolution?" We will try to answer these questions here.

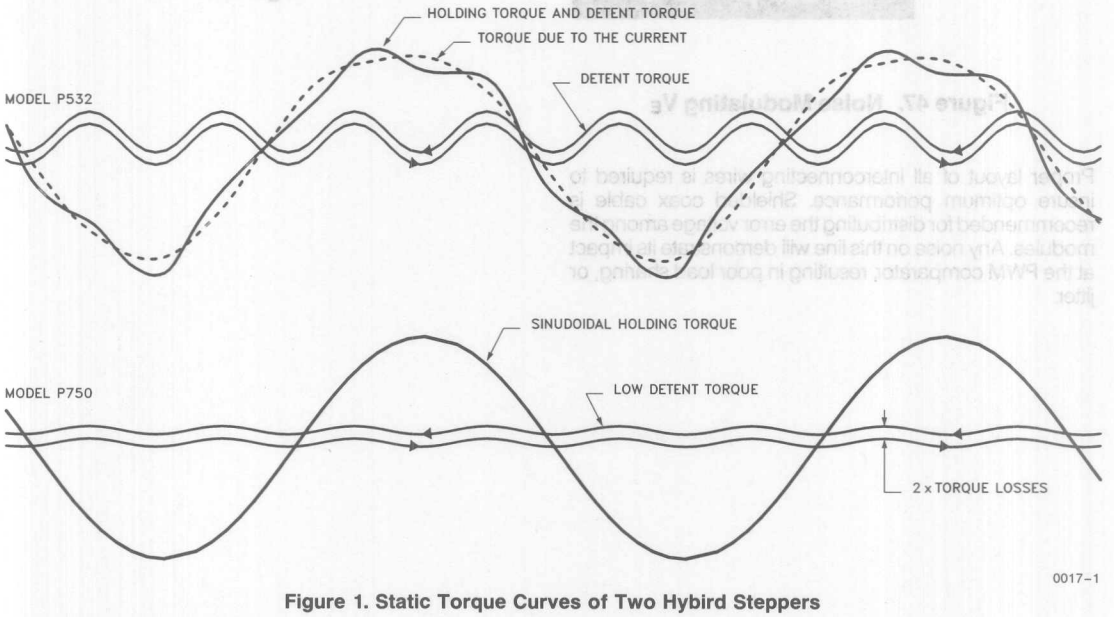


Figure 1. Static Torque Curves of Two Hybird Steppers

STATIC TORQUE CURVES

The curves in Figure 1 illustrate how a stepping motor torque behaves as a function of rotor angle. The detent torque component is a consequence of the magnetic field produced by the rotor magnet (or magnets), and is present with or without phase currents applied. It can be seen that this component contributes a fourth harmonic distortion to the static torque curves. The energized torque curves, in general, have additional harmonic components, mostly the third and fifth. Note that the two motors depicted in Figure 1 have very different characteristics in this respect. The distortion observed in the static torque characteristic is of no great consequence in the more usual applications of stepping motors, using either full step or half step sequences. It is when we start thinking about increasing the positioning resolution of these motors by some method of apportioning currents between the two phases, that we begin to be concerned about the effects of harmonic distortion. Even small amounts of added har-

monics can have a very noticeable effect on the waveshape, as shown in Figure 2.

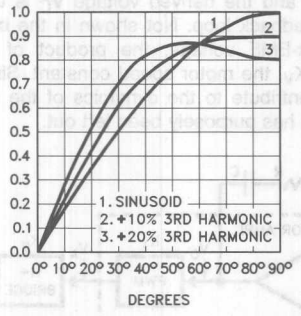


Figure 2. Effect of 10% and 20% Harmonic Content

Figure 3 shows the relationship between sine and cosine waveforms, and what it tells us is that if we can get a motor with a sinusoidal static torque characteristic—i.e., with no harmonic components—and drive phase A with a sine current function and phase B with a cosine current function, we would have smooth shaft rotation and accurate positioning at any angle.

Stepping motors having static torque curves with very low harmonic distortion are commercially available today. But most low-priced, mass produced hybrid steppers exhibit torque curves with enough harmonic components to require careful consideration in any attempt to improve resolution by what is known as *microstepping*. (The name *microstepping* originates from the fact that the required current waveforms are generated by a digital process that aproximates those waveforms incrementally. With thirty-two or sixty-four increments for an electical angle of $\pi/2$ radians, the resulting waveforms are hardly distinguishable from true sine or cosine signals.)

If the nonsinusoidal static characteristic of a given motor is known, it is possible to generate appropriate waveshapes for the phase currents so that the resulting torque curve becomes free of distortion, as required. Note that this involves no additional complexities, since it is just as easy—or difficult—to synthesize one waveform as another. Consequently, one can, in principle, linearize any motor for increased resolution and smoothness through microstepping.

Still, it should be noted that the best efficiency is obtained when the phase current waveshapes are undistorted, because of all suitable waveforms, the sine wave has the lowest form-factor.

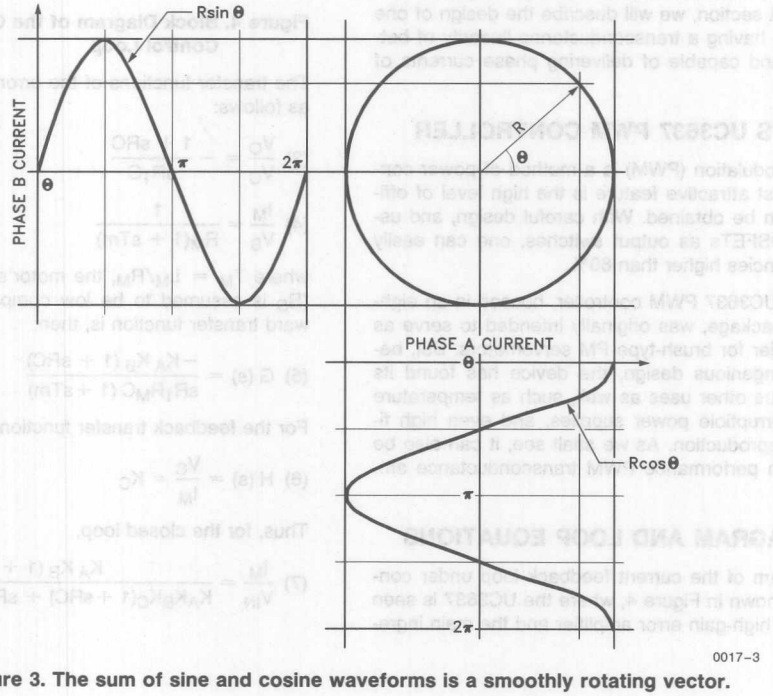


Figure 3. The sum of sine and cosine waveforms is a smoothly rotating vector.

The form-factor of a waveform is the ratio if its rms to average values. For a sine wave, this ratio is:

$$(1)\ ff_S = \frac{0.707}{0.637} = 1.111$$

Some manufacturers have used triangular waveforms—largely because they can be implemented with great simplicity—and it is interesting to note that for such a waveform, the average value is 0.5 V_{PK}, while the rms is 0.577 V_{PK}. Thus the form factor is:

$$(2)\ ff_T = \frac{0.577}{0.5} = 1.155$$

As a consequence, for the same peak power applied to the motor, the rms power of a triangular waveform is 18% less than that of a sine wave, whereas the average current is 21% less. It follows that microstepping with a triangular waveform does not use the full capabilities of the motor.

The same result is obtained with other-waveforms, as long as the peak power is limited, as it must be.

But regardless of all this, the fact remains that whether our motor has a sinusoidal torque curve or a very distorted one, the thing that will be inevitably required will be two amplifiers capable of converting the synthesized waveform into phase currents *at the required power levels*. In the next section, we will describe the design of one such amplifier, having a transconductance linearity of better than 1% and capable of delivering phase currents of up to ±6A.

UNITRODE'S UC3637 PWM CONTROLLER

Pulse width modulation (PWM) is a method of power control whose most attractive feature is the high level of efficiency that can be obtained. With careful design, and using power MOSFETs as output switches, one can easily achieve efficiencies higher than 80%.

The Unitrode UC3637 PWM controller, housed in an eighteen-pin DIL package, was originally intended to serve as a PWM amplifier for brush-type PM servomotors. But, because of its ingenious design, the device has found its way into various other uses as well, such as temperature control, uninterruptible power supplies, and even high fidelity sound reproduction. As we shall see, it can also be used in a high performance PWM transconductance amplifier.

BLOCK DIAGRAM AND LOOP EQUATIONS

A block diagram of the current feedback loop under consideration is shown in Figure 4, where the UC3637 is seen to contain the high-gain error amplifier and the main ingredients of the PWM amplifier. Since we are looking for an output of 6A, an H-bridge power stage must be added. The motor current I_M is sensed by means of a low value resistor R_S, and the derived voltage V_C is used to complete the feedback loop. Not shown in the block diagram is the back-EMF voltage, the product of motor shaft speed and K_V, the motor speed constant. Since this term does not contribute to the dynamics of the current feedback loop, it has purposely been left out.

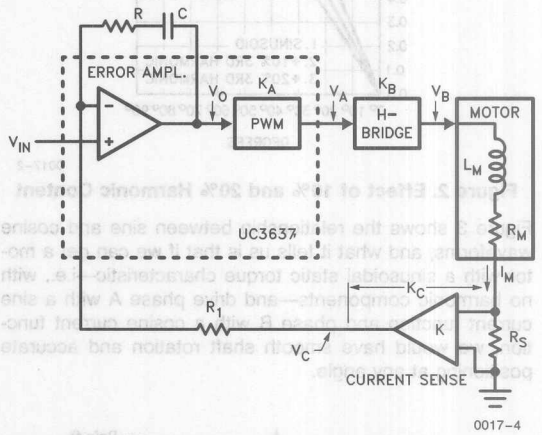


Figure 4. Block Diagram of the Complete Current-Control Loop

The transfer functions of the error amplifier and motor are as follows:

$$(3)\ \frac{V_O}{V_C} = -\frac{1 + sRC}{sR_1C}$$

$$(4)\ \frac{I_M}{V_B} = \frac{1}{R_M(1 + sTm)}$$

where $T_M = L_M/R_M$, the motor's electrical time-constant (R_S is assumed to be low compared with R_M). The forward transfer function is, then:

$$(5)\ G(s) = \frac{-K_A K_B (1 + sRC)}{sR_1R_MC (1 + sTm)}$$

For the feedback transfer functions, we have simply:

$$(6)\ H(s) = \frac{V_C}{I_M} = K_C$$

Thus, for the closed loop,

$$(7)\ \frac{I_M}{V_{IN}} = \frac{K_A K_B (1 + sRC)}{K_A K_B K_C (1 + sRC) + sR_1R_MC (1 + sTm)}$$

If we make the time-constant RC equal to the motor's time-constant T_M, this becomes:

$$(8)\ \frac{I_M}{V_{IN}} = \frac{K_A K_B}{K_A K_B K_C + sR_1 R_M C}$$

$$(9)\ \frac{I_M}{V_{IN}} = \frac{1}{K_C(1 + sT_1)}$$

where,

$$(10)\ T_1 = \frac{R_1 R_M C}{K_A K_B K_C} = \frac{R_1 L_M}{K_A K_B K_C R}$$

By making $RC = T_M$, we have eliminated one of the transfer function poles. The resulting closed-loop response, described by (7) has a gain of $1/K_C$ from $\omega = 0$ to $\omega = 1/T_1$, and drops at -6 bd/octave thereafter.

DESIGNING THE HARDWARE

In designing circuits intended to handle power, it is customary to start with the output stage. This is surely due to the fact that the power stage is more demanding of the designer's attention and care, whereas the low level circuits are far more adaptable to the requirements of the chosen output configuration.

In the present case, power MOSFETs were chosen for the H-bridge because of their low losses, and because of their compatibility with the UC3637 outputs. Each totem-pole leg of the bridge is made up of one N-channel and one P-channel device. Such a pair can be driven in many different ways, of which several were considered for this particular design. The method that was finally chosen, shown in Figure 5, requires a few comments.

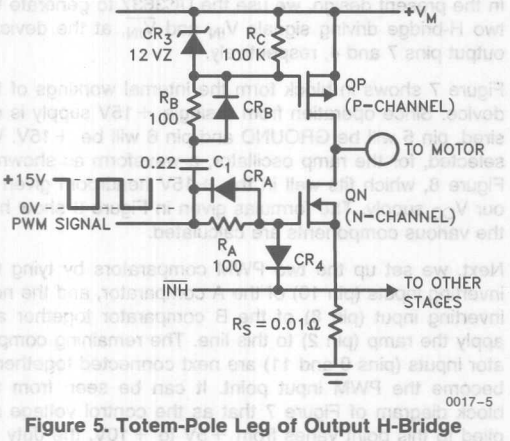


Figure 5. Totem-Pole Leg of Output H-Bridge

The first thing to notice is that the upper MOSFET, transistor QP, has its gate driven through a capacitor, C_1. This is not always practical of course, but in the case of a chopper drive combined with a stepping motor, it turns out that a driving signal is always present. At stand-still and at low speeds, it is the chopping rate that appears; at higher speeds, it is the stepping rate itself, or both. The driver is never required to deliver continuous DC (unchopped) to the motor winding, as it would to the armature of a brush-type DC motor at full speed. Consequently, QP never needs to be held in the ON state for more than a few microseconds, and for this the time constant of C1 R4 is adequate. Also, resistor R_A in parallel with CR_1, together with the gate capacitance of QN, cause this transistor to turn off faster than it turns ON. Since the same thing is done for QP, the problem of cross-conduction is neatly taken care of. The Zener diode CR3 serves as a clamp for the QP gate voltage. Finally, an inhibiting line, INH, is provided as a protection for QP and QN during the power turn-on time, when the $+V_M$ voltage is rising and C1 must be charged. An auxiliary circuit senses a positive dV_M/dt and holds the INH line low, thus keeping QN OFF during this time.

An important point in favor of this arrangement is that the gate-drive circuit losses are independent of V_M and so this voltage can be set anywhere within the Vds rating of the power MOSFETs.

We can now consider the H-bridge with its motor winding load, as shown in Figure 6. The bridge is shown schematically with its driving circuits, but the action is still as shown in Figure 5. For example, when V_{IN} is high, switch S1 is OFF and S3 is ON, and so forth. Furthermore, the opposite side of the bridge is driven by the complementary signal $\overline{V_{IN}}$. With V_{IN} low, S1 and S4 will be conducting, and the load current I_M will increase in the positive direction (indicated by the $+I_M$ arrow). Similarly, when V_{IN} is high, both S2 and S3 conduct, causing I_M to increase in the negative direction. Remember that the load is inductive, and that inductance is an energy storing element. Therefore, if we have some positive I_M, due to S1 and S4 being closed, and we switch to S2 and S3 closed, the previous value of I_M will continue to flow "uphill," so to speak, while decreasing. At the time of switching, this current ceases to flow down through sense resistor R_{S4} to ground and starts flowing up through R_{S3} and back to the supply.

Switches S1 through S4 are able to conduct in either direction when in the ON state—a very neat feature of power MOSFETs. Furthermore, their intrinsic diode protects the devices from reverse voltage pulses during the switching no-overlap transition. Since we wish to control this current very closely in both magnitude and direction, it is

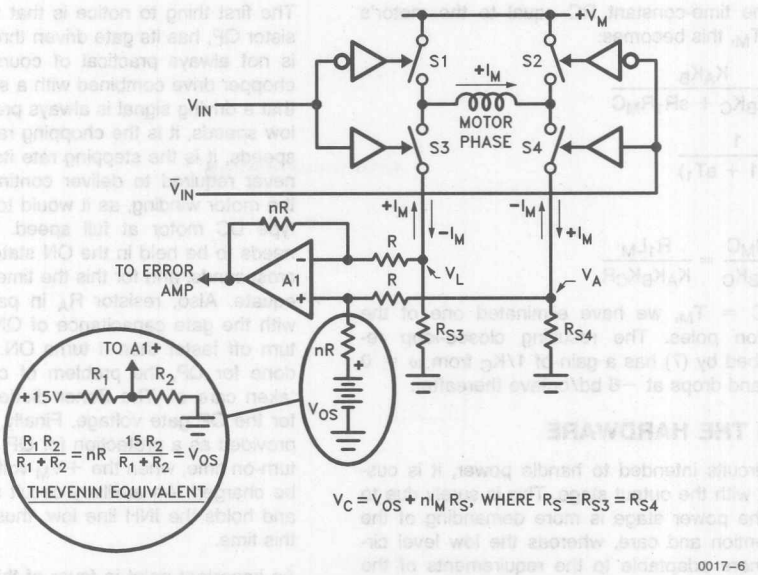


Figure 6. H-Bridge Configuration with Bidirectional Current Sensing

now necessary to generate a voltage V_C that gives an accurate indication of the current I_M over the full range from maximum positive to maximum negative. This is done by the circuit section of Figure 6 which includes the op-amp A1.

In that circuit, the voltage V_{OS} is meant to offset the output V_C of A1 to some chosen value that will correspond to $I_M = 0$. The value of V_C can be written as:

$$(11)\ V_C = V_{CS} + nI_MR_S$$

This offset is necessary when the design requires a single polarity supply, as in our case. When two supply polarities are available for the control circuit, one can simply make $V_{OS} = 0$. For the single supply case, the nR and V_{OS} combination is implemented by a simple resistor divider from $\pm V_{CC}$ to ground (a Thevenin equivalent) of the required impedance and open voltage.

To keep the circuit losses to a minimum, we should use low values for the sense resistors R_{S3} and R_{S4}. Yet, they need to be accurate and temperature-stable. In our case, having decided on a V_C scale of 0.5V per motor ampere, we have selected $R_S = 0.1\Omega$ and a current sense amplifier gain $n = 5$. We have also set $V_{OS} = V_{CC}/2 = 7.5V$, so that we will have $V_C = 7.5 + 0.5\ I_M$. This means that as the current I_M varies from $+6A$ to $-6A$, the analog voltage V_C will vary from $+10.5V$ to $+4.5V$. At $I_M = 0$, V_C will be equal to 7.5V.

SETTING UP THE PWM CONTROLLER

Having designed the power output stage (H-bridge) and the current-sense circuit, we can proceed to the PWM controller (UC3637) and its external components. The device itself has been described in great detail in its data sheet and in an application note (Publication U-102, available from Unitrode Integrated Circuits Corporation).

In the present design, we use the UC3637 to generate the two H-bridge driving signals V_{IN} and $\overline{V_{IN}}$, at the device's output pins 7 and 4, respectively.

Figure 7 shows in block form the internal workings of the device. Since operation from a single $+15V$ supply is desired, pin 5 will be GROUND and pin 6 will be $+15V$. We selected, for the ramp oscillator, a waveform as shown in Figure 8, which fits well in the $+15V$ headroom given by our V_{CC} supply. The formulas given in Figure 8 show how the various components are calculated.

Next, we set up the two PWM comparators by tying the inverting inputs (pin 10) of the A comparator, and the noninverting input (pin 8) of the B comparator together and apply the ramp (pin 2) to this line. The remaining comparator inputs (pins 9 and 11) are next connected together to become the PWM input point. It can be seen from the block diagram of Figure 7 that as the control voltage applied to this point varies from $+5V$ to $+10V$, the duty cycle of the output at pins 4 and 7 also varies. V_4 and V_7 are complementary signals; and the voltage swing of each of these signals is from a low value between 0V and $+2V$, and a high value between ($V_{CC} - 2V$) and V_{CC}.

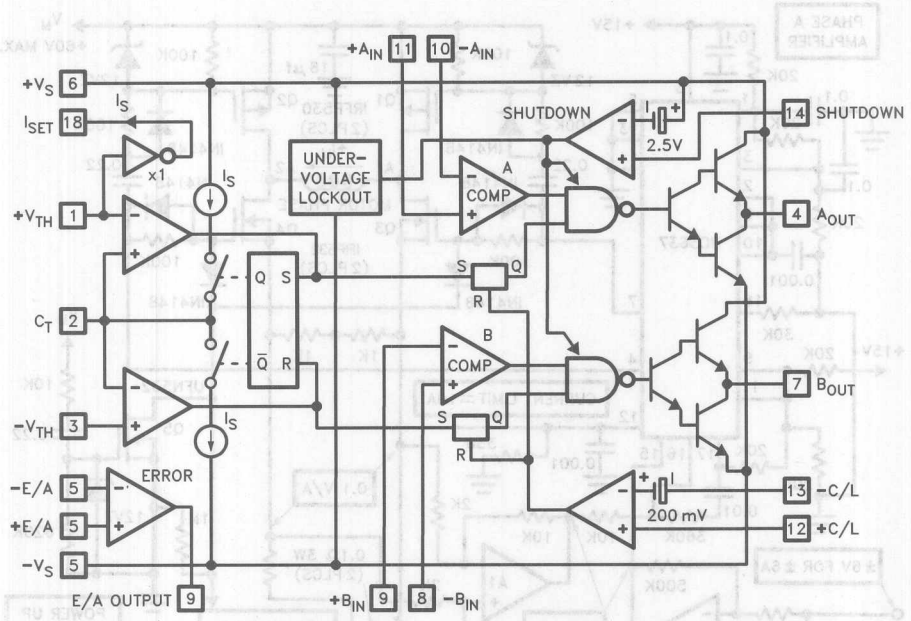
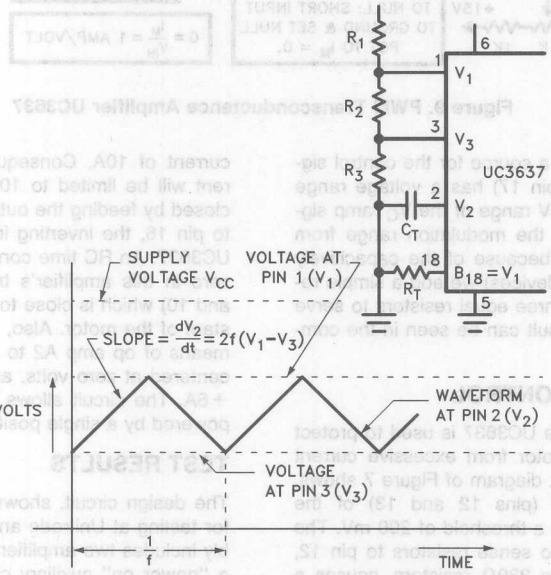


Figure 7. Block Diagram of the UC3637. The two outputs can drive power MOSFETs directly.



f = ramp frequency

$I_T = \frac{V_{18}}{R_T} = \frac{V_1}{R_T}$ (should be about 0.5 mA)

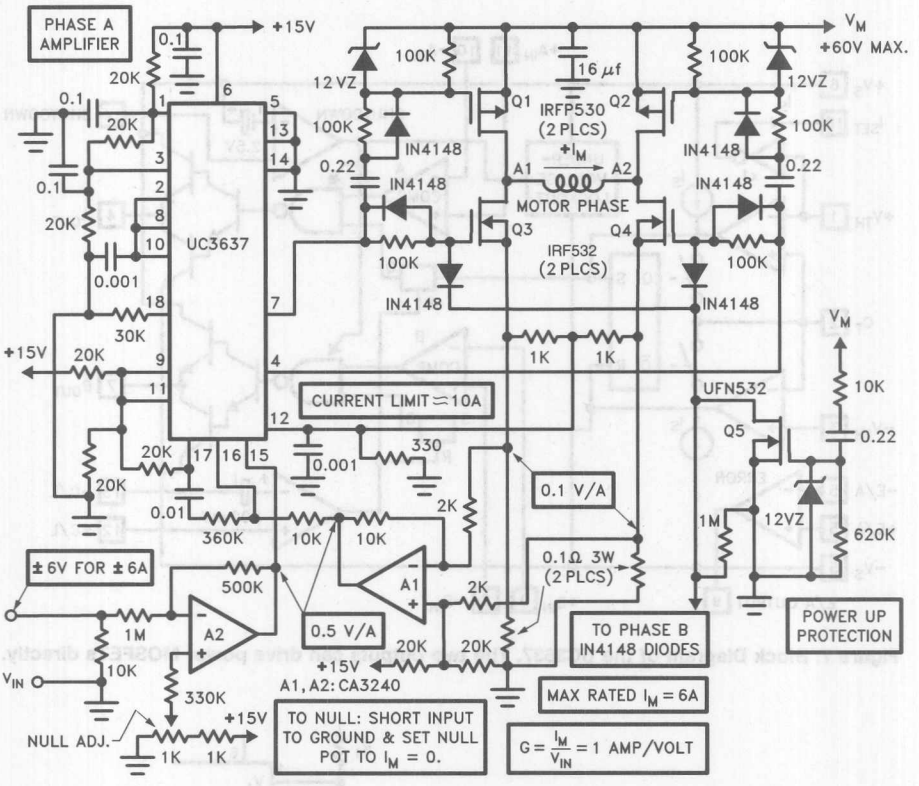
then, $R_T = 2000\ V_1\ (\Omega)$

$C_T = \frac{250 \times 10^{-6}}{f(V_1 - V_3)}(fd)$

Figure 8. Setting up the ramp oscillator requires only five external components.

3

APPLICATION NOTES



0017-9

Figure 9. PWM Transconductance Amplifier UC3637

The error amplifier is used as a source for the control signal. But because its output (pin 17) has a voltage range greater than the +5V to +10V range of the V_C ramp signal, and we want to prevent the modulation range from ever reaching 0% or 100% (because of the capacitively coupled P-channel MOSFET devices) we add a simple resistive network consisting of three equal resistors to serve as an attenuator. The final result can be seen in the complete schematic of Figure 9.

CURRENT LIMIT AND CONTROL

The current limit feature of the UC3637 is used to protect the output transistors and motor from excessive current (6A in this case). As the block diagram of Figure 7 shows, the current limit comparator (pins 12 and 13) of the UC3637 is internally biased to a threshold of 200 mV. The network that connects the two sense resistors to pin 12, consisting of two 1K and one 330Ω resistors, causes a voltage of 200 mV to appear at pin 12 when the voltage at either sense resistor is about 1V, corresponding to a current of 10A. Consequently, the maximum output current will be limited to 10A. The current feedback loop is closed by feeding the output of the current sense amplifier to pin 16, the inverting input of the error amplifier of the UC3637. An RC time constant of 3.6 msec is used for the zero in this amplifier's transfer function (equations 8, 9, and 10) which is close to the effective electrical time constant of the motor. Also, a level-shift circuit is provided by means of op amp A2 to permit the use of a control input centered at zero volts, and a control range from −6A to +6A. The circuit allows this even though the op amp is powered by a single positive supply.

TEST RESULTS

The design circuit, shown in Figure 9, was breadboarded for testing at Unitrode and also at Portescap. The assembly includes two amplifiers, one for each motor phase and a "power on" auxiliary circuit for protection of the power MOSFETs. The output devices are equipped with small sheet metal heat sinks.

The circuit draws about 65 mA from the +15V supply. The power output section operates with a supply ranging from +20V to +60V, with no damage occurring if this voltage is lower than +20V.

The circuit performed very well, with excellent linearity and phase matching. The various plots taken, showing output current versus input voltage, are quite straight, and the transconductance is accurate to within 1%. Furthermore, the PWM frequency was subsequently increased to slightly above 100 KHz (by reducing C_T) and the performance re-checked. The result was a marked increase in motor efficiency, due to reduced current ripple, with all other results remaining excellent.

CONCLUSION

Microstepping is a technique of considerable interest in the design of many products, particularly those in which the lower cost of open-loop positioning is an essential parameter. A motor such as Portescap's Model P-750, with its accurately sinusoidal torque curve, becomes even more attractive once its microstepping driver is shown to be fairly simple and inexpensive. The end result is not only precise open loop positioning, but quiet operation, freedom from resonance problems, and excellent electrical efficiency. Incidentally, the motor is available with two quadrature speed sensing coils that can be used for speed and position control, if desired.

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APPLICATION NOTE

DESIGN NOTES ON PRECISION PHASE LOCKED SPEED CONTROL FOR DC MOTORS

ABSTRACT

There are a number of high volume applications for DC motors that require precision control of the motor's speed. Phase locked loop techniques are well suited to provide this control by phase locking the motor to a stable and accurate reference frequency. In this paper, the small signal characteristics, and several large signal effects, of these loops are considered. Models are given for the loop with design equations for determining loop bandwidth and stability. Both voltage and current motor drive schemes are addressed. The design of a loop for a three phase brushless motor is presented.

PHASE LOCKING GIVES PRECISION SPEED CONTROL

The precise control of motor speed is a critical function in today's disc drives. Other data storage equipment, including 9 track tape drives, precision recording equipment, and optical disc systems also require motor speed control. As the storage density requirements increase for these media, so does the precision required in controlling the speed of the media past the read/write mechanism. One of the best methods for achieving speed control of a motor is to employ a phase locked loop.

With a phase locked loop, a motor's speed is controlled by forcing it to track a reference frequency. The reference input to the phase locked loop can be derived from a precision crystal controlled source, or any frequency source with the required stability and accuracy. A block diagram of the phase locked loop is shown in Figure 1.

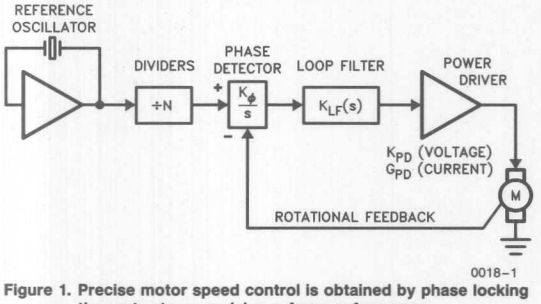


Figure 1. Precise motor speed control is obtained by phase locking the motor to a precision reference frequency.

In Figure 1, a precision crystal oscillator's frequency is digitally divided down to provide a fixed reference frequency. Alternatively, the motor could be forced to track a variable frequency source with zero frequency error. The motor speed is sensed by either a separate speed winding or, particularly in the case of the DC brushless motor, a Hall effect device. The two signals, motor speed and reference frequency, are inputs to a phase detector. The detector output is a voltage signal that is a function of the phase error between the two inputs. The transfer function of the phase detector, K_ϕ, is expressed in volts/radian. A 1/s multiplier accounts for the conversion of frequency to phase, since phase is the time integral of frequency.

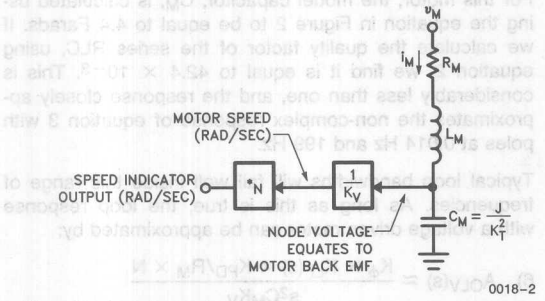
Following the phase detector is the loop filter. This block contains the required gain and filtering to set the loop's overall bandwidth and meet the necessary stability criteria. The output of the loop filter is the control input to the motor drive. Depending on the type of drive used, voltage or current, the driver will have respectively, a V_{OUT}/V_{IN} transfer characteristic, or an I_{OUT}/V_{IN} transconductance.

At first glance, it seems that the motor has simply replaced the V_{CO} (voltage controlled oscillator), in the classic phase locked loop. In fact, it is a little more complicated. The mechanical and electrical time constants of the motor come into play, making the transfer function of the motor more than just a voltage-in, frequency-out block. In order to analyze the loop's small and large signal behavior it is essential to have an equivalent electrical model for the motor.

A SIMPLE ELECTRICAL MODEL FOR A DC MOTOR

Figure 2 is an electrical representation of a DC motor. The terms used are defined here:

- L_M Motor winding inductance in henrys
- R_M Motor winding resistance in Ωs
- J Total moment of inertia of the motor in Nm-sec^2 (**Note:** 1 Nm = 141.6 oz-in)
- K_T Motor torque constant in Nm/Amp
- K_V Voltage constant (back EMF) of motor in voltage-sec/rad (**Note:** $K_V = K_T$ in SI units)



*N = Number of speed sense cycles per motor revolution

Figure 2. This simple electrical model is useful for determining the small and large signal characteristics of the motor. Capacitor, C_M is used to model the mechanical energy storage of the motor.

In this model the winding inductance and resistance elements correlate directly with the corresponding physical parameters of the motor, with values taken directly off the manufacturer's data sheet. The capacitor, C_M, models the mechanical energy storage of the motor. Current into the capacitor equates, via motor constant K_T, to motor torque, and the voltage across the capacitor is equal to the motor back EMF. The back EMF voltage equates to motor velocity through the inverse of K_V. In the model, the term N is simply a multiplier equal to the number of feedback cycles obtained per revolution of the motor. For example, in a 4 pole brushless DC motor the commutation Hall effect device outputs will be at twice the rotational frequency of the motor, making N equal to 2.

The equation for the capacitor, given in Figure 2, has the units of Farads if J and K_T are expressed in SI units. In modeling the overall transfer characteristic, it is important that the moment of inertia of the load on the motor be added to the moment of inertia of the motor itself.

It is worthwhile to note that the current into the motor, minus idling current, is proportional to acceleration of the motor. This is easily seen from the model by realizing that the time derivative of the capacitor voltage relates directly to acceleration. The effects of loads on the motor can be modeled by including a current source across the capacitor for constant torque loads, or a resistor for loads that are linearly proportional to motor speed.

TRANSFER FUNCTIONS FOR VOLTAGE AND CURRENT DRIVEN MOTORS

Using the electrical model, the small signal transfer function of the motor is easily derived. Equations 1a and 1b give the small signal frequency response for both the current and voltage driven cases respectively.

$$1a)\quad \frac{N \times \omega_M(s)}{i_M(s)} = \frac{N}{K_V} \times \frac{1}{sC_M}$$

$$1b)\quad \frac{N \times \omega_M(s)}{v_M(s)} = \frac{N}{K_V} \times \frac{1}{1 + sC_MR_M + s^2 L_MC_M}$$

The transfer function given in equation (1a) describes the small signal response of motor speed, $\omega_M(s)$, to changes in the drive current. Equation (1b) relates the dependence of motor speed to motor drive voltage.

The small signal response of the motor for the current driven case has a DC pole that results from the relationship of motor torque to velocity, that is, motor velocity is proportional to the integral of motor torque over time. In the current driven motor neither the winding resistance nor inductance appear in the transfer function. This is because these elements are in series with the current source output of the driver stage. As long as the output impedance of the driver remains large relative to the impedance of these elements, the resistance and inductance of the motor will have a negligible effect on the small signal response.

The voltage driven response has a second order characteristic that results from the interaction of the series RLC. In many cases the transfer function of the voltage driven case can be simplified. If the quality factor of the series RLC of the motor model is much less than one, as defined in equation 2, then the response of the motor can be accurately approximated by equation 3.

$$2)\quad Q_M = \frac{1}{R_M}\sqrt{\frac{L_M}{C_M}} = \frac{K_T}{R_M}\sqrt{\frac{L_M}{J}}$$

$$\therefore Q_M \ll 1 \quad \text{If } R_M \gg K_T\sqrt{\frac{L_M}{J}}$$

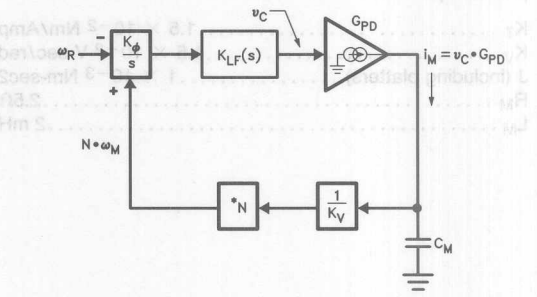
$$3)\quad \text{For } Q_M \ll 1$$

$$\frac{N \times \omega_M(s)}{v_M(s)} = \frac{N}{K_V} \times \frac{1}{(1 + sC_MR_M)(1 + sL_M/R_M)}$$

CONSIDERING THE WHOLE LOOP

Figure 3 shows the complete speed control loop for the current driven case. The overall open loop response, A_{OLC}, is easily written.

$$4)\quad A_{OLC}(s) = \frac{K_\phi \times K_{LF}(s) \times G_{PD} \times N}{s^2C_M \times K_V}$$



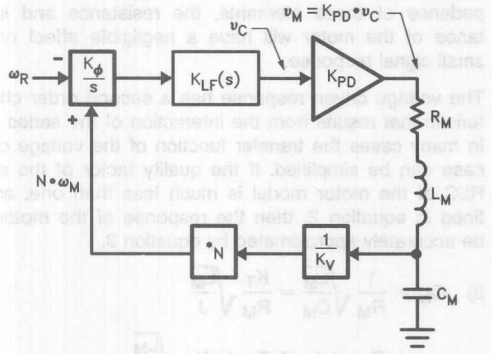
*N = Number of feedback cycles per motor revolution

Figure 3. In this phase locked loop, with current mode drive to the motor, the motor winding resistance and inductance can be ignored as long as the current driver maintains a high output impedance.

For this loop, note that there are two poles in the response at DC, i.e., s = 0. One pole is due to the response of the current driven motor, the second pole is from the frequency to phase transformation of the phase detector. The 180 degrees of phase shift this pair of poles introduce force a phase lead configuration of the loop filter in order to obtain a loop phase margin greater than zero.

The complete voltage loop is shown in Figure 4, and its open loop response, $A_{OLV}(s)$, in equation 5.

$$5)\quad A_{OLV}(s) = \frac{K_\phi \times K_F(s) \times K_{PD} \times N}{sK_V \times (1 + sC_MR_M + s^2 L_MC_M)}$$



*N = Number of feedback cycles per motor revolution

Figure 4. With voltage mode drive to the motor the electrical time constant of the motor plays a part in the small signal response of the speed control loop.

This response has only one pole at DC, although the total number of poles is three versus two for the current driven case. For most motors, particularly those used in constant velocity applications, this transfer function can be simplified by applying the results of equations 2 and 3. This is best illustrated by looking at an example. Consider the following motor, (typical 3-phase brushless for disc drive applications):

K_T ..... 1.5×10^{-2} Nm/Amp
K_V ..... 1.5×10^{-2} V-sec/rad
J (including platters) ..... 1×10^{-3} Nm-sec2
R_M 2.5Ω
L_M ..... 2 mH

For this motor, the model capacitor, C_M, is calculated using the equation in Figure 2 to be equal to 4.4 Farads. If we calculate the quality factor of the series RLC, using equation 2, we find it is equal to 42.4×10^{-3}. This is considerably less than one, and the response closely approximates the non-complex response of equation 3 with poles at 0.014 Hz and 199 Hz.

Typical loop bandwidths will fall well inside this range of frequencies. As long as this is true, the loop response with a voltage driven motor can be approximated by:

$$6)\quad A_{OLV}(s) \approx \frac{K_\phi \times K_{LF}(s) \times K_{PD}/R_M \times N}{s^2 C_M K_V}$$

$$\text{If } Q_M \ll 1 \text{ and } \frac{1}{2\pi C_M R_M} < f < \frac{R_M}{2\pi L_M} \left(f = \left|\frac{s}{2\pi}\right|\right)$$

This expression is the same as the current driven response, equation 4, with the transconductance of the current drive stage, G_{PD}, replaced by the gain of the voltage drive stage divided by the motor winding resistance, K_{PD}/R_M.

CLOSING THE LOOP

When it comes to closing the loop the goal is to have a stable loop with the required loop bandwidth. The variables that must be considered are:

1) The motor
2) The power driver, type and gain
3) The phase detector gain
4) Loop bandwidth
5) The loop filter

The first four of the above variables are usually dictated by conditions other than the stabilizing of the loop. This leaves the loop filter as the tool for achieving the small signal loop requirements.

For many cases involving constant velocity loops for DC motor speed control, the following simple Bode analysis can be applied for determining the design of the loop filter. Assuming we know, or have preliminary guesses for the first four variables listed above, we can plot the Bode asymptotes for phase and gain of the combined response of the motor and power driver. Figure 5 shows, for a typical case, such a plot on a frequency scale that has been normalized to the desired loop bandwidth, or open loop unity gain frequency. This figure illustrates the small signal open loop response for the current driven case, equation 4, minus the response of the loop filter, K_{LF}. If the previously noted assumptions hold, this plot will also apply to the voltage driven case i.e., equation 6.

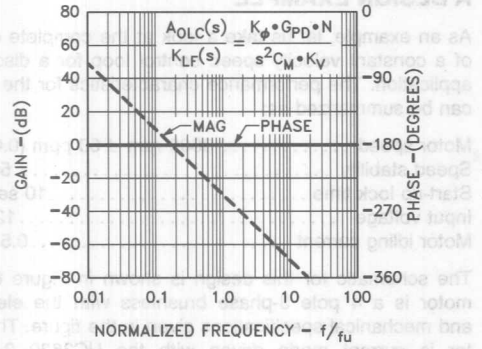


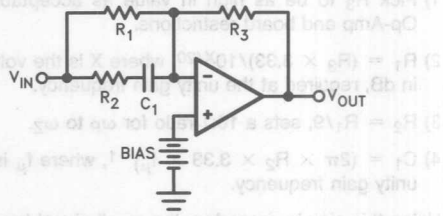
Figure 5. A Bode plot of the combined gain and phase response of the motor, motor drive, and phase dectector is useful in determining the requirements on the loop filter. This plot is normalized to the desired open loop unity gain frequency.

From Figure 5 two restrictions on the loop filter are readily apparent. First, since the remaining portion of the loop has 180° of phase shift over the entire frequency range, the loop filter must have a phase lead at the unity gain frequency and at all frequencies below the unity gain frequency. By meeting this restriction the small signal loop will be unconditionally stable.

Secondly, in order to achieve the desired loop bandwidth, the loop filter must have a voltage gain at the desired unity gain frequency of 30 dB. This level is simply the inverse of the remaining loop's voltage gain at the unity gain frequency.

A loop filter configuration that will meet these restrictions is shown in Figure 6. Also shown in this figure is the small signal response equation for the filter. The response starts out from DC with a flat inverting gain that breaks upward at the zero frequency, ω_Z, and then flattens out again at the pole, ω_P. The pole in this response is necessary to prevent excess feedthrough of residual reference frequency that is present at the outputs of many digital type phase detectors—in fact, as will be discussed in the design example, a separate reference filter is normally required.

A good choice for the relative positioning of the pole and zero of the loop filter response is to space them apart by 1 decade of frequency, and center them around the unity gain frequency. Figure 7 shows the Bode plots of this suggested positioning applied to the case illustrated in Figure 5. As shown, a phase margin of about 45° is obtained with this configuration.



$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{-R_3}{R_1} \times \frac{1 + s/\omega_Z}{1 + s/\omega_P}$$

$$\omega_Z = \frac{1}{(R_1 + R_2)\,C_1}$$

$$\omega_P = \frac{1}{R_2 C_1}$$

Figure 6. This loop filter configuration provides the required phase lead and gain at the loop crossover frequency.

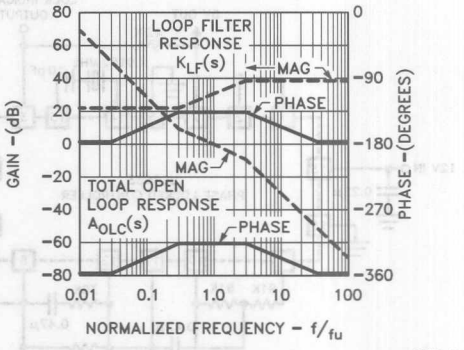


Figure 7. Using the criteria set forth for the design of the loop filter, the resulting Bode plot indicates a phase margin of 45°.

If the above results are acceptable, then the following simple steps can be applied to pick the loop amplifier component values. Referring to Figure 6.

1) Pick R_3 to be as high in value as acceptable for the Op-Amp and board restrictions.

2) $R_1 = (R_3 \times 3.33)/10^{X/20}$, where X is the voltage gain, in dB, required at the unity gain frequency.

3) $R_2 = R_1/9$, sets a 10:1 ratio for ω_P to ω_Z.

4) $C_1 = (2\pi \times R_2 \times 3.33 \times f_\mu)^{-1}$, where f_μ is the loop unity gain frequency.

Using this simple procedure the small signal loop is easily closed for stable static operation.

A DESIGN EXAMPLE

As an example, let us take a look at the complete design of a constant velocity speed control loop for a disc drive application. The performance characteristics for the circuit can be summarized as:

Motor speed ..... 3600 rpm ±60 ppm (0.006%)
Speed stability ..... ±50 ppm
Start-up lock time ..... 10 seconds
Input voltage ..... 12 Volts
Motor idling current ..... 0.5 Amps

The schematic for this design is shown in Figure 8. The motor is a 4 pole 3-phase brushless with the electrical and mechanical specifications given in the figure. The motor is current mode driven with the UC3620 3-phase Switchmode Driver. The speed control function is realized with the UC3633 Phase Locked Controller.

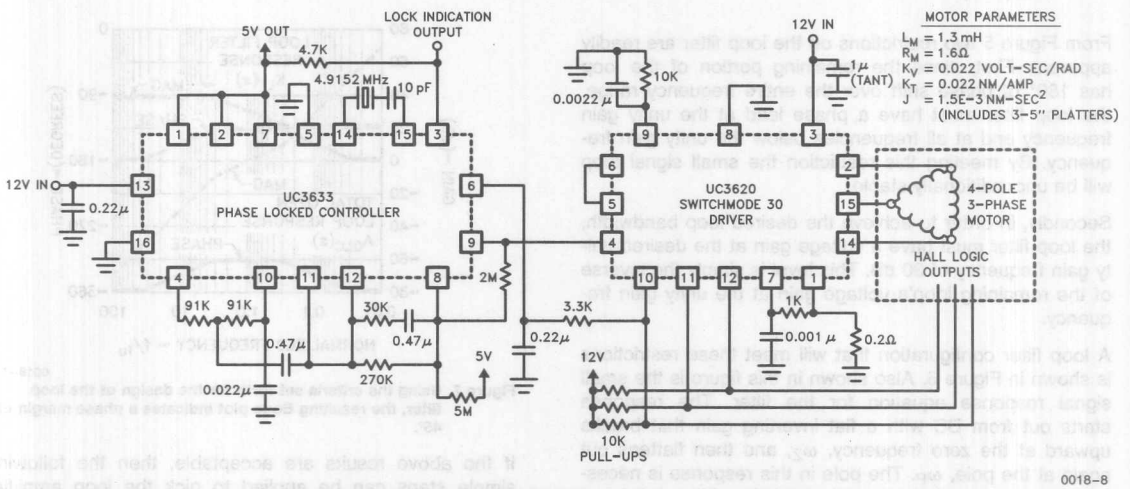


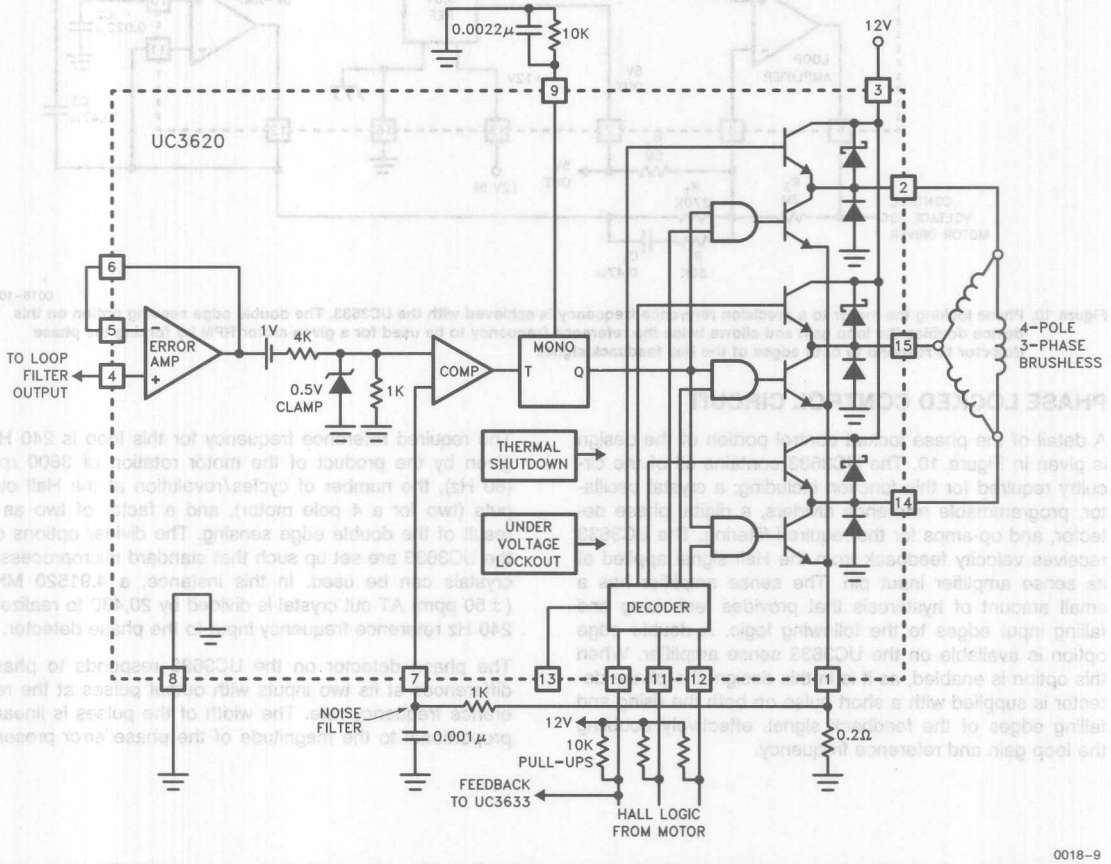
Figure 8. A precision speed control loop uses the UC3620 Switchmode 3-phase Driver and the UC3633 Phase Locked Controller to spin a DC brushless motor at 3600 rpm, ±60 ppm.

POWER DRIVER STAGE

In Figure 9 a detail of the driver IC and the associated circuitry is shown. The UC3620 is a current-mode, fixed off-time, chopper. Three 2-Amp totem pole output stages with catch diodes drive the three motor phases. The outputs are enabled by the internal commutation logic that responds to the three Hall logic signals from the motor. The motor is equipped with open collector Hall devices making the three 10k pull-up resistors on the UC3620 Hall inputs necessary.

Current is controlled by chopping the lowside drive to the phase winding under the command of the UC3620's current sense comparator. The RC combination on the timing pin of the driver sets the off-time at 22 μs. This results in a chopping frequency of well over 20 kHz under normal operating conditions.

The transconductance of the driver is set by the value of current sense resistor used at the emitter pin of the UC3620. With a value of 0.2Ω the transconductance from the error amplifier output to the driver outputs is 1 Amp/Volt. The UC3620 error amplifier is configured here as a unity gain buffer, thus the drive control signal is applied at the non-inverting error amplifier input with the same overall transconductance. An internal 0.5V clamp diode at the current sense comparator input results in a 2.5 Amp maximum drive current. There is a 1V offset internal to the UC3620 that is reflected to the drive control input at zero current. This offset combines with the 0.5 Amp idling current level of the motor to set the steady state DC voltage at the driver control input to be 1.5V.



0018-9

Figure 9. The UC3620 is a current mode fixed off-time driver. This device includes all the drive and commutation circuitry for a three phase brushless motor. The 0.2Ω current sense resistor and the internal divide by five sets the transconductance of this power stage to 1 Amp/Volt.

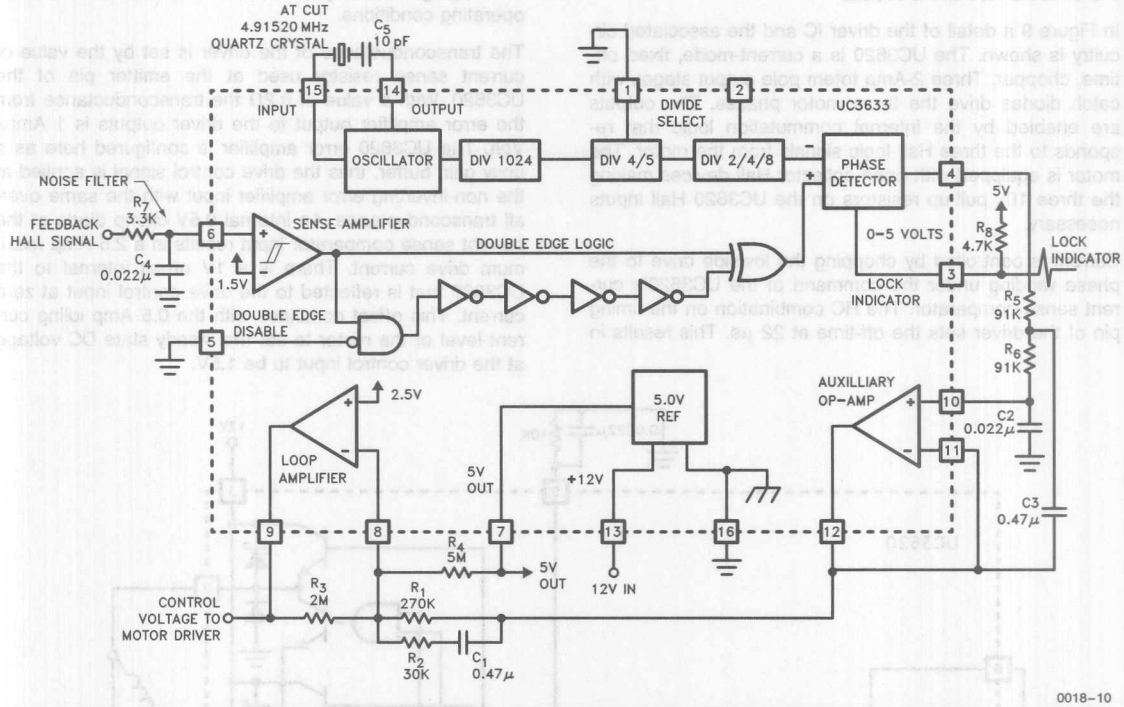


Figure 10. Phase locking the motor to a precision reference frequency is achieved with the UC3633. The double edge sensing option on this device doubles the loop gain and allows twice the reference frequency to be used for a given motor RPM by forcing the phase detector to respond to both edges of the Hall feedback signal.

PHASE LOCKED CONTROL CIRCUIT

A detail of the phase locked control portion of the design is given in Figure 10. The UC3633 contains all of the circuitry required for this function including: a crystal oscillator, programmable reference dividers, a digital phase detector, and op-amps for the required filtering. The UC3633 receives velocity feedback from the Hall signal applied at its sense amplifier input pin. The sense amplifier has a small amount of hysteresis that provides fast rising and falling input edges to the following logic. A double edge option is available on the UC3633 sense amplifier. When this option is enabled, as it is in this design, the phase detector is supplied with a short pulse on both the rising and falling edges of the feedback signal, effectively doubling the loop gain and reference frequency.

The required reference frequency for this loop is 240 Hz, given by the product of the motor rotation of 3600 rpm (60 Hz), the number of cycles/revolution at the Hall outputs (two for a 4 pole motor), and a factor of two as a result of the double edge sensing. The divider options on the UC3633 are set up such that standard microprocessor crystals can be used. In this instance, a 4.91520 MHz (±50 ppm) AT cut crystal is divided by 20,480 to realize a 240 Hz reference frequency input to the phase detector.

The phase detector on the UC3633 responds to phase differences at its two inputs with output pulses at the reference frequency rate. The width of the pulses is linearly proportional to the magnitude of the phase error present.

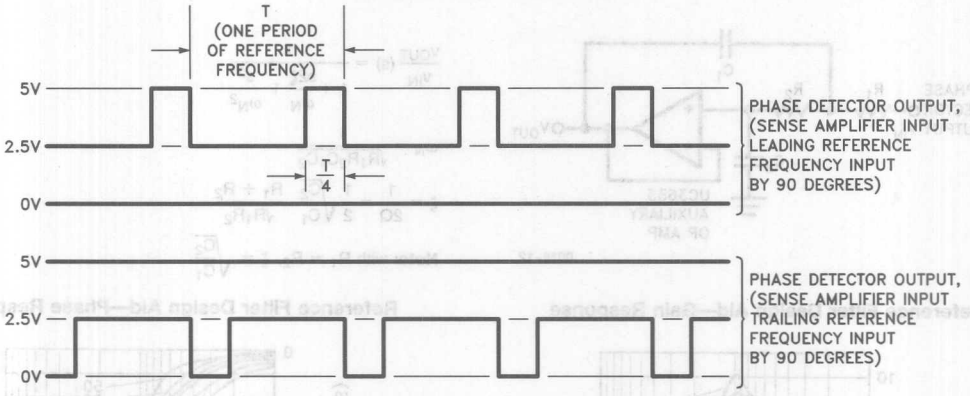


Figure 11. The phase detector on the UC3633 is a digital circuit that responds to phase error with a pulsed output at the reference frequency rate. The width and polarity of the pulses depend respectively on the phase error magnitude and polarity. If any static frequency error is present, the detector will respond with a constant 0 Volt or 5 Volt signal depending on the sign of the error present.

The pulses are always 2.5V in magnitude and are referenced to 2.5V at the detector output. The polarity of the output pulses tracks the polarity of the input phase error. This operation is illustrated in Figure 11. The resulting phase gain of the detector is $2.5V/2\pi$ radians, or about 0.4V/rad, with a dynamic range of $\pm 2\pi$ radians.

The phase detector also has the feature of absolute frequency steering. If any static frequency error exists between the two inputs, the output of the detector will stay in a constant high, or low state; 5V, if the feedback input rate is greater than the reference frequency and 0V, if the opposite frequency relationship exists. The lock indicator output on the UC3633 provides a logic low output when any static error exists between the feedback and reference frequencies.

A unity gain bandwidth of 4 Hz was chosen for this loop. This unity gain frequency is well below the effective sampling frequency, the 240 Hz reference, and is sufficently high to not significantly affect the start-up lock time of the drive system. The design of the loop filter follows the guidelines described earlier. The magnitude of the loop gain, minus the loop filter, at 4 Hz is equal to:

$$\frac{K_\phi \times G_{PD} \times N}{(2\pi f)^2 \times C_M \times K_V} = \frac{(0.4)(1)(4)}{(2\pi 4)^2(3.1)(0.022)}$$

$= 37.2$ E-3 or -28.6 dB.

This dictates that the loop amplifier has a gain of 28.6 dB at 4 Hz. A value for the loop amplifier feedback resistor, R_3, of 2 MΩ was chosen. The values for R_1, R_2 and C_1 were calculated as follows.

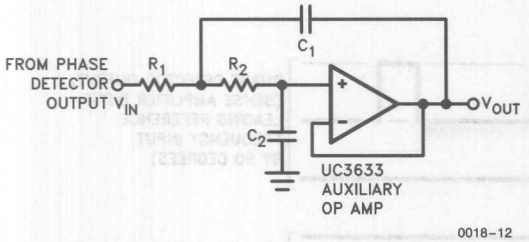
$R_1 = (2E6 \times 3.33)/10^{28.6/20} = 248\ k\Omega$ (270 kΩ used).

$R_2 = 270/9 = 30\ k\Omega$

$C_1 = (2\pi \times 30E3 \times 3.33 \times 4)^{-1}$
$= 0.4\ \mu F$ (0.47 μF used).

The additional op-amp on the UC3633 is used to realize a second order active filter to attenuate the reference component out of the phase detector. The filter is a standard quadratic with a natural frequency of 17.2 Hz and a Q of about 2.3. This circuit provides 46 dB of attenuation at 240 Hz while adding only 5° of phase shift at the 4 Hz loop crossover frequency. In Figure 12 design guidelines and response curves for this filter are given.

Reference Filter Configuration



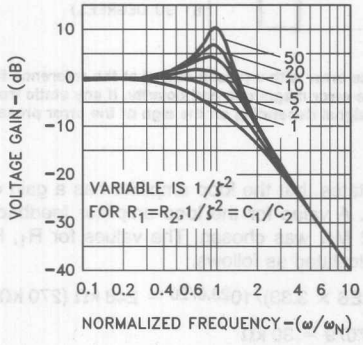
$$\frac{V_{OUT}}{V_{IN}}(s) = \frac{1}{1 + \frac{s2\zeta}{\omega_N} + \frac{s^2}{\omega_N^2}}$$

$$\omega_N = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}}$$

$$\zeta = \frac{1}{2Q} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}}\ \frac{R_1 + R_2}{\sqrt{R_1 R_2}}$$

Note: with $R_1 = R_2$, $\zeta = \sqrt{\frac{C_2}{C_1}}$

Reference Filter Design Aid—Gain Response



Reference Filter Design Aid—Phase Response

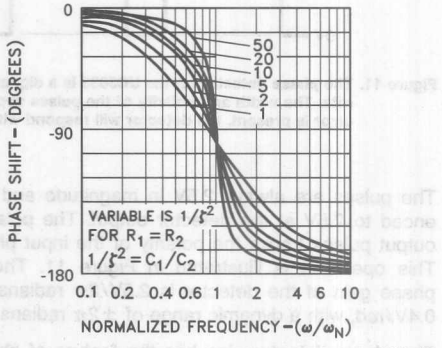


Figure 12. To keep feedthrough of the residual reference frequency at the phase detector output to a minimum, a simple quadratic filter can be used. The design of this filter is easily accomplished with the above equations and response curves.

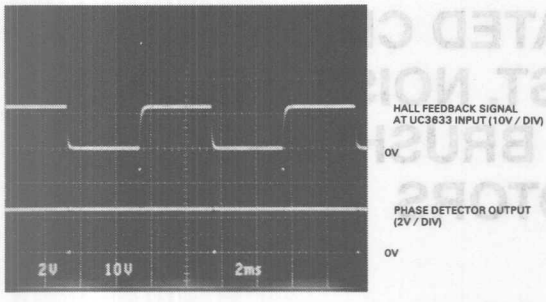
As mentioned earlier, a separate reference filter is required in this type of phase locked loop to attenuate the reference frequency feedthrough at the output of the phase detector. With the active filter following the phase detector, the feedthrough to the loop amplifier is kept to less than $20mV_{pp}$ under the worst case condition of $\pm\pi(180°)$ phase error. This is small compared to the 1.25V DC signal out of the detector at this phase error. If the reference ripple into the loop amplifier becomes large compared to the averaged phase error term, large signal instabilities may result. These are primarily the result of the unidirectional nature of the motor drive.

The static reference ripple at the motor drive input, during phase locked conditions, can be minimized by forcing the loop to lock at zero phase error—at zero phase error there is no reference frequency component at the detector output. The finite DC gain through the loop filter, dictated by the inherent second order nature of the loop, results in a static phase error that is a function of: the DC level required at the motor drive input, the DC gain and reference voltage of the loop amplifier, and the voltage levels out the phase detector. The addition of resistor R_4, see Figure 10, from the loop amplifier's inverting input to

the 5V reference sets the zero phase operating voltage at the loop filter output to 1.5V. This matches the nominal operating voltage required at the UC3620 control input, taking into account the 0.5 Amp idling current of the motor and the 1V offset of the driver. This cancellation is subject to variations due to shifts in DC operating levels, so, while it does significantly reduce static reference feedthrough, it can not be expected to reliably set exactly zero phase operation.

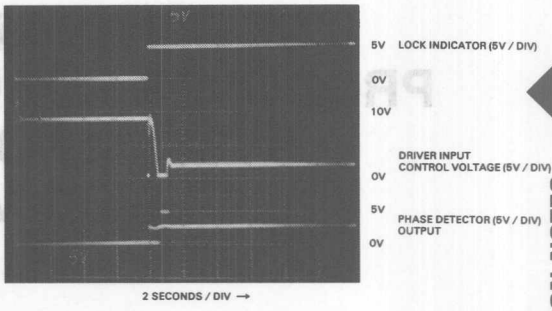
The oscilliscope traces in Figure 13 show the Hall input to the UC3633 along with the output waveform of the digital phase detector under static phase locked conditions. Notice that the phase detector output is alternating between positive and negative output pulses. This is a result of a slight asymmetry on the Hall input signal in conjunction with the use of the double edge sensing being used. In this case, the asymmetry is due to differences in the rising and falling edges of the Hall signal that result from the RC filter at the sense amplifier input. This filter is required to keep high frequency noise from the motor drive out of the phase detector.

The startup response of the motor is pictured in Figure 14. Shown are the voltage waveforms at the lock indicator output, the loop amplifier output, and the phase detector output of the UC3633. At the moment the lock indicator goes high the motor has reached its operating velocity. The absolute frequency steering of the phase detector forces a slight overshoot in frequency that delays the settling of the loop by about 1 second. Without the frequency steering feature the phase detector would command a much lower average drive signal during startup, extending the start time by over 50%.



0018-15

Figure 13. This oscilloscope trace shows the static waveforms at the Hall sensor input, and phase detector output of the UC3633. The static phase error has been adjusted, with R_4 in Figure 10, to be very small. The alternating positive and negative pulses at the output of the phase detector is due to an asymmetry in the Hall signal.



0018-16

Figure 14. The startup lock time of the motor is minimized with the absolute frequency steering feature of the phase detector, keeping lock times under 10 seconds.

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APPLICATION NOTE U-115

By R. Neidorff

NEW INTEGRATED CIRCUIT PRODUCES ROBUST, NOISE IMMUNE SYSTEM FOR BRUSHLESS DC MOTORS

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APPLICATION NOTE

New Integrated Circuit Produces Robust, Noise Immune System For Brushless DC Motors

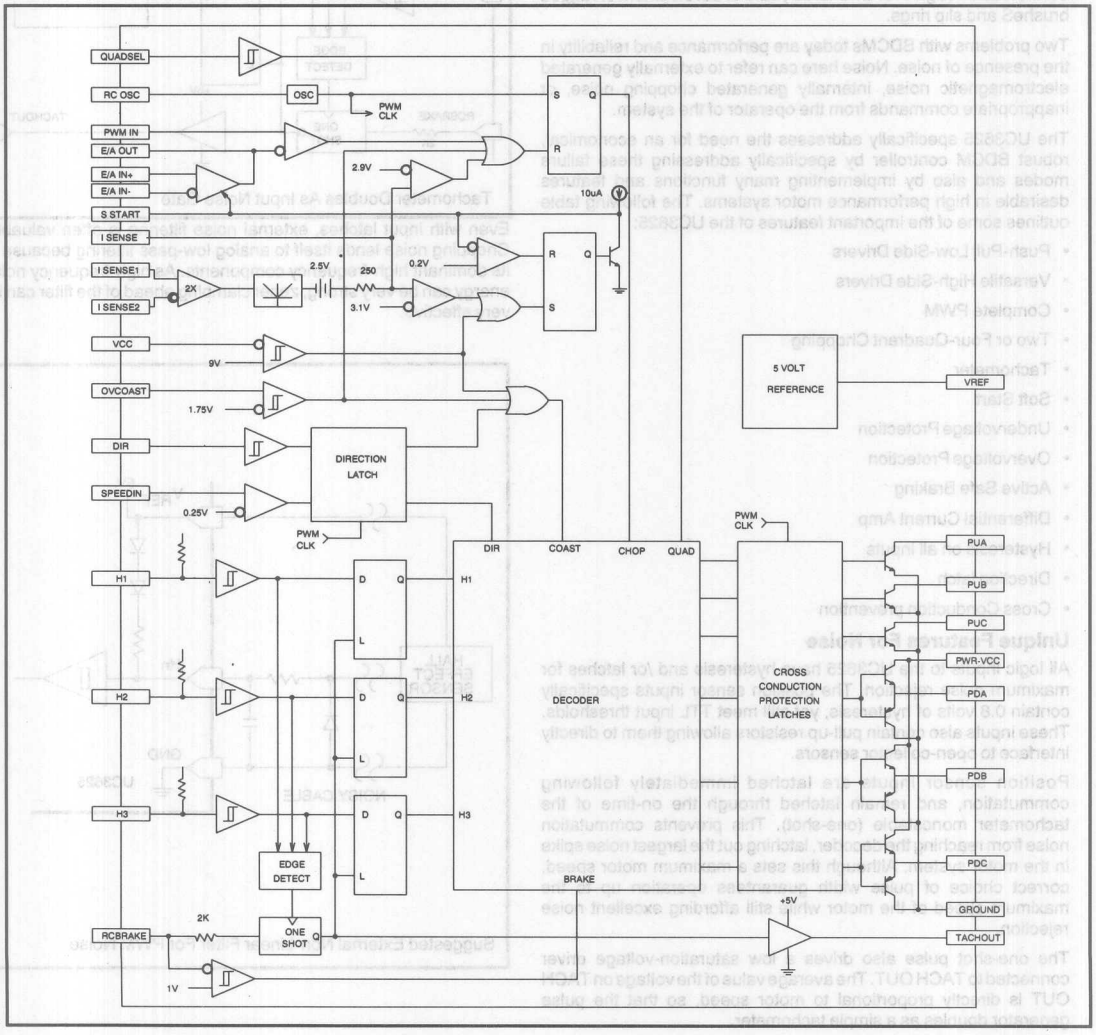
Bob Neidorff, Unitrode Integrated Circuits Corp., Merrimack, NH

Abstract

A new integrated circuit for brushless DC motor control is presented that implements many new techniques to enhance reliability and reduce the detrimental effects of noise. In addition to safety features and noise rejection circuitry, the new circuit contains a complete pulse-width modulator (PWM), a practical tachometer, a precision voltage reference, a high-speed current-sense amplifier, and high-voltage, high power, output stages.

Various applications of the IC are discussed in detail, including using the PWM for fixed frequency and fixed off-time control, driving power MOSFETs, driving bipolar power transistors, and sensing winding current. The IC is shown in applications that allow braking and direction reversal without damage to the motor or the power semiconductors.

BLOCK DIAGRAM OF THE UC3625



The Problem

Conventional brush motors have proven reliable and versatile. They remain popular partly because the pressures to improve haven't been high, and partly because nothing better has been available that is practical. Brushless DC motors (BDCMs) can pack the same horsepower into smaller, lighter boxes. They can also accelerate faster due to inherently lighter rotor construction. Without the friction and arcing of brushes, they are acoustically quieter. As they have permanent magnet rotors, they are faster to manufacture. Permanent magnet rotors also dissipate very little power, so BDCMs have far less heat dissipation problems.

One thing that has held the motor industry back has been the availability of economical control electronics. Recent price trends in power MOSFETs and monolithic motor controllers have reduced these limits. The final hurdle to broad acceptance is assurance of reliability. Brush motors proved their reliability not through design, but instead through over a hundred years of development of rugged brusheS and slip rings.

Two problems with BDCMs today are performance and reliability in the presence of noise. Noise here can refer to externally generated electromagnetic noise, internally generated chopping noise, or inappropriate commands from the operator of the system.

The UC3625 specifically addresses the need for an economical, robust BDCM controller by specifically addressing these failure modes and also by implementing many functions and features desirable in high performance motor systems. The following table outlines some of the important features of the UC3625:

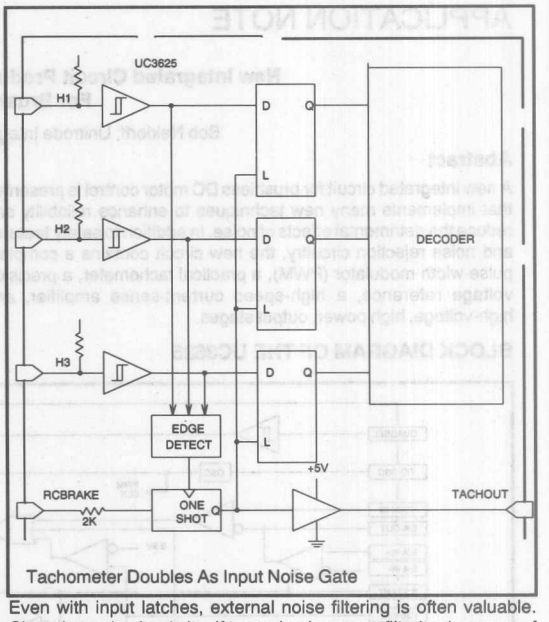
- Push-Pull Low-Side Drivers
- Versatile High-Side Drivers
- Complete PWM
- Two or Four-Quadrant Chopping
- Tachometer
- Soft Start
- Undervoltage Protection
- Overvoltage Protection
- Active Safe Braking
- Differential Current Amp
- Hysteresis on all inputs
- Direction latch
- Cross Conduction prevention

Unique Features For Noise

All logic inputs to the UC3625 have hysteresis and /or latches for maximum noise rejection. The position sensor inputs specifically contain 0.8 volts of hysteresis, yet still meet TTL input thresholds. These inputs also contain pull-up resistors allowing them to directly interface to open-collector sensors.

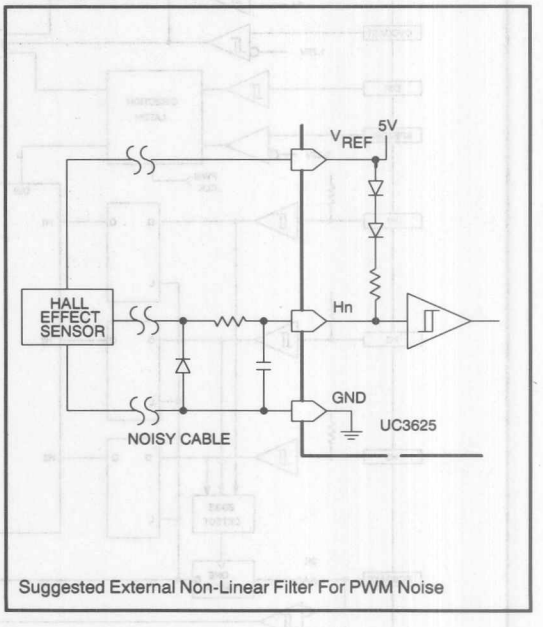
Position sensor inputs are latched immediately following commutation, and remain latched through the on-time of the tachometer monostable (one-shot). This prevents commutation noise from reaching the decoder, latching out the largest noise spike in the motor system. Although this sets a maximum motor speed, correct choice of pulse width guarantees operation up to the maximum speed of the motor while still affording excellent noise rejection.

The one-shot pulse also drives a low saturation-voltage driver connected to TACH OUT. The average value of the voltage on TACH OUT is directly proportional to motor speed, so that the pulse generator doubles as a simple tachometer.



Tachometer Doubles As Input Noise Gate

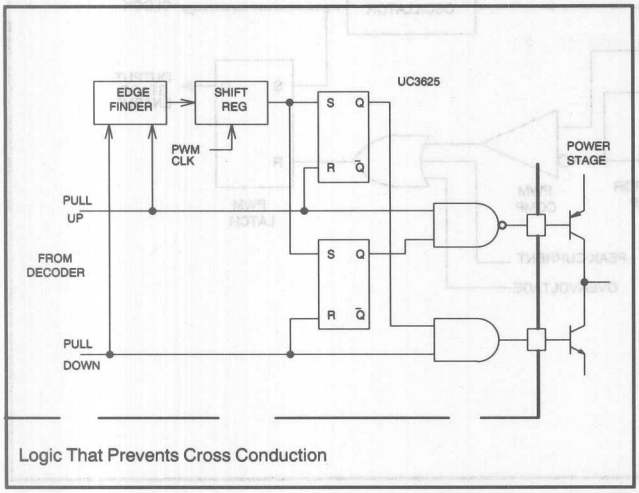
Even with input latches, external noise filtering is often valuable. Chopping noise lends itself to analog low-pass filtering because of its dominant high-frequency components. As high-frequency noise energy can be very strong, zener clamping ahead of the filter can be very effective.



Suggested External Non-Linear Filter For PWM Noise

Cross-Conduction Prevention

To further assure noise immunity, the UC3625 contains latches and a shift register to guarantee that all power stages turn off and remain off for a minimum time before changing states. In addition to preventing noise-induced cross conduction, this prevents cross conduction due to slow power stages.



Logic That Prevents Cross Conduction

The delay time is only inserted when an output is commanded from high to low or vice versa. During normal three phase commutation, outputs are turned off (opened) for a full cycle before changing states, so this delay will not impede normal operation. The only times that this delay will be inserted are during noise spikes, direction reversal, and braking.

Pulse-Width Modulation System

Motors perform better with higher operating voltages because for a given value of inductance, higher voltages can change winding current faster. A necessary adjunct to higher supply voltages is current control, either by linear amplifiers of pulse-width modulation (PWM). The UC3625 uses fixed frequency PWM for chopping.

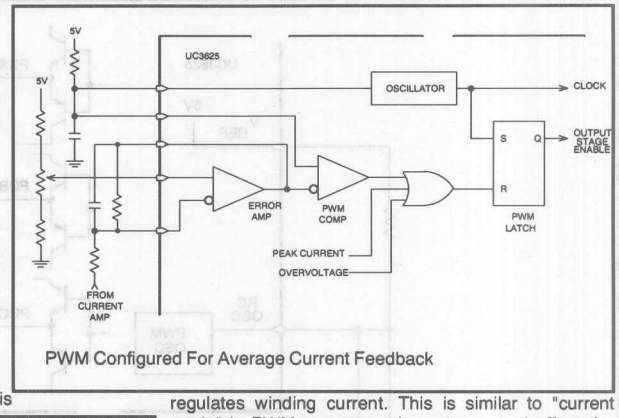
At the heart of the PWM is a sawtooth oscillator. The oscillator is programmed up to 500kHz with one resistor to the reference and one capacitor to the ground. This oscillator is used to enable the PWM latch every cycle, and also to clock the protection shift registers.

Another fundamental part of the PWM is the PWM latch. The output of this latch enables the power stages. The latch is set once per cycle by the oscillator, and cleared by either the PWM comparator, a peak current signal generated in current-sense circuitry, or by a fault signal from the OV/COAST input. This latch is reset dominant, meaning that a steady reset signal from any of three sources completely inhibits the power stages.

The other elements in the PWM are the PWM comparator and the error amplifier. The PWM comparator is an NPN-input comparator dedicated to comparing the output of the error amplifier to some other signal such as a command voltage, ramp, or sensed signal. The error amplifier is a PNP-input op-amp compensated for unity-gain operation, who's inputs can operate linearly down to ground.

The PWM can be configured into any number of different loops that regulate winding current (torque is nearly proportional to winding current), regulate speed, or regulate some other parameter. The PWM is internally configured for peak current control as well, although this is not intended to be the principle feedback loop.

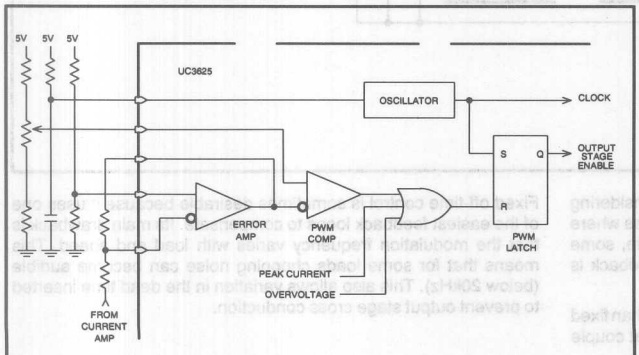
The approach above compares winding current to a DC voltage with the PWM comparator, and pulse-by-pulse regulates winding current. This is similar to "current mode" in PWM power-supply systems, and offers the advantage of removing the pole caused by load inductance from the feedback loop.



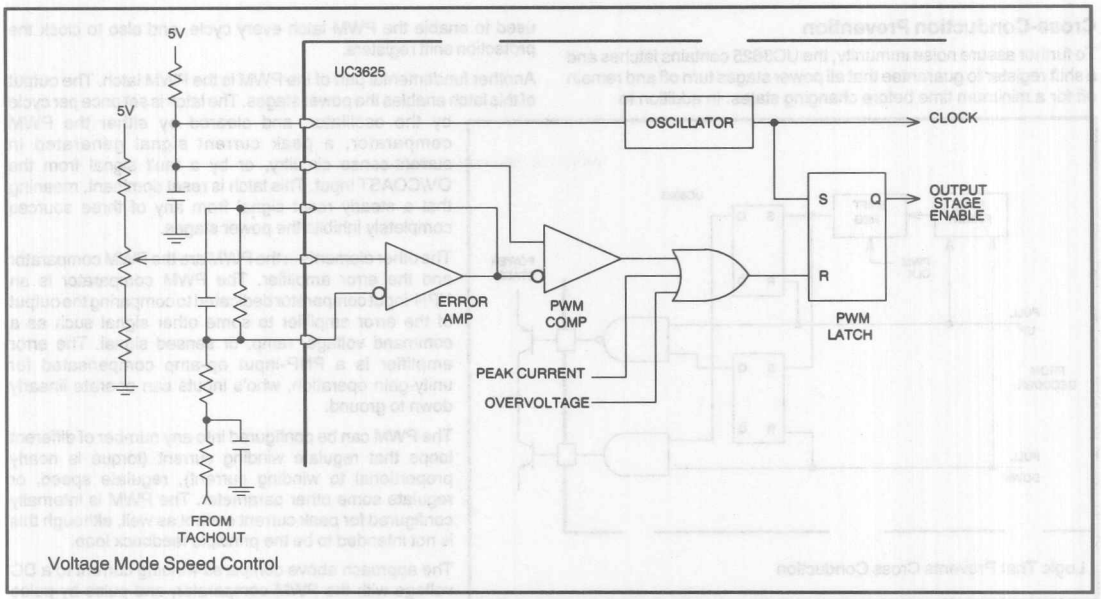
PWM Configured For Average Current Feedback

The PWM can also be configured to use the error amplifier to amplify the difference between the winding current and a desired current, and to use the PWM comparator to compare the error amp output to the oscillator ramp. This current loop operates on average, rather than peak current.

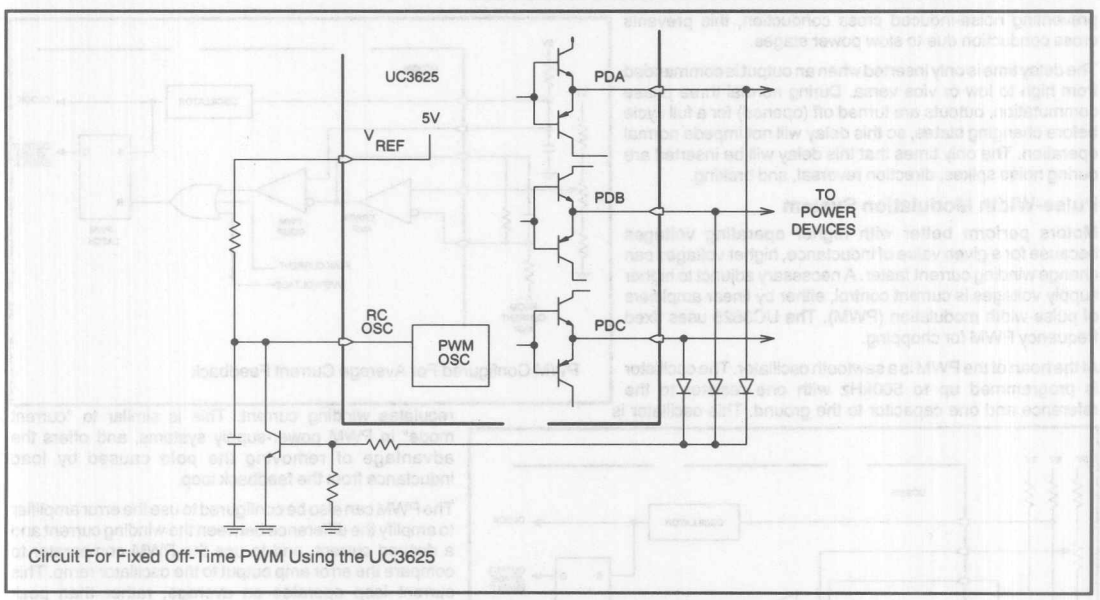
If the PWM comparator is used to compare the oscillator ramp to a DC voltage, then the load duty cycle is directly proportional to the applied DC voltage, as is the average load voltage. This "voltage mode" loop comes close to controlling speed because speed is nearly proportional to average winding voltage. If an overall speed feedback loop is required to regulate speed, this "voltage mode" topology can serve as a local feedback loop to make the system transfer function more linear, and the error amplifier can be used as the overall loop amplifier.



UC3625 PWM Block Diagram Configured For Pulse-By-Pulse Current Control



Voltage Mode Speed Control



Circuit For Fixed Off-Time PWM Using the UC3625

The advantages of each topology must be weighed considering complexity, overall stability, and sensitivity to load. In cases where current feedback seems nearly impossible to compensate, some compromise between currrent feedback and voltage feedback is dictated.

The PWM is also configurable to fixed off-time PWM rather than fixed frequency PWM by adding a few external components that couple the output off signal back into the oscillator.

Fixed off-time control is sometimes desirable because it uses one of the easiest feedback loops to compensate. Its main drawback is that the modulation frequency varies with load and speed. This means that for some loads chopping noise can become audible (below 20kHz). This also allows variation in the dead time inserted to prevent output stage cross conduction.

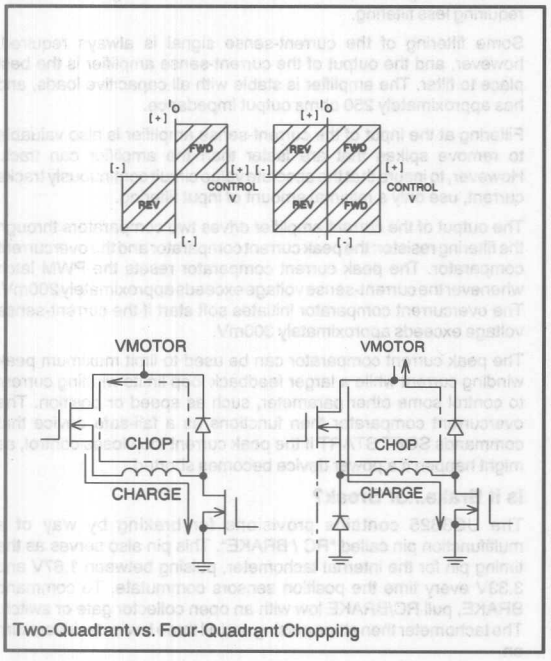
Different Chopping Techniques

Chopping capitalizes on the inductance of the load to maintain load current when the driving voltage is removed. The driving voltage is normally supplied through power switches, and diodes normally conduct across the load when the switches are opened.

Two different methods are common for chopping. The more efficient method chops one low-side power switch while one high-side switch is on. This is referred to as a two-quadrant PWM.

Two-quadrant PWM normally operates with a low duty cycle, as winding current is charged principally by the supply voltage, yet winding inductance is discharged by the voltage drop in the diode circuit (see figure below). Motor back EMF reduces the effective supply voltage and increases the effective diode voltage drop, so the duty cycle tends to increase with speed.

The main advantage of two-quadrant chopping is efficiency. Its main drawback is that it can't quickly decrease winding current. This can be very troublesome in position feedback systems.



Two-Quadrant vs. Four-Quadrant Chopping

In contrast, four-quadrant PWM systems chop both switches, and circulate load current through two diodes backwards into the supply.

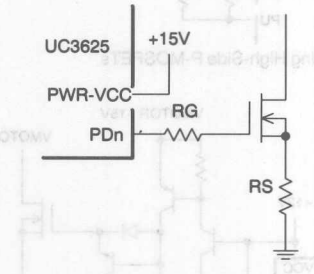
Again ignoring back EMF, four-quadrant chopping produces a nearly symmetrical current waveform, as current rises due to the supply voltage impressed on the load inductance, and decays due to reverse supply and load inductance. With four-quadrant chopping, a motor can decelerate as quickly as it can accelerate.

To program the UC3625 for one approach or the other, apply a logic signal to the QUAD SEL input. QUAD SEL can also be changed during operation to tailor performance to specific requirements.

Power Drivers

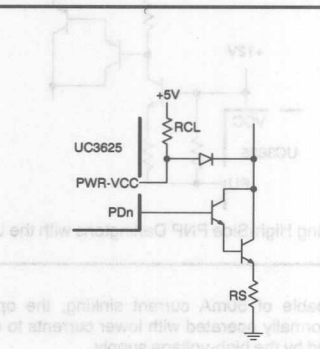
The overwhelmingly dominant power output device in new designs is the N-Channel Enhancement-Mode Power MOSFET. Bipolar power transistors and power darlingtons still have advantages in very high-voltage systems, but these advantages are being continuously eroded by developments in MOSFET structures and merged bipolar MOSFET devices. The UC3625 is able to drive both power MOSFETs and bipolar transistors.

The low-side drivers in the UC3625 are totem-poles capable of greater than 250mA peak gate or base current, but the package and the die are not constructed for continuous power dissipation greater than 1 watt, which imposes an upper limit on the available current for bipolar device drive.



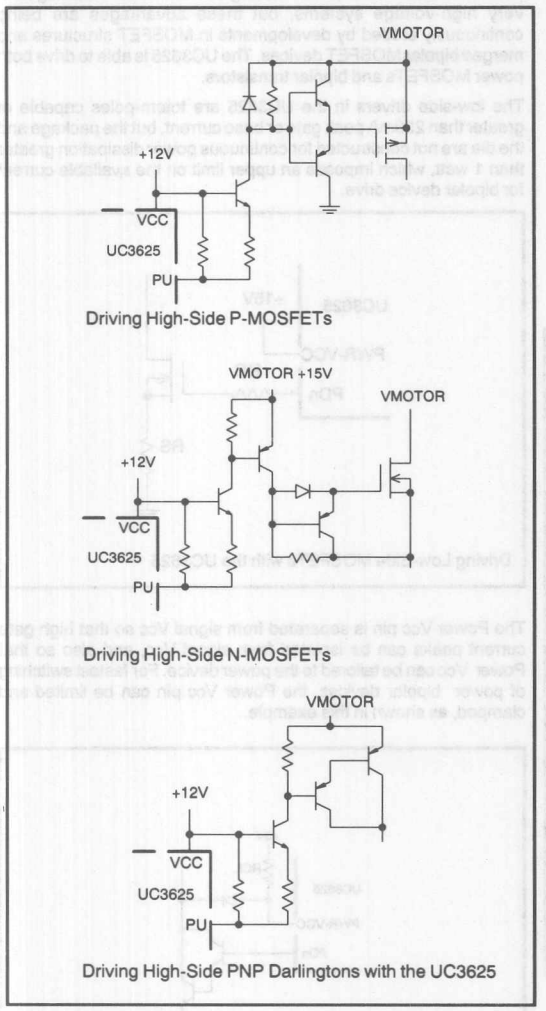
Driving Low-Side MOSFETs with the UC3625

The Power Vcc pin is separated from signal Vcc so that high gate current peaks can be isolated from signal Vcc, and also so that Power Vcc can be tailored to the power device. For fastest switching of power bipolar devices, the Power Vcc pin can be limited and clamped, as shown in this example.



Driving Low-Side Darlingtons with the UC3625

Driving high-side devices with the UC3625 requires level shifting if the motor supply is greater than 50V. The UC3625 high-side outputs are open collector NPN transistors which pull low to turn on high-side MOSFETs or bipolar transistors.



Although capable of 50mA current sinking, the open collector outputs are normally operated with lower currents to minimize the power supplied by the high-voltage supply.

As a high-side switch, P-channel power MOSFETs are far easier to drive than N-Channel power MOSFETs because the gate of P-channel MOSFETS need not be pulled above the positive supply to obtain low voltage drop. Unfortunately, P-channel power MOSFETs are more expensive and less available than N-channel devices, so the added supply in the N-channel design is often justified.

Current Sense

The UC3625 contains a high-speed gain-of-two differential amplifier dedicated to current sensing. This amplifier can be connected directly across a low-value current-sense resistor or between two different current-sense resistors. Since the amplifier common mode range allows operation one volt below ground, the amplifier has excellent common-mode noise rejection.

The current-sense amplifier also embodies an ideal diode that performs absolute value and level shifting of the input, giving a transfer function of:

$$Vo = 2.5 + 2\ ABS\ (Vi_2 - Vi_1)$$

If the low-side power devices and the lower catch diodes are returned to the same current-sense resistor, and the UC3625 is chopping in four-quadrant mode, then the winding current always flows through the current-sense resistor. The voltage on the current-sense resistor flips polarity every time the PWM chops, but the absolute value current-sense amplifier rectifies this, giving a smoother representation of continuous winding current, and requiring less filtering.

Some filtering of the current-sense signal is always required, however, and the output of the current-sense amplifier is the best place to filter. The amplifier is stable with all capacitive loads, and has approximately 250 ohms output impedance.

Filtering at the input of the current-sense amplifier is also valuable to remove spikes that are faster than the amplifier can track. However, to insure that the absolute value circuit continuously tracks current, use only a minimal amount of input filtering.

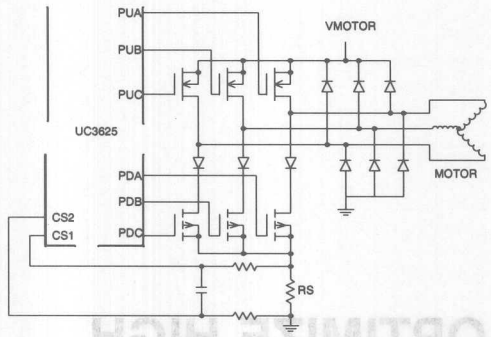
The output of the current amplifier drives two comparators through the filtering resistor: the peak current comparator and the overcurrent comparator. The peak current comparator resets the PWM latch whenever the current-sense voltage exceeds approximately 200mV. The overcurrent comparator initiates soft start if the current-sense voltage exceeds approximately 300mV.

The peak current comparator can be used to limit maximum peak winding current while a larger feedback loop limits winding current to control some other parameter, such as speed or position. The overcurrent comparator then functions as a fail-safe device that commands SOFT START if the peak current loop loses control, as might happen if a power device becomes shorted.

Is it Brake...or Break?

The UC3625 contains provisions for braking by way of a multifunction pin called "RC / BRAKE". This pin also serves as the timing pin for the internal tachometer, pulsing between 1.67V and 3.33V every time the position sensors commutate. To command BRAKE, pull RC/BRAKE low with an open collector gate or switch. The tachometer then stops pulsing and all three low-side drivers turn on.

Normal PWM configurations do not allow braking current to be modulated because the braking current does not normally flow through the sense resistor. The motor control circuit below includes three added diodes that, during BRAKE and all other circumstances causes winding current to flow through the sense resistor. Using this circuit, the UC3625 stops a motor as fast as the peak limit current setting allows and protects the output power devices and the motor.



Circuit For Safe Braking Series diodes guarantee that braking current will flow in the current-sense resistor

Direction Reversal is Worse

As with braking, direction reversal can also force excessive current into power devices if not checked. Direction reversal forces two of the three driver channels to go from high to low or low to high directly. With the UC3625, cross conduction is completely prevented, but high winding current is dependent upon the application. The higher the speed, the higher back EMF, and the higher the potential peak current.

The approach mentioned for braking also limits peak winding current during direction reversal. In addition, the direction latch and shift register in the UC3625 can be configured to prevent direction reversal until motor speed drops to a safe level. This latch also commands COAST whenever a direction reversal is commanded and motor speed is too high.

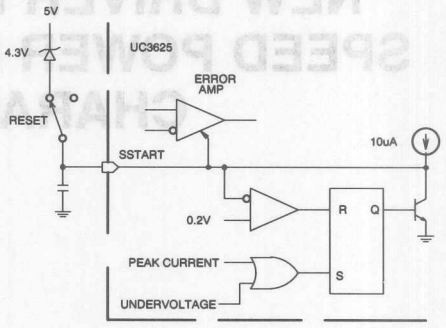
The easiest way to configure this protection is using the internal tachometer to drive "SPEED IN" through a low-pass RC filter. The "SPEED IN" threshold is set to prevent reversal whenever input voltage exceeds approximately 250mV.

Other Protection Features

To prevent confusion or insufficient drive to power MOSFETs, the UC3625 contains a comparator to lock off all six outputs until the Vcc input exceeds 9V, called under-voltage lock-out. The UC3625 also contains an uncommitted comparator that inhibits the outputs and clears the PWM latch whenever its input exceeds 1.75V. This can be used with a voltage divider for an over-voltage inhibit, or can be directly driven from TTL or CMOS for a logic controlled COAST input.

To prevent very high power supply current spikes and to limit average current during faults, the UC3625 contains latched soft start. The latch is set by low power-supply voltage or overcurrent fault, and is only cleared when the setting condition goes away and the soft start input discharges to below approximately 200mV.

Normally, the UC3625 is configured with a capacitor from soft start to ground, which is charged by the soft start 10uA current source. The UC3625 can also be configured to latch soft start until cleared by connecting a 4.3 volt zener and a normallly closed switch from Vref to soft start. The switch then functions as a reset switch.



Manual Fault Reset Circuit Uses Zener Diode to Latch Faults

Voltage Reference

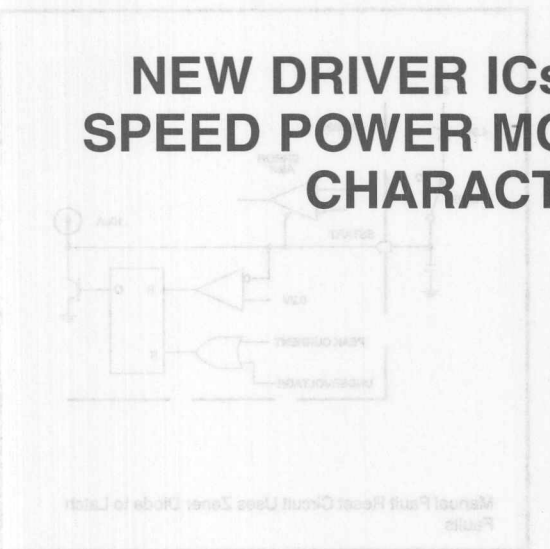
Finally, the UC3625 contains a precision voltage reference trimmed to 5V +/- 2%. This reference powers most of the internal circuitry for supply rejection and is available on the "Vref" pin for driving other circuitry such as Hall-effect position sensors and bias circuits. Operation of the voltage reference is guaranteed with loads up to 30mA, and the reference is also short circuit current limited to approximately 100mA.

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APPLICATION NOTE U-118

By Bill Andreycak

NEW DRIVER ICs OPTIMIZE HIGH SPEED POWER MOSFET SWITCHING CHARACTERISTICS



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APPLICATION NOTES

NEW DRIVER ICs OPTIMIZE HIGH SPEED POWER MOSFET SWITCHING CHARACTERISTICS

Bill Andreycak
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ABSTRACT

Although touted as a high impedance, voltage controlled device, prospective users of Power MOSFETs soon learn that it takes high drive currents to achieve high speed switching. This paper describes the construction techniques which lead to the parasitic effects which normally limit FET performance, and discusses several approaches useful to improve switching speed. A series of drivers ICs, the UC3705, UC3706, UC3707 and UC3709 are featured and their performance is highlighted. This publication supercedes Unitrode Application Note U-98, origionally written by R. Patel and R. Mammano of Unitrode Corporation.

INTRODUCTION

An investigation of Power MOSFET construction techniques will identify several parasitic elements which make the highly-touted "simple gate drive" of MOSFET devices less than obvious. These parasitic elements, primarily capacitive in nature, can require high peak drive currents with fast rise times coupled with care that excessive di/dt does not cause current overshoot or ringing with rectifier recovery current spikes.

This paper develops a switching model for Power MOSFET devices and relates the individual parameters to construction techniques. From this model, ideal drive characteristics are defined and practical IC implementations are discussed. Specific applications to switch-mode power systems involving both direct and transformer coupled drive are described and evaluated.

POWER MOSFET CHARACTERISTICS

The advantages which power MOSFETs have over their bipolar competitors have given them an ever-increasing utilization in power systems and, in the process, opened the way to new performance levels and new topologies.

A major factor in this regard is the potential for extemely fast switching. Not only is there no storage time inherent with MOSFETs, but the switching times can be user controlled to suit the application. This, or course, requires that the designer have an understanding of the switching dynamics inherent in these devices. Even though power MOSFETs are majority carrier devices, the speed at which they can switch is dependent upon many parameters and parasitic effects related to the device's construction.

THE POWER MOSFET MODEL

An understanding of the parasitic elements in a power MOSEFT can be gained by comparing the construction details of a MOSFET with its electrical model as shown in Figure 1. This construction diagram is a simplified sketch of a single cell - a high power device such as the IRF 150 would have ≈ 20,000 of these cells all connected in parallel.

In operation, when the gate voltage is below the gate threshold, Vg(th), the drain voltage is supported by the N-drain region and its adjacent implanted P region and there is no conduction.

When the gate voltage rises above Vg(th), however, the P area under the gate inverts to N forming a conductive layer between the N+ source and the N-drain. This allows electrons to migrate from source to drain where the electric field in the drain sweeps them to the drain terminal at the bottom of the structure.

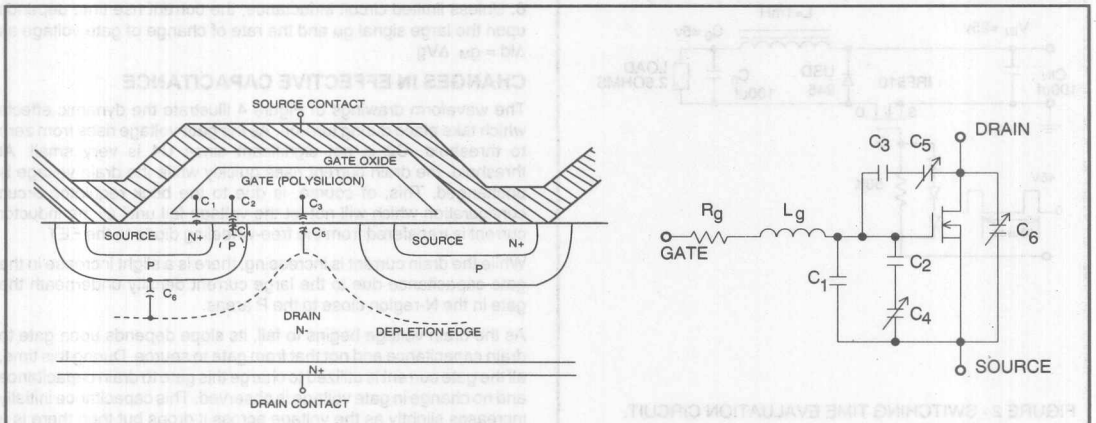


FIGURE 1 - SIMPLIFIED CROSS SECTION OF A POWER MOSFET CELL AND ITS ELECTRICAL EQUIVALENT.

3 APPLICATION NOTES

In the equivalent model, the parameters are defined as follows:

1. Lg and Rg represent the inductance and resistance of the wire bonds between the package terminal and the actual gate, plus the resistance of the polysilicon gate runs.

2. C1 represents the capacitance from the gate to both the N+ source and the overlying source interconnecting metal. Its value is fixed by the design of the structure.

3. C2 + C4 represents additional gate-source capacitance into the P region. C2 is dielectric capacitance and is fixed while C4 is due to the depletion region between source and drain and varies with the gate voltage. Its contribution causes total gate-source capacitance to increase 10-15% as the gate voltage goes from zero to Vg(th).

4. C3 + C5 is also made up of a fixed dielectric capacitance plus a value which becomes significant when the drain to gate voltage potential reverses polarity.

5. C6 is the drain-source capacitance and while it also varies with drain voltage, it is not a significant factor with respect to switching times.

EVALUATING FET PARASITIC ELEMENTS

Although it is clearly not the best way to drive a power MOSFET, using a constant gate current to turn the device on allows visualization of the capacitive effects as they affect the voltage waveforms. Thus the demonstration circuit of Figure 2 is configured to show the gate dynamics in a typical buck-type switching regulator circuit. This simulates the inducitve switching of a large class of applications and is implemented here with a IRF-510 FET, which is a 4 amp, 100V device with the following capacitances:

Ciss ≈ C1 + C4 + C5 = 135 - 150 pF

Crss ≈ C5 = 20 - 25 pF Vgs = 0V

Coss ≈ C5 + C6 = 80-100 pF

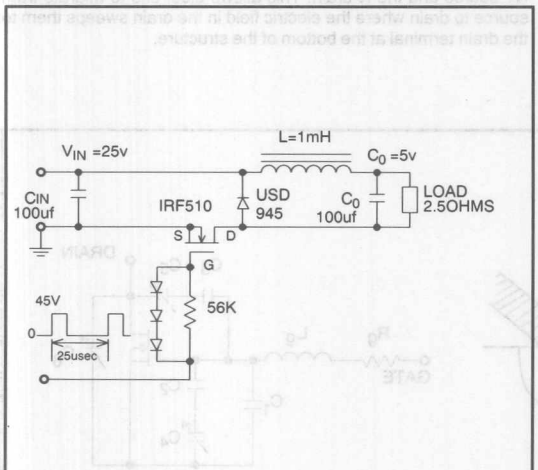


FIGURE 2 - SWITCHING TIME EVALUATION CIRCUIT.

In this illustration, the load portion of the circuit is established with Vin = 25V. Io = 2A. and f = 25Khz. The resultant turn-on waveforms are shown in Figure 3 from which the following observations may be made:

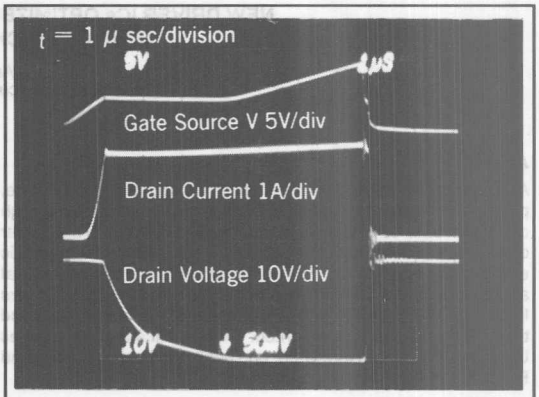


FIGURE 3-FET TURN-ON SWITCHING CHARACTERISTICS WHEN DRIVEN WITH A CONSTANT GATE CURRENT

1. For a fixed gate drive current, the drain current rise tiime is 5 times faster than the voltage fall time.

2. There is a 10-15% increase in gate capacitance when the gate voltage reaches Vg(th).

3. The gate voltage remains unchanged during the entire time the drain voltage is falling because the Miller effect increases the effective gate capacitance.

4. The input gate capacitance is approximately twice as high when drain current is flowing as when it is off.

5. The drain voltage fall time has two slopes because the effective drain-gate capacitance takes a significant jump when the drain-gate potential reverses polarity.

6. Unless limited circuit inductance, the current rise time depends upon the large signal g_M and the rate of change of gate voltage as $\Delta Id = g_M \Delta Vg$

CHANGES IN EFFECTIVE CAPACITANCE

The waveform drawings of Figure 4 illustrate the dynamic effects which take place during turn-on. As the gate voltage rises from zero to threshold. C2 is not significant since C4 is very small. At threshold, the drain current rises quickly while the drain voltage is unchanged. This, of course, is due to the buck regulator circuit configuration which will not let the voltage fall until all the inductor current is transfered from the free-wheeling diode to the FET.

While the drain current is increasing, there is a slight increase in the gate capacitance due to the large current density underneath the gate in the N-region close to the P areas.

As the drain voltage begins to fall, its slope depends upon gate to drain capacitance and not that from gate to source. During this time, all the gate current is utilized to charge this gate to drain capacitance and no change in gate voltage is observed. This capacitance initially increases slightly as the voltage across it drops but then there is a significant jump in value when the drain falls lower than the gate. When the polarity reverses from drain to gate, a surface charge accumulation takes place and the entire gate structure becomes part of the gate to drain capacitance. At this point the drain voltage fall time slows for the duration of its transition.

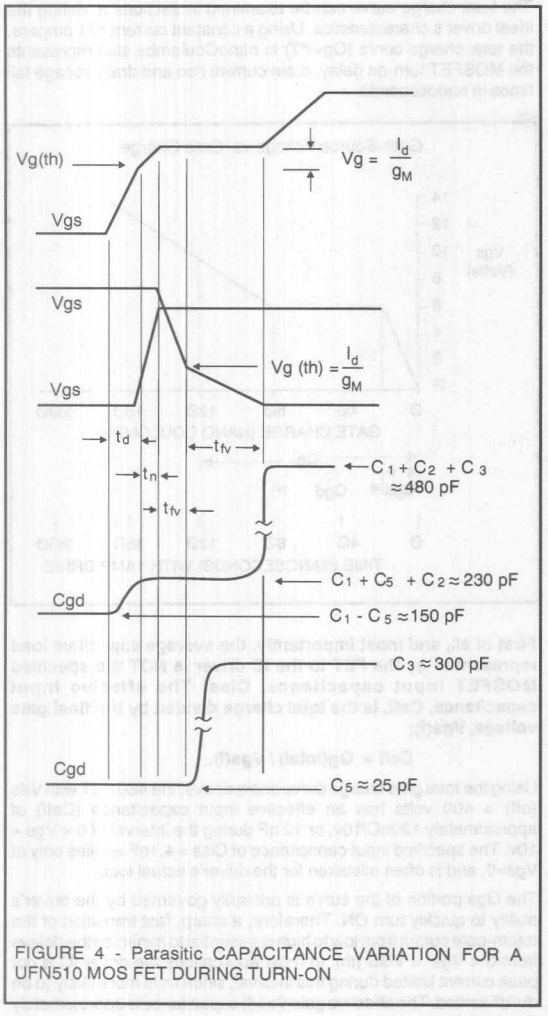


FIGURE 4 - Parasitic CAPACITANCE VARIATION FOR A UFN510 MOS FET DURING TURN-ON

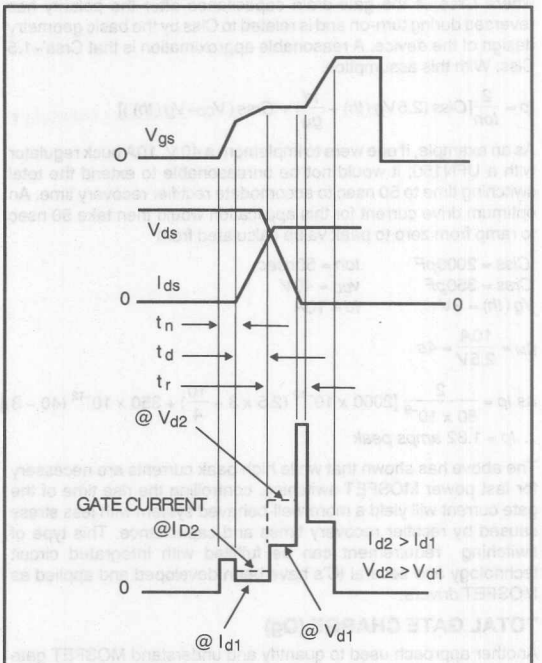


FIGURE 5 - AN "IDEAL" GATE CURRENT TURN-ON DRIVE TO PROVIDE EQUAL CURRENT RISE AND VOLTAGE FALL TIMES WITH AN INDUCTIVE LOAD

AN OPTIMUM GATE DRIVE

In most switching power supplly applications, if a step function in gate current is provided, the drain current rise time is several times faster than the voltage fall time. This can result in substantial switching power losses which are most often combated by increasing the gate drive current. This creates a problem, however, in that it further reduces current rise time which can cause overshoot, ringing, EMI and power dissipation due to recovery time for the rectifiers which are much happier with a more slowly changing drain current.

In an effort to meet these conflicting requirements, an idealized gate current waveform was derived based upon the goal of making the voltage fall time equal to the current rise time. This optimum gate current waveform is shown in Figure 5 and consists of the following elements

1. An initial fast pulse to get the gate voltage up to threshold.

2. A lesser amount to slow the drain current rise time. This value however, will also be a functiion of the required drain current.

3. Another increase to get the drain voltage to fall rapidly with a large current pulse added when the drain gate potential reverses.

4. A continued amount to allow the gate voltage to charge to its final value.

Obviously this might be a little difficult to implement in exact form, however, it can be approximated by a gate current waveform which, instead of being constant, has a rise time equal to the desired sum of the drain current rise time and the voltage fall time, and a peak value high enough to charge the large effective capacitance which appears during the switching transition. The peak current requirement can be calculated on the basis of defining the amount of charge required by the parasitic capacitance through the switching period.

A linear current ramp will deliver a charge equal to

$$Q = \frac{Ip \cdot ton}{2} \qquad \text{where we define } ton = td + tn + tfv$$

The total charge required for switching is

$$Q = Ciss\,[Vg\,(th) - \frac{Id}{gM}] - Crss\,[V_{DD} - Vg\,(th)] - CrssV_g\,(th)$$

where Crss' is the gate-drain capacitance after the polarity has reversed during turn-on and is related to Ciss by the basic geometry design of the device. A reasonable approximation is that Crss'≈1.5 Ciss. With this assumption.

$$Ip \approx \frac{2}{ton}[Ciss\,(2.5Vg\,(th) + \frac{Id}{g_M}) + Crss\,(V_{DD} - Vg\,(th))]$$

As an example, if one were to implement a 40 V. 10A buck regulator with a UFN150, it would not be unreasonable to extend the total switching time to 50 nsec to accomodate rectifier recovery time. An optimum drive current for this application would then take 50 nsec to ramp from zero to peak value calculated from

$Ciss = 2000pF$ $\quad ton = 50nsec$
$Crss = 350pF$ $\quad V_{DD} = 40V$
$Vg\,(th) = 3V$ $\quad Id = 10A$

$$g_M = \frac{10A}{2.5V} = 4s$$

$$as\ Ip = \frac{2}{50 \times 10^{-9}}\,[2000 \times 10^{-12}\,(2.5 \times 3 + \frac{10}{4}) + 350 \times 10^{-12}\,(40 - 3)]$$

$\therefore\ Ip = 1.32\ amps\ peak$

The above has shown that while high peak currents are necessary for fast power MOSFET switching, controlling the rise time of the gate current will yield a more well-behaved system with less stress caused by rectifier recovery times and capacitance. This type of switching requirement can be fulfilled with integrated circuit technology and several IC's have been developed and applied as MOSFET drivers.

TOTAL GATE CHARGE (Qg)

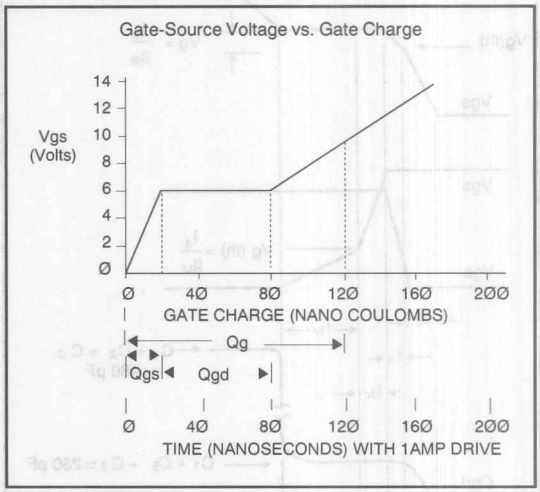
Another approach used to quantify and understand MOSFET gate drive requirements is much simpler than that of examining the instantaneous voltages, currents and capacitances. The term "Total Gate Charge", or Qg specifies the amount of gate charge required to drive the FET gate-to-source voltage (Vgs) from zero to ten volts, or vice-versa. For most high voltage devices, these thresholds correspond to the FET being either completely on or off.

Charge (Q) can be expressed as the product of either current multiplied by time (I*T), or capacitance multiplied by voltage (C*V) in the units of Coulombs. Most contemporary devices have total gate charge requirements in the tens to low hundreds of nano Coulombs, dependent almost entirely on die's geometry. For example, an IRF710 (size 1) FET has a total gate charge requirement of only 7.7 nC whereas the IRFP460 (size 6) demands 120 nC, and both are typical values.

PARAMETER	IRFP 440	IRFP 450	IRFP 460
Qgs (NC)	6.2	11	18
Qgd (NC)	22	43	62
Qg (NC)	42	86	120
Ciss (Nf)	1.3	2.7	4.1

There are two specified parameters contained within the total gate charge expression; Qgs, the gate-to-source charge, and Qgd the gate-to-drain, or "Miller" charge. Qgs is the amount of charge required to bring the gate voltage from zero up to its threshold VGS (th), of approximately 6 volts. Qgd defines the amount of charge that must be input to overcome the "Miller" effect as the drain voltage falls. This occurs during the plateau of the gate-to-source voltage waveform where the voltage is "constant". Excess charge is added to lower the effecive Rds (on) until the gate voltage reaches 10 volts, wher Qg is specified. Further increases above this level do NOT lower Rds (on), so a 10-12 volt driver bias is ideal.

The total charge curve can be examined in sections to define the ideal driver's characteristics. Using a constant current of 1 ampere, the total charge curve (Qg=I*T) in nanoCoulombs also represents the MOSFET turn-on delay, drain current rise and drain voltage fall times in nanoseconds.



First of all, and most importantly, the average capacitive load represented by the FET to the IC driver is NOT the specified MOSFET input capacitance, Ciss. The effecive input capacitance, Ceff, is the total charge divided by the final gate voltage, Vgs(f);

Ceff = Qg(total) / Vgs(f).

Using the total gate charge curve show above, the 460 FET with Vds (off) = 400 volts has an effective input capacitance (Ceff) of approximately 120nC/10v, or 12 nF during the interval of 0 < Vgs < 10v. The specified input capacitance of Ciss = 4.1nF applies only at Vgs=0, and is often mistaken for the driver's actual load.

The Qgs portion of the curve is primarily governed by the driver's ability to quickly turn ON. Therefore, a sharp, fast transition of the totem-pole output from low to high is essential to minimize the delays from 0 < Vgs < VGS (th). In most applications the driver IC is not peak current limited during this interval, since its is more likely to be dV/dT limited. The effective gate (load) capacitance is approximately Qgs / VGS(th), or Ciss.

Evident from the charge specifications, most of the popular size FETs used in switch-mode power supplies (sizes 4. 5 and 6) have much larger Qgd demands than their gate-to-source counterpart, Qgs. During this Qgd interval, the gate voltage remains "constant" while gate charge accumulates and the drain voltage collapses. It is also during this period that most drive circuits are simply peak current limit, whether by the driver IC or an external resistor. High peak currents are necessary for fast transitions through this interval, especially when driving large geometry FETs.

Full drain current is flowing at the beginning of the Qgd portion of the Qg curve, and notice that the drain voltage remains high. FET power loss is at its maximum here, and decreases linearly with Vds. A majority of the Qgd charge goes to combat the "Miller" effects as the drain voltage falls from that of its off condition to Vgs, or approximately Vgs(th). The remainder of the charge is used to bring the drain voltage down below that of the gate, decreasing the

effecive gate capacitance over the Qgd interval since there is relatively no change in gate voltage. The important fact, however, is that high peak currents are needed to minimize the FET power loss and transition time.

The remainder of the gate charge brings the gate voltage from VGS (th) to 10 volts. This "excess" charge reduces the FET "ON" resistance to its minimum, and raising the gate voltage above 10 volts has no further effect on reducing the Rds (on). The effective gate capacitance, which is high, can be obtained by dividing the charge input by the change in gate voltage during this region.

Ceff = [Qg - (Qgd+Qgd)] / (10v - VGS (th)) = 40nC/4v = 10nF for the IRFP460

FET DRIVER ICS

In searching for IC's capable of providing the fast transitions and high peak currents required by power MOSFETs, one of the first devices which became popular was the DS0026. While this IC was origionally designed to be dual clock driver for MOS logic, it was capable of supplying up to 1.5 amps as either a source or sink. In addition, it was made with a gold doped, all NPN process which minimizes storage delays, and as a result, offers transition times of approximately 20 nsec. Its disadvantages, however, are high cross conduction currents, as well as requiring excessive supply current when the output is in the low (OFF) state. This leads to higher power dissipation and junction temperature than optimum.

This brings us to newer ICs designed specifically as power MOSFET drivers for switchmode power supply applications. Several factors were taken into consideration while developing the new UC3705 /06 /07 /09 series of high current drivers; the most important of which, was to isolate the high power switching noise from the low level analog signals at the PWM. Seperate supply and return paths at the driver to its signal inputs and power outputs further enhances noise immunity. Additionally, several desireable features including an analog shutdown comparator have been incorporated in the UC3706 and UC3707 devices, whereas the UC3705 and UC3709 drivers are optimized for low cost applications which incorporate this function elsewhere in the design. Each driver features TTL compatible input thresholds, undervoltage lockout, thermal shutdown and low cross-conduction, high speed output circuitry. The corresponding block diagrams and pin assignments are shown in figures 6 thru 9, and followed by the feature selection index.

UC3705 Block Diagram

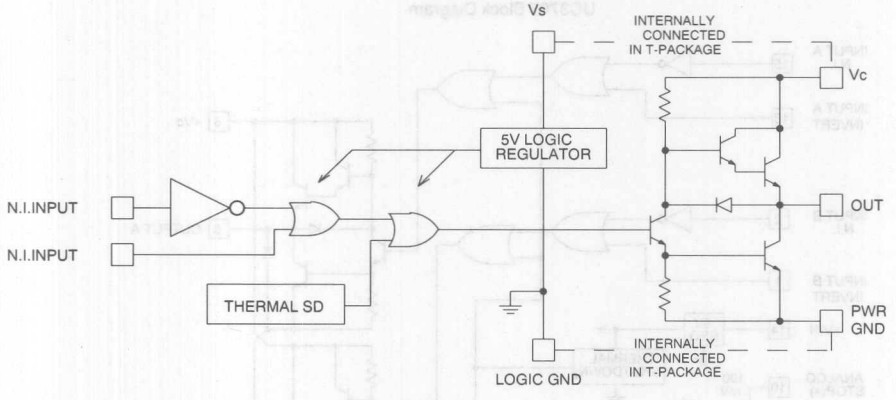


Figure 6

UC3706 Block Diagram

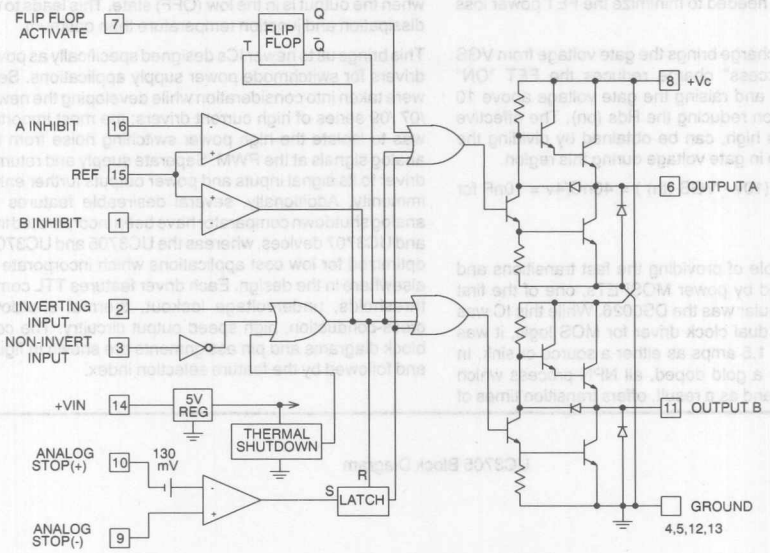


Figure 7

UC3707 Block Diagram

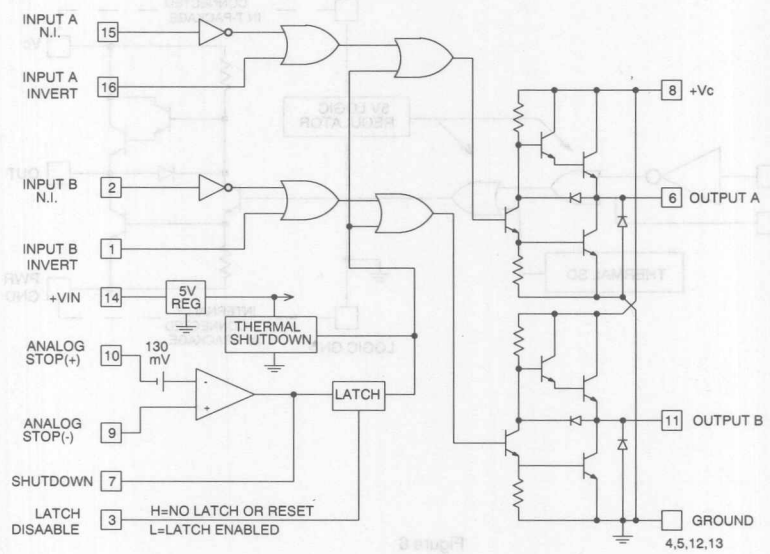
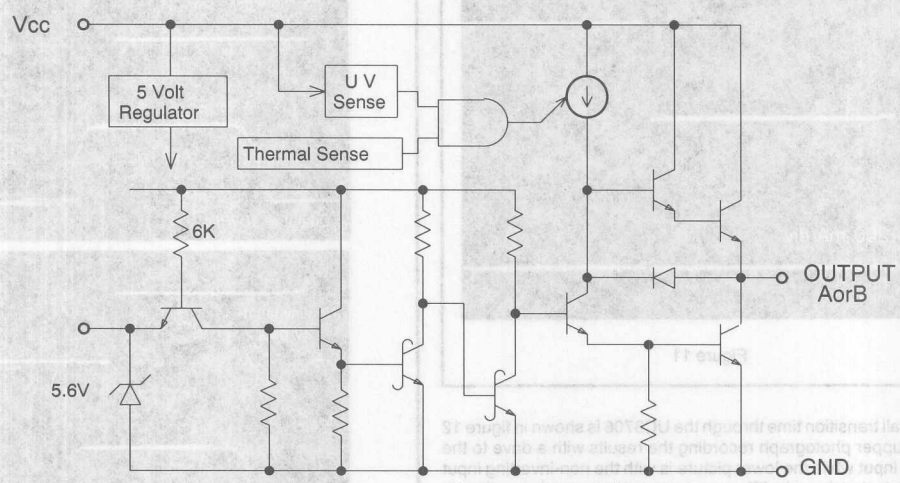


Figure 8

UC3709 Block Diagram



NOTE: One Output Shown

Figure 9

DRIVER FEATURES

- 1.5 Amp Peak Output Current (Per Output)
- 40 Nanosecond Rise & Fall Times into 1NF
- Low Cross Conduction Current Spike
- 5 to 40 Volt Operation
- High Speed Power MOSFET Compatable
- Thermal Shutdown Protection

	DUAL OUTPUTS	INVERTING INPUTS	NON-INVERTING INPUTS	SEPERATE V_C & V_{IN}	SEPERATE PGND & SGND	ANALOG SHUTDOWN	DIGITAL INHIBIT	TOGGLE F/F	LATCH RESET
UC3705		X	X	X	X				
UC3706	X	X	X	X	X	X	X	X	
UC3707	X	X	X	X	X	X	X		X
UC3709	X	X							

1.5 AMP PEAK TOTEM-POLE OUTPUTS

The schematic of the UC3706 output drive circuit is shown in figure 10, which is similar to the other devices in this family. While first appearing as a fairly conventional totem-pole design, the subtleties of this circuit are the slowing of the turn-off of Q3 and the addition of Q4 for rapid turn-off of Q8. The result is shown in figure 11 where it can be seen that while maintaining fast transition times, the cross conduction current spike has been reduced to zero when going low and only 20 nsec with a high transition. This offers negligible increase in internal circuit power dissipation at frequencies in excess of 500KHz.

Typical Output Schematic

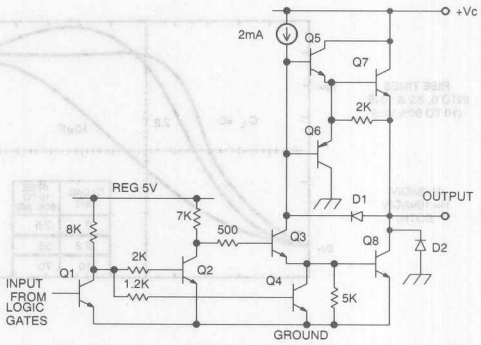


Figure 10

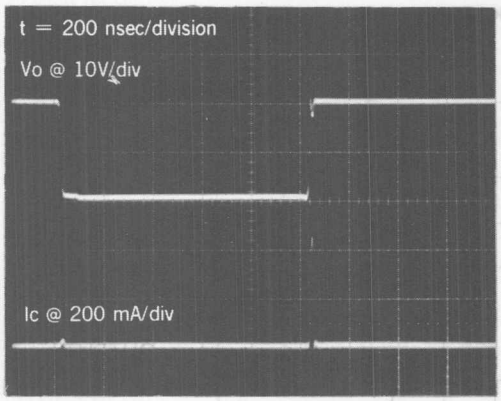


Figure 11

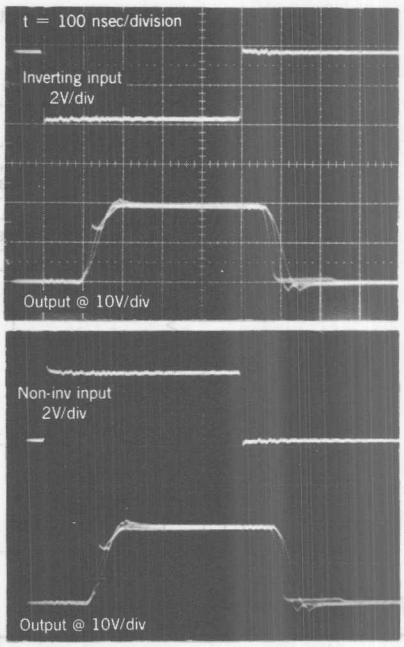
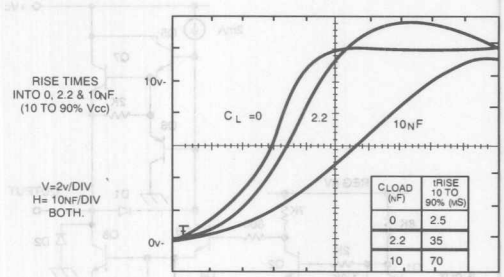


Figure 12

The overall transition time through the UC3706 is shown in figure 12 with the upper photograph recording the results with a drive to the inverting input while the lower picture is with the non-inverting input driven. Note that the only difference in speed between the two inputs is an additional 20 nSec delay in turning off when the non-inverting input is used. Here, and in further discussions note that ON and OFF relate to the driven output switch, i.e., On is with the output HIGH, and vice versa. The shutdown, inhibit and protective functions all force the output LOW when active.

Note that the typical rise and fall times of the output waveform average 20 nsec with no load, 25 nsec with 1 nF, and 35 nsec when the capacitive load is 2.2 nF at room temperature. Multilayer ceramic capacitors are used in this test and located as physically close to the IC output as possible to minimize lead and connection inductance.



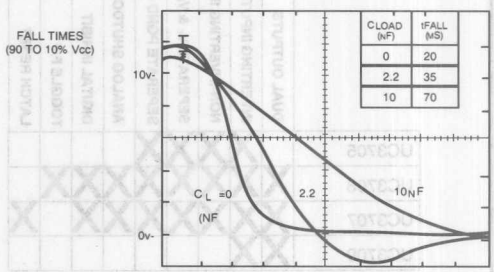


Figure 13

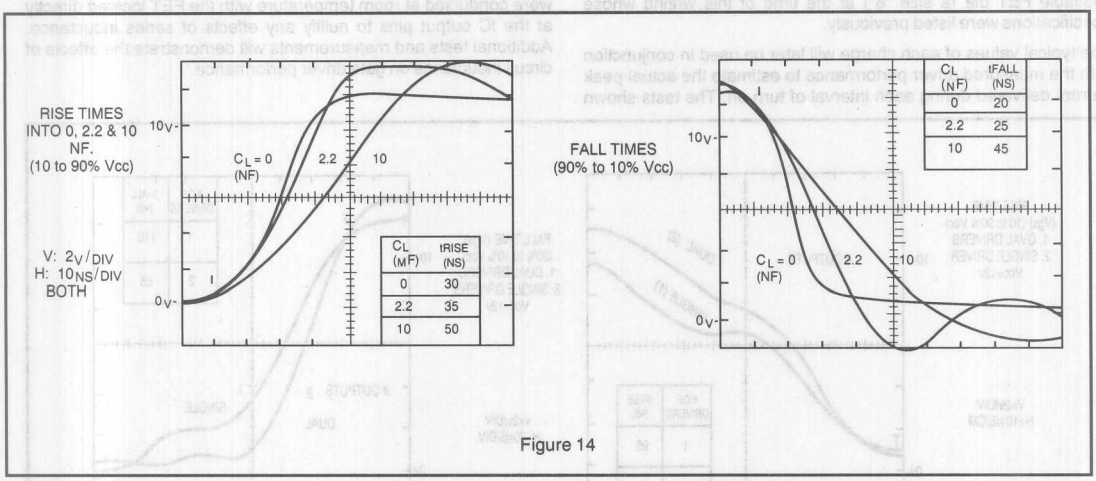


Figure 14

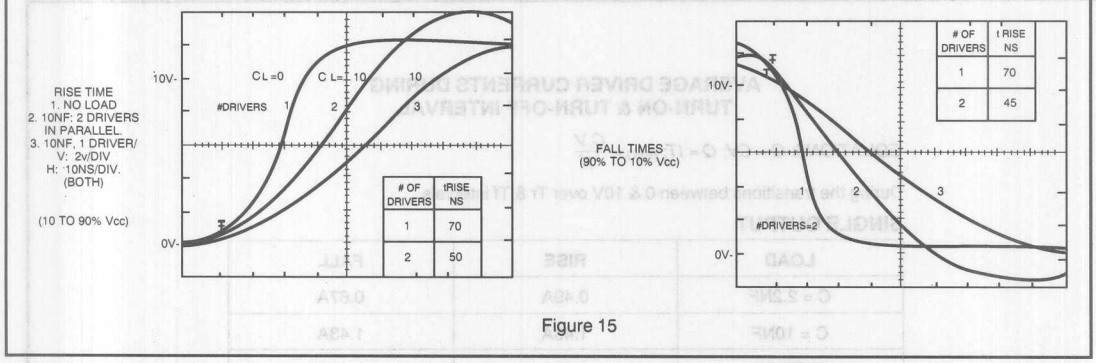


Figure 15

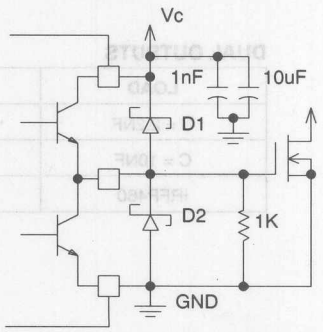
The peak current of each totem-pole output, whether source or sink, is 1.5 amps. However, on dual output versions like the UC3706, UC3707 and UC3709, both of the outputs can be paralled for 3 amp peak currents. In close proximity on the same die, each output virtually shares identical electrical and thermal characteristics. Saturation voltage is high at this current level but falls to under 2V at 500ma per output. Examples of typical switching characteristics are displayed.

It should be noted that while optimized for driving power MOSFET device, the UC3705 /06 /07 /09 ICs perform equally well into bipolar NPN transistors. In a steady-state off condition, the output saturation voltage is less than 0.4 volts as currents to 50 milliamps.

DIRECT COUPLED MOSFET DRIVE

The circuit of figure 17 shows the simplest interface to a power mosfet, direct coupling. In this example, an IRFP460 will be used to demonstrate the typical rise and fall times obtainable with a single 1.5 amp peak totem-pole driver. Further testing will include paralleling both outpus of a dual driver for a 3 amp peak capability. The IRFP460 device was selected, being the largest commercially

POWER MOSFET DRIVE CIRCUIT



D1.D2:UC3611 SCHOTTKY DIODES

Figure 16

available FET die (a size "6") at the time of this writing whose specifications were listed previously.

The typical values of each charge will later be used in conjunction with the measured driver performance to estimate the actual peak current delivered during each interval of turn-on. The tests shown were conducted at room temperature with the FET located directly at the IC output pins to nullify any effects of series inductance. Additional tests and measurements will demonstrate the effects of circuit inductance on gate driver performance.

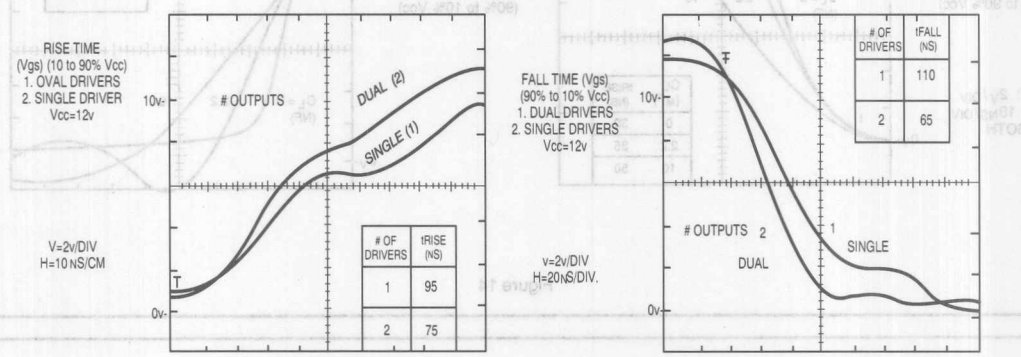


Figure 17

AVERAGE DRIVER CURRENTS DURING TURN-ON & TURN-OFF INTERVAL

EQUATIONS: $Q = CV$; $Q = IT$; $i_{AVG} = \frac{C.V}{T}$

During the transitions between 0 & 10V over Tr & Tf intervals

SINGLE OUTPUT

LOAD	RISE	FALL
C = 2.2NF	0.49A	0.67A
C = 10NF	1.43A	1.43A
IRFP460	1.26A	1.10A

DUAL OUTPUTS

LOAD	RISE	FALL
C = 2.2NF	0.63A	0.88A
C = 10NF	2.0A	2.22A
IRFP460	1.6A	1.85A

While directly connecting the FET gate to the output of the driver is straightforward for testing purposes, it does not represent the "real" application which may include several inches or wire or printed circuit board traces. Here, wiring inductance will sharply degrade the transitions and cause substantial overshoot by ringing with the gate capacitance. Extreme examples of this can cause the gate-to-source voltage to overshoot beyond the specified maximum ratings.

Additionally, negative transitions (below ground) at the deriver output can raise havoc with the internal circuitry, leading to undesireable performance. While this is more of a concern with PWMs, (which use low level analog input signals) it will also detract from the drivers peak performance. Both of these conditions can easily be avoided by Schottky clamping the circuit to the auxiliary supply rails.

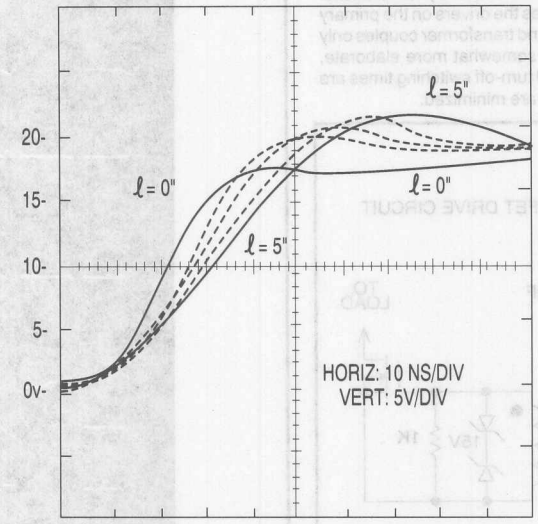


Figure 18

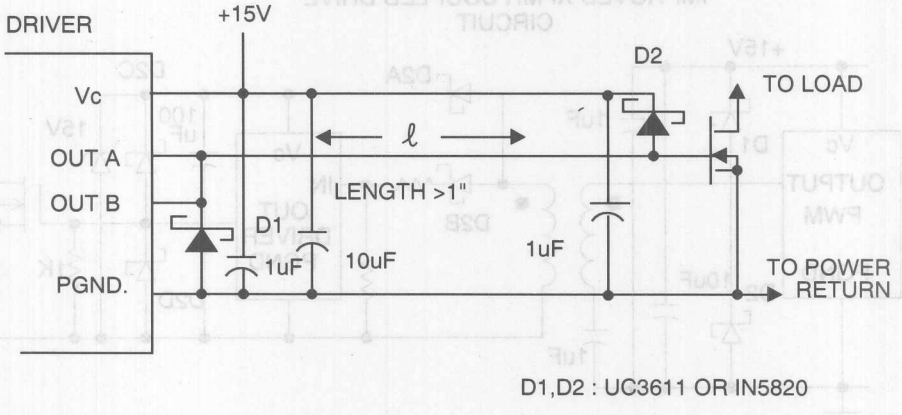
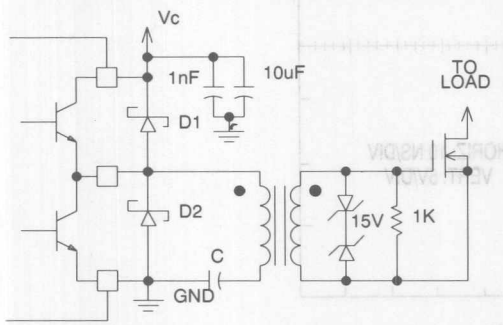


Figure 19

ISOLATED GATE DRIVE

In certain applications, the PWM is referenced to the load or secondary side of the power supply and the gate drive is transformer coupled across the isolation boundary to the power FETs. While this technique may work adequately at low switching frequencies, any series circuit inductance, as shown, will significantly degrade switching speeds and performance as the frequency is increased. An improved version of this circuit locates the drivers on the primary side, as close as possible to the FETs, and transformer couples only the low power input signals. Although somewhat more elaborate, significant improvements in turn-on and turn-off switching times are obtained and the FET switching losses are minimized.

TRANSFORMER COUPLED MOSFET DRIVE CIRCUIT



D1.D2:UC3611 SCHOTTKY DIODE ARRAY

Figure 20

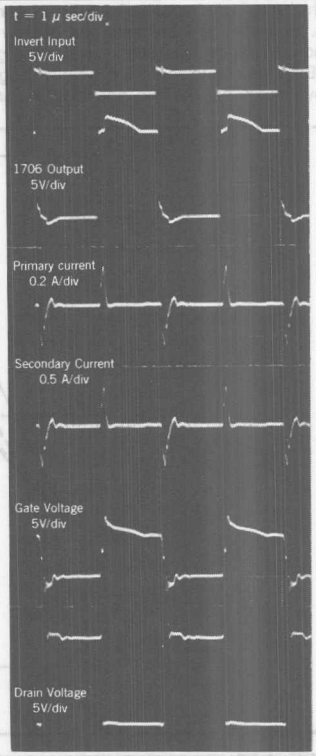


Figure 21

IMPROVED XFMR COUPLED DRIVE CIRCUIT

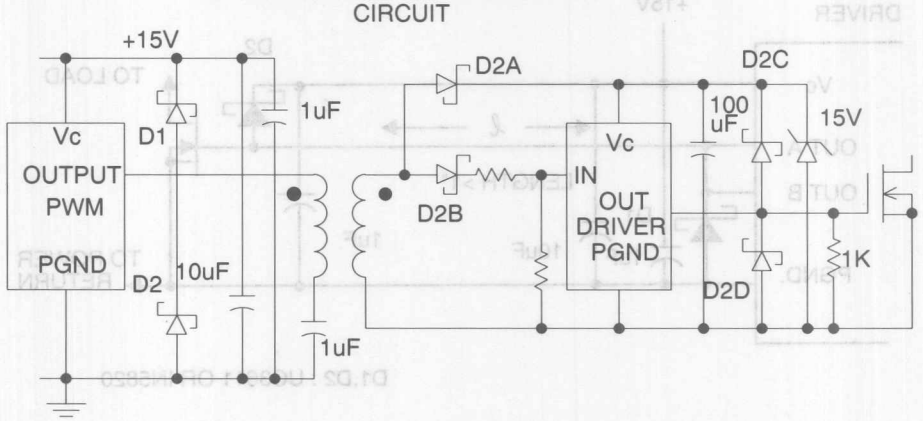


Figure 22

PUSH-PULL TRANSFORMER COUPLING

The totem-pole outputs of the UC3706 can easily be configured for implementing the balanced transformer drive as shown in figure24. Outputs A and B are alternating now as the internal flip-flop is active and the output frequency is halved. Note that when one UC3706 output goes high, the other is held low during the dead time between output pulses. With balanced operation, no coupling capacitor on the primary is necessary since there is no net DC in the primary. Schottky clamp diodes on the primary side and back-to-back zeners on the secondaries are necessary to minimize the overshoot causes by the ringing of the gate capacitance with circuit inductances. Waveforms of all significant points within this circuit are shown.

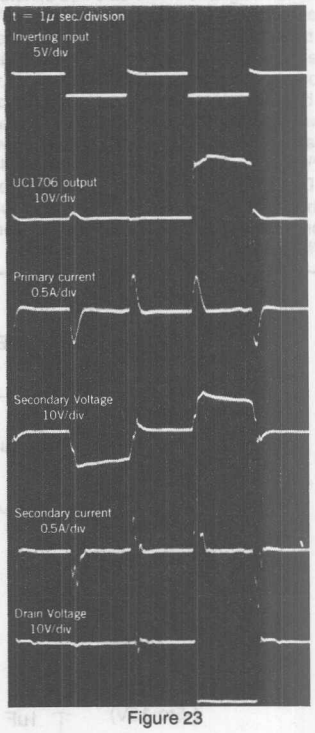


Figure 23

UC 3706 CONVERTS SINGLE OUTPUT PWMS TO HIGH CURRENT PUSH-PULL CONFIGURATION

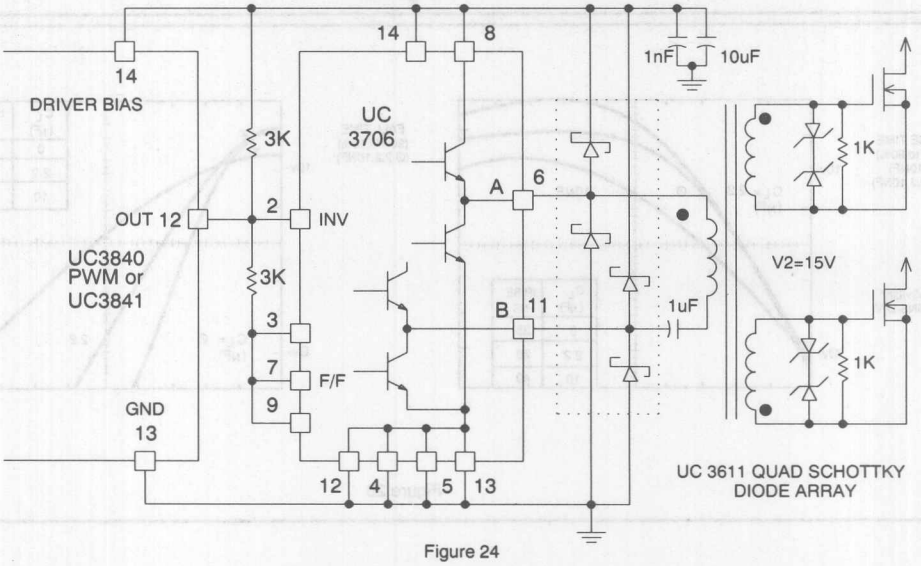


Figure 24

SUPPLYING POWER TO THE DRIVERS

From the block diagrams of figures 6 thru 8, note that the UC3705, UC3706 and UC3707 have two supply terminals, Vin and Vc. These pins can be driven from the same or different voltages and either can range from 5 to 40 volts. Vin drives both the input logic and the current sources providing the pull-up for the outputs. Therefore, Vin can also be used to activate the outputs and no current is drawn from Vc when Vin is low. This is useful in off-line applications where its desireable for the control circuit to have a low start-up current. Several PWM controllers, like the UC1840, UC1841 and the UC1851 feature a Driver Bias output which goes high once the undervoltage lockout threshold is crossed, thus supplying bias to the driver. Adaptations of this technique can be made to work with a variety of other PWMs and control circuits.

USING "SPLIT" SUPPLIES

Many applications utilize a negative voltage rail in the drive circuit to guarantee complete turn-off of power MOSFETs, especially those with low gate threshold voltages, typical of "logic level" input devices. This is easy to implement with any of the UC3705 thru UC3709 drivers by offsetting the input signals with a zener diode equal in voltage to the negative supply, Vee. Although referenced at the driver IC to the Vee rail, these inputs are offset by an equal amount to the PWM controller, simulating a ground referenced input. This technique also offers moderate improvements in FET switching speeds at the penalty of slightly increased effective delay times from the driver inputs. The end results are listed below, which may be beneficial in applications where a tailored gate drive is required to alter the MOSFET switching charcteristics.

POWER MOSFET DRIVE CIRCUIT
USING NEGATIVE BIAS VOLTOGE AND LEVEL SHIFTING
TO GROUND REFERENCED PWMS

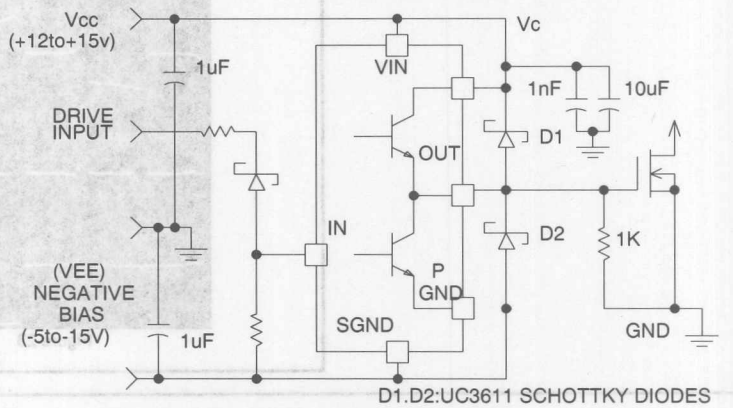


Figure 25

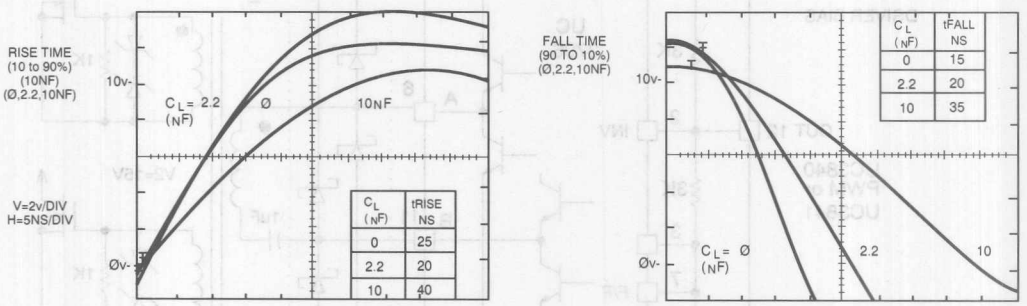


Figure 26

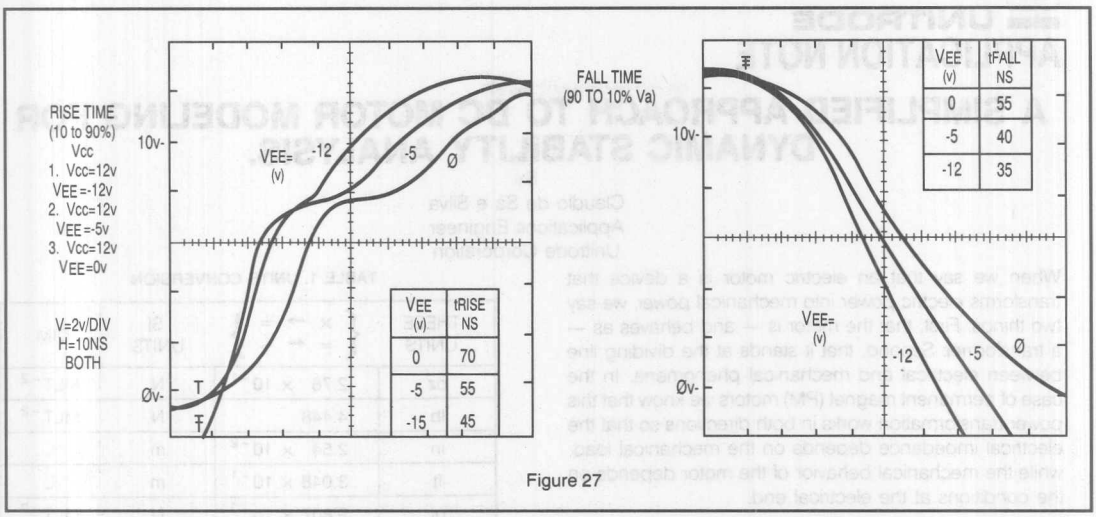


Figure 27

VEE (V)	td Rise to '0" V (NS)	T Rise 0-10V (NS)	Td Fall to begin (NS)	T Fall 10-0V (NS)I	T Delay total (NS)	Tr & Tf total (NS)	T Total tr+tf+trd (NS)
0	56	50	50	45	106	95	201
-5	70	42	50	33	120	75	195
-10	86	34	50	29	136	63	199
-12	93	32	50	28	143	60	203
-15	100	30	50	27	150	57	207

VEE (V)	Delay trd+tfd (NS)	Transition Times tr+tf (NS)
0	Minimum (106NS)	Maximum (95NS)
-15V	Maximum (143NS)	Minimum (60NS)

VEE (V)	Rise	Fall
0	2.4A	2.67A
-5	2.86A	3.64A
-10	3.53A	4.14A
-15	4.0A	4.4A

SUMMARY

This paper has presented an understanding of the dynamics of high speed power MOSFET switching in an attempt to define the optimum gate drive requirements to meet specific applications. The need for high peak gate currents with controlled rise times has led to the development of several integrated circuits aimed towards achieving these goals. The UC3705, UC3706, UC3707 and UC3709 drivers provide high speed response, 1.5 amps of peak current per output and ease the implementing of either direct or transformer coupled drive to a broad range of power MOSFETs. With these new devices, one more specialized function has been developed to further aid the power supply designer simplify his tasks and enhance power MOSFET switching characteristics.

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UNITRODE
APPLICATION NOTE

A SIMPLIFIED APPROACH TO DC MOTOR MODELING FOR DYNAMIC STABILITY ANALYSIS.

By
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When we say that an electric motor is a device that transforms electric power into mechanical power, we say two things. First, that the motor is — and behaves as — a transformer. Second, that it stands at the dividing line between electrical and mechanical phenomena. In the case of permanent magnet (PM) motors we know that this power transformation works in both directions so that the electrical impedance depends on the mechanical load, while the mechanical behavior of the motor depends on the conditions at the electrical end.

This being the case, it should be possible to represent a motor's mechanical load, on the electrical side, by a set of familiar electrical components such as capacitors or resistors.

CHOOSING A UNIT SYSTEM

Before we get started, let us consider for a moment the system of measurement units that we have chosen.

The metric system of units has undergone a number of changes in its history, of which the latest is the SI (Systeme International d'Unites). This system has become popular in most of the industrialized world, largely because it is a coherent system, in which the product or quotient of two or more units is the unit of the resulting quantity. It will be seen here that certain simplifications result from using this form of the metric system.

In the SI system, force is measured in Newtons (N) and distance in meters (m). Consequently, the units of torque are Nm (see Conversion Table). If a motor shaft rotates at an angular velocity of ω_M radians per second, with torque T_M, the mechanical power output will be equal to the product T_M and ω_M and the units will be watts if T_M is in Nm.

Motor manufacturers usually specify a torque constant (K_T) and a voltage constant (K_V) for their motors. These constants have different values when the torque and speed are measured in English units, but they have the same numerical value when SI units are used. This becomes obvious when you consider that the electrical input power must be equal to the mechanical output power:

(1) $V_A I_A = T_M \omega_M$ (watts)

(2) $\frac{V_A}{\omega_M} = \frac{T_M}{I_A} = K_{TV}$

*where V_A is the internally generated armature voltage, or back emf, and I_A is the armature current. (See Fig. 1 for definition of motor terms.)

TABLE 1. UNITS CONVERSION

THESE UNITS	$\{ \times \rightarrow = \atop = \leftarrow \div \}$	SI UNITS	DIM.
oz	2.78×10^{-1}	N	MLT^{-2}
lb	4.448	N	MLT^{-2}
in	2.54×10^{-2}	m	L
ft	3.048×10^{-1}	m	L
gf	9.807×10^{-3}	N	MLT^{-2}
g cm^2	10^{-7}	Nm sec^2	ML^2
ft lb sec^2	1.356	Nm sec^2	ML^2
oz in sec^2	7.063×10^{-3}	Nm sec^2	ML^2
ft lb	1.356	Nm	ML^2T^{-2}
oz in	7.063×10^{-3}	Nm	ML^2T^{-2}

NOTE. The dimensions are M (mass), L (length), and T (time). The gram (g) is a unit of mass, and the gram-force (gf) is a unit of force. The pound (lb) and the ounce (oz) are included as units of force only.

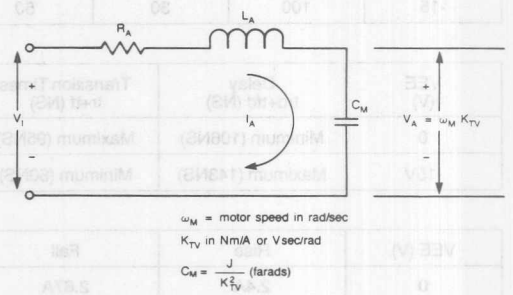


FIGURE 1. THIS SERIES RLC CIRCUIT IS AN EXCELLENT MODEL OF A DC MOTOR LOADED WITH AN ESSENTIALLY INERTIAL LOAD. HERE, J IS THE TOTAL MOMENT OF INERTIA, INCLUDING THE ROTOR'S J_M.

If we do the same thing with the familiar electrical transformer, we get the turns ratio:

(3) $V_1 I_1 = V_2 I_2$ (watts)

(4) $\frac{V_1}{V_2} = \frac{I_2}{I_1} = \frac{N_1}{N_2}$

Thus, the non-dimensional turns ratio N_1/N_2 is analogous to the dimensional torque (or voltage) constant K_{TV}. Furthermore, equations (2) and (4) give us a clear hint that the angular velocity (ω_M) is analogous to voltage, while the torque (T_M) is analogous to current.

The units of K_{TV} may be either Nm/A, or V sec/rad. Thus, specifying both K_T and K_V for a motor is like measuring and specifying both the voltage ratio and the current ratio of a transformer, and can only make sense where redundancy is required.

THE MOTOR AS A TRANSFORMER

We have established an analogy between K_{TV} and a transformer's turns ratio; between angular velocity and voltage; and between torque and current. If the motor behaves as a transformer, then we would expect to find the square of K_{TV} involved in something analogous to impedance transformation.

Suppose we apply a constant current I_A to the armature of a motor whose load is its own moment of inertia J_M (Nm sec^2). We know that according to Newton's law for rotating objects,

(5) $T_M = J_M \alpha_M$

where α_M is the angular acceleration $d\omega_M/dt$.

Since $T_M = I_A K_{TV}$ (Eq. 2)

$$(6)\quad I_A K_{TV} = J_M \frac{d\omega_M}{dt}$$

Furthermore, also from Eq. 2,

$$(7)\quad \omega_M = \frac{V_A}{K_{TV}}$$

so that

$$(8)\quad I_A = \frac{J_M}{K_{TV}^2} \cdot \frac{dV_A}{dt}$$

Equation 6 has a familiar form, and we recognize at once the quantity J_M/K_{TV}^2 as a capacitor. It follows that the motor "reflects" a moment of inertia J_M back to the electrical primary as a capacitor of J_M/K_{TV}^2 farads.

A neat way to check this result is to equate the energy stored kinetically in J_M with the electrical energy stored in a capacitor C_M:

$$(9)\quad \tfrac{1}{2} C_M V_A^2 = \tfrac{1}{2} J_M \omega_M^2$$

$$(10)\quad C_M = J_M \left(\frac{\omega_M}{V_A}\right)^2$$

Since $\frac{\omega_M}{V_A} = \frac{1}{K_{TV}}$,

$$(11)\quad C_M = \frac{J_M}{K_{TV}^2} \text{ (farads)}$$

Similarly, a torsional spring with spring constant K_S (Nm/rad) is reflected as an inductance of K_{TV}^2/K_S henries. And a viscous damping component B (Nm sec/rad) appears as a resistor of K_{TV}^2/B ohms.

A MOTOR MODEL

Once we can represent the mechanical load by means of electric elements, we can draw an equivalent circuit of the motor and its mechanical load. The armature has a finite resistance R_A and an inductance L_A, through which the torque-generating current I_A must flow. These components are not negligible, and must be included. An inertially loaded motor can be represented as in Fig. 1, where the moment of inertia J is the sum of the load's J_L and the rotor's J_M.

It turns out that in practice, the moment of inertia that the motor must work against — or with, depending on how you look at it — is by far the most important component of the mechanical load. A frictional component also exists, to be sure, but because it is largely independent of speed, it would be represented electrically as a constant current source, which could not affect the dynamic behavior of the motor. And since a torsional spring — which would affect it — is rarely found in practice, we will concentrate on the inertial problem only.

MEASURING THE COMPONENTS

The measurement of R_A and L_A is not difficult. A good ohmmeter will get you R_A, and you can measure the electrical time constant τ_E to calculate L_A:

$$(12)\quad L_A = \tau_E R_A$$

Just make sure that the rotor remains stationary during these measurements.

In order to determine the value of the capacitor, C_M, we will need to measure the shaft speed. If the motor being measured is a brushless DC motor, we can use the signal from one of the Hall effect devices as a tachometer. If the Hall frequency is f_H, and the number of rotor poles is P, the angular velocity ω_M is

$$(13)\quad \omega_M = \frac{4\pi f_H}{P} \text{ (rad/sec)}$$

With other motors you will need a strobe-light or some other means to measure speed.

A good way to measure C_M is through a measurement of the mechanical time constant T_M. We do this by driving the motor with a constant voltage driver and measuring the time it takes to accelerate from zero speed to 63% of the highest speed achievable at the voltage used. To set a safe limit to the starting current we can reduce the supply voltage or add a series resistor with the motor, or both. The set-up is shown in Fig. 2. Note that the armature resistance R_A is already known, and we add resistors R_B, if needed, to limit the armature current I_A to a value that is safe for both driver and motor.

The first thing to do is let the motor run freely and measure ω_{MAX} and I_{MAX}, and use these values to calculate the armature voltage V_{MAX}:

$$(14)\quad V_{MAX} = V_{CC} - V_{SAT} - I_{MAX}(R_A + R_B)$$

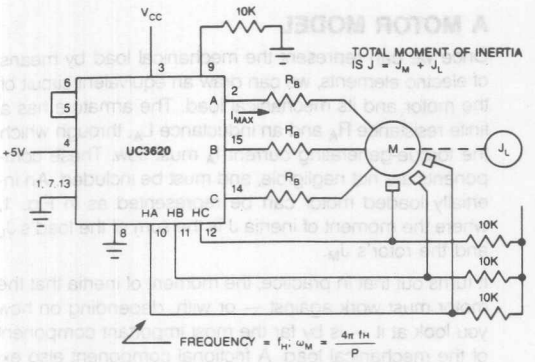


FIGURE 2. SET-UP FOR MEASUREMENT OF $C_M = J/K_{TV}$ OF A 3-PHASE BRUSHLESS DC MOTOR WITH INERTIAL LOAD J1. THE MOTOR VOLTAGE $V_M = V_{CC} - V_{SAT}$, WHERE V_{SAT} IS THE OUTPUT SATURATION VOLTAGE.

Here V_{CC} is the supply voltage, V_{SAT} is the saturation voltage of the driving circuit, and I_{MAX} is the current drawn by the unloaded motor at maximum speed.

Thus we can calculate

$$(15)\quad K_{TV} = \frac{V_{MAX}}{\omega_{MAX}} \quad \text{(Vsec/rad)}$$

Next, set the oscilloscope time scale to that you can easily read a Hall frequency equal to 63% of ω_{MAX}, so that:

$$(16)\quad \omega_M = 0.63\ \omega_{MAX}$$

By holding and releasing the motor shaft, take several readings of the time T_M required to accelerate from zero to ω_M. Remember that these readings are taken "on the fly," since the motor continues to accelerate towards the maximum speed ω_{MAX}. Having obtained a good value of T_M you can now calculate

$$(17)\quad C_M = \frac{T_M}{(R_A + R_B)} \quad \text{(farads)}$$

This completes the RLC equivalent circuit, If the value of J_M is also required, it too can be calculated:

$$(18)\quad J_M = C_M K_{TV}^2$$

THE MOTOR'S TRANSFER-FUNCTION

In the circuit of Fig. 1, V_1 is the voltage applied to the motor leads, and V_A is the actual armature voltage, or back EMF. This latter voltage is equal to $\omega_M K_{TV}$, as we have seen, so that if we want to derive an expression relating the speed to the applied voltage, we can write:

$$(19)\quad \frac{\omega_M}{V_1} = \frac{1}{K_{TV}} \cdot \frac{V_A}{V_1} \quad \text{(rad/Vsec)}$$

If V_1 is a constant voltage, the speed ω_M will also be constant. This is clear from the circuit of Fig. 1 as well as from our experience with motors. If, however, V_1 varies sinusoidaly at some frequency f, the speed ω_M will vary similarly, but the amplitude and phase will in general be different from those of the driving function. This fact is very important if we are to include the motor in a feedback loop, because the motor's contribution to the overall loop gain and phase shift is an important factor in determining stability. The motor's transfer function — i.e. Eq. 19 expressed as a function of frequency — gives us a precise description of how the amplitude and phase behave at different frequencies. To do this, we use the variable $j\omega$, where $j = \sqrt{-1}$, and $\omega = 2\pi f$.

$$(20)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{(j\omega C_m)^{-1}}{j\omega^2 L_A C_M + j\omega R_A C_M + 1}$$

$$(21)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{1}{(j\omega)^2 L_A C_M + j\omega R_A C_M + 1}$$

$$(22)\quad L_A C_M = \frac{1}{\omega_n^2}$$

where ω_n is the natural frequency of the circuit.

$$(23)\quad R_A C_M = \frac{R_A C_M L_A}{L_A} = \frac{R_A}{\omega_n^2 L_A} = \frac{1}{Q\omega_n}$$

since the circuit Q is

$$Q = \frac{\omega_n L_A}{R_A}.$$

Therefore,

$$(24)\quad \frac{V_A(j\omega)}{V_1(j\omega)} = \frac{1}{\left(\frac{j\omega}{\omega_n}\right)^2 + \frac{j\omega}{Q\omega_n} + 1}$$

Furthermore, using Eq. 19,

$$(25)\quad \frac{\omega_M(j\omega)}{V_1(j\omega)} = \left(\frac{1}{K_{TV}}\right) \cdot \frac{1}{\left(\frac{j\omega}{\omega_n}\right)^2 + \frac{j\omega}{Q\omega_n} + 1}$$

Since we know the values of K_{TV}, ω_n and Q, we can calculate the magnitude and phase angle of Eq. 25 for various values of $j\omega$. For a given $\omega = \omega_1$, Eq. 25 can be evaluated into a complex number $A_1 + jB_1$, whose angle is,

$$(26)\quad \theta_1 = \tan^{-1}\frac{B_1}{A_1}$$

and whose magnitude can be expressed in decibels as follows:

$$(27)\quad M_1 = 20 \log_{10} \sqrt{A_1^2 + B_1^2}$$

A plot of these quantities, using a logarithmic frequency scale, is called a Bode plot, and can be a handy tool in understanding how the device will affect the final loop performance.

A DISC - DRIVE EXAMPLE

A small three phase brushless DC motor, measured as above, has the following characteristics:

K_{TV} = 0.015 Nm/A, or Vsec/rad.
R_A = 2.5 ohm
L_A = 0.002 Hy
J = 0.001 Nm sec_2

The J value was measured with three magnetic discs mounted, and represents the actual value required for the application. Using Eq. 11.

$$(28)\quad C_M = \frac{J}{K_{TV}^2} = \frac{.001}{(0.015)^2} = 4.44 \text{ fd}$$

This may seem like an unusually large value for a capacitor, but it simply reflects the large amounts of kinetic energy that can be stored in the included inertia.

From Eq. 22

$$(29)\quad \omega_n = \frac{1}{\sqrt{L_A C_M}} = \frac{1}{\sqrt{0.002 \times 4.44}}$$

$$= 10.61 \text{ rad/sec}$$

From Eq. 23

$$(30)\quad Q = \frac{\omega_n L_A}{R_A} = \frac{10.61 \times 0.002}{2.5} = 0.0085$$

(The quality factor Q has no units). The motor transfer function, given in Eq. 25, is

$$(31)\quad \frac{\omega_M(j\omega)}{V_1(j\omega)} = \frac{66.67}{\left(\frac{j\omega}{10.61}\right)^2 + \frac{j\omega}{0.09} + 1} \text{ (rad/Vsec)}$$

A calculator that is pre-programed to operate with complex numbers (HP 28C, for example, or 15C) makes the evaluation, of this equation an easy task. With the 28C you can set up a USER routine called BODE, as follows:

<<DEG DUP ABS LOG 20 X SWAP ARG>>

This will convert a complex number x + jy into 20 log $\sqrt{x^2+y^2}$ at level 2, and arc tan (y/x) at level 1. Table 2 shows a list of several such computations of Eq. 31:

At ω = 0, the gain is simply 66.67 rad/Vsec. As ω increases from zero up, the gain decreases as shown in the GAIN column of Table 2. For our Bode plot, we want to show the gain relative to the initial, or DC, gain. Therefore, we subtract 66.67db from each gain value in Table 2 and plot the result. This is the same as plotting only the function

$$(32)\quad G(j\omega) = \frac{1}{\left(\frac{j\omega}{10.61}\right)^2 + \frac{j\omega}{0.09} + 1}$$

which should be compared with Eq. 31. The results are shown in Fig. 3.

TABLE 2. CALCULATED VALUES OF EQUATION 31.

ω (rad/sec)	$\frac{\omega_M(j\omega)}{V_1(j\omega)}$	GAIN (db)	PHASE (deg)
0.01	65.9 − j 7.32	36.4	−6.3
0.03	60 − j 20	36.0	−18.4
0.1	29.8 − j 33.2	33.0	−48.0
0.3	5.5 − j 18.4	25.7	−73.3
1.0	0.53 − j 5.95	15.5	−84.9
3.0	0.06 − j 2.00	6.0	−88.4
10.0	0 − j 0.60	−4.4	−89.9
30.0	-4.2×10^{-3} − j 0.20	−14.0	−91.2
100	-4.7×10^{-3} − j 0.06	−24.5	−94.5
300	-4.5×10^{-3} − j 0.02	−34.2	−103.5
1000	$-2.9 \times 10^{-3} - j\, 3.7 \times 10^{-3}$	−46.6	−128.6
3000	$-7.1 \times 10^{-3} - j\, 3 \times 10^{-4}$	−62.3	−157.4

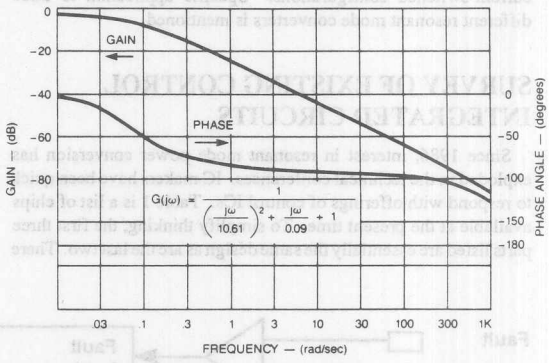


FIGURE 3. BODE PLOT OF MOTOR DATA IN EXAMPLE.

Note that up to about 100 rad/sec (15.9 Hz) the phase lag barely exceeds 90 degrees. The first pole occurs at ω = 0.09 rad/sec, at which point the phase lag is 45 degrees. The second pole, widely separated from the first in this case, occurs at a frequency in excess of 1000 rad/sec, as we can see from the further bend in the phase curve. The gain, which was drooping at a rate of −20db per decade below 100 rad/sec, now begins to bend towards a steeper droop of 40db/dec after the second pole is reached. At very high frequencies, the phase lag will reach 180 degrees.

Used in a speed control feedback loop, this motor will perform well provided that the user takes this gain and phase behavior into account. This is done by incorporating the motor transfer function into the overall loop equation, which will include other components. One's understanding of the motor's behavior improves with this type of analysis, which makes comparisons between different motors more clear and articulate.

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APPLICATION NOTE

A NEW FAMILY OF INTEGRATED CIRCUITS CONTROLS RESONANT MODE POWER CONVERTERS

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ABSTRACT

A new family of integrated circuits is introduced. Devices from this family implement the necessary architecture to control a broad range of resonant mode converters. Key features in the areas of switch timing, fault management, and soft-start technique are unique to this family. Individual devices are customized to handle off-line or DC to DC, single-ended or dual-switch, zero-voltage-or-current-switched configurations. Specific application to three different resonant mode converters is mentioned.

SURVEY OF EXISTING CONTROL INTEGRATED CIRCUITS

Since 1986, interest in resonant mode power conversion has exploded in the technical conferences. IC makers have been quick to respond with offerings of control ICs. Table 1 is a list of chips available at the present time. To simplify thinking, the first three parts listed are essentially the same design as are the last two. There are significant differences in features and performance levels between the three groups. However, a common operational philosophy is shared by all: fixed-pulse-width variable-frequency. This approach has been applied to zero-current-switched (ZCS), quasi-resonant mode converters with reported success.

Table 1. List of Resonant Mode Control ICs

LD405
GP605
CS3805
- - - - - -
UC3860
- - - - - -
MC34066
CS360

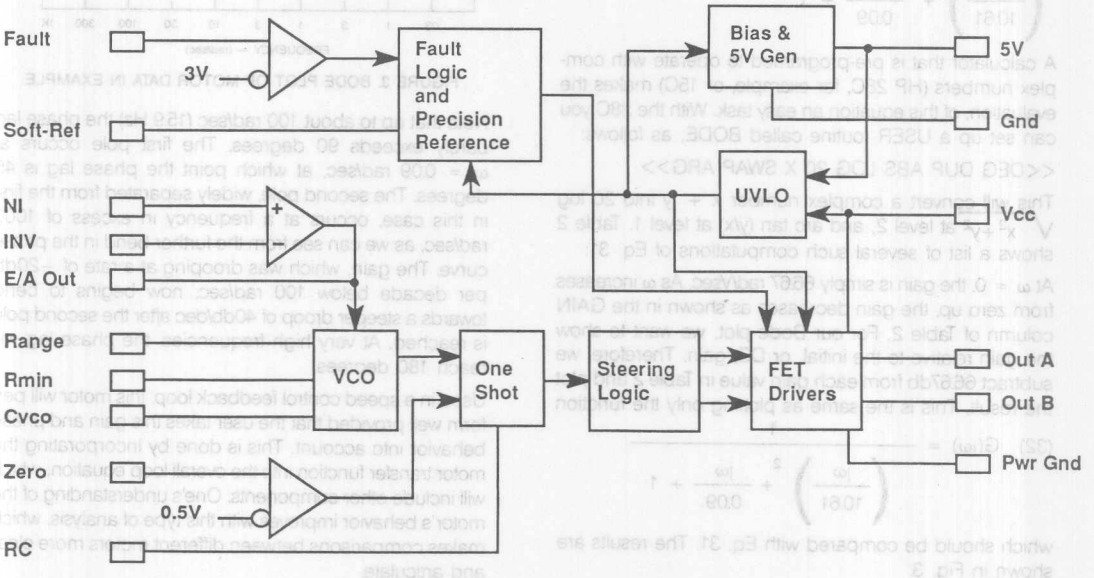


Figure 1. Controller Block Diagram

NEW FAMILY OF RESONANT MODE CONTROL INTEGRATED CIRCUITS

As the discipline is maturing, the advantage of some feature changes has become apparent. Versatility to control both ZCS and zero-voltage-switched (ZVS) converters is needed. The ability to control proper switch times (on or off) with changing line, load, or component values is needed. To address these needs, a family of controllers based on a common silicon die has been developed. Three members of the family, the UC1861, UC1864, and UC1865 will be covered in detail.

The common block diagram of the family is illustrated in figure 1. These parts feature an error amplifier (E/A), voltage controlled oscillator (VCO), one shot timing generator with a zero wave-crossing detection comparator, steering logic to two output drivers, a 5V bias generator, and under voltage lockout (UVLO). A latched fault management scheme provides soft start, restart delay, and a precision reference.

Die options can be produced that give different UVLO levels, as well as different output properties. There are two UVLO options. The first, suited for off-line operation has thresholds of 16 and 10V. While UVLO is active, Icc is less than 0.3mA. The other option is 8 and 7V, to accommodate lower input voltage DC/DC converters.

The flavor of the outputs required by different resonant mode topologies requires the steering logic to be configured specially for each application. The basic options that can be built allow for single or dual switch drive, and controlled on or off times. Zero-current-switching applications require controlled switch on times while zero-voltage-switching applications require controlled switch off times. Figure 2 shows these options.

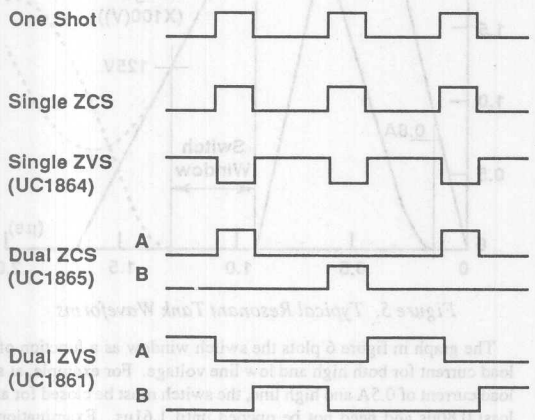


Figure 2. Output Drive For Different Converters

Table 2 details the options implemented in the 1861, '64, and '65. Other options can be built from the same die.

Table 2. Implemented Options in the 1861, '64, '65.

Device	UVLO Vth	Outputs	Zero-(?)-Switching
UC1861	16/10V	Dual	Voltage
UC1864	8/7V	Single	Voltage
UC1865	16/10V	Dual	Current

PRIMARY CONTROL BLOCKS

The fundamental control blocks essential for a majority of resonant mode converters are an error amplifier, VCO, one shot timing generator, and output stage to drive power mosfets.

ERROR AMP & VOLTAGE CONTROLLED OSCILLATOR

Figure 3 details the E/A and VCO. The E/A output directly controls the VCO via the Irange generator. The VCO has inputs for two resistors, R_{ange} and R_{min}, and one capacitor, C_{vco}. R_{min} and C_{vco} determine minimum frequency.

$$F_{min} = \frac{3.6}{(R_{min} * C_{vco})} \quad (1)$$

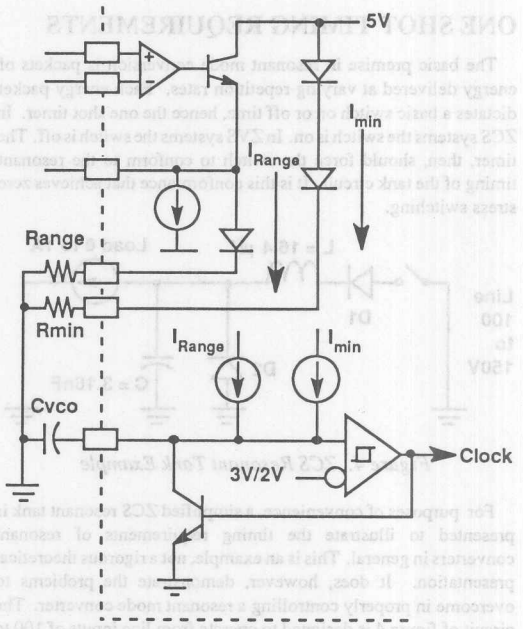


Figure 3. Error Amplifier and Voltage Controlled Oscillator

When the output of the E/A is less than or equal to one diode drop above ground, the VCO operates at minimum frequency. The E/A output can go as high as one diode drop below 5V. When at this potential, the VCO frequency is at its maximum.

$$F_{max} = \frac{3.6}{(R_{ange} \| R_{min}) * C_{vco}} \quad (2)$$

Usable maximum frequency tops out around 1.5MHz. The Frequency range is the difference in equations 2 and 1.

$$\Delta F = \frac{3.6}{R_{ange} * C_{vco}} \quad (3)$$

Since the nominal E/A output swing is approximately 3.6V for full variation in VCO frequency, the gain of the VCO block is

$$dF/dV = \frac{1}{R_{ange} * C_{vco}} \quad (4)$$

In ZCS power supplies, an increase in frequency will correspond to an increase in the converter's output voltage. For these applications the E/A non-inverting input is connected to a reference voltage while the output voltage sense is fed back to the inverting input. For ZVS power supplies, a decrease in frequency corresponds to an increase in output voltage. For these systems, the inputs to the E/A are exchanged.

The common mode range of the E/A is from zero to 6V. This feature allows zero volts to be a valid reference voltage applied to the E/A. Soft start, covered later, takes advantage of this feature.

ONE SHOT TIMING REQUIREMENTS

The basic premise in resonant mode conversion is packets of energy delivered at varying repetition rates. Each energy packet dictates a basic switch on or off time, hence the one shot timer. In ZCS systems the switch is on. In ZVS systems the switch is off. The timer, then, should force the switch to conform to the resonant timing of the tank circuit. It is this conformance that achieves zero stress switching.

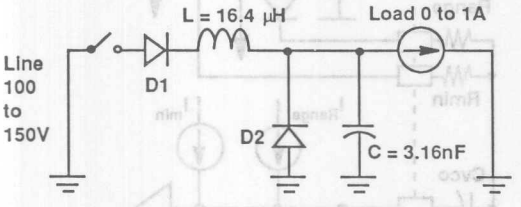


Figure 4. ZCS Resonant Tank Example

For purposes of convenience, a simplified ZCS resonant tank is presented to illustrate the timing requirements of resonant converters in general. This is an example, not a rigorous theoretical presentation. It does, however, demonstrate the problems to overcome in properly controlling a resonant mode converter. The circuit of figure 4 is designed to operate from line inputs of 100 to 150V and 0 to 1A load current. The tank frequency is arbitrarily selected to be 700kHz. A reasonable first guess for tank impedance is determined by

$$Z_o = \frac{V_{lowline}}{I_{max} * 1.386} \quad (5)$$
$$= 72 \text{ ohms.}$$

From the equations governing resonant tank natural frequency and impedance, L and C can be calculated.

$$F_o = \frac{1}{2\pi\sqrt{LC}} = 700\text{kHz} \quad (6)$$

$$Z_o = \sqrt{\frac{L}{C}} = 72 \text{ ohms} \quad (7)$$

$$L = \frac{Z_o}{2\pi F_o} = 16.4\,\mu\text{H} \quad (8)$$

$$C = \frac{1}{2\pi Z_o F_o} = 3.16\text{nF} \quad (9)$$

Figure 5 shows the pertinent current and voltage waveforms for the case of 125V input and 0.8A output. When the switch closes at zero time, the current starts to build linearly. Once the current reaches 0.8A, then load current is completely supplied through the inductor and D2 carries no current. At this point in time the L and C resonate together until inductor current returns to zero. At this time the switch is allowed to turn off, but it doesn't necessarily have to. D1 prevents reverse current in the switch. It isn't necessary to open the switch until the capacitor voltage decays to line voltage. It is acceptable to open the switch any time during this "switch window". If it is opened too soon, the circuit will suffer severe switching losses. If it is not opened, the tank will resume resonating, as shown by the dashed curves. If the switch is opened later than the switch window, not only will the circuit suffer switching losses, but the transfer function becomes overly complex.

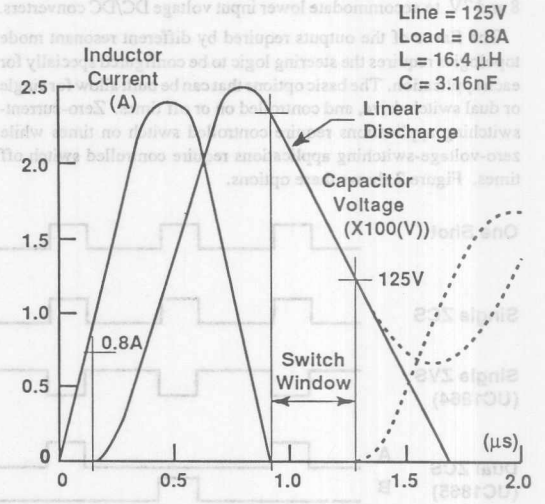


Figure 5. Typical Resonant Tank Waveforms

The graph in figure 6 plots the switch window as a function of load current for both high and low line voltage. For example, at a load current of 0.5A and high line, the switch must be closed for at least 0.80us and need not be opened until 1.61us. Examination reveals the most stringent switch window, 1.03 to 1.21us, occurs at low line and full load. Furthermore, this window is a subset of all other windows. This might lead to choosing a fixed on-time of 1.12us under the assumption that it is relatively easy to build a fixed time one-shot circuit with total variations less than +/-8%. However, further consideration will lead to a different conclusion.

In order to insure that the example in question can be produced, the variations of the resonant components and the possibility of output overload must also be examined. This example continues by assuming total variations for the capacitor are under 10% while under 20% for the inductor. A 20% overload is also allowed.

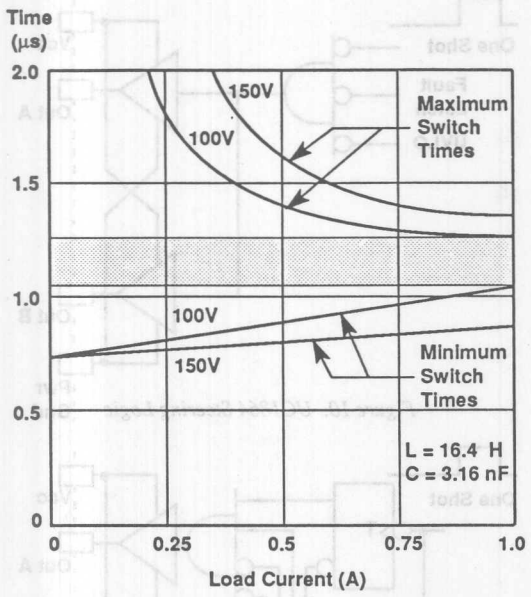


Figure 6. Minimum/Maximum Switch Time vs Load Current

Figure 7 shows the valid switch windows at 1.2A and 100V for nominal component values as well as the four tolerance corners. Several observations can be made. Firstly, the window for the case of +20% inductor and -10% capacitor variations has zero tolerance.

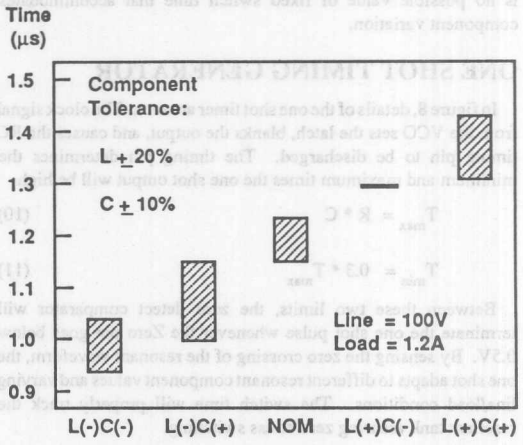


Figure 7. Switch Window vs Component Value

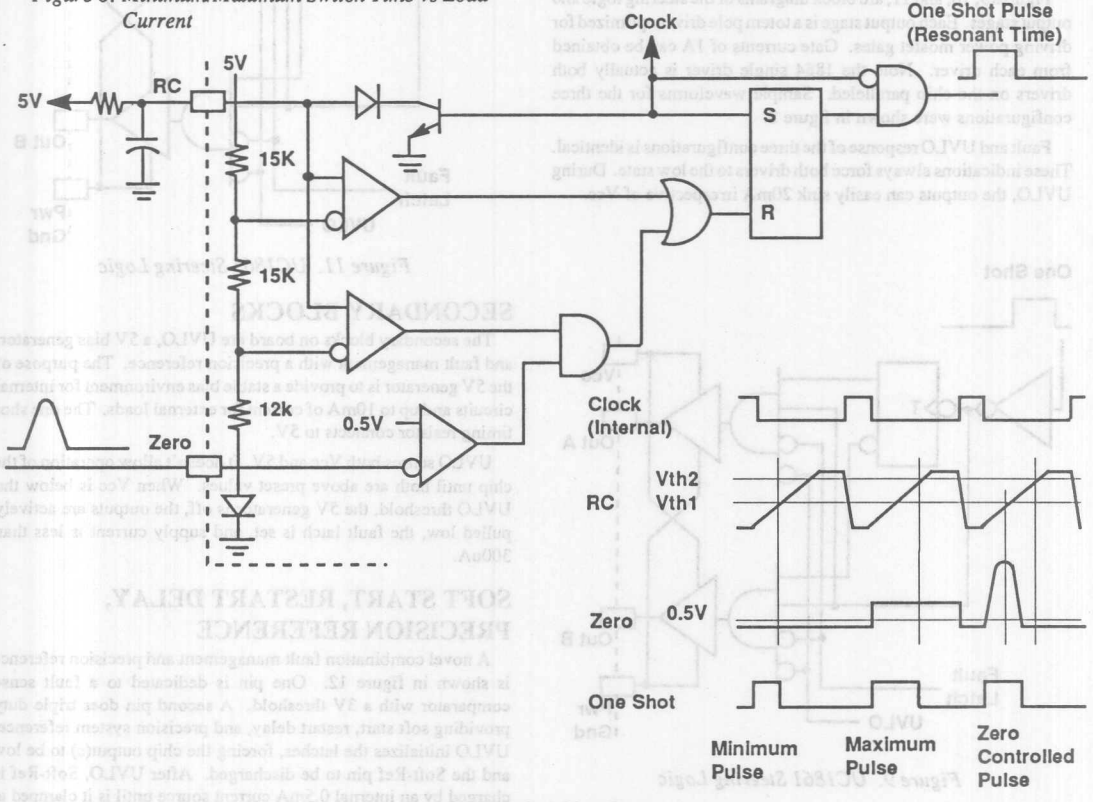


Figure 8. One Shot Timer.

The switch must turn off at 1.30us. This is because the tank impedance is exactly the ratio of low line voltage to overload current for these component values. This is the source of the 1.386 factor in equation 5. Secondly, and the point of the illustration, there is no possible value of fixed switch time that accommodates component variation.

ONE SHOT TIMING GENERATOR

In figure 8, details of the one shot timer are seen. The clock signal from the VCO sets the latch, blanks the output, and causes the RC timing pin to be discharged. The timing pin determines the minimum and maximum times the one shot output will be high.

$$T_{max} = R * C \quad (10)$$

$$T_{min} = 0.3 * T_{max} \quad (11)$$

Between these two limits, the zero detect comparator will terminate the one shot pulse whenever the Zero pin goes below 0.5V. By sensing the zero crossing of the resonant waveform, the one shot adapts to different resonant component values and varying line/load conditions. The switch time will properly track the resonant tank assuring zero stress switching.

STEERING LOGIC & OUTPUT STAGE

Figures 9, 10, and 11, are block diagrams of the steering logic and output stages. Each output stage is a totem pole driver optimized for driving power mosfet gates. Gate currents of 1A can be obtained from each driver. Note the 1864 single driver is actually both drivers on the chip paralleled. Sample waveforms for the three configurations were shown in figure 2.

Fault and UVLO response of the three configurations is identical. These indications always force both drivers to the low state. During UVLO, the outputs can easily sink 20mA irrespective of Vcc.

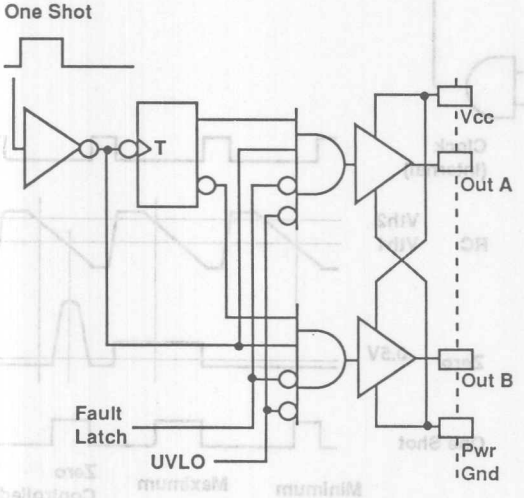


Figure 9. UC1861 Steering Logic

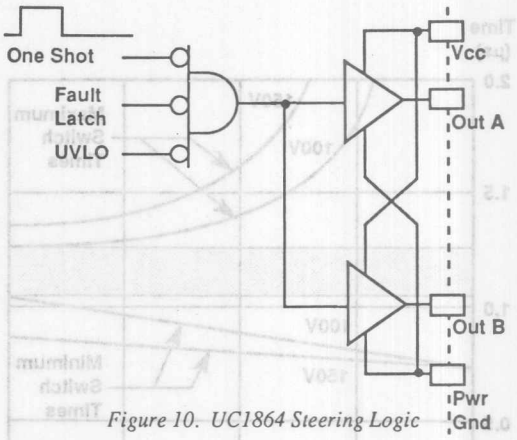


Figure 10. UC1864 Steering Logic

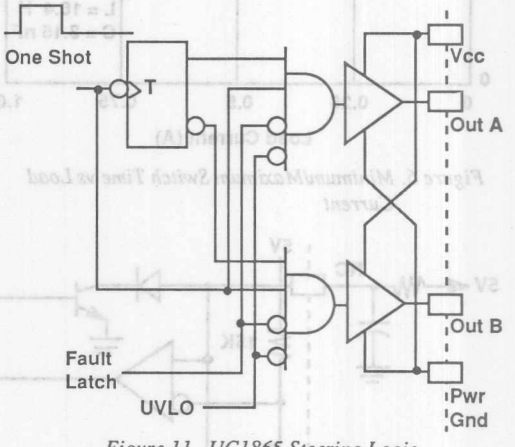


Figure 11. UC1865 Steering Logic

SECONDARY BLOCKS

The secondary blocks on board are UVLO, a 5V bias generator, and fault management with a precision reference. The purpose of the 5V generator is to provide a stable bias environment for internal circuits and up to 10mA of current for external loads. The one shot timing resistor connects to 5V.

UVLO senses both Vcc and 5V. It doesn't allow operation of the chip until both are above preset values. When Vcc is below the UVLO threshold, the 5V generator is off, the outputs are actively pulled low, the fault latch is set, and supply current is less than 300uA.

SOFT START, RESTART DELAY, PRECISION REFERENCE

A novel combination fault management and precision reference is shown in figure 12. One pin is dedicated to a fault sense comparator with a 3V threshold. A second pin does triple duty providing soft start, restart delay, and precision system reference. UVLO initializes the latches, forcing the chip output(s) to be low and the Soft-Ref pin to be discharged. After UVLO, Soft-Ref is charged by an internal 0.5mA current source until is it clamped at

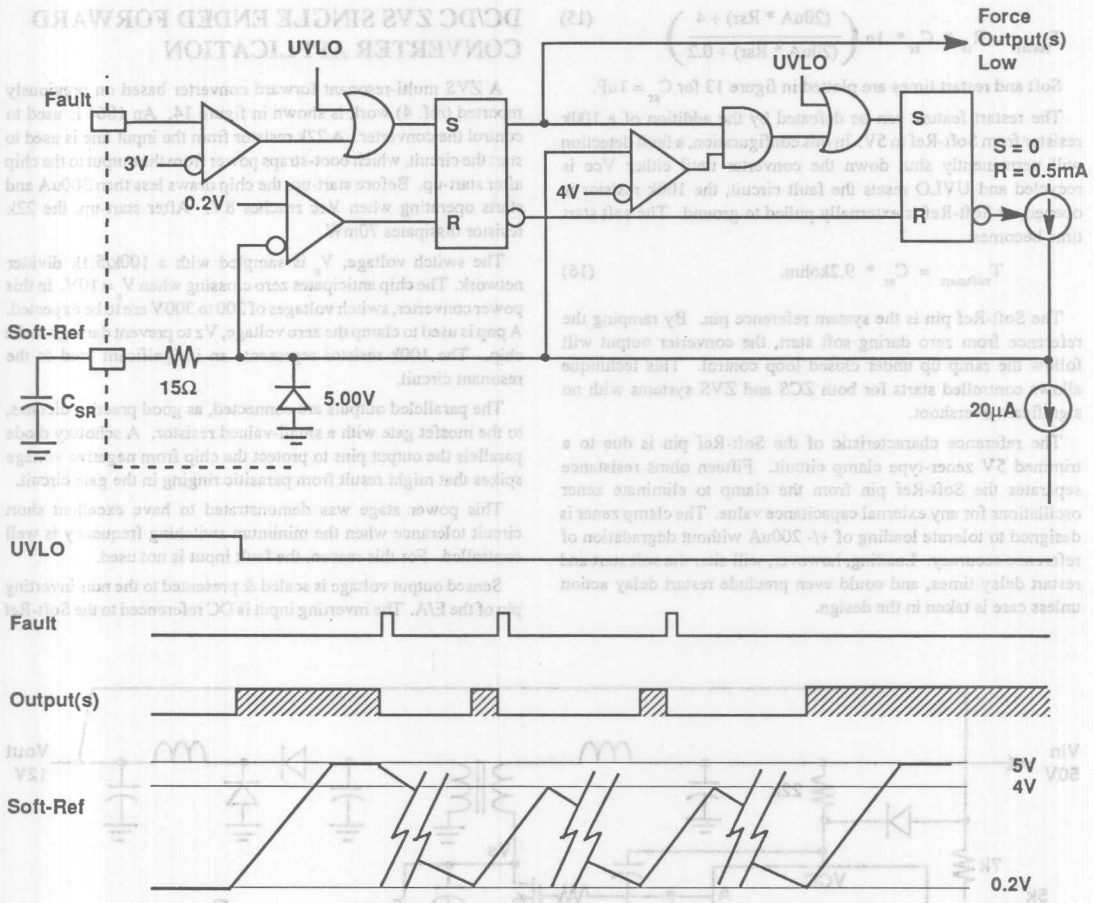


Figure 12. Fault Comparator, Soft Start, Restart Delay And Precision Reference

5V. The soft start time is approximately given by:

$$T_{softstart} = C_{sr} * 10kohms. \quad (12)$$

The recognition of a fault causes the outputs to be driven low and the Soft-Ref pin to be discharged with a 20uA current source. This is the restart delay period. When Soft-Ref reaches 0.2V, the outputs are enabled and the pin is recharged by the 0.5mA current. If a fault should occur before completion of the charge cycle, the outputs are immediately driven low, but the Soft-Ref pin is charged to 4 Volts before the 20uA restart delay current discharges the pin. The restart delay time during continuous fault operation is:

$$T_{restart} = C_{sr} * 190kohms. \quad (13)$$

The ratio of restart delay to soft start is 19:1. If shorter restart delay times are desired, a resistor of 20k or larger can be added from Soft-Ref to ground. The timing equations then become:

$$T_{softstart} = R_{sr} * C_{sr} * \ln\left(\frac{(0.48mA * Rsr) - 0.2}{(0.48mA * Rsr) - 5}\right) \quad (14)$$

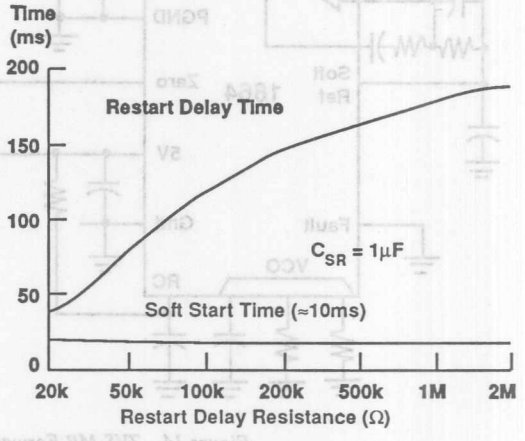


Figure 13. Soft Start And Restart Delay Times

$$T_{restart} = R_{sr} * C_{sr} * 1n\left(\frac{(20uA * Rsr) + 4}{(20uA * Rsr) + 0.2}\right) \quad (15)$$

Soft and restart times are plotted in figure 13 for C_{sr} = 1uF.

The restart feature can be defeated by the addition of a 100k resistor from Soft-Ref to 5V. In this configuration, a fault detection will permanently shut down the converter until either Vcc is recycled and UVLO resets the fault circuit, the 100k resistor is opened, or Soft-Ref is externally pulled to ground. The soft start time becomes:

$$T_{softstart} = C_{sr} * 9.2kohm. \quad (16)$$

The Soft-Ref pin is the system reference pin. By ramping the reference from zero during soft start, the converter output will follow the ramp up under closed loop control. This technique allows controlled starts for both ZCS and ZVS systems with no significant overshoot.

The reference characteristic of the Soft-Ref pin is due to a trimmed 5V zener-type clamp circuit. Fifteen ohms resistance separates the Soft-Ref pin from the clamp to eliminate zener oscillations for any external capacitance value. The clamp zener is designed to tolerate loading of +/- 200uA without degradation of reference accuracy. Loading, however, will alter the soft start and restart delay times, and could even preclude restart delay action unless care is taken in the design.

DC/DC ZVS SINGLE ENDED FORWARD CONVERTER APPLICATION

A ZVS multi-resonant forward converter based on previously reported (ref. 4) work is shown in figure 14. An 1864 is used to control the converter. A 22k resistor from the input line is used to start the circuit, which boot-straps power from the output to the chip after start-up. Before start-up, the chip draws less than 300uA and starts operating when Vcc reaches 8V. After start-up, the 22k resistor dissipates 70mW.

The switch voltage, V_s is sampled with a 100k/5.1k divider network. The chip anticipates zero crossing when V_s = 10V. In this power converter, switch voltages of 200 to 300V are to be expected. A pnp is used to clamp the zero voltage, Vz to prevent damage to the chip. The 100k resistor represents an insignificant load to the resonant circuit.

The paralleled outputs are connected, as good practice dictates, to the mosfet gate with a small-valued resistor. A schottky diode parallels the output pins to protect the chip from negative voltage spikes that might result from parasitic ringing in the gate circuit.

This power stage was demonstrated to have excellent short circuit tolerance when the minimum switching frequency is well controlled. For this reason, the fault input is not used.

Sensed output voltage is scaled & presented to the non-inverting pin of the E/A. The inverting input is DC referenced to the Soft-Ref

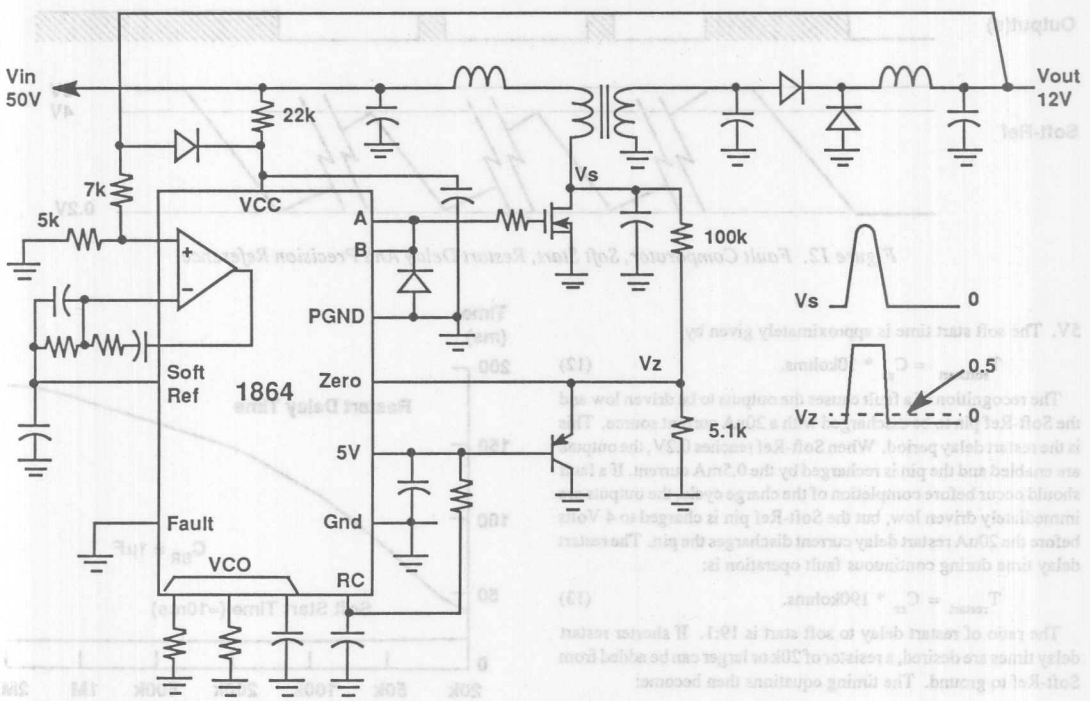


Figure 14. ZVS-MR Forward Converter Controlled By UC1864.

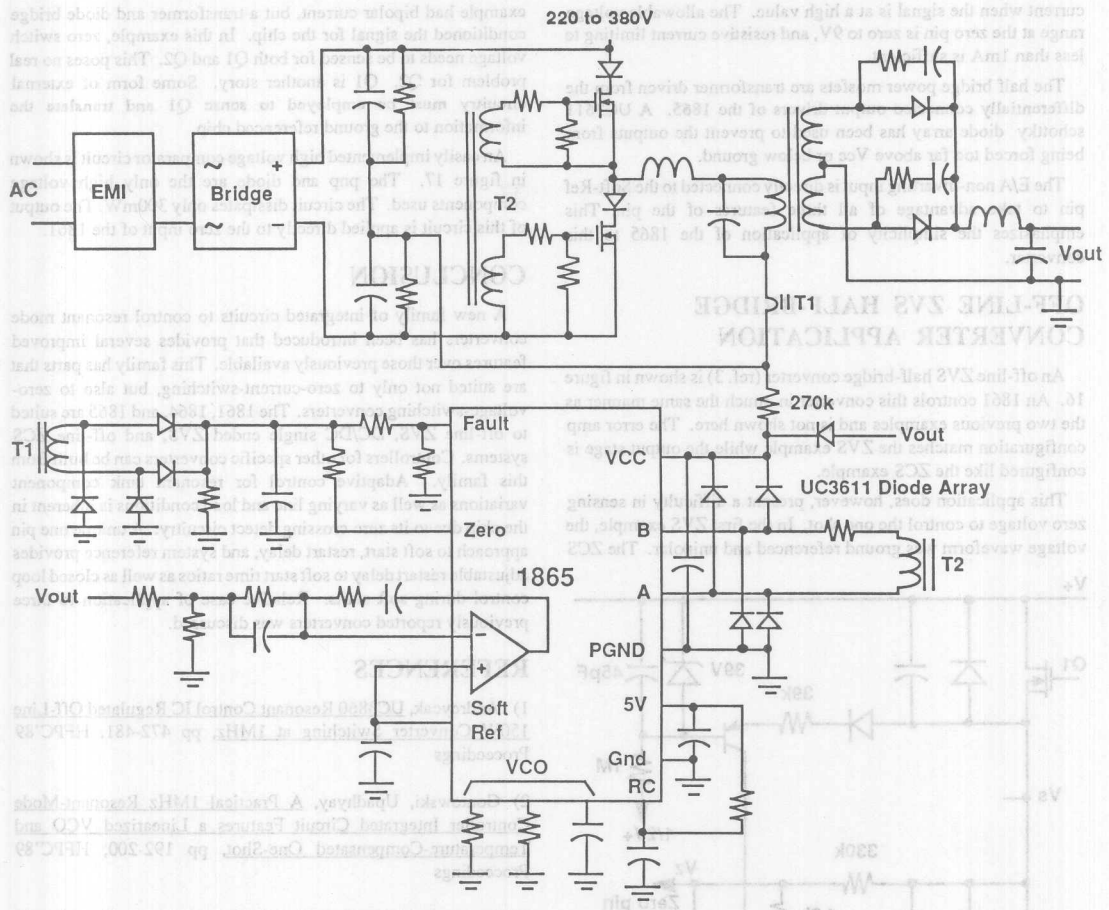


Figure 15. ZCS Off-Line Half-Bridge Converter With UC1865

pin, 5V. The compensation network shown represents zero DC load to the Soft-Ref pin. As long as C_{sr} is much larger than the feedback capacitor, then soft start behavior will be essentially as described in equation 12.

OFF-LINE ZCS HALF-BRIDGE CONVERTER APPLICATION

A ZCS off-line half-bridge converter (ref. 1) with an 1865 control IC is shown in figure 15. Irrelevant details in the converter have been simplified. The wide UVLO hysteresis and low start current of the chip have been used in start-up. A single resistor from the high voltage bus is used to start the circuit which then sustains itself from output voltage.

This circuit samples resonant current with transformer T1. Rectified secondary current, converted to an analog voltage, is applied to the fault and zero inputs of the 1865. Excessive current in the resonant tank will effect a shutdown and restart. The resistor between current sense transformer and the zero pin is to limit

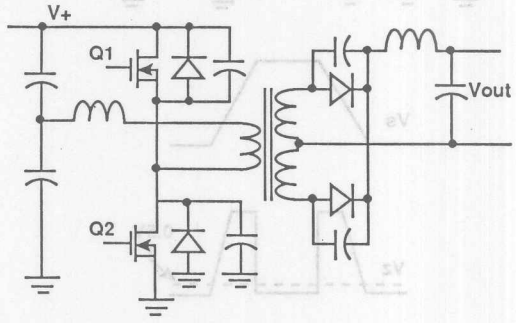


Figure 16. ZVS Half-Bridge Converter

current when the signal is at a high value. The allowable voltage range at the zero pin is zero to 9V, and resistive current limiting to less than 1mA is sufficient.

The half bridge power mosfets are transformer driven from the differentially connected output drivers of the 1865. A UC3611 schottky diode array has been used to prevent the outputs from being forced too far above Vcc or below ground.

The E/A non-inverting input is directly connected to the Soft-Ref pin to take advantage of all three features of the pin. This emphasizes the simplicity of application of the 1865 to this converter.

OFF-LINE ZVS HALF-BRIDGE CONVERTER APPLICATION

An off-line ZVS half-bridge converter (ref. 3) is shown in figure 16. An 1861 controls this converter in much the same manner as the two previous examples and is not shown here. The error amp configuration matches the ZVS example while the output stage is configured like the ZCS example.

This application does, however, present a difficulty in sensing zero voltage to control the one shot. In the first ZVS example, the voltage waveform was ground referenced and unipolar. The ZCS example had bipolar current, but a transformer and diode bridge conditioned the signal for the chip. In this example, zero switch voltage needs to be sensed for both Q1 and Q2. This poses no real problem for Q2. Q1 is another story. Some form of external circuitry must be employed to sense Q1 and translate the information to the ground referenced chip.

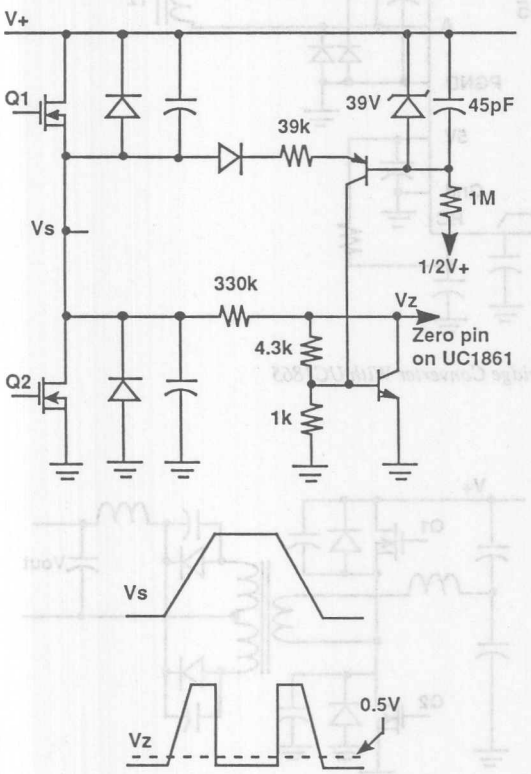


Figure 17. Zero Voltage Sensing Scheme For ZVS Half-Bridge Converter

An easily implemented high voltage comparator circuit is shown in figure 17. The pnp and diode are the only high voltage components used. The circuit dissipates only 300mW. The output of this circuit is applied directly to the zero input of the 1861.

CONCLUSION

A new family of integrated circuits to control resonant mode converters has been introduced that provides several improved features over those previously available. This family has parts that are suited not only to zero-current-switching, but also to zero-voltage-switching converters. The 1861, 1864, and 1865 are suited to off-line ZVS, DC/DC single ended ZVS, and off-line ZCS systems. Controllers for other specific converters can be built from this family. Adaptive control for resonant tank component variations as well as varying line and load conditions is inherent in the chip due to its zero crossing detect circuitry. A unique one pin approach to soft start, restart delay, and system reference provides adjustable restart delay to soft start time ratios as well as closed loop control during soft starts. Relative ease of application to three previously reported converters was discussed.

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UNIQUE CHIP PAIR SIMPLIFIES ISOLATED HIGH SIDE SWITCH DRIVE

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Abstract

High voltage, high current N-channel MOSFETs, now widely accepted in the industry, have found their way into numerous high power designs. As their cost to performance ratio continually improves, gate drive circuitry becomes a more significant factor in overall switch cost. This is most notable in "high-side" switching applications where an isolated gate drive is required. A new integrated circuit pair, the UC3724/UC3725, will be presented which implements a simple, isolated MOSFET gate drive circuit. To achieve a cost effective high side switch drive, UNITRODE has developed a unique modulation technique which transmits both signal and power across a small pulse transformer. This publication supercedes Unitrode Application Note U-124, originally written by C.S.Silva.

INTRODUCTION

Designers of power drives for PWM motor controls and switching power supplies often face the problem of driving the high-side MOSFET transistor in a high voltage power stage. In many applications, for example, bridge and three phase configurations, there are several of these switch drives to implement, and the level of complexity can be discouraging. From a cost standpoint, it is advantageous to utilize N- channel MOSFET devices in comparison to their more expensive - yet easier to drive P- channel counterparts. However, these high-side switch gate drive circuits can quickly become extravagant, and frequently result in complicated or unreliable schemes.

Probably the most common technique used in high-side drive circuits is to generate an isolated, or "floating" auxiliary supply voltage. Referenced to the high-side MOSFET's source, this supply powers a conventional gate drive circuit. The average auxiliary power consumed is generally well below one watt, and varies with switching frequency, FET size and number of paralleled FETs used to configure "one" switch. A typical circuit using this method is shown in figure 1.

With the realization that average MOSFET gate drive power is quite small, charge pump circuits are frequently used to implement the floating supply. In these designs, the storage capacitor can become large in an attempt to minimize the supply's ripple voltage and may impair the useable range of frequencies and duty cycles. Due to this constraint, the switch on-time must be limited by the control circuit, and preferably, undervoltage lockout incorporated in the driver circuit to assure reliable operation.

A simple alternative to this discrete approach can be obtained by using a high voltage IC - provided that the maximum switch voltage and on-time are within it's capability. There is, however, a cost penalty for this single chip solution. While the basic gate drive and protection circuitry have a low voltage requirement, the level shifting transistors necessitate a high voltage IC process - an option which is inherently expensive. Additionally, many motor drive circuits cannot tolerate an on-time limitation, and require an auxiliary power supply for continuous (DC) operation.

Typically, an opto-coupler is used to translate the switch activation command from the ground referenced, or "low-side" control circuitry up to the high-side driver. Unfortunately, this technique comes with its own set of reliability issues which includes low common mode transient immunity, and performance degradation over time and temperature. High voltage MOSFET circuit slew rates can easily exceed 20 kV/us causing opto-coupler self turn-on or turn-off. The opto-coupler's AC common mode rejection must be carefully evaluated, as this specification is usually influenced by common mode voltage as well as dv/dt. Power up and power down sequences also present potential failure without undervoltage lockout circuitry.

TYPICAL HIGH SIDE DRIVER APPLICATION

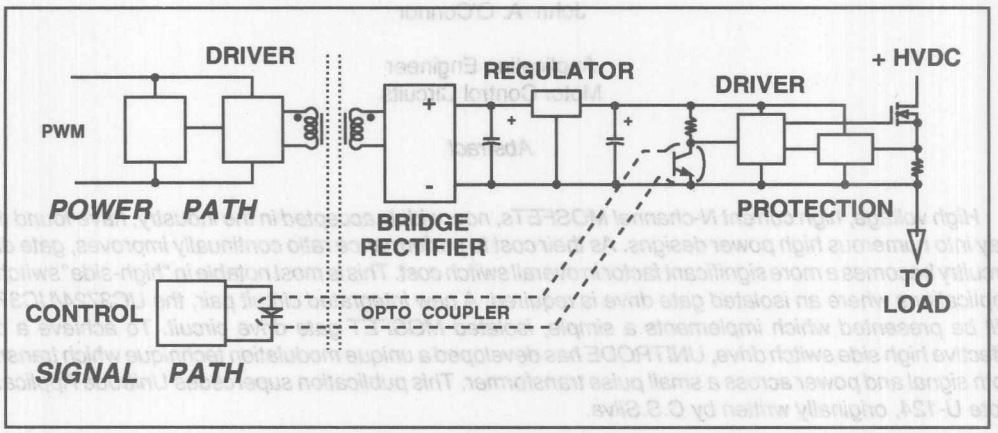


Figure 1.

UC3724 / UC3725 DRIVER PAIR - BASIC CIRCUIT

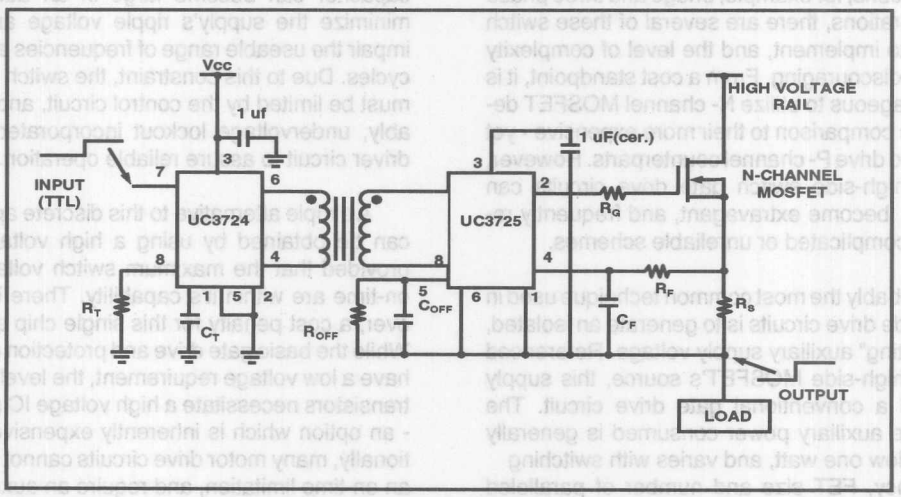


Figure 2.

UC3724/UC3725 DRIVER PAIR

The Unitrode UC3724/UC3725 IC pair offers a compact, and comparatively inexpensive design solution to the problem of supplying both isolated power and command signals. Figure 2 shows the basic circuit implementation. The two ICs, a pulse transformer, and a few passive components form a complete isolated MOSFET driver. A unique modulation technique simultaneously transmits power and command information across the transformer.

Provided the operational voltage is low, integrated circuit technology allows sophisticated circuits to be implemented at low cost. Transformers can easily provide several thousand volts of isolation, while supplying both power and signal. By exploiting each device's strengths, a low cost, high performance solution is achieved.

The UC3724 transmitter IC generates the carrier signal, with one of two possible duty cycles as commanded by the TTL level input. A unique carrier oscillator design not only sets the operating frequency, but also prevents the transformer from saturating, by assuring that the transformer magnetizing current is zero before initiating a subsequent oscillator cycle. Average transformer voltage is always zero, even under the transient conditions caused by input command changes. Saturation of the transformer core is virtually impossible using this technique.

To minimize transformer size and cost, a high frequency carrier is used. Although the carrier frequency limits the maximum transmitted switching frequency, it has no effect on input to output delay, which is solely determined by circuit propagation time.

The UC3725 driver IC rectifies the transformer isolated carrier to power the driver circuitry. Additionally, comparator circuitry determines the input command by sensing which duty cycle is transmitted, driving the MOSFET gate accordingly with the high current output stage. A comparator with programmable off time circuitry implements local over-current protection, while an enable input provides additional control and protection flexibility.

UC3724 ISOLATED DRIVE TRANSMITTER - BLOCK DIAGRAM

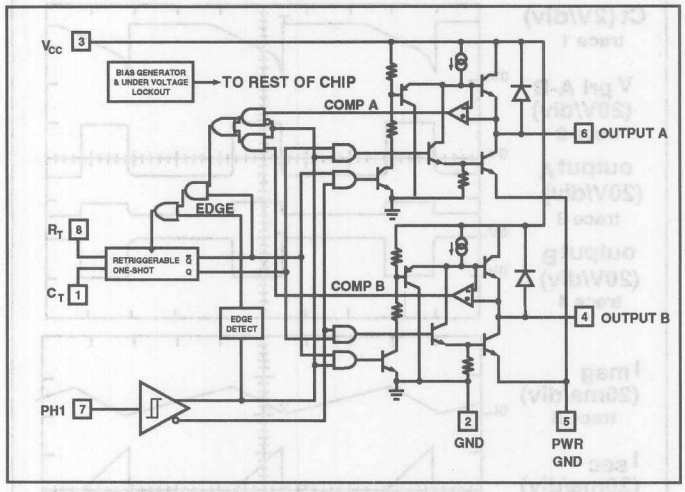


Figure 3.

UC3724 DRIVE TRANSMITTER

The UC3724 block diagram is shown in figure 3. The circuit consists of a bias voltage generator with under voltage lockout, control logic, a retriggerable one-shot, a TTL compatible input with hysteresis, two tri-level output drivers, and two zero current sense comparators.

The under voltage lockout inhibits the output drivers when the input supply voltage is below 9 volts. Once adequate supply voltage is present,

the bias generator supplies the appropriate internal voltages and currents, allowing the outputs to be enabled. This assures correct operation at power-up and power-down.

The carrier oscillator uses both a one-shot pulse width and the transformer core reset time to set the overall period. The one shot pulse width (T_{PW}) equals one-third of the nominal carrier period, and is set by timing resistor (R_T) and capacitor (C_T).

1) $T_{PW} = 0.51 \bullet R_T \bullet C_T + 150ns$ (sec)

"Full" supply voltage is applied to the transformer primary during this time by driving one output high and the other low. Transformer magnetizing current rises linearly at a rate determined by the primary inductance and applied voltage.

2) $di/dt = \dfrac{V_A - V_B}{L_{pri}}$ (*amps* / sec)

When the one-shot pulse ends, the low output switches high, and the high output switches to approximately one-half of the supply voltage. This applies "half" supply voltage to the primary, effectively in a reverse polarity to that of it's previous state. Internal offset circuitry compensates for output conduction voltage drops and maintains the full/half voltage ratio over temperature and supply voltage variations.

Power is transferred to the secondary circuit only while full voltage is applied to the primary. During this period the primary current is a composite of load and magnetizing current. The load current is interrupted when the half voltage is applied, so the residual primary current flowing is the magnetizing current.

With half voltage applied, the magnetizing current falls at one-half of the rate at which it had increased. An interval twice the programmed one-shot period is therefore necessary to reset the cores magnetizing current to zero and prevent any possibility of core saturation. The UC3724 incorporates a zero current detection circuit which guarantees that the magnetizing current has reached zero before initiating another oscillator cycle.

UC3724 OPERATIONAL WAVEFORMS (STEADY STATE)

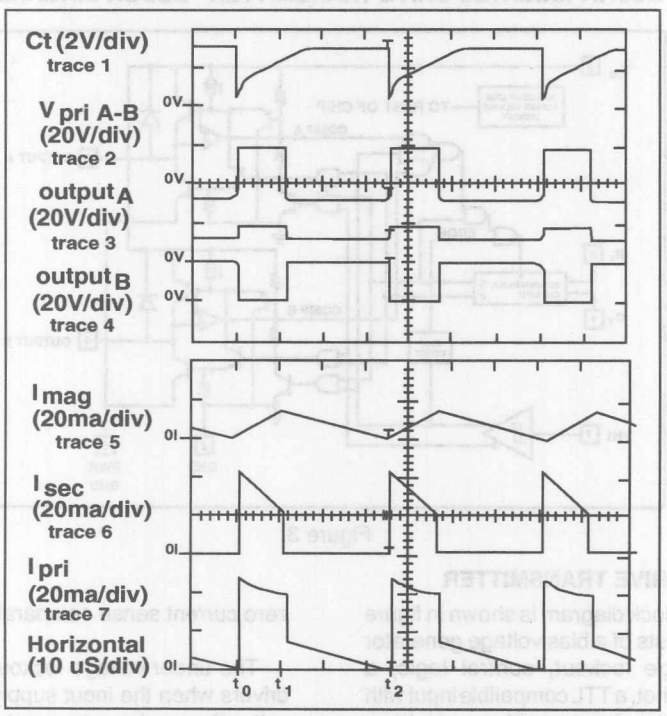


Figure 4.

Steady-state (continuous logic low input command) waveforms are shown in figure 4. The first trace shows timing capacitor (C_T) voltage, which is charged by a current set by the timing resistor (R_T). At time t_0, the one-shot is triggered, discharging the timing capacitor. Output$_A$ (trace 3) switches high, and output$_B$ (trace 4) switches low, with the resulting differential voltage V_{priA-B} (trace 2) applied across the transformer primary. The transformer magnetizing current (trace 5) increases linearly at a rate described by equation 2.

At time t_1, the timing capacitor voltage reaches the 2.5 volt threshold, ending the one-shot period. Output$_A$ is switched to $(V_{CC}/2) + V_{offset}$, and output$_B$ is switched high, allowing it's catch diode to conduct. The primary voltage (V_{priA-B}), is inverted, and reduced in half, causing the magnetizing current to fall at half the rate at which it had increased.

Output$_A$'s current sense comparator senses that the magnetizing current has reached zero at t_2, triggering the one-shot, thus initiating another oscillator cycle. If a continuous high is commanded, the waveforms for output$_A$ and output$_B$ are interchanged, and the magnetizing current is inverted.

At an input command transition, the existing oscillator cycle is terminated, the A and B outputs are reversed, and a new oscillator cycle is initiated. This applies full voltage of the appropriate polarity across the transformer primary for detection by the UC3725. Although the oscillator cycle has been terminated without allowing the core to reset, there is no danger of saturation. By reversing the outputs, the magnetizing current must first cross through zero before rising in the opposite polarity. The peak magnetizing current is actually less than a normal cycle, reducing the fall time, and hence the oscillator period.

UC3725 ISOLATED SIDE MOSFET DRIVER BLOCK DIAGRAM

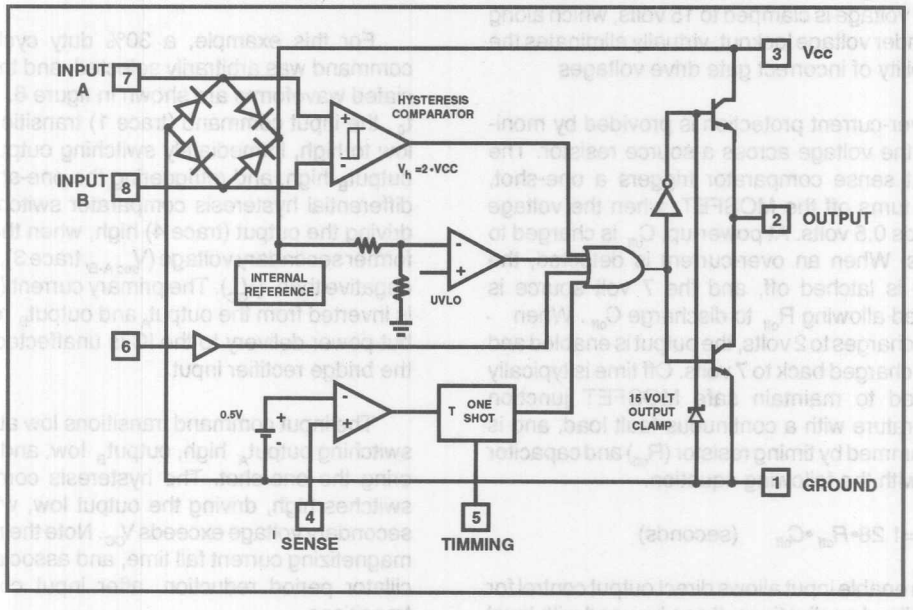


Figure 5.

UC3725 ISOLATED MOSFET DRIVER

The block diagram for the UC3725 is shown in figure 5. The circuit consists of a Schottky bridge rectifier, an internal reference with under voltage lock out, a differential hysteresis comparator, a high current totem-pole driver, a current sense comparator with programmable off time one-shot, and an enable input.

The Schottky bridge rectifies the isolated secondary voltage, providing power for the IC. A small capacitor, typically a 1uf ceramic, provides filtering and bulk storage to supply the high peak currents required to rapidly charge the MOSFET gate.

The undervoltage lockout inhibits the output driver when the supply voltage is below 12 volts. This assures that sufficient voltage is available to drive the MOSFET gate, preventing possible destructive linear operation.

The output driver is capable of delivering nearly two amps peak, which is more than adequate for most applications. The UC3725 features a self biasing drive arrangement which actively sinks gate current during under voltage lockout, preventing MOSFET self turn on. No additional gate to source resistor is required. The output voltage is clamped to 15 volts, which along with under voltage lockout, virtually eliminates the possibility of incorrect gate drive voltages

Over-current protection is provided by monitoring the voltage across a source resistor. The current sense comparator triggers a one-shot, which turns off the MOSFET, when the voltage exceeds 0.5 volts. At power-up, C_{off} is charged to 7 volts. When an over-current is detected, the output is latched off, and the 7 volt source is disabled allowing R_{off} to discharge C_{off}. When C_{off} discharges to 2 volts, the output is enabled and C_{off} is charged back to 7 volts. Off time is typically selected to maintain safe MOSFET junction temperature with a continuous fault load, and is programmed by timing resistor (R_{off}) and capacitor (C_{off}) with the following equation.

3) $T_{off} = 1.28 \bullet R_{off} \bullet C_{off}$ (seconds)

An enable input allows direct output control for specialized applications. It can be used with level shifting transistors, optocouplers, or other source referenced circuitry such as a UC3730 thermal monitor circuit for MOSFET over-temperature protection.

The input command, transmitted by the UC3724, is demodulated using a differential hysteresis comparator. The comparator senses whether the "full voltage" applied to the transformer is positive or negative, corresponding to an "off" or "on" input command. The bridge rectifier causes the peak secondary voltage to always be two diode drops above V_{CC} while the comparator hysteresis is internally set to twice V_{CC}. The MOSFET is turned on when the secondary voltage is more negative than $-(V_{CC})$, and turned off when more positive than V_{CC}. Note that there is a logic inversion between the hysteresis comparator and the gate driver.

Referring to steady-state waveforms (figure 4), the secondary current (trace 6) charges the supply capacitor during the full voltage output segment of the oscillator cycle (time t_0 thru t_1). During the half voltage output segment (time t_1 thru t_2), no secondary current flows, thus only magnetizing current is present in the primary current (trace 7), allowing proper oscillator operation.

For this example, a 30% duty cycle input command was arbitrarily selected, and the associated waveforms are shown in figure 6. At time t_0, the input command (trace 1) transitions from low to high, immediately switching $output_A$ low, $output_B$ high, and retriggering the one-shot. The differential hysteresis comparator switches low, driving the output (trace 4) high, when the transformer secondary voltage ($V_{sec\ A\text{-}B}$, trace 3), is more negative than $-(V_{CC})$. The primary current (trace 2) is inverted from the $output_A$ and $output_B$ reversal, but power delivery to the IC is unaffected due to the bridge rectifier input.

The input command transitions low at time t_1, switching $output_A$ high, $output_B$ low, and retriggering the one-shot. The hysteresis comparator switches high, driving the output low, when the secondary voltage exceeds V_{CC}. Note the reduced magnetizing current fall time, and associated oscillator period reduction, after input command transitions.

OPERATIONAL WAVEFORMS AT 30% DUTY CYCLE

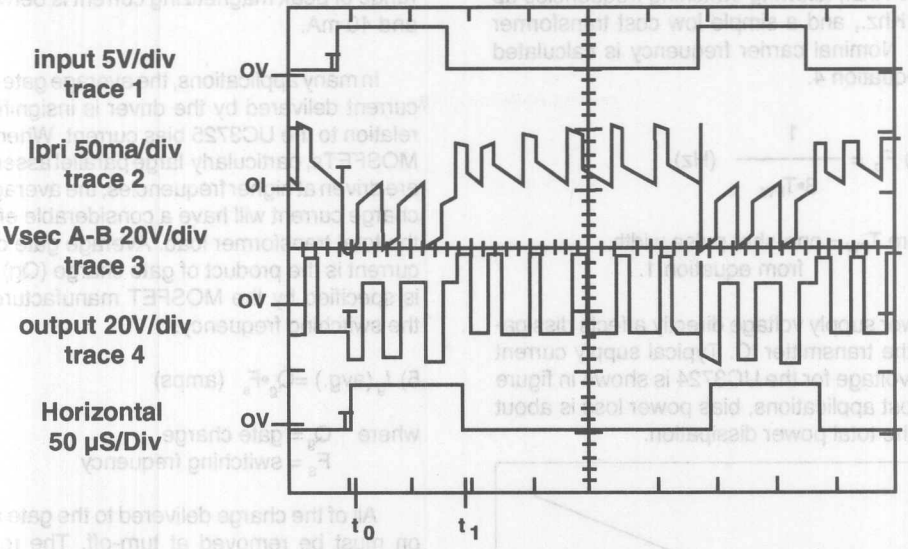


Figure 6.

PRACTICAL CONSIDERATIONS

The selection of carrier frequency (or more appropriately one-shot period since carrier frequency varies at switching transitions), is influenced more by transformer design than performance objectives. The minimum switching command period should be limited to four times the one-shot pulse width, to assure that adequate time is available to reset the core. Note that this limits the maximum switching frequency - but not the duty cycle range which is always 0 to 100%.

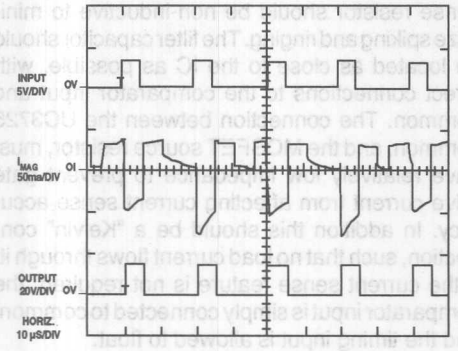


Figure 7.

Waveforms for a command period approximately four times the one shot pulse width are shown in figure 7. The carrier oscillator has sufficient time to reset the transformer core and prevent saturation.

The one-shot period has no effect on input to output propagation delay, since the leading edge provides the output command information. Turn-on and turn-off propagation delay waveforms are shown in figure 8.

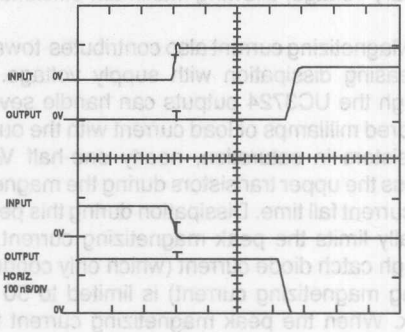


Figure 8.

The maximum carrier frequency is limited to 600 Khz. Most circuits will operate between 200 and 600 Khz., allowing switching frequencies up to 450 Khz., and a simple low cost transformer design. Nominal carrier frequency is calculated using equation 4.

$$4)\ F_c = \frac{1}{3 \bullet T_{PW}} \quad (Hz)$$

where T_{PW} = one-shot pulse width from equation 1.

Power supply voltage directly affects dissipation in the transmitter IC. Typical supply current verses voltage for the UC3724 is shown in figure 9. In most applications, bias power loss is about half of the total power dissipation.

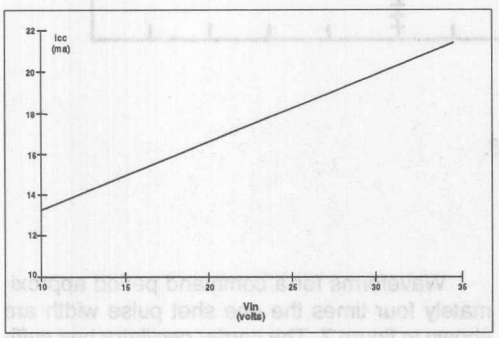


Figure 9.

The UC3725 driver IC provides sufficient gate voltage with a 15 volt supply. Any further increase, although safe since the output is clamped to 15 volts, causes additional bias power dissipation. By adjusting the transformer turns ratio, a 15 to 18 volt secondary supply can be generated with any primary voltage, allowing maximum efficiency .

Magnetizing current also contributes towards increasing dissipation with supply voltage. Although the UC3724 outputs can handle several hundred milliamps of load current with the output transistors in saturation, nearly one-half V_{CC} is across the upper transistors during the magnetizing current fall time. Dissipation during this period usually limits the peak magnetizing current, although catch diode current (which only conducts falling magnetizing current) is limited to 50 mA peak. When the peak magnetizing current falls below 10 ma, the required primary inductance becomes excessive, resulting in a large number of turns or larger core size. Therefore, the optimal range of peak magnetizing current is between 10 and 40 mA.

In many applications, the average gate charge current delivered by the driver is insignificant in relation to the UC3725 bias current. When larger MOSFETs, particularly large parallel assemblies, are driven at higher frequencies, the average gate charge current will have a considerable effect on the total transformer load. Average gate charge current is the product of gate charge (Qg), which is specified by the MOSFET manufacturer, and the switching frequency.

$$5)\ I_g(avg.) = Q_g \bullet F_s \quad (amps)$$

where Q_g = gate charge
F_s = switching frequency

All of the charge delivered to the gate at turn-on must be removed at turn-off. The resultant average power dissipated by the driver and gate resistor is described by equation 6.

$$6)\ P_g = Q_g \bullet V_g \bullet F_s \quad (Watts)$$

where V_g = fully charged gate voltage

The over-current input on the UC3725 has a typical delay time of 150 ns. Most applications require a small RC filter to attenuate leading edge current spikes caused by parasitic capacitance and catch rectifier reverse recovery. Careful attention to layout and component selection is necessary to prevent false triggering. The current sense resistor should be non-inductive to minimize spiking and ringing. The filter capacitor should be located as close to the IC as possible, with direct connections to the comparator input and common. The connection between the UC3725 common, and the MOSFET source resistor, must have relatively low impedance to prevent gate drive current from affecting current sense accuracy. In addition this should be a "Kelvin" connection, such that no load current flows through it. If the current sense feature is not required, the comparator input is simply connected to common, and the timing input is allowed to float.

DESIGN PROCEDURE

Typically, the application dictates the MOSFET(s), switching frequency, and switch isolation voltage. For cost considerations, a supply voltage common with other circuitry, is usually chosen to power the UC3724. The designer is then left with the carrier frequency and peak magnetizing current to select. A high carrier frequency is normally used to minimize transformer size and cost. Magnetizing current is initially set to a nominal value, such as 20 ma, and then adjusted if necessary to optimize the transformer design.

The one-shot pulse width is set to 1/3 the carrier frequency using equation 1. By rearranging equation 2, and allowing 2 volts for saturation, the transformer primary inductance can be calculated.

$$7)\ L_{pri} = \frac{(V_{cc}-2)\bullet T_{pw}}{I} \quad \text{(Henries)}$$

where V_{CC} = supply voltage
T_{PW} = one-shot pulse width
I_{mag} = peak transformer magnetizing current

Transformer core selection is an iterative process based on the following two equations.

$$8)\ \Delta B = \frac{V_{applied}\bullet T_{on}\bullet 10^4}{N_{turns}\bullet A_c} \quad \text{(Tesla)}$$

$$9)\ N_{turns} = \sqrt{\frac{L_{pri}\bullet 10^9}{A_L}} \quad \text{(turns)}$$

A toroid is usually the most cost effective core geometry for this application. The core material should be chosen for low losses and high permeability at the design frequency to minimize transformer size and number of turns. Thermal resistance and loss factors provided by the manufacturer are used to select the optimum core size. A flux density of .05 Tesla (500 Gauss) will cause approximately a 20 degree C rise at 500 KHz with common power materials such as Ferroxcube 3C8.

Typically most toroids used for this application have an AL between 1000 and 3000 mH/1000 turns. An estimated number of turns is calculated using an average A_L value of 2000 mH/1000 turns in equation 8. By rearranging equation 7, an approximate core are is calculated using a flux density of .05 Tesla, and the estimated number of turns. This leads to a first core selection, and an actual A_L value, which is used in equation 8 to calculate N_{turns}. The flux density is then checked using equation 7, and a larger or smaller core is selected if necessary.

The turns ratio is calculated using the following equation, which allows 2 volts for UC3724 output saturation, and 3 volts for UC3725 rectifier drop and output saturation.

$$10)\ \text{Turns ratio} = \frac{V_{cc}-2}{V_{gate}+3}$$

The power supplied by the transformer is the sum of the UC3725 bias loss and the average gate charge power. For minimum wire size, the resulting RMS winding currents can be calculated, although typically there sufficient space to use 24 to 28 AWG wire for ease of handling.

High voltage isolation is implemented by sleaving the primary winding with an insulation suitable for the required breakdown voltage. For low leakage inductance, bifilar windings are used, with additional turns added to the primary or secondary for non 1:1 turns ratios.

DESIGN EXAMPLE

The following design example is a general purpose isolated MOSFET gate driver. Up to 200 milliwatts is available for gate drive, which is suitable for most applications. A 15 volt power supply provides sufficient secondary voltage by using a step-up transformer.

Driver specifications :
* 200 milliwatts average gate drive power
* 100 KHz. switching rate
* 15 V supply voltage
* 1KV minimum isolation voltage

A 600KHz. carrier frequency is selected to minimize transformer size and cost. The one-shot pulse width is calculated by rearranging equation 4.

$$T_{pw} = \frac{1}{3 \cdot 600\ KHz}$$

$$= 556ns$$

Since the carrier frequency is near maximum, 2K will be used for R_T . C_T is calculated with equation 1.

$$C_T = \frac{(556-150)\ ns}{0.51 \cdot 2K}$$

$$= 398pf \text{ (use 390pf)}$$

30mA is selected for the peak magnetizing current. The corresponding primary inductance is calculated with equation 7.

$$L_{pri} = \frac{(15-2)\ V \cdot 556ns}{30\ mA}$$

$$= 241\mu H$$

The estimated number of turns are calculated using equation 9 with an average value of 2000 mH/1000 turns for A_L.

$$N_{turns} = \sqrt{\frac{241 \cdot 10^9}{2000}}$$

$$= 11 \text{ turns}$$

The approximate core area is calculated with equation 8, using a flux density of 0.05 Tesla.

$$A_c = \frac{13V \cdot 556ns \cdot 10^4}{11\ turns \cdot 0.05\ Tesla}$$

$$= 0.131\ cm^2$$

A one-half inch diameter toroid, Ferroxcube part number 204T250-3C8, is selected which has the following specifications.

$$Ac = 0.148\ cm^2$$

$$A_L = 1620\ mH/1000\ turns$$

N_{turns} is calculated using the actual A_L value in equation 9.

$$N_{turns} = \sqrt{\frac{241 \cdot 10^9}{1620}}$$

$$= 12.2 \text{ turns (use 12 turns)}$$

The flux density is checked using equation 8.

$$\Delta B = \frac{(15-2)\ V \cdot 556ns \cdot 10^4}{12\ turns \cdot 0.148\ cm^2}$$

$$= 0.041 \text{ Tesla}$$

The turns ratio is calculated using equation 10 for a gate voltage of 12 to 14 volts.

$$\text{Turns ratio} = \frac{(15-2)\ V}{(12+3)\ V}$$

$$= 0.867$$

Therefore N_{sec}= 14 turns

The transformer is wound with 26AWG magnet wire for ease of handling. A teflon insulation sleeve is slipped over the primary winding to improve the primary to secondary breakdown voltage. The primary and secondary are wound bifilar, to minimize leakage inductance, then the two remaining secondary turns are wound.

To verify operation, the test circuit shown in figure 10 was built. The over current, gate and bulk storage components are selected per MOSFET and load requirements. Figure 11 and 12 show turn-on and turn-off waveforms respectively.

The lower MOSFET in figure 10 was configured to test self turn-on of the upper driver during high transformer dv/dt. With 300 volts slewing at a rate in excess of 25 kv/us, no evidence of driver self turn-on was observed.

APPLICATIONS

Although the lower MOSFET driver is configured for faster switching than would normally be required, figure 10 is typical of half bridge outputs, where two or three of these circuits could implement a full or three phase bridge respectively. Full isolation for UL or VDE requirements can be met

by using isolated drivers for both upper and lower MOSFETs. This configuration can also greatly reduce noise in high current applications, by completely isolating the control circuitry from output devices.

TYPICAL HIGH SIDE DRIVE APPLICATION CIRCUIT SCHEMATIC

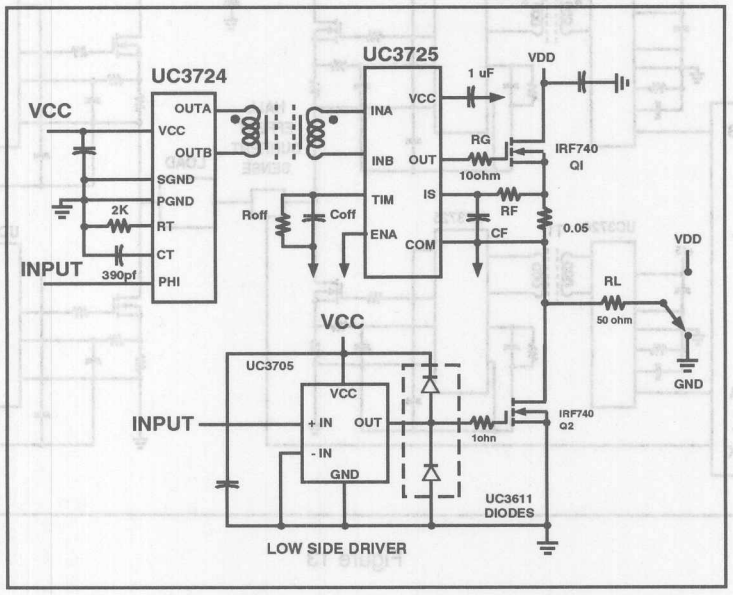


Figure 10

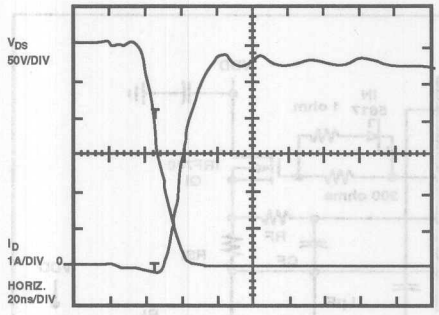


Figure 11

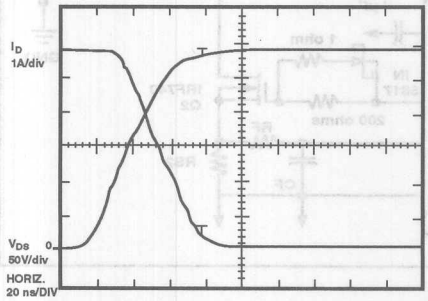


Figure 12

FULL BRIDGE OUTPUT

Some circuits have multiple MOSFETs driven from the same command, which are isolated from each other. A most notable example is the full bridge, which is commonly used in brush and stepper motor drives. Multiple secondaries can drive additional isolated UC3725 circuits, from a single UC3724, further reducing cost and complexity.

Figure 13 shows a fully isolated bridge circuit. By isolating all of the MOSFETs and the current sense signal, complete control to output isolation is achieved. Dual secondaries on each transformer eliminates the requirement for two additional transformers and UC3724s. For feedback and protection, a hall effect current sensor monitors load current directly, while providing high voltage isolation. The local over-current circuit in the upper FET drivers protects during load to ground shorts.

FULL BRIDGE OUTPUT CIRCUIT

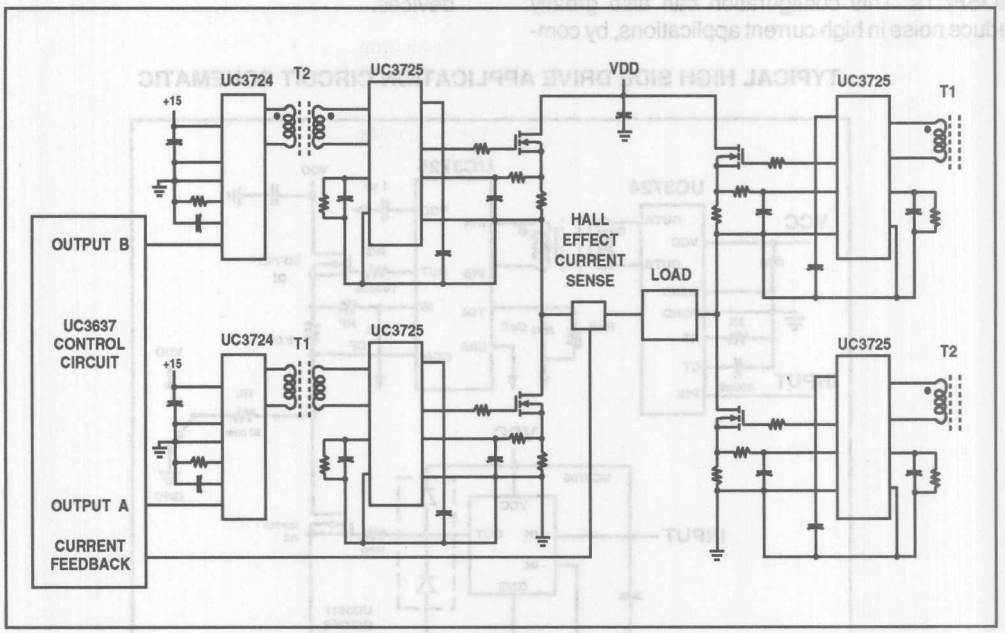


Figure 13

HALF BRIDGE OUTPUT CIRCUIT

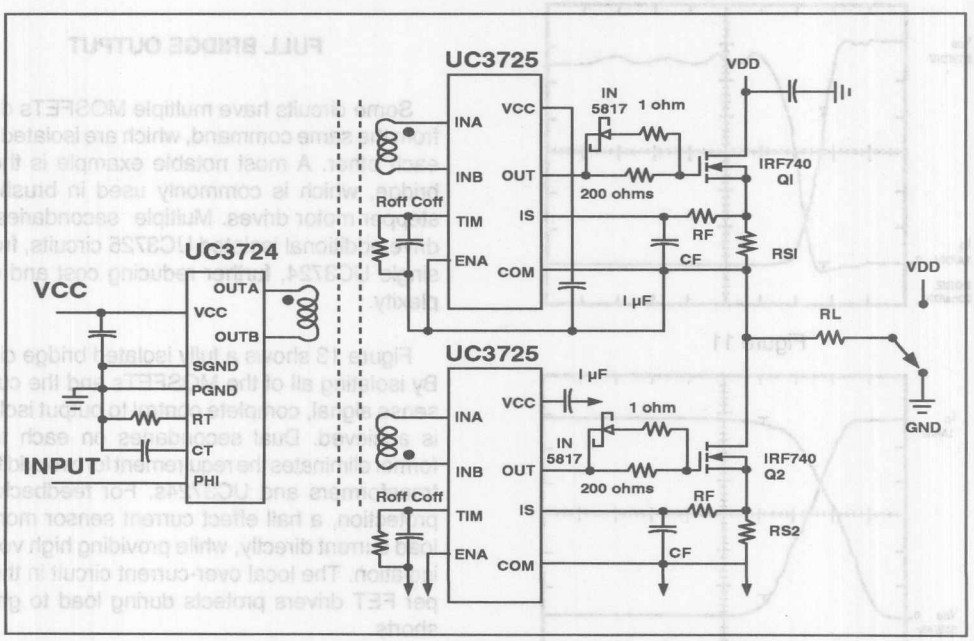


Figure 14

HALF BRIDGE OUTPUT

By reversing the polarity of one of the secondary windings on a dual secondary transformer, two FETs are switched out of phase from each other. A typical application for this arrangement is the half bridge, and is shown in figure 14. Dead-time between turn-off and turn-on is difficult to implement using this technique. To turn off both FETs, the UC3724 supply voltage must be removed, or the UC3725 enable inputs driven high. While shutting down the supply voltage is suitable for power-up/power-down protection, it is to slow to control dead-time. Isolating or level shifting the enable inputs adds complexity and negates the advantage of using a dual secondary transformer. Cross conduction is easily minimized however, by the gate resistor arrangement which provides rapid turn-off and slow turn-on. This technique is also typically used to minimize cross conduction caused by stored charge in the MOSFET body diode.

LEVEL SHIFT DRIVER

The UC3725 makes an excellent level shifted driver for lower voltage, non-isolated applications. All of the necessary protection features which are often omitted in discrete designs are incorporated in the UC3725, assuring reliable operation under all conditions. Figure 15 shows a typical level shift circuit with a "boot-strap" supply. The MPS-U10 level shift transistor has a maximum V_{ceo} of 300 volts, although it's dissipation without a heatsink limits the maximum supply to approximately 200 volts. Figure 16 shows input to output propagation delay while switching 150 volts and 3 amps. A 20 mA current source with a voltage compliance 15 volts above the supply rail can be used in place of the boot-strap circuit, for applications which cannot tolerate an on-time limitation. The cost effectiveness of this approach will depend on supply voltage and number of high-side MOSFETs.

LEVEL SHIFT CIRCUIT

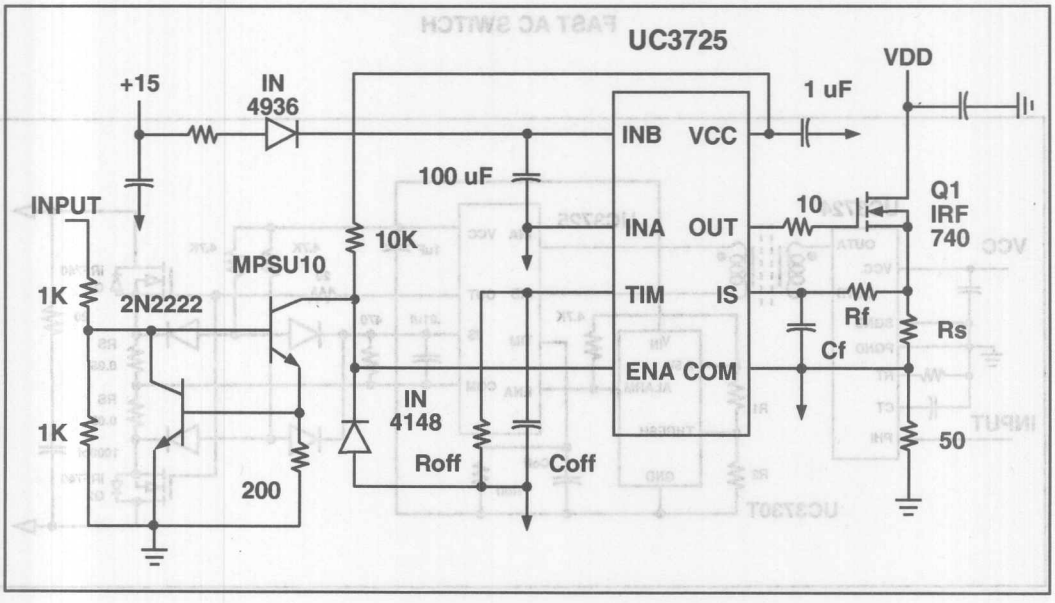


Figure 15

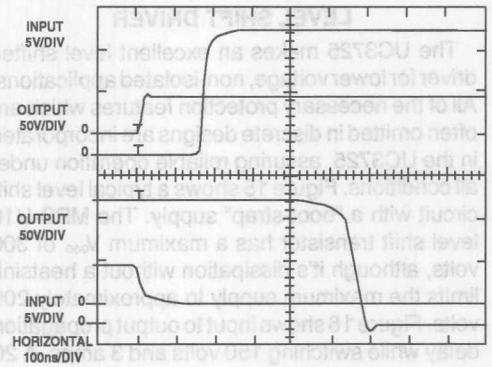


Figure 16.

LATCHED OVER-CURRENT FAULT

Current limiting is provided by the control circuit in many applications. Local protection from the UC3725 is therefore only required for fault conditions which result in high di/dt such as output shorts. It may be desirable to latch the output off under such a fault, rather than enable after a fixed off-time. Figure 17 shows a simple circuit used in place of the timing resistor and capacitor which will latch the output off after the over-current comparator is triggered. The 10uf capacitor resets the circuit at power-up by holding the timing input below the 2 volt one-shot threshold. When an over-current is sensed, the timing input voltage falls, and is clamped at 5.1 volts. The one-shot period normally ends when C_{off} is discharged below 2 volts, but by clamping the voltage, the time constant effectively appears infinite.

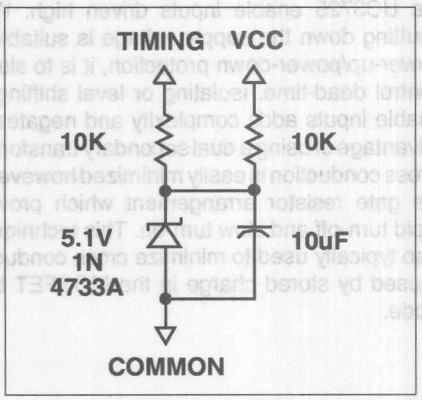


Figure 17

FAST AC SWITCH

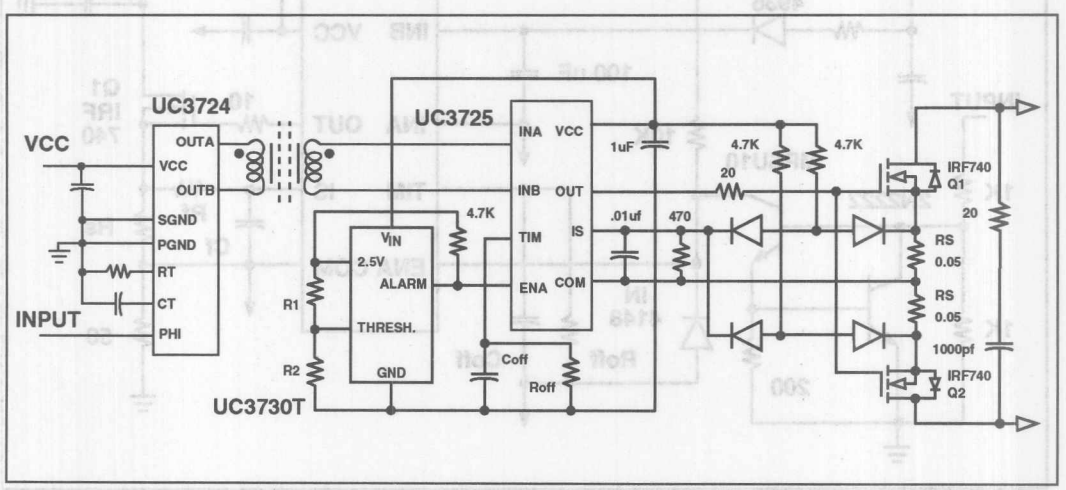


Figure 18

FAST AC SWITCH

Fully isolated gate drive lends itself to unique power switching circuits which are otherwise extremely difficult to implement. Figure 18 is a fast AC switch with over-current and over-temperature protection. The MOSFETs are selected to withstand the peak AC voltage, with each FET blocking in the opposite polarity. Figure 19 shows a 100 ohm load switched across 115 VAC, 60 Hz. The diode network allows current sensing in both directions, with the 4.7K resistors functioning as current sources. Protection against excessive MOSFET junction temperature is accomplished by mounting both FETs and the UC3730T on the same heatsink. MOSFET thermal resistance (junction to heatsink), and maximum FET dissipation must be considered when selecting the shut-down temperature set by R1 and R2. Refer to UC3730 data sheet for additional information. A 1000pf/20 ohm snubber is connected across the switch to reduce turn-off voltage spiking. The actual snubber values required are determined by load conditions.

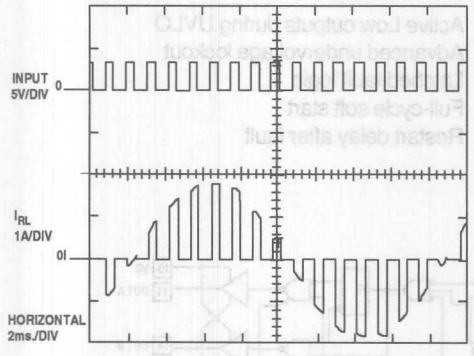


Figure 19.

SUMMARY

A unique integrated circuit pair, the UC3724/UC3725 has been presented that provides a simple, low cost, isolated MOSFET gate drive solution. Protection features prevent abnormal gate drive voltage, and provide over-current limiting. Duty cycle or on time limitations typical of other techniques are avoided, and by utilizing a transformer for isolation, there are no inherent isolation voltage limitations. The circuit is suitable for fully isolated systems which must meet UL or VDE requirements, as well as typical high-side switch applications.

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APPLICATION NOTE

THE UC3823A,B AND UC3825A,B ENHANCED GENERATION OF PWM CONTROLLERS

BILL ANDREYCAK

ABSTRACT

This application note will highlight the enhancements incorporated in four new PWM control ICs, the UC3823A, UC3823B, UC3825A and UC3825B devices. Based upon the industry standard UC3823 and UC3825 controllers, this advanced generation features several key improvements in protection and performance over their predecessors. Newly developed techniques such as leading edge blanking of the current sense input and full cycle soft start protection following a fault have been incorporated into the design. Numerous enhancements to existing standard functions and features have also been made.

INTRODUCTION

Higher degrees of integrated functions within PWM IC controllers are necessary to remain in pace with todays advancing power supply technology. Many external features, used almost universally by designers, have been built into this new generation of UC3823A,B and UC3825A,B PWM controllers. These control enhancements can be classified as either a performance or protection improvement, and an itemized description of each will be presented. The new features are:

PERFORMANCE IMPROVEMENTS

- Lower startup current
- Accurate oscillator frequency
- Leading Edge Blanking
- Higher current totempole outputs
- Higher G.B.W. Error Amplifier

PROTECTION ENHANCEMENTS

- Active Low outputs during UVLO
- Advanced undervoltage lockout
- Latched fault logic
- Full-cycle soft start
- Restart delay after fault

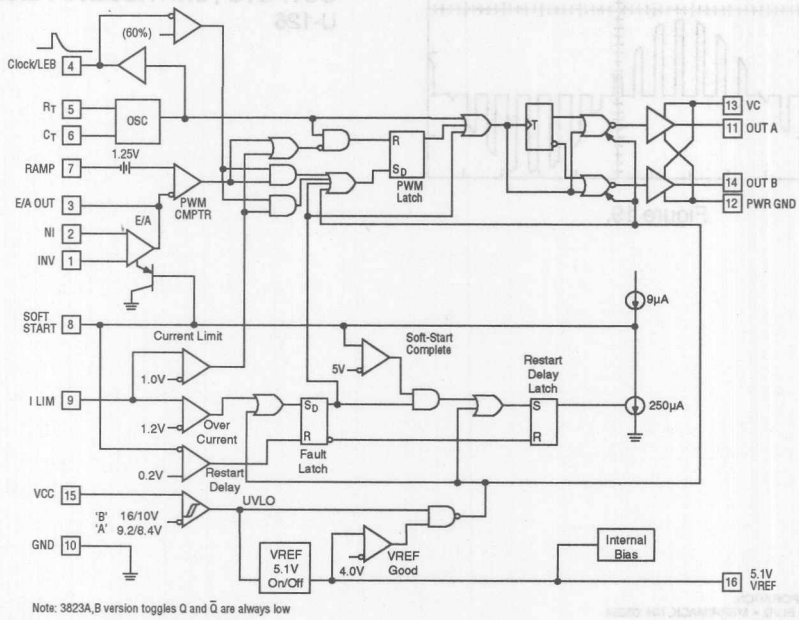


Figure 1 - UC3823A,B and UC3825A,B Block Diagram

UC3823A,B AND UC3825A,B FEATURES PREVIEW AND APPLICATIONS GUIDE

In most applications, the UC3823A and UC3825A devices are enhanced drop-in replacements for the UC3823 and UC3825 high speed PWMs. The "A" suffix versions (UC3823A and UC3825A) feature similar undervoltage lockout (UVLO) thresholds to the preceding generation which turn on at 9.2 volts and turn off at 8.4 volts. Off-line power supplies can benefit from the wider UVLO hysteresis of the "B" version devices (UC3823B and UC3825B) which turn on at 16 volts and off at 10 volts. This, in conjunction with the lower startup current of 100 microamps can streamline the IC's power supply and minimize startup circuitry power loss.

One significant difference will be found on the UC3823A and UC3823B controllers. Formerly, the UC3823 (non A or B version) provided access to the current limit comparator's threshold at pin 11. This could be accurately set by the user within the range of 1.0 to 1.25 volts with an external reference voltage. The UC3823A and UC3823B devices use pin 11 as a high current totempole output, identical to that found on pin 14. These outputs can be paralleled - effectively doubling the peak output current capability to 4 amps. No access to the previous current limit reference (I LIM REF) comparator is provided as this threshold is internally set to 1.0 volts with a +/- 5% accuracy over all operating conditions. Existing applications can incorporate the UC3823A or UC3823B devices by simply removing any of the former external biasing components to pin 11.

One other major difference to the prior generation of PWMs is the reduced maximum operating supply (Vcc) and collector supply (Vc) voltages of 22 volts versus 30 volts. This characteristic is a principal consideration when determining the IC power supply, as nearly all applications utilize a supply voltage between 10 and 15 volts. Typical supply current is higher; 28 mA versus the former 22 mA, however the maximum Icc is unchanged at 33 mA.

Since many of the enhancements in this new family of PWMs are executed using internal circuitry, most applications require no additional components externally to realize a performance or protection advantage. The list of improvements which includes latched fault protection and full cycle soft start should not require any PC board changes. The leading edge blanking feature, however, will require one capacitor from the CLOCK/LEB (pin4) to ground to facilitate programming.

The improved oscillator section can be optimally programmed for the correct frequency and maximum duty cycle combination. No changes to the timing component values of Rt and Ct are necessary. Additionally, high frequency current mode applications can benefit from the high gain bandwidth error amplifier (12 MHz). Unity gain bandwidth is also up from 5.5 MHz to 9 MHz. This should not require changes to the PC board layout unless the compensation circuit design relied upon the older 5.5 MHz UGBW for high frequency roll-off.

STARTUP FEATURES

Since a majority of PWM applications are off-line converters, a low startup current is desirable. This attribute minimizes the complexity and power loss of the startup power supply once normal operation is attained. Every milliamp of additional startup current drawn by the controller results in a power loss of approximately 385 milliwatts in a power factor corrected application. Heat, PC board real estate and additional cost are unnecessary extras which can be eliminated with a lower startup current controller.

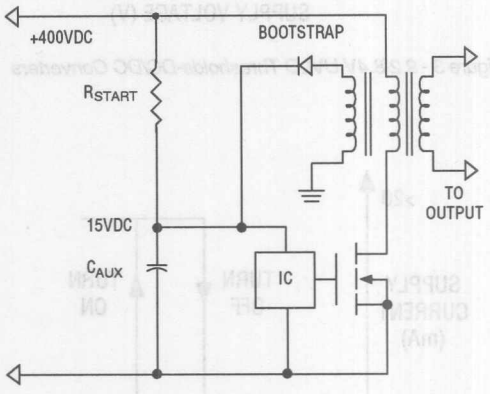


Figure 2 - Startup/Bootstrap Circuit

This new generation of UC3823A,B and UC3825A,B control ICs minimizes the startup current to 100uA typically. Once the IC crosses its undervoltage lockout threshold, the current drawn will increase to the typical running current.

In an off-line converter, two things are necessary to get the main converter up and running when the control IC turns on. First, the IC should contain wide undervoltage lockout hysteresis. Second, the bootstrap supply should come up and into regulation very quickly before the auxiliary capacitor voltage drops below the ICs lower (turn-off) undervoltage lockout threshold.

Undervoltage lockout thresholds are primarily determined by the allowable MOSFET gate voltage range. Operation with gate-to-source voltages above sixteen volts can cause overstress to the device, and voltages lower than about nine volts can cause linear FET operation. The "B" suffix designator (UC3823B and UC3825B) is used to define devices which exhibit typical undervoltage lockout thresholds of

16V (turn-on) and 10V (turn-off) for off-line applications. The "A" suffix parts (UC3823A and UC3825A) incorporate 9.2V (turn-on) and 8.4V (turn-off) thresholds for DC to DC converter applications, and are compatible with existing UC3823 and UC3825 (non A,B) UVLO thresholds.

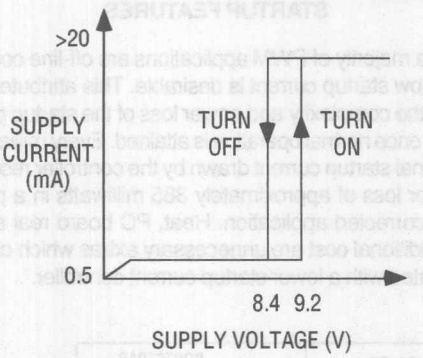


Figure 3 - 9.2/8.4V UVLO Thresholds-DC/DC Converters

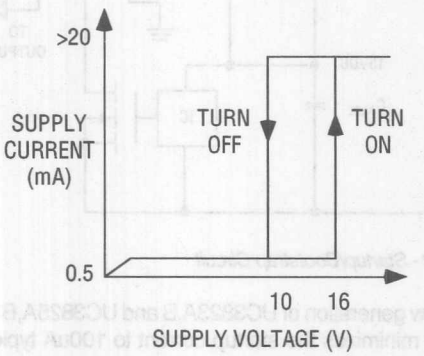


Figure 4 - 16/10V UVLO Thresholds-Off Line Power Supplies

SELF BIASING, ACTIVE LOW OUTPUTS DURING UV LOCKOUT

Another enhancement to the new UC3823A,B and UC3825A,B controllers is found in the output stages. During undervoltage lockout almost all internal functions of the control IC are disabled, primarily to obtain a low startup current. Generally, this would result in little or no available bias to actively keep the outputs low during this power-up condition, when it's needed the most. Outputs are in a high impedance state which is typically about 1 megohm. As the DC (bulk) high voltage rises, a capacitive divider is formed at the MOSFET switch between the drain-to- gate and the gate-to-source capacitances. A quickly rising bulk supply can couple a problematic gate drive command to any FET driven without a gate pull down circuit. Since the control IC is below its turn on threshold, the unbiased output drivers of older PWMs cannot prevent the switch from turning on under these circumstances.

One solution to prevent this parasitic turn-on during undervoltage lockout is to incorporate an active low, self biasing totem-pole design in the driver output. As shown in figure 5, a PNP drive transistor (Q2) is connected between the output pin of the IC and the lower NPN output transistor (Q3). As the output voltage rises, transistor Q1 is biased on through the 50K ohm resistance. This causes the base of Q2 to go low, turning Q2 on. The output pin supplies drive bias to the main totem-pole transistor, Q3, directly through the saturated PNP. Increasing voltage on the output pin provides more drive to transistors Q1, Q2 and Q3. The saturation voltage of this circuit at moderate currents (10mA) is well below the turn on thresholds of the power switching MOSFETs. This circuit is removed from operation once the undervoltage lockout requirements have been satisfied. Transistor Q4 is turned on with a valid UVLO which voids the possibility of transistor Q1 from ever turning on during normal operation. Additionally, a 250 microamp current source from Vcc keeps the PNP predriver (Q2) off after UVLO.

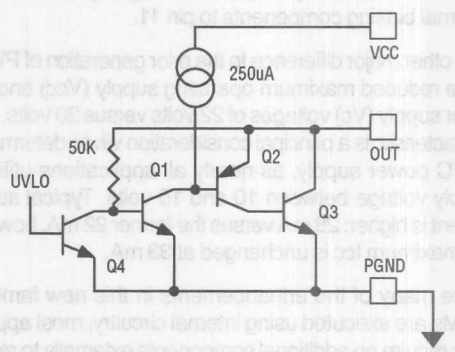


Figure 5 - UVLO Self Biasing Outputs

Another benefit of this technique is obtained during power down. As the IC crosses below its lower UVLO threshold, the self biasing circuitry is enabled. Any residual voltage on the output will similarly turn the totempole stage on which actively pulls the output low. This feature insures correct gate drive operation regardless of the turn off sequence.

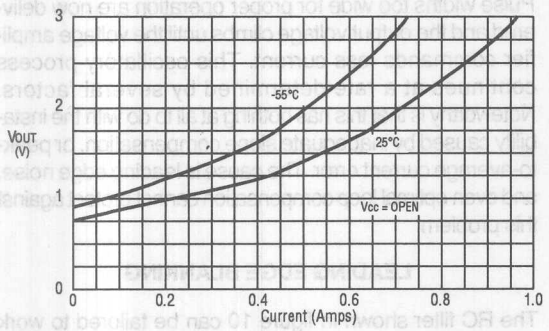


Figure 6 - Output V and I During UVLO

OSCILLATOR ACCURACY

Fundamental to the design of any switchmode converter is maintaining an accurate switching frequency. The UC3823A/B and UC3825A/B ICs utilize two pins for the sawtooth oscillator; one each for the timing resistor (Rt) and timing capacitor (Ct). The resistor programs the charging current to the timing capacitor via an internal current mirror with high accuracy. Maximum switch on-time is determined by the rising capacitor voltage whereas deadtime, the programmed switch off time is determined by the timing capacitors discharge.

Considerable improvement has been made to the accuracy of the oscillator discharge current. The previous generation of UC3823/25 devices endured variations of plus or minus forty percent (+/- 40%) over the full military temperature range and production tolerances. This new generation of UC3823A/B and UC3825A/B PWM controllers features a well controlled oscillator discharge current which is "trimmed" at wafer probe testing to +/- 1 milliamp. Oscillator initial accuracy (400 KHz nominal) has been tightened to 375 KHz minimum and 425 KHz maximum. Total variation over all line and temperature ranges is limited to 350 and 450 KHz. A new specification for 1 MHz accuracy has been added, demonstrating a plus or minus fifteen percent total frequency variation at high frequency.

CLOCK OUTPUT

The UC3823A,B and UC3825A,B controllers also feature a TTL/CMOS compatible CLOCK output pin. Specified amplitudes are 3.7 volts in the high (off) state and 0.2 volts during its low state. Additionally, this pin is also used for programming of the leading edge blanking function. Notice that unlike their non A,B predecessors, these enhanced versions cannot be externally synchronized by an input to the clock pin. Synchronization is obtained by forcing a SYNC pulse across a resistor in series with the timing capacitor.

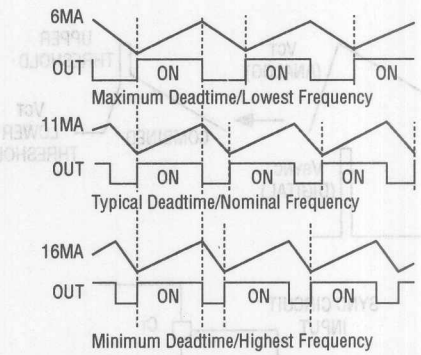


Figure 7 - Frequency and Deadtime Variations vs. Discharge Current Tolerances

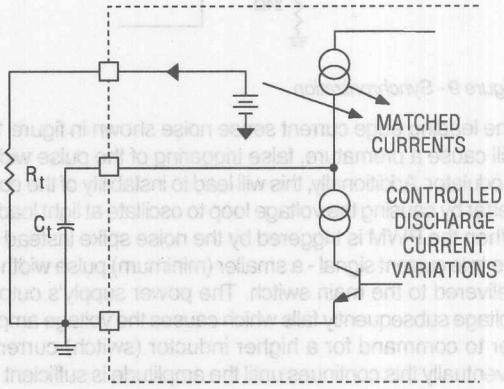


Figure 8 - Controlled Discharge Current

LEADING EDGE NOISE IN THE CURRENT SENSING CIRCUIT

One of the most difficult tasks with peak current mode control is sensing the inductor current. Instead, switch current is generally sensed by means of either a series resistor or current sense transformer. There is some difficulty with using this technique accurately, especially at light current levels. As the switch turns on, circuit parasitics in the power stage, output rectifier reverse recovery characteristics and high current gate drive pulses can create significant noise pulses on the leading edge of the current sense signal. Traditionally, this problem has been overcome by adding a small R-C noise filter between the current sense resistor and the PWM controllers current sense input. At low operating frequencies and high output current levels this R/C filtering technique will generally deliver satisfactory results. However, at higher switching frequencies, and almost always at lighter load currents the leading edge spike amplitude can greatly exceed the peak current sense signal.

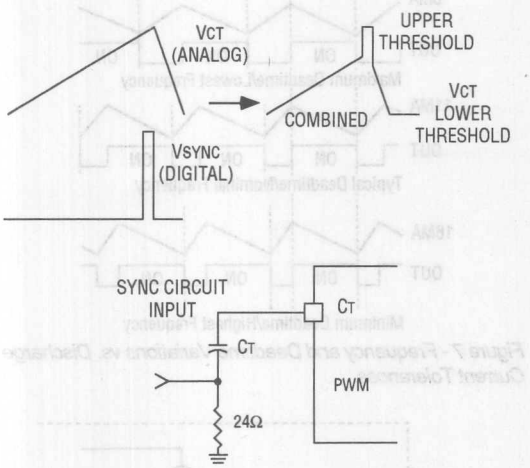


Figure 9 - Synchronization

The leading edge current sense noise shown in figure 10 will cause a premature, false triggering of the pulse width modulator. Additionally, this will lead to instability of the converter by causing the voltage loop to oscillate at light loads. When the PWM is triggered by the noise spike instead of the true current signal - a smaller (minimum) pulse width is delivered to the main switch. The power supply's output voltage subsequently falls which causes the voltage amplifier to command for a higher inductor (switch) current. Eventually this continues until the amplitude is sufficient to rise above the leading edge noise spike.

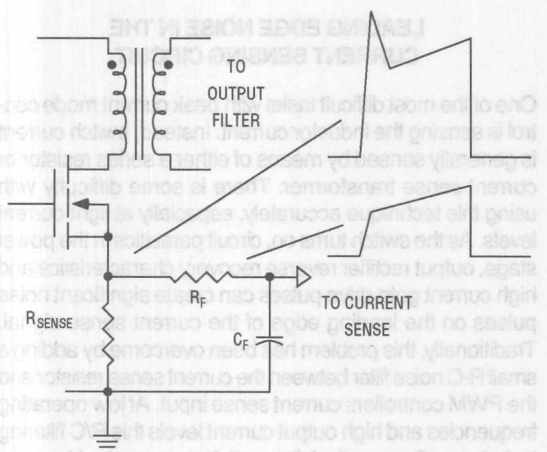


Figure 10 - Current Sensing Technique

Pulse widths too wide for proper operation are now delivered and the output voltage climbs until the voltage amplifier commands less current. This oscillatory process continues at a rate determined by several factors. Noteworthy is that this has nothing at all to do with the instability caused by inadequate slope compensation, or peak-to-average current error. The cause is leading edge noise, and even optimal loop compensation cannot protect against this problem.

LEADING EDGE BLANKING

The RC filter shown in figure 10 can be tailored to work well over a limited range of applications and power levels. Another technique, known as Leading Edge Blanking (LEB) essentially blindfolds (blanks) the PWM comparator for a specific amount of time during the beginning of the cycle. The blanking duration is user programmable and should correspond to the width of the leading edge noise spike. This eliminates the need for filtering of the current sense signal in peak current mode controlled circuits.

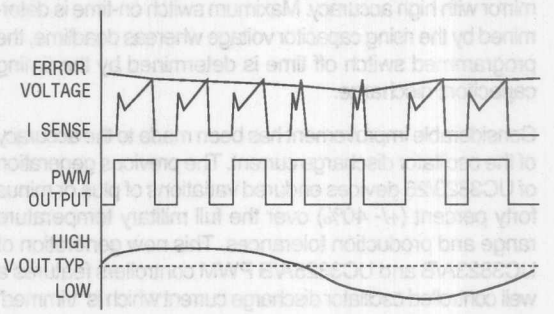


Figure 11 - Instability Caused By Leading Edge Noise Triggering

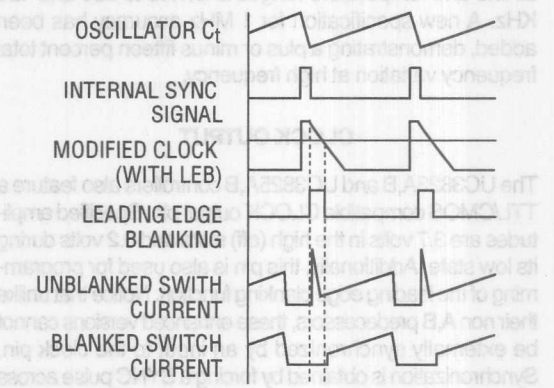


Figure 12 - Leading Edge Blanking Operational Waveforms

LEB IMPLEMENTATION

The focal point of any fixed frequency PWM controller is its clock. Used to accurately program the switching frequency and maximum duty cycle, the clock serves as the trigger source for the leading edge blanking circuitry. A digital representation of the timing capacitor charge/discharge status is developed by internal logic. This is made available at the PWMs CLOCK pin for external purposes. The UC3823A,B and UC3825A,B all use a high output to indicate the OFF period of the switching cycle, and a low to indicate the maximum ON time. These levels will be incorporated into the design of the leading edge blanking circuitry.

The clock output of the UC3823A,B and UC3825A,B is pulled high during the oscillator deadtime to approximately 4 volts. A capacitor added to the CLOCK output pin programs the leading edge blanking duration. An internal comparator with an accurate threshold set at 60% of the peak clock amplitude has been added. The LEB programming capacitor is discharged by an internal 10K ohm resistance to ground. The LEB interval is defined by the time required for the capacitance to discharge from 4 volts to the 60% threshold. Once the LEB capacitor discharges below this threshold, the PWM operates normally without any blanking. Programming should accommodate the worst case of leading edge noise. With no programming capacitor added, the ICs function similarly to their predecessors and provide no blanking.

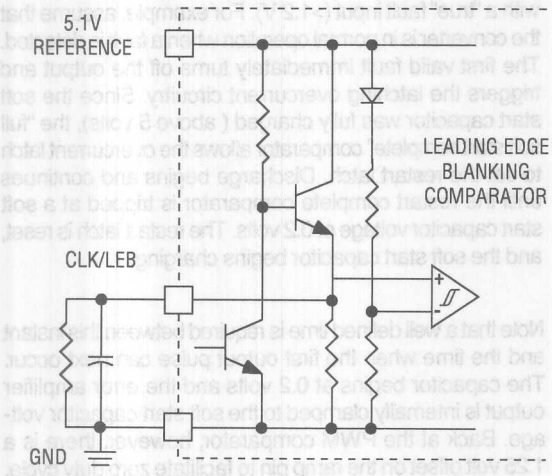


Figure 13 - LEB Circuitry

Because of the leading edge blanking, the PWM outputs will exhibit a minimum ON time in normal operation. The duration corresponds directly to that of the LEB programming, so a minimum duty cycle has also been established. Resolution between zero duty cycle and this minimum duty cycle cannot be obtained - which should also be taken into account when programming the LEB circuitry.

Zero duty cycle is a valid operating condition which can be achieved by one of two methods. The most obvious technique is to bias the error amplifier such that its output is driven below the PWM zero duty cycle threshold of 1.1V. The ICs error amplifier can easily accomplish this while sinking current up to 1 mA, worst case. The second technique utilizes the current limiting feature (ILIM) at pin 9. An ILIM input held above the 1.2V (typ) FAULT threshold will force the PWM's on-time and duty cycle to zero. More details of the interface between the PWM and fault circuitry will be found in the following fault protection section.

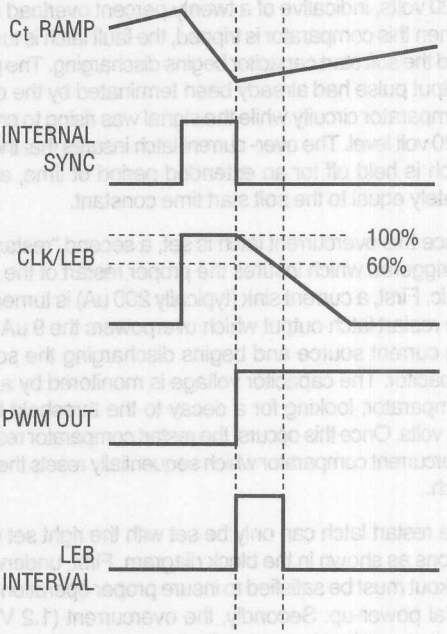


Figure 14 - Blanking Waveforms

LATCHED FAULT PROTECTION

While the previous generation of control ICs offered fault protection circuitry, they did not feature a fully latched shutdown after detecting a fault. The unlatched technique only

discharges the soft start capacitor during the duration of the fault - a duration which can be very brief with a high speed controller. As a result, the duty cycle is not significantly reduced, and the IC continues delivering output pulses at the the switching frequency. Typically, the switching components can easily be dangerously overstressed while also dissipating a significant amount of power.

The new UC3823A,B and UC3825A,B controllers feature a latched fault protection circuit as shown in figure 15. Two comparators are used to offer two stage protection - depending on the amplitude of the fault. The first comparator has a one volt threshold for cycle-by-cycle current limiting. In normal operation this terminates the immediate switch drive pulse but does not trigger the latching fault logic. One volt has been selected as the peak amplitude of the current sense signal for normal operation and slight overloads to accommodate transients.

The second comparator has a slightly higher threshold of 1.20 volts, indicative of a twenty percent overload or fault. When this comparator is tripped, the fault latch is turned on and the soft start capacitor begins discharging. The present output pulse had already been terminated by the one volt comparator circuity while the signal was rising to cross the 1.20 volt level. The over- current latch insures that the PWM latch is held off for an extended period of time, approximately equal to the soft start time constant.

Once this overcurrent latch is set, a second "restart" latch is triggered which insures the proper restart of the control logic. First, a current sink (typically 200 uA) is turned on by the restart latch output which overpowers the 9 uA charging current source and begins discharging the soft start capacitor. The capacitor voltage is monitored by a restart comparator, looking for a decay to the threshold level of 0.2 volts. Once this occurs, the restart comparator resets the overcurrent comparator which sequentially resets the restart latch.

The restart latch can only be set with the right set of conditions as shown in the block diagram. First, undervoltage lockout must be satisfied to insure proper operation during initial power-up. Secondly, the overcurrent (1.2 V) comparator must be triggered, indicative of a valid fault. Last, and most important, is that a full soft start cycle must be completed before the restart latch can be retriggered. A fourth comparator insures that the soft start capacitor voltage has charged to a 5 volt threshold. This indicates that a complete discharge followed by a complete charge has occurred.

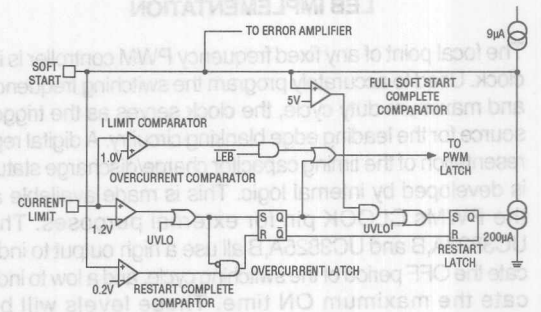


Figure 15 - Latched Fault And Full Cycle Soft Start Protection Circuitry

FULL CYCLE / CONTINUOUS FAULTS

During a fault, many designers prefer to reduce the repetition rate at which the switch is driven rather than to continue at the normal switching frequency. Often called "hiccup", this delayed restart will significantly reduce the overstress and power dissipated during abnormal conditions. Implementation of the latched fault technology results in significantly lower power dissipation during a continuous fault or shorted output stage. Instead of delivering minimum duty cycle pulses at the oscillator frequency, the retry sequence occurs at a repetition rate approximately equal to the soft start period with a continuous fault.

In the worst case, two PWM outputs can occur in a time less than the soft start time constant, but this happens only once with a "true" fault input (>1.2 V). For example, assume that the converter is in normal operation when a fault is detected. The first valid fault immediately turns off the output and triggers the latching overcurrent circuitry. Since the soft start capacitor was fully charged (above 5 volts), the "full soft start complete" comparator allows the overcurrent latch to set the restart latch. Discharge begins and continues until the restart complete comparator is tripped at a soft start capacitor voltage of 0.2 volts. The restart latch is reset, and the soft start capacitor begins charging.

Note that a well defined time is required between this instant and the time when the first output pulse can next occur. The capacitor begins at 0.2 volts and the error amplifier output is internally clamped to the soft start capacitor voltage. Back at the PWM comparator, however, there is a 1.25 volt offset on the ramp pin to facilitate zero duty cycle. Therefore, the soft start capacitor must charge from 0.2 volts to 1.25 volts before the PWM comparator is active.

This provides a slight interval between the worst case of successive output pulses into a shorted load. From this point on, the soft start capacitor must fully charge up to the five volt threshold of the "full soft start complete" comparator. Once in this mode, only one PWM output per soft start period can be obtained into a fault as shown in figure 16.

LEB AND FAULT DETECTION

The leading edge blanking circuitry is interfaced to also blank some of the fault detection circuitry. While numerous arrangements are possible, only one configuration offers a reasonable compromise between quick response and noise immunity. As demonstrated in figure 12, leading edge blanking does inhibit the one volt, cycle-by-cycle current limit comparator during the programmed interval. However, the blanking does not disable the 1.2 volt overcurrent comparator and fault logic. This adaptation will accommodate a moderate amount of leading edge noise without having to significantly filter the current sense, and fault signals. Even if a moderate amount of filtering is required, the latched full cycle shutdown protection minimizes the power dissipation.

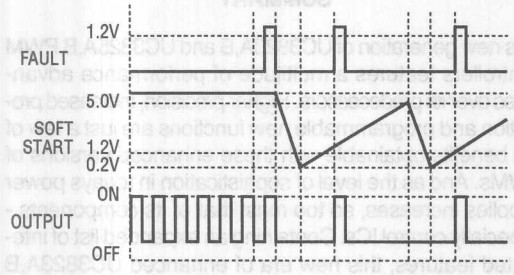


Figure 16 - Full Cycle Soft Start - Operational Waveforms

TIGHTER FAULT THRESHOLDS

This latest generation of IC controllers utilizes a thin film resistor process which provides improved control of the tolerance. These resistors are used to generate accurate voltage thresholds by dividing down the IC's reference voltage internally. Both of the current limiting comparator thresholds have been tightened in the "A" and "B" versions of controllers. The cycle-by-cycle current limit threshold range has been tightened to +/- 5% from its previous +/- 10% specification. The new limits are 0.95V minimum, 1.05V maximum with the center remaining at the previous 1.0 volts.

The overcurrent (fault) threshold, however, has been centered at 1.2 volts instead of the 1.4 volt midpoint of the non A,B versions. The new specifications are 1.14 volts minimum to 1.26 volts maximum. Applications converting to the newer controllers may need to adjust the current sense resistor value accordingly. Typical propagation delay is unchanged at 50 ns typical, and 80 ns maximum.

HIGHER GAIN-BANDWIDTH ERROR AMPLIFIER

Many of the critical UC3823/25 error amplifier specifications have been improved. The characteristics which significantly differ are: input offset voltage - reduced from 10 to 7 mV, unity gain bandwidth - increased from 5.5 MHz to 9 MHz, typical slew rate - reduced from 12 to 9 V/us. Notice that the minimum slew rate is unchanged at 6 V/us.

HIGH POWER OUTPUTS

The industry need for higher switching frequencies and improved efficiency has directly effected the design of the totem-pole output drivers. Many of the capacitive loads (MOSFETS) placed directly on the PWM outputs require high peak currents to obtain adequate switching transitions. The high speed UC3823A,B and UC3825A,B controllers feature peak current ratings of 2 amps, and are capable of slewing 15 volts in 35 nanoseconds into 1000pF. Separate collector supply (Vc) and power ground connections (PGND) help decouple the analog circuitry from the high power gate drive noise.

TYPICAL APPLICATION

The 1.5 MHz, 50 Watt push-pull converter detailed in Application Note U-110 was redesigned to accept the UC3825"B" device. The basic power stage remained similar while an emphasis was placed on control circuit improvements. These enhancements included Leading Edge Blanking of the current sense signal and Restart Delay following a fault. Also, a current sense transformer was installed which not only reduced losses but allowed amplification of the current sense signal to approximately 2.5 volts, thus enhancing noise immunity.

Improvements to the power section of the converter include the use of larger MOSFETS (IRF640's) and the addition of a bootstrap winding for the auxiliary bias supply. The startup resistor from the input supply was increased since the UC3825"B" device features a wide UVLO hysterisis of six volts.

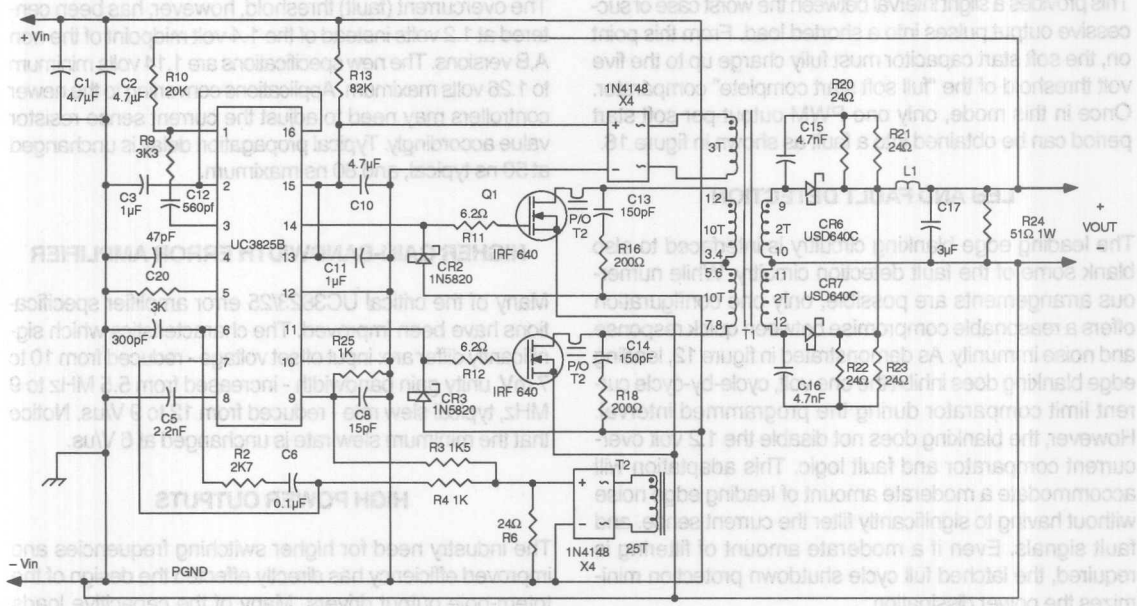


Figure 17 UC3825B Controlled 1.5 MHz Push Pull Converter

CONVERTER PERFORMANCE

The redesigned converter exhibited similar line, load and transient response to the original converter, which was excellent due to the high conversion frequency. A significant improvement was made in the short circuit performance by comparison. While operating into a continuous short circuited output, the UC3825"B" controlled version reduced the converter input power (and dissipation) to approximately one-hundredth of the original design. Featuring the programmable Restart Delay circuitry, the redesigned 50 Watt converter draws only one-quarter of a Watt (1/4 W) of input power with a shorted circuited output.

SUMMARY

This new generation of UC3823A,B and UC3825A,B PWM controllers features a multitude of performance advantages over its predecessors. Higher precision, increased protection and programmable new functions are just a few of the benefits obtainable with these enhanced versions of PWMs. And as the level of sophistication in todays power supplies increases, so too must that of its components - especially control ICs. Containing an expanded list of integrated features, this new era of enhanced UC3823A,B and UC3825A,B controllers overcomes the challenges of the power supply industry for higher levels of power, protection and performance.

ADDITIONAL INFORMATION AND REFERENCES

1. New Pulse Width Modulator Chip Controls 1 MHz Switchers; UNITRODE Application Note # U- 107
2. 1.5 MegaHertz Current Mode IC Controlled 50 Watt Power Supply; UNITRODE IC Databook, Application Note # U-110
3. "Practical Considerations in Current Mode Power Supplies"; UNITRODE IC Databook, Application Note # U-111

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UC3907 LOAD SHARE IC SIMPLIFIES PARALLEL POWER SUPPLY DESIGN

MARK JORDAN
SENIOR DESIGN ENGINEER

INTRODUCTION

Many power supply manufacturers have found it economically feasible to make standard modular power supplies which are easily paralleled for higher current applications. If special provisions are not made to equally distribute the load current among the paralleled supplies, then one or more units will hog the load current leaving the other units essentially idle. This results in greater thermal stresses on specific units and a reduction in the system reliability. For example, reliability predictions will indicate that a component operating at 50 degrees above ambient will have one-sixth the lifetime of the same component operating at 25 degrees above ambient [1].

This paper will examine methods for load sharing presently being implemented discretely and then cover Unitrode's single chip solution, the UC3907 Load Share Controller, in several parallel power applications.

SYSTEM REQUIREMENTS

The basic requirements of a power supply system consisting of a number of sources paralleled to increase the total load current are:

- Maintain a regulated output voltage under variations in line or load.
- Control the output current of each supply so they share the total load current equally.

To maximize reliability of the system, there are the following features:

- Achieve redundancy, so that a failure of any one supply can be tolerated as long as there is sufficient current capacity available from the remaining power units.
- Implement a load sharing method without any external control system.

In addition, these are the following desirable features:

- To have a common, low bandwidth share bus interconnecting all power units.
- Achieve good load sharing transient response.
- The ability to margin the system output voltage with one control.

In other words, the combination of power supplies behave like one large supply with equal stress on each of the units. Also, reliability can be optimized by taking advantage of load sharing to incorporate modular redundancy.

LOAD SHARING TECHNIQUES

There are a number of schemes to achieve load sharing. Five approaches are discussed here, with an attempt made to investigate their application, highlighting features and concerns.

THE DROOP METHOD

The simplest method to load sharing is referred to as the droop method. It is an open loop technique which programs the output impedance of the power supplies to obtain load sharing. This method exhibits very poor current sharing at low currents and improves at higher currents, but can still have large current imbalances between supplies. An example of this method is shown in Fig 1 where as the individual supply current increases, the feedback voltage will decrease. This will allow other supplies to distribute more current. The programmed output impedance is given by:

$$Rout = 0.01\ Rs\ N$$

The disadvantages to the droop method are: degradation of load regulation, each module must be individually tweaked to achieve good current sharing, and difficulty in current sharing between parallel modules with different power ratings.

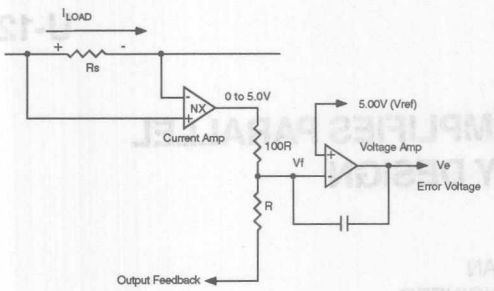


Fig 1 - The Droop method programs the output impedance of the power supplies to achieve load sharing. It is a simple open loop method, but is not accurate.

DEDICATED MASTER

Current mode supplies can accommodate several configurations to achieve a form of load sharing. One approach is to select a master module to perform the voltage control and force the remaining modules (slaves) to act as current sources, as shown in Fig. 2. This technique is facilitated with current mode control, since the error voltage is proportional to load current. If the units were similar in design then a given error voltage on the output of the voltage, or error amplifier will force all units to source the same load current. This technique achieves load sharing but does not achieve redundancy, since if the master fails, the entire system becomes disabled. Another concern with this technique is that the high bandwidth voltage loop is being bussed around the system and is prone to noise pick-up.

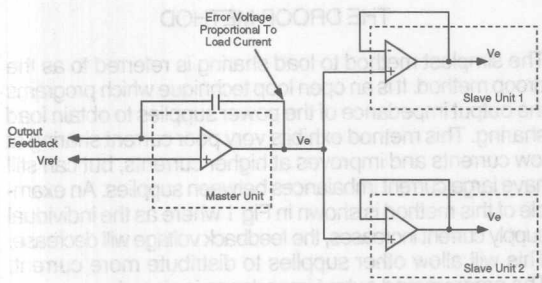


Fig 2 - A dedicated Master approach with current mode supplies will facilitate current sharing but does not achieve redundancy.

EXTERNAL CONTROLLER

Another method is to use an external controller to perform the load sharing. This is achieved by comparing all load sharing signals from the individual power units and adjust the corresponding feedback signal to balance the load currents. This system does perform well but requires an additional controller and multiple connections between the controller and each supply.

AUTOMATIC CURRENT SHARING - AVERAGE CURRENT METHOD

For Automatic current sharing no external controller is required and a single share bus interconnects all the supplies. This requires an adjustment amplifier that compares a current signal from the share bus to the individual units current, and adjusts the reference of the voltage amp until equal load current distribution is achieved.

The average Current method is a patented technique where each power module's current monitor drives a common share bus via a resistor, as shown in Fig 3. The adjust amplifier will sense if there is a differential across the resistor, equating to a load current imbalance, and adjusts the reference accordingly. The node where all resistors connect is a representation of the average load current contribution. While this scheme performs accurate current sharing, it can result in specific application problems. An example is when a supply runs into current limit, causing the share bus to be loaded down and the output voltage to regulate to the lower adjust limit. A similar failure mode will exist if the share bus is shorted or if any unit on the share bus is inoperative.

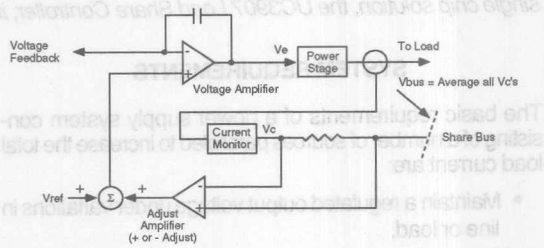


Fig. 3 - The average current method compares the individual load currents to the average load current.

AUTOMATIC CURRENT SHARING - HIGHEST CURRENT METHOD

This technique for automatic current sharing shown in Fig 4 compares the highest current module to each individual current, and adjusts the reference voltage accordingly to correct the imbalance of load current. This technique is similar to the average current method except that the resistor is replaced with a diode, allowing only one unit to communicate on the share bus. This method provides for excellent sharing among the slaves with an error in the master's load current contribution because of the diode.

The UC3907 Load Share Regulator has improved on this method by replacing the diode with a unidirectional buffer to reduce the master's error. An inoperative or insufficient capacity supply will not effect the sharing of the operational units. A shorted share bus will disable the reference adjustment section used for load sharing, making the units operate as stand alone.

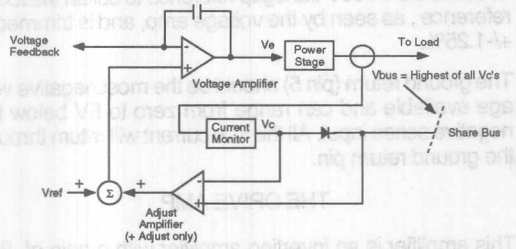


Fig. 4 - The highest current method compares the individual load currents to that of the highest. This method has several advantages over the average current method of load sharing. The UC3907 has implemented and improved version of this technique.

USING THE UC3907 - LOAD SHARE REGULATOR IC

A review of the current sharing technique used on the UC3907 and operating principles will help the reader to understand the application examples that follow and to use the IC in other examples.

A generic load share system with the basic bus connections required to perform accurate output voltage control and load sharing is shown in Fig 5. The output voltage is sensed with a fully differential, high-impedance voltage amplifier. Each individual power supply current is sensed with a differential current amplifier, and is used for the load share portion of the circuit. The share bus signal interconnecting all the paralleled modules is a low-impedance, noise insensitive line. The connection diagram is shown in FIG 6. The following discussion of the voltage and current sharing loops should help the reader understand the operation and features of the IC.

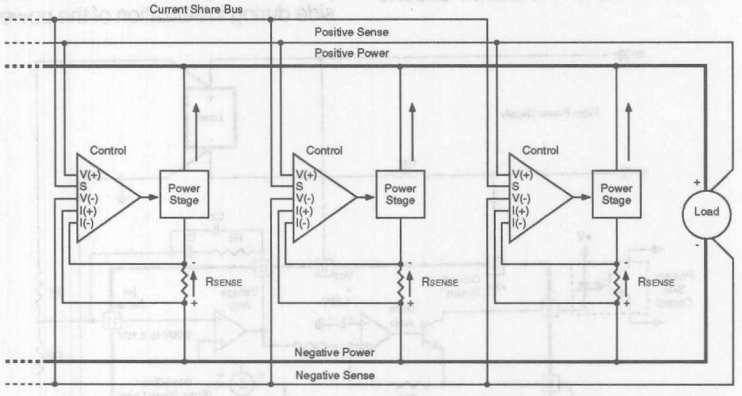


Fig. 5 - System connections for modules with independent load sharing.

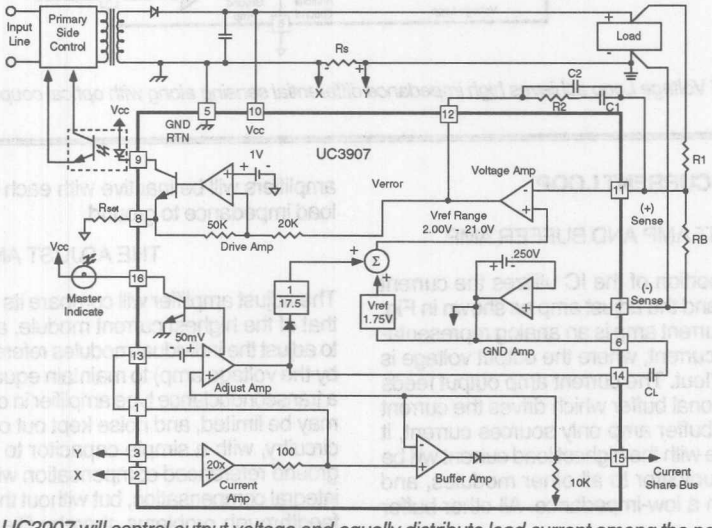


Fig. 6 - The UC3907 will control output voltage and equally distribute load current among the power modules.

THE VOLTAGE LOOP

THE VOLTAGE AMP

This Amplifier is the feedback control gain stage for the power modules output voltage regulation, and the overall voltage loop compensation will normally be applied around this amplifier. The output swing is limited to 2 Volts to improve the large signal response of the system. The voltage amplifier accomplishes the high impedance positive sensing, and the ground amp, the high impedance negative sensing.

THE GROUND AMP

This amplifier is a unity gain buffer with a 0.250V offset. The offset allows the amplifier negative headroom to return all control bias and operating currents while maintaining a high impedance negative sense input (pin 4), where this input is referred to as "true" ground. The output of this amplifier is referred to as Artificial Ground. The 0.250V offset is added to the 1.750V bandgap reference to obtain the 2.00V reference , as seen by the voltage amp, and is trimmed to +/-1.25%.

The ground return (pin 5) should be the most negative voltage available and can range from zero to 5V below the negative sense input. All the IC's current will return through the ground return pin.

THE DRIVE AMP

This amplifier is an inverting amplifier with a gain of -2.5, which couples the feedback signal to the power controller. The Current setting resistor Rset helps to establish the forward transfer function of the control loop and the maximum drive current. The polarity of the drive amp stage is such that an increasing voltage at the plus sense input (pin 11), will increase the opto-couplers current, thereby reducing the primary side PWM's duty cycle. This will insure proper startup since there is no energy on the secondary side during initialization of the power system.

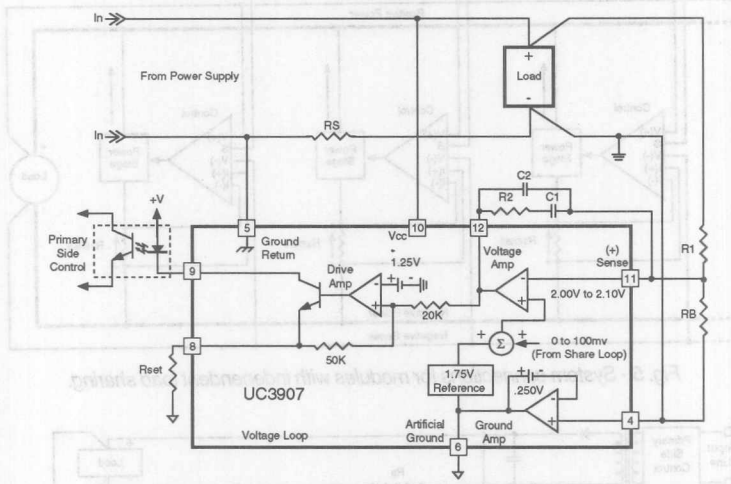


Fig. 7 - The UC3907 Voltage Loop achieves high impedance differential sensing along with optical coupler driving capability.

THE CURRENT LOOP

THE CURRENT AMP AND BUFFER AMP

The current sharing portion of the IC utilizes the current amp, the buffer amp, and the adjust amp as shown in Fig. 8. The Output of the current amp is an analog representation of individual load current, where the output voltage is given by: Vca=20*Rs*Iout. The current amp output feeds an input of a unidirectional buffer which drives the current share bus. Since the buffer amp only sources current, it insures that the module with the highest load current will be the master, or communicator to all other modules, and drives the bus through a low-impedance. All other buffer amplifiers will be inactive with each exhibiting a 10K ohm load impedance to ground.

THE ADJUST AMP

The adjust amplifier will compare its own load current with that of the highest current module, and force a command to adjust the individual modules reference voltage, (as seen by the voltage amp) to maintain equal current sharing. It is a transconductance type amplifier in order that its bandwidth may be limited, and noise kept out of the reference adjust circuitry, with a simple capacitor to artificial ground. The ground referenced compensation will act similar to that of integral compensation, but without the non-inverting signal feedthrough problems, thereby filtering both inputs from

unwanted noise. The adjust amplifier has a built in 50 millivolt offset on its inverting input, which forces the unit acting as a master to have a low output resulting in a zero adjust command. While the 50mv offset represents an error in current sharing, the gain of the current amplifier reduces it to 2.5 millivolts across the sense resistor. This results in all slave modules sharing equally and the master module running a few percent higher. The offset also provides some immunity from cycling, or fighting for master position due to low frequency noise.

STATUS INDICATE

The status indicate pin is designed to indicate which unit is acting as the master. Its open collector output is activated when the adjust amp output is in the low state. In a case of an overcurrent fault with one of the many paralleled units, this pin will indicate the unit with the highest current which will help diagnose the faulted module. A zero current or low current fault is transparent to the other supplies' and has no effect on voltage regulation and current sharing.

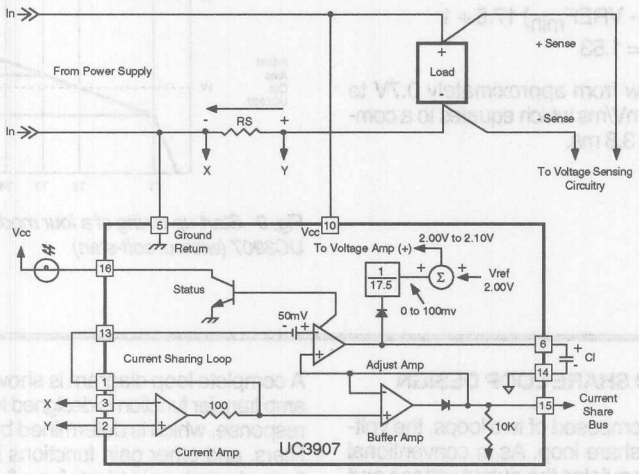


Fig. 8 - Current sharing is achieved with the UC3907 by comparing the individual module's current to that of the highest current module. The necessary adjust command increases the voltage amp reference to accomplish equal load sharing.

START-UP FOR A PARALLEL POWER SYSTEM

Start-up conditions need to be considered in a parallel power supply architecture. A start-up timing example of four 5V power modules in parallel is shown in Fig. 9. Once the primary power is applied, the power stage will be requesting maximum duty cycle until the individual units feed back a signal to regulate the output voltage. At time t1, supply #1 has become the master due to its higher reference voltage. This forces the output voltage to regulate above the other units. The other units will feedback a zero duty cycle signal to the power stage and remain idle. At this point the master unit is supplying all the supply current, and outputting the corresponding current signal on the share bus. The other units' adjust amplifiers sense the difference between their individual load currents and the master's, and start to slew up the adjust amp output to increase their references. At the same time the master's adjust amplifier output remains clamped below the adjust threshold having no effect on its original reference. At time t2 the other three adjust amps have exceeded the adjust threshold and have started to effect the reference as seen by the voltage amp.

At time t3 the unit with the closest reference to the master, supply #2, has reached the point where its references is essentially equal to the master's and the load current becomes equally distributed between the two. The other two modules, #3 and #4, are still adjusting their references and are not yet contributing to the load current. At time t4 the 3rd unit has reached the desired reference and the load current has been equally split between the three, and at time t5 the final unit has completed its reference adjustment, thereby completing the load sharing. If it is necessary to have the units come up sharing, then a soft-start scheme will need to be implemented on the primary side modulator which needs to be much slower than the adjust time. The total adjust time from t1 to t5 for this example is given by:

$$t = \frac{Cl\ Va}{I}$$

where Cl = adjust amp compensation
Va = adjust amp swing
I = Adjust amp max current - 220ua

Cl is chosen from the desired bandwidth

$$Cl = \frac{gm}{2\pi F}$$

where typ gm = 3mS and F = Adjust amp bandwidth.

If the required adjust amp bandwidth were 500 Hz, then Cl will be 1uF. The adjust amp output for the lowest reference will adjust to a voltage calculated as follows:

$$Vadj = (VREF_{max} - VREF_{min})\ 17.5 + 1$$
$$= (30mv\ 17.5) + 1 = 1.53$$

The adjust amp must slew from approximately 0.7V to 1.53V at a slew rate of 220mV/ms which equates to a complete sharing delay time of 3.8 ms.

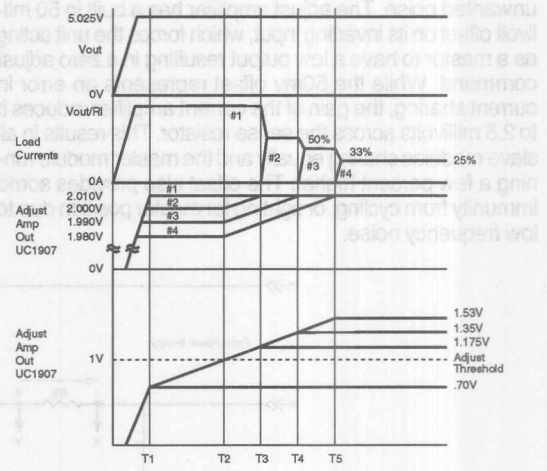


Fig. 9 - Start-up timing of a four module power system using the UC3907 (without soft-start).

THE VOLTAGE AND SHARE LOOP DESIGN

A load sharing system is composed of two loops, the voltage loop and the current share loop. As in conventional designs, the voltage loop regulates the output voltage and is the faster responding loop. The current sharing loop is a lower bandwidth loop to eliminate noise pick-up on the share line, and should be low enough in bandwidth to eliminate interactions with the voltage loop.

A complete loop diagram is shown in Fig. 10. The voltage amp transfer function is designed to optimize the voltage loop response, which is determined by the modulator topology, filters, and other gain functions in the loop. We will work through each gain block for a flyback converter example using the UC3907, and from this the user should be able to expand the design to any topology.

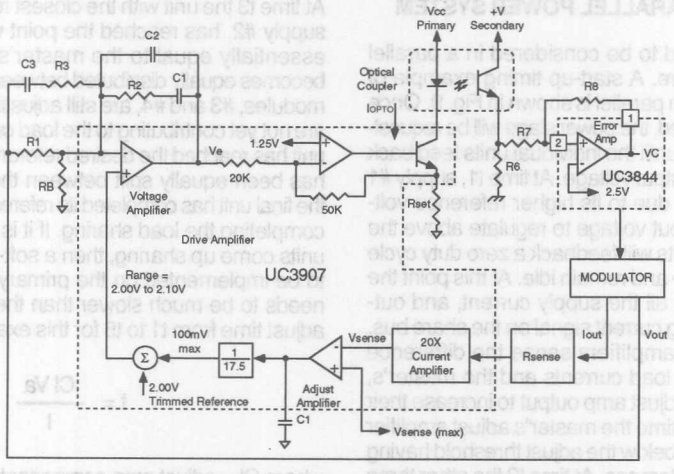


Fig. 10 - The UC3907 can be easily implemented to perform voltage control, and optical coupler drive for isolated applications.

Compensated as shown, the voltage amp response is given by:

$$UGF = \frac{1}{2\pi R_1(C_1 + C_2)} \qquad Pole = Origin$$

UGF = Unity Gain Frequency.

$$Pole\ 2 = \frac{1}{2\pi R_1 C_3} \qquad Pole\ 3 = \frac{1}{2\pi R_2\left(\frac{C_1C_2}{C_1 + C_2}\right)}$$

$$Zero\ 1 = \frac{1}{2\pi R_2 C_1} \qquad Zero\ 2 = \frac{1}{2\pi(R_1 + R_3)C_3}$$

The drive amp will convert the output of the voltage amp to an error current to be applied to the opto coupler. The current is given by:

$$I_{opto} = \frac{(1.25 - Ve)2.5 + 1.25}{Rset}$$

where Ve = output of the voltage amp - error voltage and the small signal gain is:

$$\frac{I_{opto}}{v_e} = \frac{-2.5}{Rset}$$

The control voltage for the UC3844 pulse width modulator is given by:

$$V_c = (2.5 - I_{opto}\,CTR\,R_6)\left(\frac{R_8}{R_6 + R_7}\right) + 2.5$$

where CTR is the current transfer ratio of the opto coupler. and the small signal gain is given by:

$$\frac{v_c}{I_{opto}} = -CTR\,R_6\left(\frac{R_8}{R_6 + R_7}\right)$$

therefore the UC3907 error voltage to PWM control voltage gain is given by:

$$\frac{v_c}{v_e} = CTR\,R_6\left(\frac{R_8}{R_6 + R_7}\right)\left(\frac{2.5}{R_{set}}\right)$$

The CTR spread can vary from 0.4 to 2 on a given device type, but many manufacturers can sort them out to a +/- 30% tolerance. The CTR is also a function of the driving current and therefore introduces a non-linearity in the feedback gain.

The control to output gain of the modulator for various topologies is referenced in the Unitrode power supply design seminar book. For example, the control to output gain for the discontinuous flyback with current mode control is:

$$\frac{v_o}{v_c} = \sqrt{\frac{Ro\,L\,F}{2}}\,\frac{\left(1 + \frac{S}{wz}\right)}{\left(1 + \frac{S}{wp}\right)}$$

Where $wz = \frac{1}{Rc\,C}$ $\qquad wp = \frac{1}{Ro\,C}$

Rc = esr of C's in parallel
Ro= Load resistance
C= Total output Capacitance
L= Primary inductance
F= Switching frequency

The total voltage loop gain is given by:

$$G(S) = A(s)\left(\frac{v_c}{v_e}\right)\left(\frac{v_o}{v_c}\right)$$

where A(s) is the voltage amp transfer function

To bandwidth limit the share loop, the adjust amplifier is compensated where the unity gain frequency of the adjust amp is given by :

$$F = \frac{gm}{2\pi C_l}$$

where typical gm = 3mS.

AN OFF-LINE LOAD SHARE APPLICATION

An off-line power supply application utilizing the UC3907 Load Share Controller is shown in Fig. 11 for a flyback regulator. The UC3844 is the modulator and its switching frequency is determined by Fs = 1.72/(Rt Ct). The resistor R5 will sense the primary inductor current, where the maximum peak current for the UC3844 is given by ISmax= 1.0V/R5. Startup is achieved with R1 and C5 until bootstrap winding W2 can feedback to power the UC3844. The snubber network D3, C4, and R2 prevents turn-off voltage spikes from exceeding the FET breakdown voltage. The primary soft-start circuit is comprised of Q1, R9 and C10.

Note that the resistor Rset and adjust compensation is connected to artificial ground (pin 6). Artificial ground is a replica of the "true" ground voltage on pin 4, negative sense, plus a 0.250V level shift. This allows a low impedance point for ground referenced elements to connect.

A master indicator lamp is included in the design so that the unit supplying the most load current and determining the output regulating voltage can be detected. There are many useful applications for this pin as in supply voltage margining or determination of a faulted supply which is supplying an excess voltage/current.

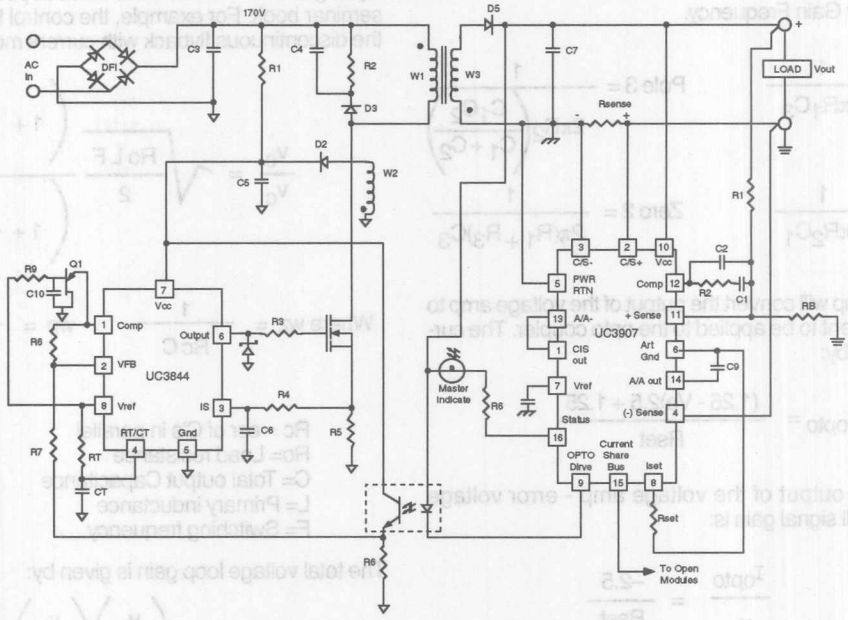


Fig. 11 - The UC3907 in an off-line isolated application.

NON-ISOLATED CONVERTER APPLICATIONS

There are applications were non-isolated DC to DC converters are paralleled to make a power system. Fig. 12 shows a step down, or buck, regulator utilizing the UC3524A voltage mode PWM and the UC3907 Load share IC. For non-isolated parallel power supply applications the current sensing must be done on the high side. The reason for this is that if the sensing was performed on the low side where the power supply inputs and outputs are common, then all the current sense resistors will end up in parallel, defeating the individual sensing and load sharing. The only limitation to high side current sensing in a non-isolated application is that the current amplifier of the UC3907 has a common mode range of 0V to Vin -2V, therefore a form of level shifting or average current sensing would be required.

Since the opto-coupler is not required, an inversion has been eliminated which the driving scheme must accommodate for. The Iset voltage is a gained up inverted error voltage from the UC3907 voltage amp. The UC3524A error amp is set up as an inverter and cancels out the drive amp inversion leaving the error voltage of the UC3907 to be transposed to the UC3524A in proper phase. The iset voltage will swing from 0v to 3.8V min. Current limiting is achieved by taking the current amp output signal from the UC3907 and feeding it in to the UC3524A current limit amplifier, where the current limit is given by:

$$Icl = \frac{5\left(\frac{R_{12}}{R_{11}+R_{12}}\right)+0.2}{20\,R_{sense}}$$

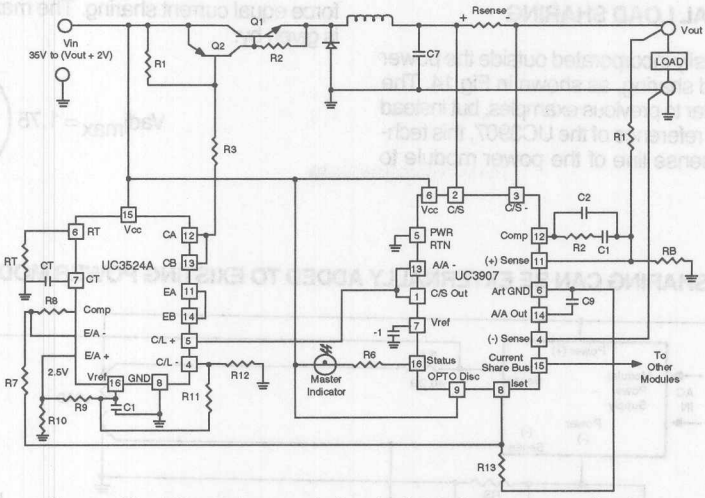


Fig. 12 - The UC3907 in a non-isolated DC to DC converter application.

LINEAR REGULATOR EXAMPLE

A simple linear regulator with load sharing using the UC3907 IC and a few external components is shown in Fig. 13. The phasing of the opto drive pin facilitates darlington drive, and supply current limiting is achieved by Q3, C1, R11, and R12 with the current limit given by:

$$Icl = \frac{VBE_{Q3}\left(1 + \frac{R_{11}}{R_{12}}\right)}{20\,R_{sense}}$$

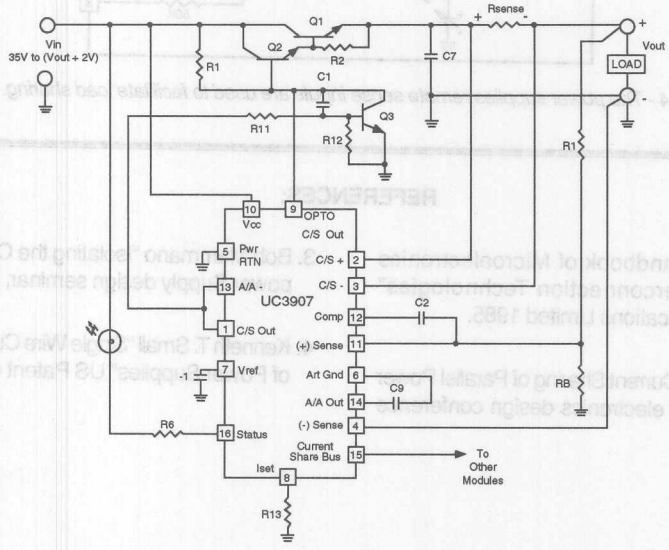


Fig. 13 - With a few external components the UC3907 can make a simple linear regulator with load sharing.

EXTERNAL LOAD SHARING

The UC3907 can be easily incorporated outside the power module to achieve load sharing, as shown in Fig 14. The load sharing loop is similar to previous examples, but instead of adjusting the internal reference of the UC3907, this technique adjusts the (+) sense line of the power module to force equal current sharing. The maximum adjust voltage is given by:

$$Vadj_{max} = 1.75\left(\frac{R_1}{R_2}\right)$$

LOAD SHARING CAN BE EXTERNALLY ADDED TO EXISTING POWER MODULES

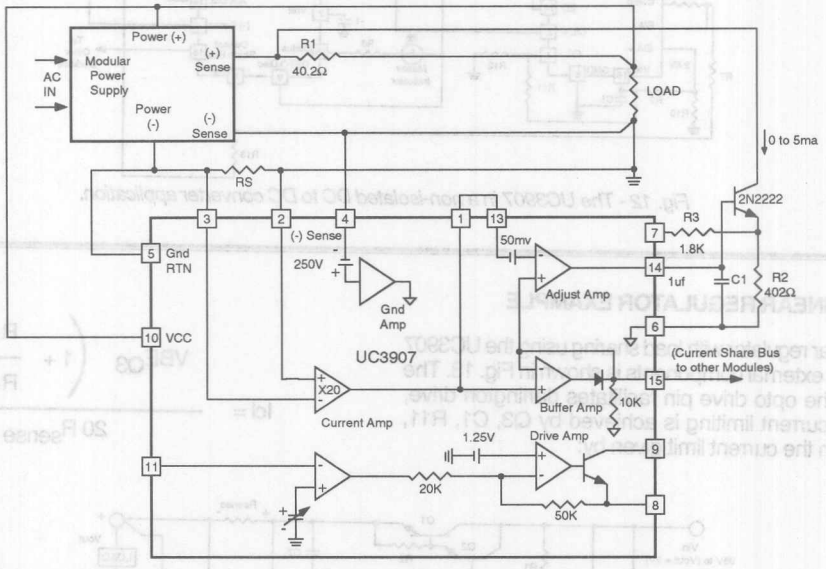


Fig. 14 - The power supplies remote sense inputs are used to facilitate load sharing.

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UNITRODE
APPLICATION NOTE

DEDICATED ICs SIMPLIFY BRUSHLESS DC SERVO AMPLIFIER DESIGN

John A. O'Connor

INTRODUCTION

Brushless DC motors have gained considerable commercial success in high end four quadrant servo systems, as well as in less demanding, one and two quadrant requirements. Cost sensitive four quadrant applications thus far have not fared as well. Designs which meet cost goals often suffer from poor linearity, and cumbersome protection circuits to assure reliable operation in all four quadrants. Better performance entails more complex circuitry and the resulting additional components quickly increase size and cost. Part of the design challenge results from the lack of control ICs tailored to four quadrant applications. The other major obstacle has been implementing a reliable and cost effective high-side switch drive. With recently introduced integrated circuits in both areas, it is now possible to design a rugged, low cost, four quadrant brushless DC servo amplifier with relatively low component count and cost.

SERVO AMPLIFIER REQUIREMENTS

First, let's quickly review general servo amplifier requirements. Figure 1 displays motor speed versus torque, depicting four possible modes of operation. While a system may be considered four quadrant by simply having the ability to operate reliably in all four modes, a servo system generally requires *controlled* operation in all four modes. In addition, a smooth, linear transition between quadrants is essential for high accuracy position and velocity control. The major performance differences between brushless DC servo amplifiers are related to accuracy, bandwidth, and quadrant transition linearity.

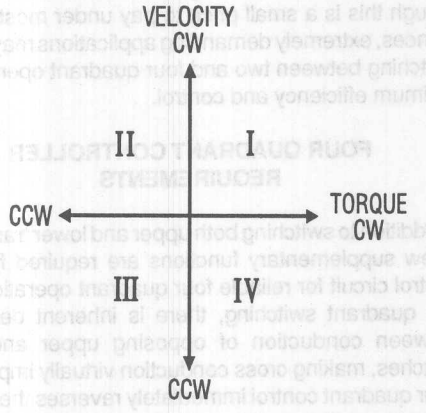


Figure 1 - Four Quadrants of Operation

Most simple brushless DC amplifiers provide two quadrant control, since even the simplest output stages (typically 3 phase bridge) allow rotation reversal. Note that this is operation in quadrants one and three where torque and rotation are in the same direction. This differs from brush motor terminology where two quadrant control normally implies unidirectional rotation with torque control in either direction. Although limited to a single rotation direction, bidirectional torque allows servo velocity control, with rapid, controlled acceleration and deceleration. These characteristics are well suited to numerous applications such as spindle and conveyer drives. With the two quadrant brushless DC amplifier, there are no provisions other than friction to decelerate the load, limiting the system to less demanding applications. Attempting to operate in quadrants two and four will result in extremely nonlinear behavior, and under many circumstances, severe damage to the output stage will follow. This occurs because the two quadrant brushless DC amplifier is unable to completely control current during torque reversal.

TWO QUADRANT VERSUS FOUR QUADRANT CONTROL

Figure 2 shows a three phase bridge output stage for driving a brushless DC motor. Current flow is shown for two quadrant control when operation is in quadrants one or three. The switches commutate based on the motor's

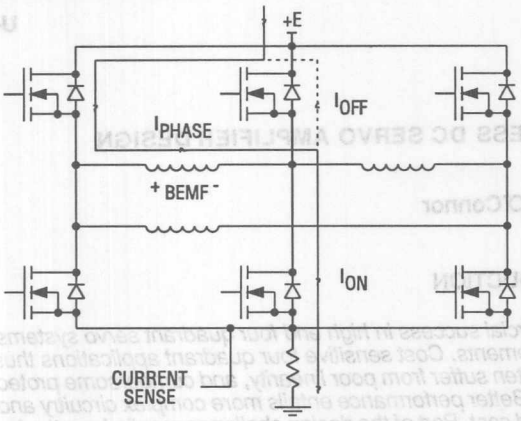


Figure 2 - Two Quadrant Chopping

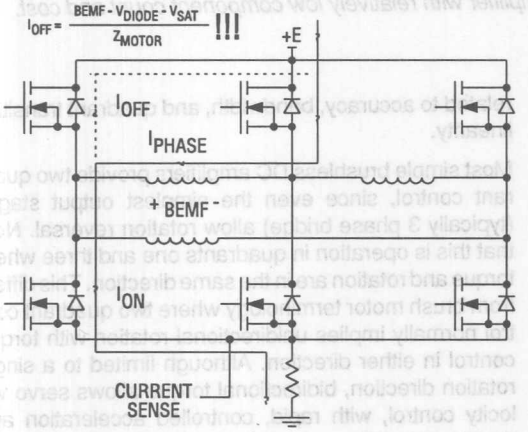


Figure 3 - Two Quadrant Reversal

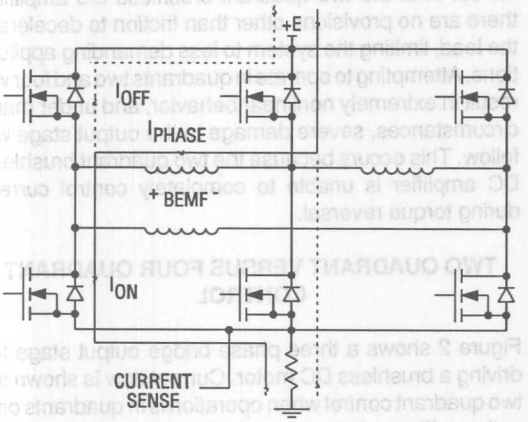


Figure 4 - Four Quadrant Reversal

rotor position, typically using Hall effect sensors for position feedback. Current is controlled by pulse width modulating (PWM) the lower switches. Figure 3 shows current flow if the direction of torque were reversed. The upper switch essentially shorts the motor's back EMF (BEMF), causing current to quickly decay and reverse direction. The current then rises to a value limited only by the motor and drive impedance, yet is undetected by supply or ground sense resistors. As the motor speed rises, its BEMF proportionally increases, quickly escalating the potential circulating current. Even if the output stage is built rugged enough to withstand this abuse, the high uncontrolled current causes high uncontrolled torque, making this technique unsuitable for most servo control applications.

By pulse width modulating the upper switches along with the lower switches, uncontrolled circulating currents are avoided. With both upper and lower switches off during during the PWM off time, motor current will always decay as shown in figure 4. Additionally, motor current always flows through the ground sense resistor, allowing easy detection for feedback. The remainder of this article will feature this mode of control, as it is well suited for a variety of demanding requirements. It should be noted however, that a penalty in the form of reduced efficiency must be paid for the improvement in control characteristics. With two switches operating at the PWM frequency, as opposed to one with two quadrant control, switching losses are nearly doubled. Ripple current is also increased which results in greater motor core loss. Although this is a small price to pay under most circumstances, extremely demanding applications may require switching between two and four quadrant operation for optimum efficiency and control.

FOUR QUADRANT CONTROLLER REQUIREMENTS

In addition to switching both upper and lower transistors, a few supplementary functions are required from the control circuit for reliable four quadrant operation. With two quadrant switching, there is inherent dead time between conduction of opposing upper and lower switches, making cross conduction virtually impossible. Four quadrant control immediately reverses the state of opposing switches at torque reversal, thus requiring a delay between turning the conducting device off and the opposing device on to avoid simultaneous conduction and possible output stage damage.

When torque is reversed, energy stored in the rotating load is transferred back to the power supply, quickly charging the bus storage capacitor. A clamp circuit is

typically used to dissipate the energy and limit the maximum bus voltage. As a second line of defense, an over-voltage comparator is often employed to disable the output if the bus voltage exceeds the clamp voltage by more than a few volts.

CURRENT LOOP CONTROL TECHNIQUE

A transconductance amplifier is normally used for brushless DC servo applications, providing direct control of motor torque. Average current feedback is usually employed rather than the more familiar peak current

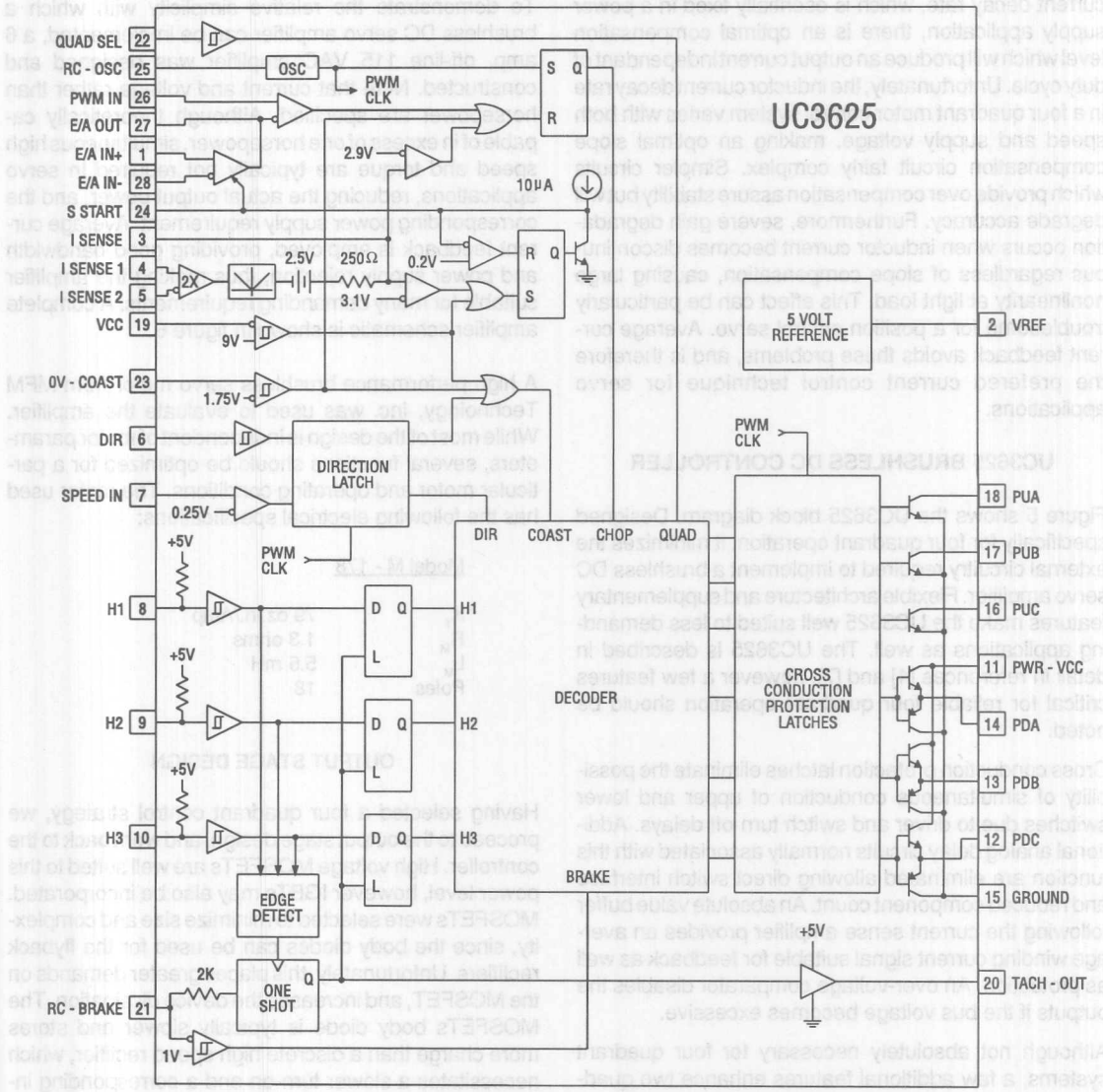


Figure 5 - UC3625 Block Diagram

control for several reasons. Peak current control is subject to subharmonic oscillation at the switching frequency for duty cycles above 50%. This condition is easily circumvented in power supply applications by summing an appropriately scaled ramp signal derived from the PWM oscillator with the current sense signal. This technique is commonly refered to as slope compensation. It can also be shown [3] that for a given inductor current decay rate, which is esentially fixed in a power supply application, there is an optimal compensation level which will produce an output current independant of duty cycle. Unfortunately, the inductor current decay rate in a four quadrant motor control system varies with both speed and supply voltage, making an optimal slope compensation circuit fairly complex. Simpler circuits which provide over compensation assure stability but will degrade accuracy. Furthermore, severe gain degradation occurs when inductor current becomes discontinuous regardless of slope compensation, causing large nonlinearity at light load. This effect can be particularly troublesome for a position control servo. Average current feedback avoids these problems, and is therefore the prefered current control technique for servo applications.

UC3625 BRUSHLESS DC CONTROLLER

Figure 5 shows the UC3625 block diagram. Designed specifically for four quadrant operation, it minimizes the external circuitry required to implement a brushless DC servo amplifier. Flexible architecture and supplementary features make the UC3625 well suited to less demanding applications as well. The UC3625 is described in detail in references [4] and [7], however a few features critical for reliable four quadrant operation should be noted.

Cross conduction protection latches eliminate the possibility of simultaneous conduction of upper and lower switches due to driver and switch turn-off delays. Additional analog delay circuits normally associated with this function are eliminated allowing direct switch interface and reduced component count. An absolute value buffer following the current sense amplifier provides an average winding current signal suitable for feedback as well as protection. An over-voltage comparator disables the outputs if the bus voltage becomes excessive.

Although not absolutely necessary for four quadrant systems, a few additional features enhance two quadrant operation and simplify implementation of switched two / four quadrant control for optimized systems. A direction latch with analog speed input prevents reversal until an acceptably low speed is reached, preventing output stage damage. Two or four quadrant switching can be selected during operation with the Quad Select input. A brake input provides current limited dynamic braking, suitable for applications which require rapid deceleration, but do not need tight servo control.

A SIMPLE BRUSHLESS DC SERVO AMPLIFIER

To demonstrate the relative simplicity with which a brushless DC servo amplifier can be implemented, a 6 amp, off-line 115 VAC amplifier was designed and constructed. Note that current and voltage rather than horsepower are specified. Although theoretically capable of in excess of one horsepower, simultaneous high speed and torque are typically not required in servo applications, reducing the actual output power, and the corresponding power supply requirement. Average current feedback is employed, providing good bandwidth and power supply rejection, thus making the amplifier suitable for many demanding requirements. A complete amplifier schematic is shown in figure 6.

A high performance brushless servo motor from MFM Technology, Inc. was used to evaluate the amplifier. While most of the design is independent of motor parameters, several functions should be optimized for a particular motor and operating conditions. The motor used has the following electrical specifications:

Model M - 178

K_T	79 oz.in./Amp
R_M	1.3 ohms
L_M	5.5 mH
Poles	18

OUTPUT STAGE DESIGN

Having selected a four quadrant control strategy, we proceed to the output stage design, and work back to the controller. High voltage MOSFETs are well suited to this power level, however IGBTs may also be incorporated. MOSFETs were selected to minimize size and complexity, since the body diodes can be used for the flyback rectifiers. Unfortunately, this places greater demands on the MOSFET, and increases the device dissipation. The MOSFETs body diode is typically slower and stores more charge than a discrete high speed rectifier, which necessitates a slower turn-on and a corresponding increase in switching losses. These losses are partially offset by choosing a MOSFET with sufficiently low conduction losses which offers the secondary benefits of greater peak current capability and reduced thermal

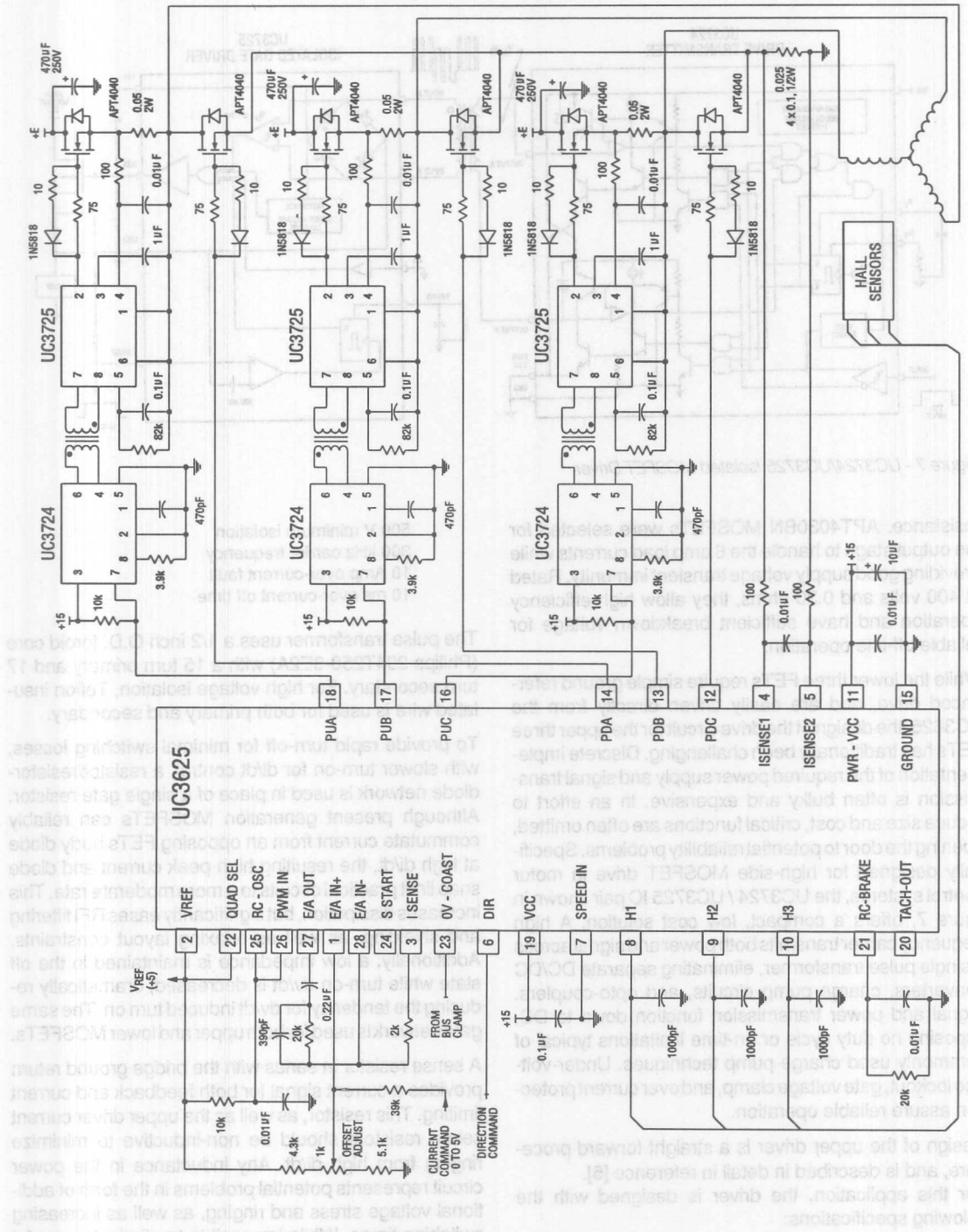


Figure 6 - Brushless DC Servo Amplifier Schematic

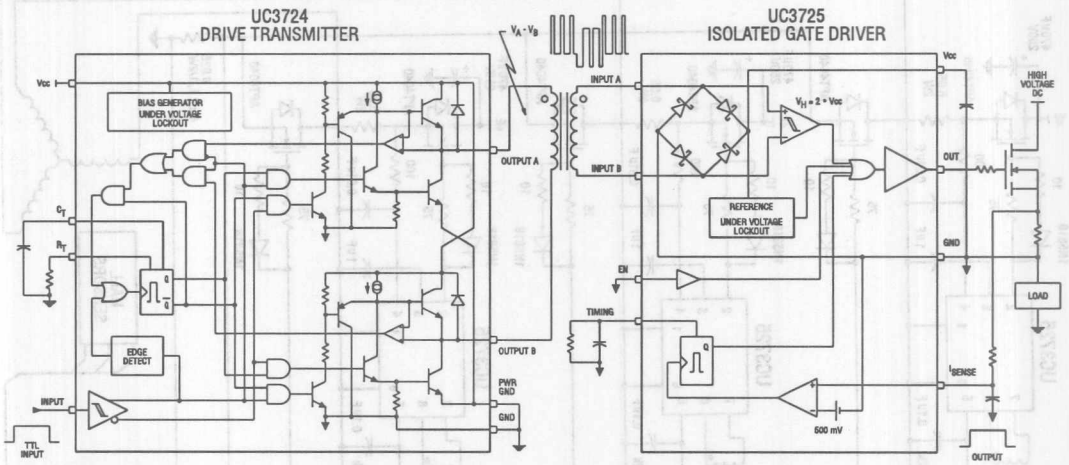


Figure 7 - UC3724/UC3725 Isolated MOSFET Driver

resistance. APT4030BN MOSFETs were selected for the output stage to handle the 6 amp load currents while providing good supply voltage transient immunity. Rated at 400 volts and 0.30 ohms, they allow high efficiency operation and have sufficient breakdown voltage for reliable off-line operation.

While the lower three FETs require simple ground referenced drive, and are easily driven directly from the UC3625, the design of the drive circuit for the upper three FETs has traditionally been challenging. Discrete implementation of the required power supply and signal transmission is often bulky and expensive. In an effort to reduce size and cost, critical functions are often omitted, opening the door to potential reliability problems. Specifically designed for high-side MOSFET drive in motor control systems, the UC3724 / UC3725 IC pair shown in figure 7, offers a compact, low cost solution. A high frequency carrier transmits both power and signal across a single pulse transformer, eliminating separate DC/DC converters, charge pump circuits, and opto-couplers. Signal and power transmission function down to DC, imposing no duty cycle or on-time limitations typical of commonly used charge pump techniques. Under-voltage lockout, gate voltage clamp, and over current protection assure reliable operation.

Design of the upper driver is a straight forward procedure, and is described in detail in reference [5].
For this application, the driver is designed with the following specifications:

500 V minimum isolation
300 kHz carrier frequency
10 Amp over-current fault
10 ms over-current off time

The pulse transformer uses a 1/2 inch O.D. toroid core (Philips 204T250-3E2A) with a 15 turn primary and 17 turn secondary. For high voltage isolation, Teflon insulated wire is used for both primary and secondary.

To provide rapid turn-off for minimal switching losses, with slower turn-on for di/dt control, a resistor/resistor-diode network is used in place of a single gate resistor. Although present generation MOSFETs can reliably commutate current from an opposing FETs body diode at high di/dt, the resulting high peak current and diode snap limit practical circuits to a more moderate rate. This increases dissipation, but significantly eases RFI filtering and shielding, as well as relaxing layout constraints. Additionally, a low impedance is maintained in the off state while turn-on dv/dt is decreased, dramatically reducing the tendency for dv/dt induced turn on. The same gate network is used for both upper and lower MOSFETs.

A sense resistor in series with the bridge ground return provides a current signal for both feedback and current limiting. This resistor, as well as the upper driver current sense resistors should be non-inductive to minimize ringing from high di/dt. Any inductance in the power circuit represents potential problems in the form of additional voltage stress and ringing, as well as increasing switching times. While impossible to eliminate, careful

layout and bypassing will minimize these effects. The output stage should be as compact as heat sinking will allow, with wide, short traces carrying all pulsed currents. Each half-bridge should be separately bypassed with a low ESR/ESL capacitor, decoupling it from the rest of the circuit. Some layouts will allow the input filter capacitor to be split into three smaller values, and serve double duty as the half-bridge bypass capacitors.

CONTROLLER SETUP

The UC3625 switching frequency is programmed with a timing resistor and capacitor. Unless the motor's inductance is particularly low, 20 kHz will provide acceptable ripple current and switching losses while minimizing audible noise.

(1) $F = 2 / R_{OSC}C_{OSC}$

The relatively small oscillator signal amplitude requires careful timing capacitor interconnect for maximum frequency stability. Circuit board traces should to be as short as possible, directly connecting the capacitor between pins 25 and 15, with no other circuits sharing the board trace to pin 15 (ground).

When tight oscillator stability is required, or multiple systems must be synchronized to a master clock, the circuit shown in figure 8 can be used. As shown, the circuit buffers, and then differentiates the falling edge of the master oscillator. The last stage provides the necessary current gain to drive the 47 ohm resistor in series with the timing capacitor. If the master clock is from a digital source, the first two stages are omitted, and the clock signal is interfaced directly to the final stage through a restive divider as shown. The slaves are programmed to oscillate at a lower frequency than the master. The pulse injected across the 47 ohm resistor causes the oscillator to terminate its cycle prematurely, and thus synchronize to the master clock.

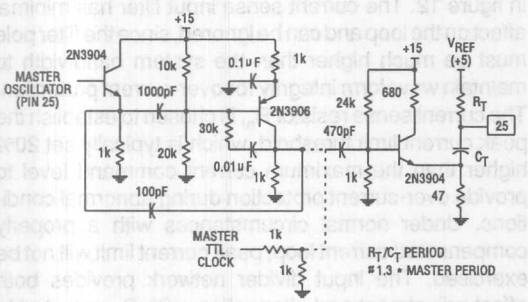


Figure 8 - External Synchronization Circuit

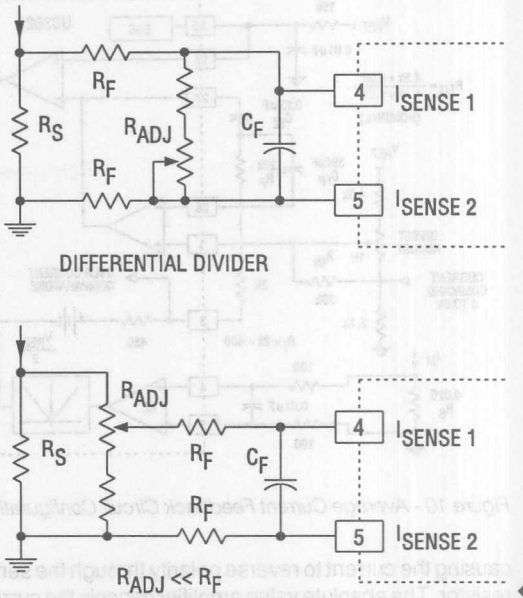


Figure 9 - Balance Impedance Current Sense Input Circuits

The RC-Brake pin serves two functions: Brake command input (not used in this design), and tachometer / digital commutation filter one-shot programming. Whenever the commutation state changes, the one-shot is triggered, outputting a tach pulse and inhibiting another commutation state change until the one-shot terminates. The one-shot pulse width is programmed for approximately 1/2 the shortest commutation period.

(2) $T_{PW} = 0.70\ R_TC_T$

where the shortest commutation period = $20 / (RPM_{MAX}N_{POLES})$

CURRENT SENSING AND FEEDBACK

For optimum current sense amplifier performance, the input impedance must be balanced. Low value resistors (100 to 500 ohm) are used to minimize bias current errors and noise sensitivity. Additionally, if the sense voltage must be trimmed, a low value input divider or a differential divider should be used to maintain impedance matching, as shown in figure 9.

An average current feedback loop is implemented by the circuit shown in figure 10. With four quadrant chopping, motor current always flows through the sense resistor. When PWM is off however, the flyback diodes conduct,

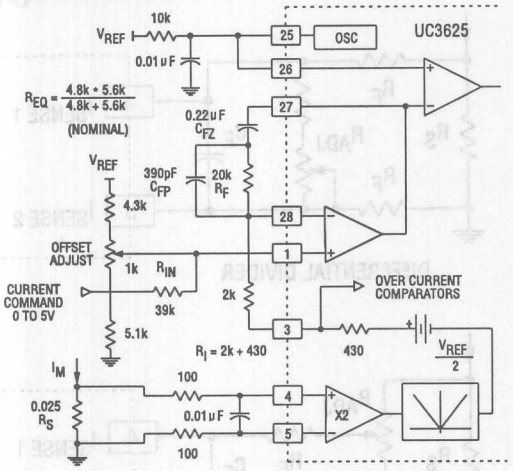


Figure 10 - Average Current Feedback Circuit Configuration

causing the current to reverse polarity through the sense resistor. The absolute value amplifier cancels the current polarity reversal by inverting the negative current sense signal during the flyback period. The output of the absolute value amplifier therefore is a reconstructed analog of the motor current, suitable for protection as well as feedback loop closure.

When the current sense output is used to drive a summing resistor as in this application example, the current sense output impedance adds to the summing resistor value. The internal output resistor and the amplifier output impedance can both significantly effect current sense accuracy if the external resistance is too low. Although not specified, the total output impedance is typically 430 ohms at 25 degrees C. Over the military temperature range of -55 to +125 degrees C, the impedance ranges from approximately 350 to 600 ohms. An external 2 k resistor will result in an actual 2.43 k summing resistance with reasonable tolerance. A higher value external resistor and trim pot will be required if high closed current loop accuracy is required.

The current sense output offset voltage is derived from the +5 V reference voltage. By developing the command offset from the +5 V reference, current sense drift over temperature is minimized. The offset divider must be trimmed initially to accommodate the current sense amplifier offset tolerance.

POWER SUPPLY AND BUS CLAMP

Input power is filtered to reduce conducted EMI, and transient protected using MOVs. Power-up current surge is suppressed using a NTC thermistor, while a bridge rectifier and capacitive filter complete the high voltage supply. A small 60 Hz. transformer supplies 15 Volts through a three pin regulator to power the control and drive circuits.

A bus clamp is easily designed around a UC3725 MOSFET driver, as shown in figure 11. As in the high-side switch drive, the UC3725 assures reliable operation, particularly during power-up and power-down. The divider current is set to 1 mA at the threshold, which is a reasonable compromise between input bias current error and dissipation. An additional tap programs the over-voltage coast a few volts above the bus clamp, saving a resistor and some dissipation while reducing the tolerance between the bus clamp and the over-voltage coast. Setting the bus clamp discharge current equivalent to the maximum motor current will assure effective clamping under all conditions. The load resistor value is therefore:

$$(3) \qquad R_L = \frac{V_{CLAMP}}{I_{MAX}}$$

The load resistor dissipation is dependant on the energy removed from the load inertia, and the frequency with which the energy is removed.

$$(4) \qquad P_{LOAD} = 1/2\, f J\, (\omega_1^2 - \omega_2^2)$$

where J = inertia in Nm sec^2
ω_1 = initial velocity in rad/sec
ω_2 = final velocity in rad/sec

Note that if the deceleration time approaches the load resistor's thermal time constant, a higher power resistor will be required to maintain reliability.

CURRENT LOOP OPTIMIZATION

The block diagram of the current control loop is shown in figure 12. The current sense input filter has minimal affect on the loop and can be ignored, since the filter pole must be much higher than the system bandwidth to maintain waveform integrity for over-current protection. The current sense resistor R_S, is chosen to establish the peak current limit threshold, which is typically set 20% higher than the maximum current command level to provide over-current protection during abnormal conditions. Under normal circumstances with a properly compensated current loop, peak current limit will not be exercised. The input divider network provides both offset adjustment and attenuation, with R_{IN} selected to accomodate the current command signal range.

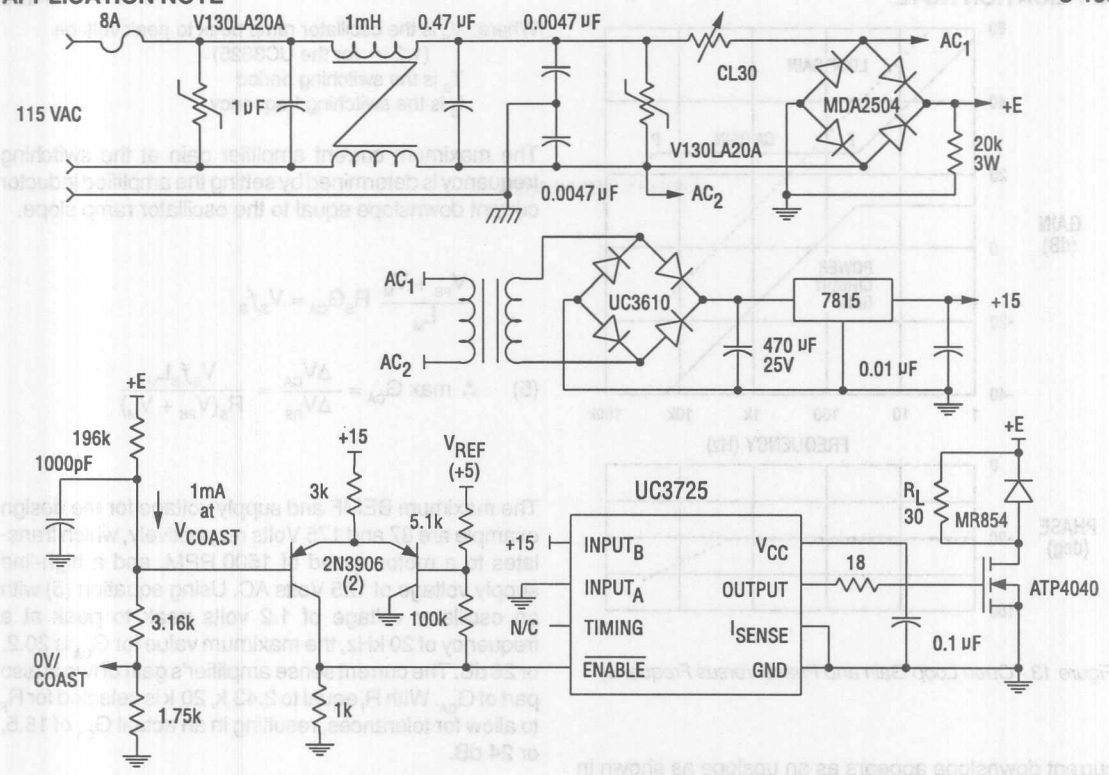


Figure 11 - Power Supply and Bus Clamp

All PWM circuits are prone to subharmonic oscillation if the modulation comparator's two input waveform slopes are inappropriately related. This behavior is most common in peak current feedback schemes, where slope compensation is typically required to achieve stability. Average current feedback systems will exhibit similar behavior if the current amplifier gain is excessively high at the switching frequency. As described by Dixon [2] to avoid subharmonic oscillation for a single pole system: *The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input.* This criterion sets the maximum current amplifier gain at the switching frequency, and indirectly establishes the maximum current loop gain crossover frequency.

A voltage proportional to motor current, which is the inductor current, is generated by the current sense resistor and the current sense amplifier circuitry internal to the UC3625. This waveform is amplified and inverted by the current amplifier and applied to the PWM comparator input. Due to the signal inversion, the motor

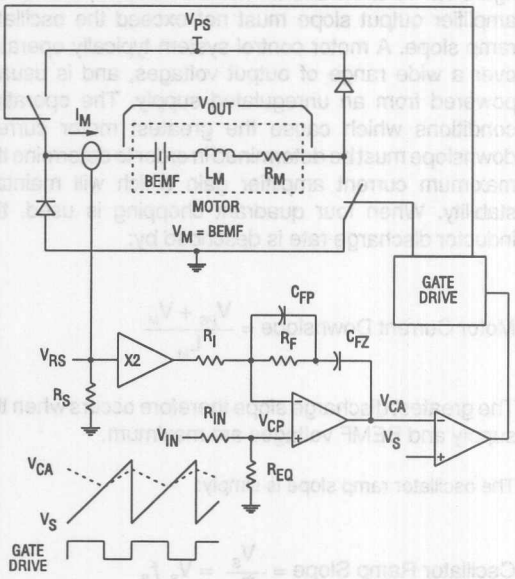


Figure 12 - Current Loop Block Diagram

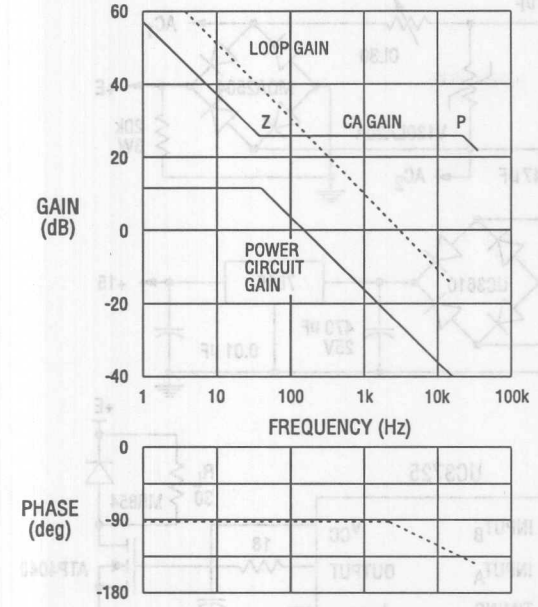


Figure 13 - Open Loop Gain and Phase Versus Frequency

current downslope appears as an upslope as shown in figure 12. To avoid subharmonic oscillation, the current amplifier output slope must not exceed the oscillator ramp slope. A motor control system typically operates over a wide range of output voltages, and is usually powered from an unregulated supply. The operating conditions which cause the greatest motor current downslope must be determined in order to determine the maximum current amplifier gain which will maintain stability. When four quadrant chopping is used, the inductor discharge rate is described by:

$$\text{Motor Current Downslope} = \frac{V_{PS} + V_M}{L_M}$$

The greatest discharge slope therefore occurs when the supply and BEMF voltages are maximum.

The oscillator ramp slope is simply:

$$\text{Oscillator Ramp Slope} = \frac{V_S}{T_S} = V_S f_S$$

Where: V_S is the oscillator ramp peak to peak voltage (1.2 V for the UC3625)
T_S is the switching period
f_S is the switching frequency

The maximum current amplifier gain at the switching frequency is determined by setting the amplified inductor current downslope equal to the oscillator ramp slope.

$$\frac{V_{PS} + V_M}{L_M} R_S G_{CA} = V_S f_S$$

$$(5) \quad \therefore \max G_{CA} = \frac{\Delta V_{CA}}{\Delta V_{RS}} = \frac{V_S f_S L_M}{R_S (V_{PS} + V_M)}$$

The maximum BEMF and supply voltage for the design example are 87 and 175 Volts respectively, which translates to a motor speed of 1500 RPM, and a high-line supply voltage of 125 Volts AC. Using equation (5) with an oscillator voltage of 1.2 volts peak to peak at a frequency of 20 kHz, the maximum value for G_{CA} is 20.2, or 26 dB. The current sense amplifier's gain of two is also part of G_{CA}. With R_I equal to 2.43 k, 20 k is selected for R_F to allow for tolerances, resulting in an actual G_{CA} of 16.5, or 24 dB.

The small-signal control to output gain of the current loop power section is described by:

$$(6) \quad \frac{\Delta V_{RS}}{\Delta V_{CA}} = \frac{R_S 2 V_{PS}}{V_S s L_M}$$

Note that the factor of two in the numerator is a result of four quadrant chopping which only utilizes one-half of the modulator's input range for a given quadrant of operation.

The overall open loop gain of the current loop is the product of the actual current amplifier gain and the control to output gain of the power circuit. The result is set equal to one to solve for the loop gain crossover frequency, f_C:

$$(7) \quad G_{CA} \frac{R_S 2 V_{PS}}{V_S 2\pi f_C L_M} = 1$$

$$(8) \quad f_C = \frac{G_{CA} R_S V_{PS}}{V_S \pi L_M}$$

At high line, where the supply is 175 Volts DC, f_C is 3.5 kHz. The crossover frequency drops to 2.8 kHz at low line, where the supply is approximately 140 Volts DC. If greater bandwidth is required, the current amplifier gain must be increased, requiring a corresponding increase in switching frequency to satisfy equation (5).

Up to this point the motor's resistance (R_M) has been ignored. This is valid since L_M predominates at the switching frequency. The motor's electrical time constant L_M/R_M, creates a pole, which is compensated for by placing zero $R_F C_{FZ}$ at the same frequency. Additionally, pole $R_F C_{FP} C_{FZ}/(C_{FP}+C_{FZ})$ is placed at f_S to reduce sensitivity to noise spikes generated during switching transitions. The filter pole at f_S also reduces the amplitude and slope of the amplified inductor current waveform, possibly suggesting that the current amplifier gain could be increased beyond the maximum value from equation (5). Experimentally increasing G_{CA} may incur subharmonic oscillation however, since equation (5) is only valid for a system with a single pole response at f_S. For the design example, standard values are chosen for C_{FZ} and C_{FP} of 0.22 µF and 390 pF respectively, placing the zero at 36 Hz, and the pole at 20 kHz. Figure 13 shows open loop gain and phase verses frequency.

At very light loads, the motor current will become discontinuous - motor current reaches zero before the switching period ends. At this mode boundary, the power stage gain suddenly decreases, and the single pole characteristic of continuous mode operation with its 90 degree phase lag disappears. The current loop becomes more stable, but much less responsive. Fortunately, the high gain of current amplifier is sufficient to maintain acceptable closed current loop gain and phase characteristics at typical outer velocity and/or position loop crossover frequencies.

When the current loop is closed, the output voltage of the current sense amplifier ($2V_{RS}$) is equal to the current programming voltage (V_{CP}) at frequencies below the crossover frequency. The closed current loop transconductance is simply:

$$(9) \quad g_M = \frac{\Delta i_M}{\Delta V_{CP}} = \frac{\Delta V_{RS}/R_S}{\Delta V_{CP}} = \frac{1}{2R_S}$$

At the open loop crossover frequency, the transconductance rolls off and assumes a single pole characteristic. The input divider network attenuates the current command signal to provide compatibility with typical servo controller output voltages, and decreases the closed loop transconductance by the ratio of $R_{EQ}/(R_{EQ}+R_{IN})$. For the design example, the overall amplifier transconductance is 1.25 amps/volt, allowing full scale current (6 amps) with a 5 volt input command.

BIPOLAR TO SIGN/MAGNITUDE CONVERSION

The servo amplifier as shown in figure 6 requires a separate sign and magnitude input command. This is convenient for many microcontroller based systems which solely utilize digital signal processing for servo loop compensation. Analog compensation circuits however, usually output a bipolar signal and require conversion to sign/magnitude format to work with this amplifier. The circuit shown in figure 14 employs a differential amplifier for level shifting and ground noise rejection, and an absolute value circuit with polarity detection for conversion to sign/magnitude format. The current command signal is slightly attenuated and level shifted up 5 volts to allow single supply operation. The input divider circuit has been slightly modified from figure 9 to restore gain and provide a suitable offset adjustment range. Precision resistors (1%) should be used for both the differential amplifier and the absolute value circuit to minimize DC offset errors. Figure 15 shows approximately 2 Amp peak motor current with a 500 Hz sinwave command. Motor current follows the input command with minimal phase lag, however some crossover distortion is present. This is not crossover distortion in the traditional sense, rather it is simply a fixed off-time caused by the cross conduction protection circuitry. Since this distortion is current amplitude independent, and decreases with frequency, its effect on overall servo loop performance is minimal.

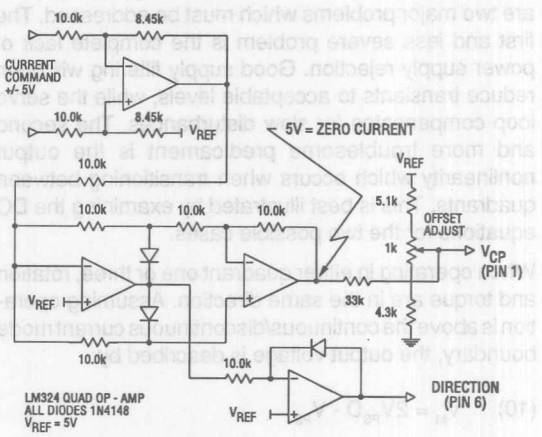


Figure 14 - Bipolar to Sign/Magnitude

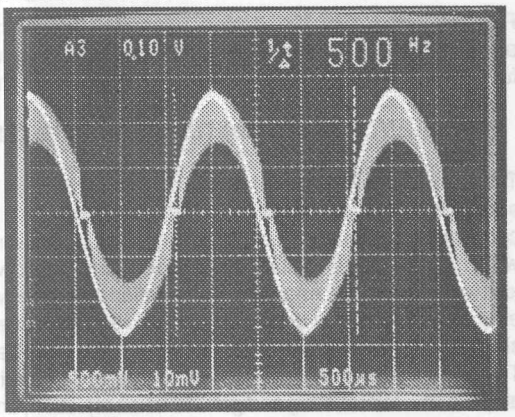


Figure 15 - 500Hz Sine Wave Command and Output Currents

DIRECT DUTY CYCLE CONTROL

There are many less demanding brushless DC servo applications which do not need a transconductance amplifier function yet require controlled operation in all four quadrants. For these systems, direct duty cycle control, also known as voltage mode control is often employed. Note that this is not voltage feedback, which requires additional demodulation circuitry to develop a feedback signal. With direct duty cycle control the amplifier simply provides open loop voltage gain. This technique is particularly advantageous when a microcontroller is used for servo loop compensation. By outputting a PWM signal directly, a digital to analog conversion is eliminated along with the analog pulse width modulator. While the simplicity of this technique is appealing, there are two major problems which must be addressed. The first and less severe problem is the complete lack of power supply rejection. Good supply filtering will often reduce transients to acceptable levels, while the servo loop compensates for slow disturbances. The second and more troublesome predicament is the output nonlinearity which occurs when transitioning between quadrants. This is best illustrated by examining the DC equations for the two possible cases.

When operating in either quadrant one or three, rotation and torque are in the same direction. Assuming operation is above the continuous/discontinuous current mode boundary, the output voltage is described by:

$$(10) \quad V_M = 2V_{PS}D - V_{PS}$$

where D = PWM duty cycle

When the direction command is reversed while the motor is rotating, operation switches to quadrant two or four, shifting the modulator's maximum output voltage point from full duty cycle to zero duty cycle.

$$(11) \quad V_M = 2V_{PS}(1\text{-}D) - V_{PS}$$

Note that the gain does not change, only the reference point has shifted. This occurs because the modulator only has a single quadrant control range - four quadrant operation results from the output control logic which is after the modulator. With the transconductance amplifier previously described, the error amplifier quickly slews during quadrant transitions, providing four quadrant control with minimal disturbance. When direct duty cycle control is used however, the servo loop filter must slew to maintain control. Unfortunately, this causes an immediate loop disturbance, with the greatest severity at the duty cycle extremes. This behavior can greatly effect the performance of an analog compensated servo, and therefore limits such systems to lower performance requirements.

With a microcontroller providing the servo loop compensation, nonlinear duty cycle changes can be accommodated, restoring linearity when transitioning between quadrants. Although nonlinear behavior still occurs when motor current becomes discontinuous, the effect on overall system performance is usually minimal. By correcting for quadrant transition nonlinearities, the advantages of an all digital interface can be exploited without severely degrading system performance. The control system is fully digital right up to the output stage, where the motor's inductance finally makes the conversion to analog by integrating the output switching waveform.

The circuit shown in figure 16 uses a PWM input from a microcontroller to set the output duty cycle and synchronize the oscillator, while another input controls direction.

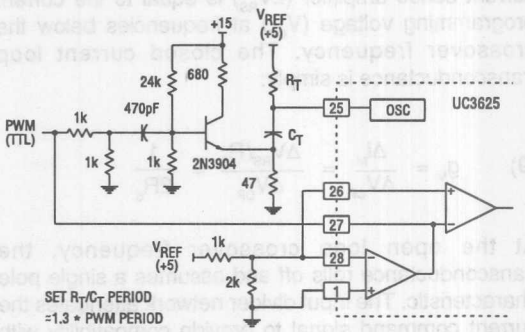


Figure 16 - Digital PWM Interface

Complete line isolation can easily be achieved by using opto-couplers. Although the performance of this technique falls short of the transconductance amplifier, the circuitry's simplicity while maintaining all of the protection features of the UC3625 make it well suited to many cost sensitive applications.

SUMMARY

The application example demonstrates the relative simplicity in implementing a brushless DC transconductance servo amplifier using the latest generation controller and driver ICs. For less demanding applications, direct duty cycle control using a dedicated controller provides size and cost reduction, without sacrificing protection features. While more and more control functions are implemented in microcontrollers today, the task of interfacing to output devices, and providing reliable protection under all conditions will remain a hardware function. Dedicated integrated circuits offer considerable improvement over the discrete solutions used in the past, reducing both size and cost, while enhancing reliability.

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UNITRODE
APPLICATION NOTE

Simple Switchmode Lead-Acid Battery Charger

John A. O'Connor

Abstract

Lead-acid batteries are finding considerable use as both primary and backup power sources. For complete battery utilization, the charger circuit must charge the battery to full capacity, while minimizing over-charging for extended battery life. Since battery capacity varies with temperature, the charger must vary the amount of charge with temperature to realize maximum capacity and life. Simple, low cost circuits are currently available for small, low power requirements, while more complex solutions are affordable only on larger more expensive systems. Often the greatest challenge is in designing mid-size, mid-price systems, where obtaining optimum performance at moderate cost and complexity may be nearly impossible without dedicated integrated circuits. This paper describes a compact lead-acid battery charger, which achieves high efficiency at low cost by utilizing switchmode power circuitry, and provides high charging accuracy by employing a dedicated control IC. The circuit described can be easily adapted to lower or higher power applications.

Lead-Acid Basics

Lead-acid battery chargers typically have two tasks to accomplish. The first is to restore capacity, often as quickly as practical. The second is to maintain capacity by compensating for self discharge. In both instances optimum operation requires accurate sensing of battery voltage and temperature.

When a typical lead-acid cell is charged, lead sulfate is converted to lead on the battery's negative plate and lead dioxide on the positive plate. Over-charge reactions begin when the majority of lead sulfate has been converted, typically resulting in the generation of hydrogen and oxygen gas. At moderate charge rates most of the hydrogen and oxygen will recombine in sealed batteries. In unsealed batteries however, dehydration will occur.

The onset of over-charge can be detected by monitoring battery voltage. Figure 1 shows battery voltage verses percent of previous discharge capacity returned at various charge rates. Over charge reactions are indicated by the sharp rise in cell voltage. The point at which over-charge reactions begin is dependent on charge rate, and as charge rate is increased, the percentage of returned capacity at the onset of over-charge diminishes. For over-charge to coincide with 100% return of capacity, the charge rate must typically be less than C/100 (1/100 amps of its amp-hour capacity). At high charge rates, controlled over-charging is typically

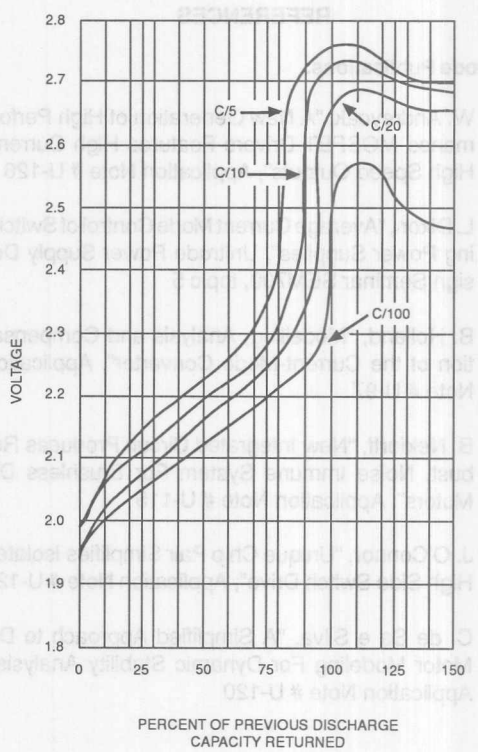


Figure 1. Over-charge reactions begin earlier (indicated by the sharp rise in cell voltage) when charge rate is increased. (Reprinted with the permission of Gates Energy Products, Inc.,)

employed with sealed batteries to return full capacity as quickly as possible.

To maintain capacity on a fully charged battery, a constant voltage is applied. The voltage must be high enough to compensate for self discharge, yet not too high as to cause excessive over-charging. While simply maintaining a fixed output voltage is a relatively simple function, the battery's temperature coefficient of -3.9mV/degree C per cell adds complication. If battery temperature is not compensated for, loss of capacity will occur below the nominal design temperature, and over-charging with degradation in life will occur at elevated temperature.

Charging Algorithm

To satisfy the aforementioned requirements and thus provide maximum battery capacity and life, a charging algorithm which breaks the charging cycle down into four states is employed. The charging algorithm is illustrated by the charger state diagram shown in figure 2. Assuming a fully discharged battery, the charger sequences through the states as follows:

1. Trickle-charge If the battery voltage is below a predetermined threshold, indicative of a very deep discharge or one or more shorted cells, a small trickle current is applied to bring the battery voltage up to a level corresponding to near zero capacity (typically 1.7V/cell @ 25 degrees C). Trickle charging at low battery voltages prevents the charger from delivering high currents into a short as well as reducing excessive out-gassing when a shorted cell is present. Note that as battery voltage increases, detection of a shorted cell becomes more difficult.
2. Bulk-charge Once the trickle-charge threshold is exceeded the charger transitions into the bulk-charge state. During this time full current is delivered to the battery and the majority of its capacity is restored.
3. Over-charge Controlled over charging follows bulk-charging to restore full capacity in a minimum amount of time. The over-charge voltage is dependent on the bulk-charge rate as illustrated by figure 1. Note that on unsealed batteries minimal over-charging should be employed to minimize out-gassing and subsequent dehydration. Initially overcharge current is the same as bulk-charge current. As the over-charge voltage is approached, the charge current diminishes. Over-charge is terminated when the current reduces to a low value, typically one-tenth the bulk charge rate.
4. Float-Charge To maintain full capacity a fixed voltage is applied to the battery. The charger will deliver whatever current is necessary to sustain the float voltage and compensate for leakage current. When a load is applied to the battery, the charger will supply the majority of the current up to the bulk-charge current level. It will remain in the float state until the battery voltage drops to 90% of the float voltage, at which point operation will revert to the bulk charge state.

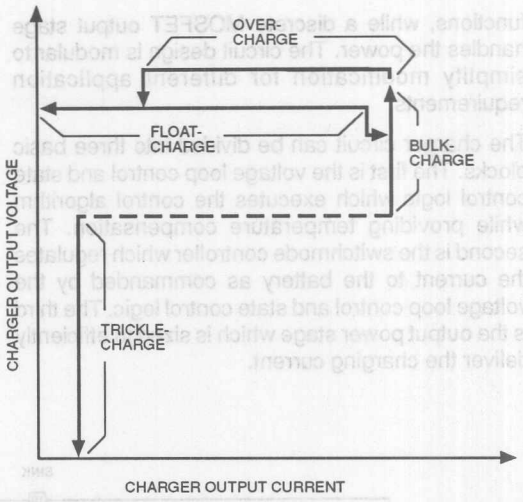


Figure 2. The charging algorithm is broken down into four states

Charger Circuit Design

There are many possible circuit configurations which will provide the necessary control and output charging current. For efficient operation, particularly at higher output currents, switching power circuitry is preferred. To minimize cost as well as complexity each IC used must provide as much functionality as possible. A circuit topology was chosen which utilizes two special purpose ICs and a general purpose op-amp to provide all of the control

functions, while a discrete MOSFET output stage handles the power. The circuit design is modular to simplify modification for different application requirements.

The charger circuit can be divided into three basic blocks. The first is the voltage loop control and state control logic which executes the control algorithm while providing temperature compensation. The second is the switchmode controller which regulates the current to the battery as commanded by the voltage loop control and state control logic. The third is the output power stage which is sized to efficiently deliver the charging current.

Voltage Loop Control and State Control Logic

Initially designed for charging small lead-acid batteries using a linear pass transistor for current control, the UC3906 directly implements the voltage loop control and state control logic while providing the appropriate temperature compensation. The block diagram of the UC3906 is shown in figure 3.

Battery voltage is monitored with a resistor divider string. This network establishes the float voltage, the over-charge voltage, and the trickle-charge threshold voltage by comparing to the precision temperature compensated reference. Since temperature is monitored on chip it is critical that the battery and the UC3906 are in close proximity, and

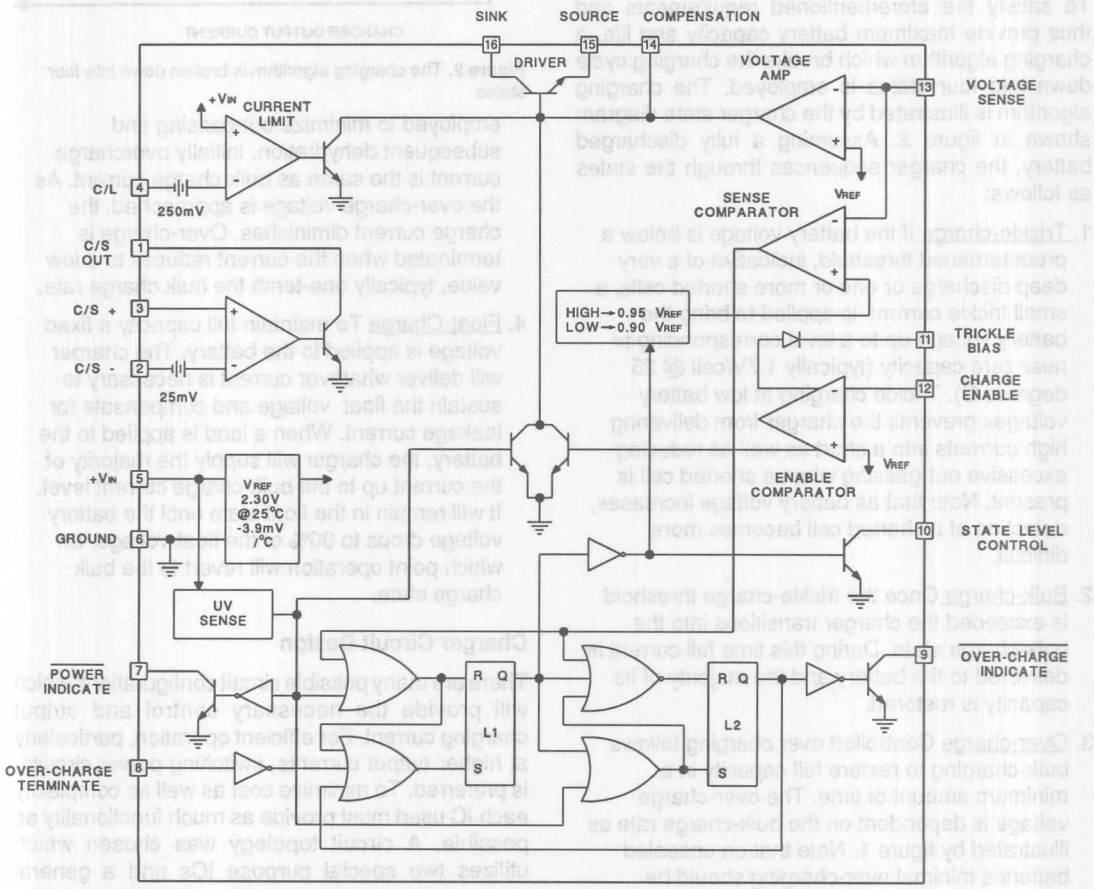


Figure 3. UC3906 Lead-Acid Battery Charger block diagram

that self-heating or heating from other components is minimized.

The differential current sense comparator is used to terminate over-charging and transition to the float state. The voltage amplifier provides gain and compensation for the voltage loop. The UC3906 is covered in detail in reference [3].

Switchmode Current Source

The charging algorithm places great demands on the current loop. during bulk charge full current must be supplied, yet during the float state the current draw may be only a few milliamps. This equates to a dynamic range in excess of 60 dB which can be very difficult to achieve with common peak current mode techniques. The wide dynamic range also requires operation with both continuous and discontinuous inductor current, potentially adding complication to voltage loop stabilization. Although load resistors can be employed to reduce the required dynamic range, their use can significantly degrade efficiency, particularly while in the float state. Note that a high value load resistor (10 k) is employed to assure operation down to zero output current and to provide a discharge path for the output capacitor. Additionally, to provide precise bulk and trickle-charge current levels the closed current loop transconductance must be accurate. Average current feedback will circumvent these potential problems, and is the key to a successful implementation of the switching current source for this application.

Figure 4 shows the basic implementation of average current feedback. While slightly more complicated than typical peak current mode control schemes, average current feedback offers several critical performance enhancements. The high gain of the error amplifier at lower frequencies provides high closed current loop accuracy and accommodates the large output stage nonlinearity which occurs when the inductor current becomes discontinuous. Good switching spike noise immunity is inherent with this technique permitting stable operation at narrow duty cycles.

A UC3823 PWM controller shown in figure 5 was chosen for the current loop control circuit for several reasons. First and most importantly it is capable of operating linearly from very small duty cycles to near

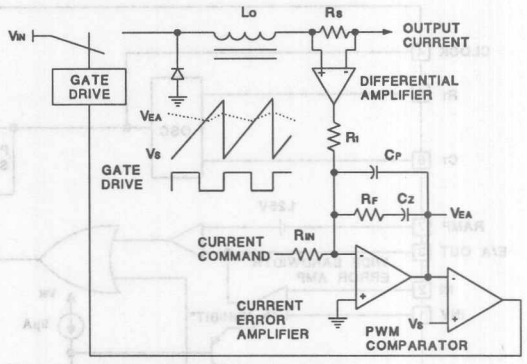


Figure 4. Average Current Feedback Loop

100% duty cycle. Secondly the error amplifier bandwidth and configuration are well suited to the average current loop's requirements. Additionally, the output driver affords a simple interface to most discrete output power stages.

A separate op-amp configured as a differential amplifier senses the output current and level shifts the signal to the appropriate voltage. The offset and common mode rejection of this amplifier are the major source of current loop error.

Output Power Stage

To simplify development a simple buck regulator output stage was used. For further simplicity the high-side switch is implemented using a direct coupled P-channel MOSFET. A switched current sink provides gate charge, turning the MOSFET on while a zener diode limits the gate to source voltage to 12 volts. A second emitter switched current sink drives a PNP which removes gate charge, turning the MOSFET off. Undoubtedly this output stage is suitable for many applications, although higher power capability and efficiency can be achieved using N-channel devices. A relatively low value output inductor was chosen to minimize size and cost since operation in the discontinuous current mode is of no concern with average current feedback. Output ripple voltage is also not critical so the output capacitor was selected for ripple current capability. High frequency ringing caused by circuit parasitics is damped with a small RC snubber across the catch rectifier. A rectifier in series with the output

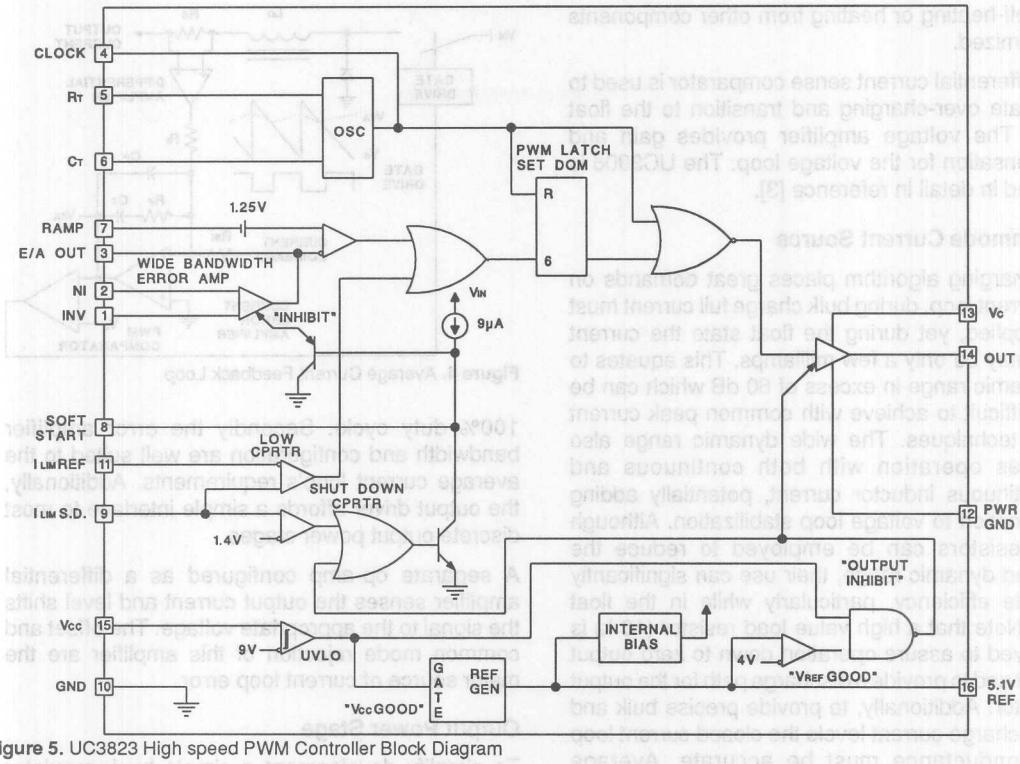


Figure 5. UC3823 High speed PWM Controller Block Diagram

prevents the battery from back driving the charger when input power is disconnected.

Complete Charger Circuit

A complete schematic for the switch-mode charger is shown in figure 6. Control circuit power is supplied from an emitter follower off a zener shunt regulator. The PWM frequency is set to 100 kHz as a reasonable compromise between output filter component size and switching loss. Output current is sensed in the battery return lead to minimize common mode voltage errors. This arrangement also allows direct current sensing for pulse by pulse current limiting adding further protection during abnormal conditions. The differential amplifier is set to a gain of 5 with the output signal referenced to the UC3823s 5.1V reference.

The current feedback signal is summed with the current command signal at the error amplifier's inverting input. To accommodate worst case offset in both the error amplifier and the differential amplifier and allow zero output current, the non-inverting input of the error amplifier is biased 130 mV below the 5.1 V reference. Trickle bias is accomplished by injecting a small current into the differential amplifier's negative op-amp input, thus causing a proportional output current to balance the loop. Additionally, a 100 pF capacitor across the PWM comparator inputs enhances noise immunity, particularly at low duty cycles.

For maximum control and float voltage accuracy, the UC3906s ground is connected to the battery's negative terminal, thereby rejecting the current sense resistors voltage drop. The internal emitter follower output transistor interfaces to the current source as illustrated in figure 7. The voltage amplifier drives the output current command signal. The current command signal is limited by clamping the voltage amplifier output through a diode to 4.2 V. The clamp also prevents the emitter follower from

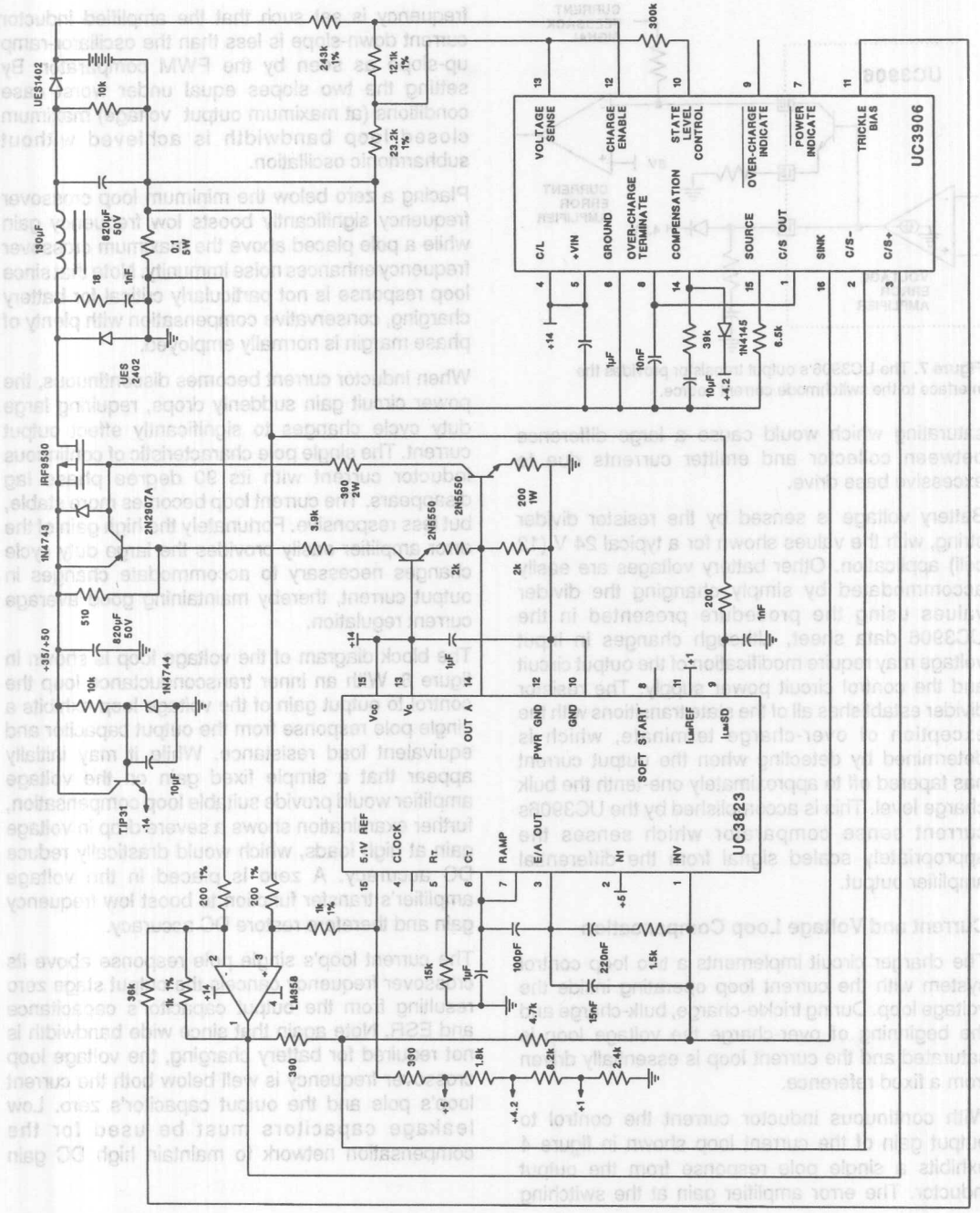


Figure 6. Switchmode Lead-Acid Battery charger schematic

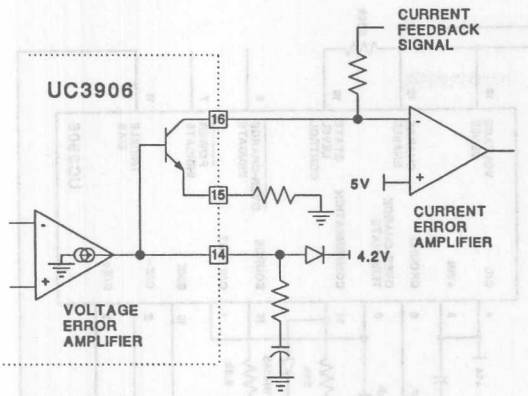


Figure 7. The UC3906's output transistor provides the interface to the switchmode current source.

saturating which would cause a large difference between collector and emitter currents due to excessive base drive.

Battery voltage is sensed by the resistor divider string, with the values shown for a typical 24 V (12 cell) application. Other battery voltages are easily accommodated by simply changing the divider values using the procedure presented in the UC3906 data sheet, although changes in input voltage may require modification of the output circuit and the control circuit power supply. The resistor divider establishes all of the state transitions with the exception of over-charge terminate, which is determined by detecting when the output current has tapered off to approximately one-tenth the bulk charge level. This is accomplished by the UC3906s current sense comparator which senses the appropriately scaled signal from the differential amplifier output.

Current and Voltage Loop Compensation

The charger circuit implements a two loop control system with the current loop operating inside the voltage loop. During trickle-charge, bulk-charge and the beginning of over-charge the voltage loop is saturated and the current loop is essentially driven from a fixed reference.

With continuous inductor current the control to output gain of the current loop shown in figure 4 exhibits a single pole response from the output inductor. The error amplifier gain at the switching frequency is set such that the amplified inductor current down-slope is less than the oscillator-ramp up-slope as seen by the PWM comparator. By setting the two slopes equal under worst case conditions (at maximum output voltage) maximum closed loop bandwidth is achieved without subharmonic oscillation.

Placing a zero below the minimum loop crossover frequency significantly boosts low frequency gain while a pole placed above the maximum crossover frequency enhances noise immunity. Note that since loop response is not particularly critical for battery charging, conservative compensation with plenty of phase margin is normally employed.

When inductor current becomes discontinuous, the power circuit gain suddenly drops, requiring large duty cycle changes to significantly effect output current. The single pole characteristic of continuous inductor current with its 90 degree phase lag disappears. The current loop becomes more stable, but less responsive. Fortunately the high gain of the error amplifier easily provides the large duty cycle changes necessary to accommodate changes in output current, thereby maintaining good average current regulation.

The block diagram of the voltage loop is shown in figure 8. With an inner transconductance loop the control to output gain of the voltage loop exhibits a single pole response from the output capacitor and equivalent load resistance. While it may initially appear that a simple fixed gain on the voltage amplifier would provide suitable loop compensation, further examination shows a severe drop in voltage gain at high loads, which would drastically reduce DC accuracy. A zero is placed in the voltage amplifier's transfer function to boost low frequency gain and therefore restore DC accuracy.

The current loop's single pole response above its crossover frequency cancels the output stage zero resulting from the output capacitor's capacitance and ESR. Note again that since wide bandwidth is not required for battery charging, the voltage loop crossover frequency is well below both the current loop's pole and the output capacitor's zero. Low leakage capacitors must be used for the compensation network to maintain high DC gain

since the voltage amplifier is a transconductance type. Loop stabilization is covered extensively in references [1] and [2].

Charger Performance Summary

The charger circuit properly executes the charging algorithm, exhibiting stable operation regardless of battery conditions including an open circuit load. The circuit was tested with 6,12 and 24 V batteries by modifying only the battery voltage sense divider. As would be expected, circuit efficiency was best at high battery voltage, approaching 85% while bulk-charging a 24 V battery with a 40 V input supply voltage.

An analysis of circuit losses indicates several areas where efficiency could be improved. Any accuracy and offset improvement in the differential amplifier will allow a corresponding decrease in current sense resistor value and hence dissipation, while maintaining the same overall current loop accuracy. Replacing the output blocking rectifier with a Schottky would save a few watts if the Schottky's leakage could be tolerated. Further improvement could be made in that area by using a relay to disconnect the charger when input power is removed. A more conservative inductor design with less resistance would save a little over one watt. As expected, the greatest losses occur in the output switch. A lower on resistance FET and a higher peak current gate drive to reduce switching losses could save more than 5 watts. Incorporating a few of these improvements will easily increase circuit efficiency to greater than 90%.

Alternate Circuit Configurations

While the charger circuit as designed may be suitable for many applications, a few modifications should satisfy the majority of additional requirements. Higher voltage batteries can be charged by designing a higher voltage output stage. N-channel MOSFETs are preferable for cost and efficiency reasons, but are more difficult to drive than P-channels. Fortunately, the remainder of the circuit will require minimal modification.

Some applications may require both the battery and charger to share a common ground and thus prohibit current sensing in the batteries negative return. The differential amplifier can sense current at the inductor output if tighter tolerance resistors to improve CMRR are used. While this simple modification renders a suitable signal for closing the current loop, another current sense signal referenced to ground must be developed for pulse by pulse current limiting. This signal is most easily derived by using a PNP level shift transistor, connecting the base to the 5.1 V reference and the emitter through a resistor to the differential amplifier output.

At higher battery voltages it may be desirable to float with a current rather than a voltage. Varying self-discharge rates of individual cells in high voltage batteries causes inevitable differences in cell charge levels. By employing a float current and applying a small continuous overcharge, variation of charge between cells is minimized. Precise output at float current levels places great demands on current loop accuracy, and will add unnecessary expense to the current sensing circuitry. A more cost effective alternative is to use a fixed linear current source which should be small and inexpensive considering the very low output current.

Thus far the input supply has not been addressed and is assumed to be from a voltage required elsewhere in the system or from a typical line frequency transformer, rectify bridge and filter capacitor. This may represent more than half the cost of the charger, and is certainly the majority of its size and weight. An obvious alternative is to replace the buck output section with a transformer coupled output, taking advantage of the switching control circuit already present. Buck derived circuits such as forward, half-bridge and full-bridge easily interface with the existing design, however resonant and flyback circuits are also applicable. A small (0.75 W) auxiliary supply will be required to power the control circuitry since the modulator will output zero at times, prohibiting the use of a bootstrap winding commonly used on switching power supplies. This

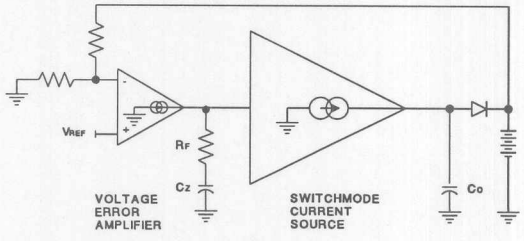


Figure 8. Voltage Control Loop block diagram

approach is particularly cost effective for stand-alone applications, allowing the design of a compact, light weight, high performance charger.

Summary

A practical switchmode lead acid battery charger circuit has been presented which incorporates all of the features necessary to assure long battery life with rapid charging capability. By utilizing special function ICs, component count is minimized, reducing system cost and complexity. With the circuit as presented, or with its many possible variations, designers need no longer compromise charging performance and battery life to achieve a cost effective system.

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POWER FACTOR CORRECTION USING THE UC3852 CONTROLLED ON-TIME ZERO CURRENT SWITCHING TECHNIQUE

BILL ANDREYCAK

INTRODUCTION

The controlled on-time, zero current switching technique provides a simple and efficient solution to obtaining high power factor correction. This discontinuous inductor current approach essentially programs a constant switch on-time during one line half-cycle. It does not require any "complex" analog square, multiply and divide functions to control the instantaneous switch current as with other PFC techniques. Additionally, zero current switching limits the peak current to exactly twice that of the average inductor current over all line and load combinations. High efficiency operation is also achieved with no boost rectifier recovery concerns and power loss. In a typical 80 Watt application the UC3852 PFC technique delivers a power factor of 0.998 with 5.8% Total Harmonic Distortion at nearly 94% efficiency.

CIRCUIT SCHEMATIC

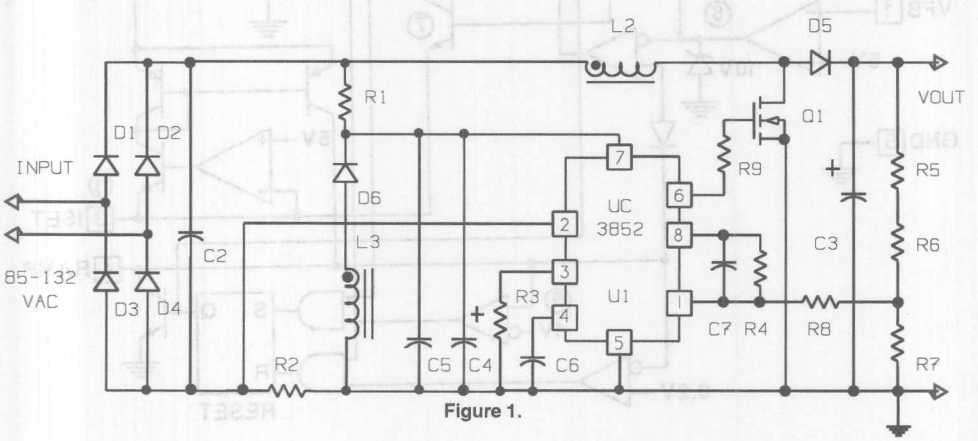


Figure 1.

UC3852 FEATURES

The UC3852 PFC controller contains several features which minimize external parts count while providing excellent performance and protection. Optimized for this off-line PFC application, the UC3852 delivers high power factor (0.997 typical) and a low cost overall solution.

OFF-LINE PROTECTION

- undervoltage lockout with hysteresis 16V turn-on, 11 V turn-off [1]
- clamped 12V gate drive output [2]
- active low, self biasing output [3]
- overcurrent protection [4]

CONTROL CIRCUIT ATTRIBUTES

- programmable maximum frequency [3 , 5]
- programmable maximum on-time [3 , 5]
- overcurrent indication output [7]

OPERATIONAL CHARACTERISTICS

- low operating current [8]
- low start-up current (0.4 mA) [1]
- few external required components
- 30 V maximum supply input [7]

CONTROL TECHNIQUE

- Zero Current Switching [9]
- controlled on-time [6]
- high noise immunity [6]

UC3852 POWER FACTOR CORRECTION CONTROL IC BLOCK DIAGRAM

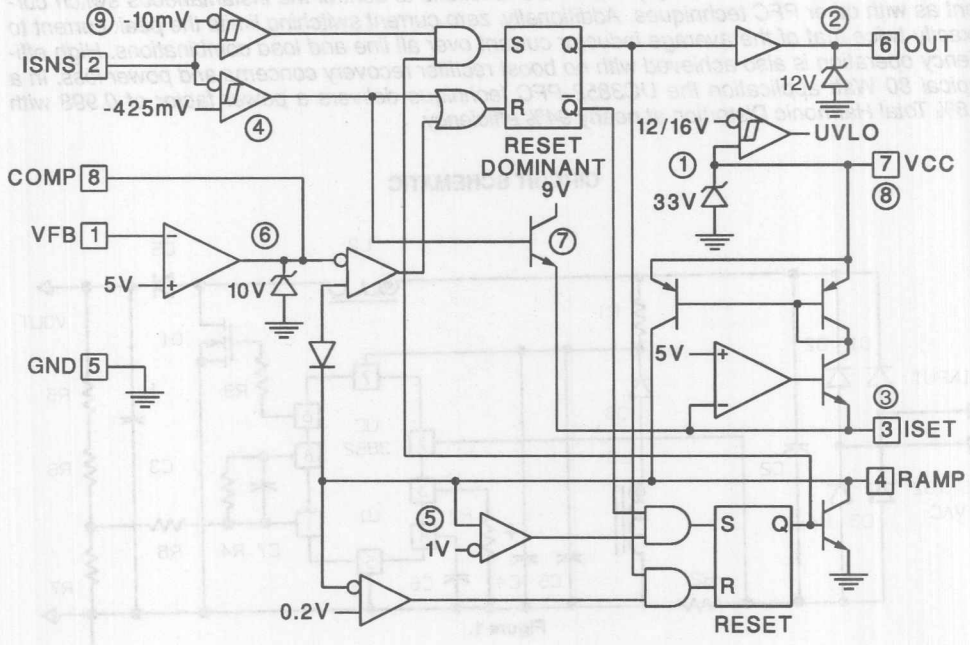


Figure 2.

UC3852 POWER FACTOR CORRECTION CONTROL IC BLOCK DIAGRAM

PFC TECHNIQUE OVERVIEW

Most power factor correction techniques incorporate the boost topology which can be operated in either the continuous or discontinuous inductor current modes and switched at a fixed or variable frequency. Generally, the fixed frequency, continuous inductor current variety is preferred for higher power applications to minimize the peak current. Below about 500 Watts, the discontinuous inductor current version operated in a variable frequency mode offers several advantages. Benefits include reduced inductor size, minimal parts count and low cost of implementation. This paper will highlight the controlled on-time, zero current switched variety of discontinuous inductor current PFC operation.

FUNDAMENTALS

CONTROLLED ON-TIME

On-time of the PFC switch is controlled by the voltage error amplifier of the UC3852 which is compared to a sawtooth waveform generated at the ICs RAMP function at pin 4. The PFC switch on-time varies with line and load conditions but should be considered constant for one line half-cycle. A low frequency bandwidth is necessary in the voltage error amplifier loop compensation which is typically rolled off to cross zero dB below the line frequency.

ZERO CURRENT SWITCHING

Zero current switching facilitates three important advantages in this application. First, the inductor current must be zero before the next switching cycle is initiated inferring high efficiency and elimination of the boost rectifier recovery loss. Secondly, the change in inductor current (delta IL) is equal to the peak inductor current (IL(pk)) since current starts and returns to zero each cycle. The discontinuous boost converter current waveform has a triangular shape with an area (charge) equal to one-half of the product of its height (peak current) multiplied by its base (time). Since the timebase can be considered as a series of consecutive triangles, the peak current is therefore limited to exactly twice that of the average current. This is valid for both the steady state and instantaneous switching cycle relationships. The converter operates right on the border between continuous and discontinuous current modes which results in variable frequency operation.

The "fixed" on-time in conjunction with zero current switching provide automatic power factor correction of the input current. This can be demonstrated by analyzing the basic inductor waveform using specific attributes of this PFC technique for either charging and discharging of the inductor current. Since the inductor charging condition is being controlled by the UC3852 circuitry it will be used for the analysis.

INDUCTOR WAVEFORM

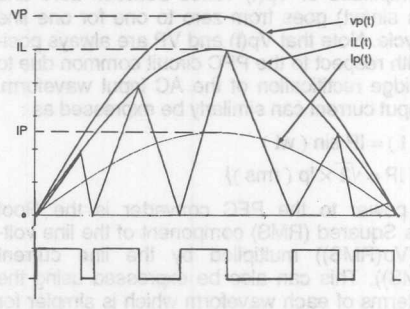


Figure 3.

1. $\frac{V}{L} = \frac{dI}{dt}$

For the PFC boost converter operation, V can be replaced by Vin(t), the instantaneous voltage across the inductor. Also, it is assumed that the inductance and the switch on-time is constant for the duration of one line-half cycle. The change in inductor current, delta I is actually the peak value of current (Ipk(t)) since the inductor always begins charging at zero current, as forced by zero current switching. Substituting these relationships into the inductor wave from equation will demonstrate the simplicity of this specific technique when used for power factor correction.

V = Vin(t)

L = constant

dI = Ipk(t)

dt = constant

2. $Ipk(t) \propto Vin(t)$

This relationship demonstrates that the instantaneous line current will exactly track that of the instantaneous line voltage. Since the input voltage waveform is sinusoidal (Vin sin(wt)), then so is the input current (Ipk sin (wt)). This controlled on-time, zero current switched technique provides automatic power factor correction with very simple control circuitry.

PFC POWER STAGE DESIGN

It is advantageous to begin the power relationships from the AC line input of the preregulator and work towards the DC output section. The instantaneous primary voltage (Vp(t)) is related to the steady state peak input (VP) by the following relationship:

3. $VP(t) = VP \sin(wt)$

where $VP = \sqrt{2} \times Vp(rms)$

The amplitude of Vp(t) varies between zero and VP as sin(wt) goes from zero to one for one line half-cycle. Note that Vp(t) and VP are always positive with respect to the PFC circuit common due to the bridge rectification of the AC input waveform. The input current can similarly be expressed as :

4. $IP(t) = IP \sin(wt)$

where $IP = \sqrt{2} \times Ip(rms)$}

Input power to the PFC converter is the Root Means Squared (RMS) component of the line voltage (Vp(RMS)) multiplied by the line current (Ip(RMS)). This can also be expressed using the peak terms of each waveform which is simpler for this application.

5. $Pin = \frac{VP}{\sqrt{2}} \times \frac{IP}{\sqrt{2}}$

$$Pin = \frac{(VP \times IP)}{2}$$

The average DC output current (Io) is determined by dividing the output power (Po) by the output voltage (Vo).

6. $Io = \frac{Po}{Vo}$

Converter efficiency (n) can also be factored into the design equations although it may typically be in the neighborhood of 94% at full load.

7. $Pin = \frac{Po}{n}$

or $Po = Pin \times n$

where $Pin = \frac{(VP \times IP)}{2}$

7A. $Po = \frac{(VP \times IP \times n)}{2}$

Equation 7A. can expressed with regard to primary current.

7B. $IP = \frac{(2 \times Po)}{(VP \times n)}$

It has been already established that the peak inductor current is exactly twice that of the average inductor current due to zero current switching.

8. $IL(pk) = 2 \times IL(avg)$

The average input current must be equal to the average inductor current since they are in series.

9. $Ipri(avg) = IL(avg)$

Combining equations yields the peak inductor current to the input current.

10. $Ipri(pk) = \frac{(4 \times Po)}{(VP \times n)}$

The inductor current can now be analyzed in its time variant form and over all line and load conditions.

11. $IL(t) = \frac{(4 \times Po \times \sin(wt))}{(VP \times n)}$

TIMING RELATIONSHIPS

Steady state conditions will be used to analyze the timing relationships of this controlled on-time PFC technique. The peak primary voltage (VP) will be used as the starting point for the calculations, so the input line must be specified.

The inductor relationship of equation 1. will be solved for the specific on-time required to charge the inductor to the correct peak current. This equation can be restated for a given set of operating conditions as:

12. $t(on) = IL(pk) \times \frac{L}{VP}$

Substituting equation 10. for IL(pk) into equation 12 results in:

12A. $t(on) = \frac{(4 \times Po \times L)}{(VP^2 \times n)}$

The instantaneous switch off-time varies not only with the line and load conditions, but also with the instantaneous line voltage. Off-time is analyzed by solving equation 1. for the inductor discharging where the voltage across the inductor is Vout minus Vin. This should be solved for the time required to discharge the current from its instantaneous peak to zero, which can be expressed as:

13. $t(off) = \frac{(IL(pk) \times L)}{(Vo - VP(\sin(wt)))}$

Substituting equation 11. for IL(pk) above will expand the off-time equation to:

13A. $t(off) = \frac{(4 \times Po \times L \times \sin(wt))}{VP \times (Vo - (VP \times \sin(wt)))}$

Due to the high efficiency during the boost inductor discharge and lack of rectifier recovery losses, the efficiency term (n) is essentially one. Loss can be ignored during the off-time since the boost diode forward voltage drop is very small in comparison to

the high voltage DC output, and resistive losses at these lower powers and currents are minimal.

CONVERSION PERIOD

The total time for one switching cycle is obtained by adding the on-time with the instantaneous off-time. Switching frequency is the reciprocal of the cyclical switching period which varies with line, load and instantaneous line voltage.

14. $t(per) = t(on) + t(off)$

$$t(per) = 4 \times Po \times L \times \left(\frac{1}{VP^2} + \frac{\sin(wt)}{VP \times [Vo - VP\sin(wt)]} \right)$$

SWITCHING FREQUENCY

15. $f(conv) = 1 / t(per)$

Switching frequency varies with the steady state line and load operating conditions along with the instantaneous input line voltage. Generally, the PFC converter is designed to operate above the audible range after accommodating all circuit and component tolerances. Many applications can use thirty kiloHertz (30 kHz) as a good first approximation. Higher frequency operation should also be evaluated as this can significantly reduce the inductor size without negatively impacting efficiency or cost. In most applications, the minimum switching frequency will coincide with full load operation during the peak of the input voltage waveform at low line. In contrast, the highest frequency conversion occurs at light load and high line conditions, just as the input voltage waveform nears the zero crossing point. A plot of t(on), t(off), t(per) and switching frequency versus instantaneous line voltage is shown in figure 4 and for the specific application circuit of figure 1. Figure 5 demonstrates the typical changes incurred in conversion frequency from low to high line inputs.

SELECTING THE OUTPUT VOLTAGE

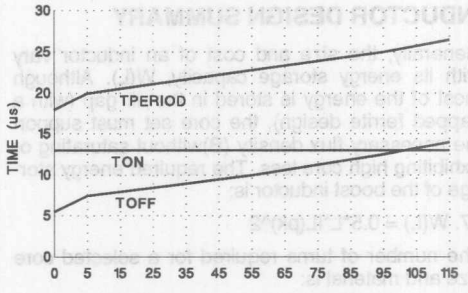
The boost converter output voltage should be designed to be at least thirty volts higher than the peak of the input voltage at high line. This will prevent long conversion cycles due to the small voltage across the discharging boost inductor. When this thirty volt margin is ignored, the minimum switching frequency will occur at the peak of high line operation and not at low line, but also at full load. This will require recalculation of the timing intervals.

INDUCTOR CONSIDERATIONS

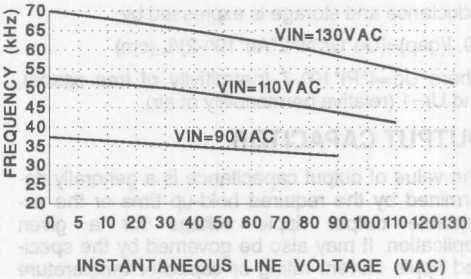
The exact inductor value can determined by solving equation 14 for the required inductance at the selected minimum operating frequency. Maximum on-time needs to be programmed into the UC3852 timing circuit. Both t(on)max and t(off)max will be individually calculated and added together to obtain the maximum conversion period, t(per)max. This is required to obtain the inductor value. Equations 12A and 13A will be solved for their respective maximums.

12B. $t\,(on)\,max = \dfrac{4 \times L \times Po\,(max)}{VP\,(min)^2}$

13B. $t\,(off)\,max = \dfrac{4 \times L \times Po\,(max)}{[VP\,(min) \times (Vo - VP\,(min)]}$



Conversion Times vs Instantaneous Line Nominal Line Voltage
Fig. 4



Conversion Frequency vs Instantaneous Line
Fig. 5.

14A. $t(per)max = t(on)max + t(off)max$

The minimum conversion frequency (F(conv)min) corresponds to the reciprocal of the maximum conversion period, t(per)max.

15A. $F(conv)min = 1 / t(per)max$

INDUCTOR VALUE

The inductance value necessary for an application can be obtained by substituting equations 12B and 13B into 15A. using the relationship of 14A.

$$16A.\ L = \frac{VP\ (min)^2 \times [Vo - VP\ (min)]}{4 \times Po\ (max) \times Vo \times F\ (conv)\ min}$$

This equation provides insight as to the possible ways to reduce the inductor value (size and cost) for a given set of design specifications. The most obvious approach is to increase the minimum conversion frequency above thirty kiloHertz if none of the other parameters (Vo, Po) can be varied.

INDUCTOR DESIGN SUMMARY

Generally, the size and cost of an inductor vary with its energy storage capacity, W(L). Although most of the energy is stored in the air gap (with a gapped ferrite design), the core set must support the necessary flux density (B)without saturating or exhibiting high core loss. The required energy storage of the boost inductor is:

17. W(L) = 0.5*L*IL(pk)^2

The number of turns required for a selected core size and material is:

18. N = L*IL(pk)*10^4 / (Bmax*Ae)

where Bmax is in Teslas and Ae is in square centimeters (cm^2)

The center leg gap to achieve the correct

inductance and storage is expressed by:

19. l(gap)={Uo*Ur*N^2*Ae*10^-2}/L (cm)

where Uo=4*Pi*10^-7 (permitivity of free space), and Ur=1 (relative permeability of air)

OUTPUT CAPACITOR

The value of output capacitance is a generally determined by the required hold-up time or the acceptable output ripple voltage for a given application. It may also be governed by the specified ripple current rating or capacitor temperature rise. Typically, an approximation of one microFarad per Watt (1uF/W) is a good starting point. The exact value can later be changed depending on conversion frequency and other factors previously mentioned.

Electrolytic capacitors are typically used near 80% of their working voltage. This will necessitate a 500 VDC rating for use in a 264 VAC PFC application which may not be practical from a cost perspective. One option is to connect two lower voltage capacitors in series, each having the same value and a 250VDC rating.

SEMICONDUCTOR SELECTION

Peak currents and voltages must first be known over all operating conditions to select the proper MOSFET switch and boost rectifier. Standard design practice is to derate all semiconductors to about 75% of their maximum ratings, indicating the use of 500+ volt devices.

Low cost bipolar transistors are an acceptable alternative to MOSFETs if the conversion frequency is maintained fairly low. Inexpensive high voltage diodes with recovery times of 200 nanoseconds, or less should be used for the boost rectifier. Two popular devices are the 1N4937 and MUR160. Speed is not an issue with the input bridge rectifiers where 1N4004 to 1N4006 types are acceptable. High frequency switching noise in the PFC converter should be well filtered before reaching the input bridge diodes due to their low speed characteristics. This is best accomplished by adding an L/C filter between the bridge rectifier DC output and the boost converter.

CONTROL CIRCUIT DESIGN :

PROGRAMMING THE UC3852

STARTUP CIRCUITRY

The UC3852 design incorporates a low startup current feature and draws less than one milliamp (mA) from the Vcc bias supply. This minimizes the power loss due to with the startup resistor after the converter begins operation when a bootstrap winding supplies the full DC supply current. The UC3852 IC turns on when Vcc reaches approximately 16 volts, and IC supply current will increase to its operational level. Undervoltage lockout protection will turn the UC3852 device off when the supply voltage falls below the lower UVLO threshold of approximately 10 volts.

The startup circuitry for this off-line consists of a startup resistor from Vcc to the input supply voltage and a storage capacitor from Vcc to ground. Typically, select Rstart to supply around 1.5 milliamps (rms) of charging current (I(charge) at low line. The exact value can be obtained from the following approximations.

$$R(start) = \frac{VP(min) - V(turn\text{-}on)}{1.41 \times I(charge)}$$

The Vcc bias supply filter capacitor value is determined by several factors, but primarily by the UC3852 undervoltage lockout hysteresis. Implementation and phasing of this boost inductor winding in addition to soft start circuitry will also effect the capacitance.

$$C(Vcc) = \frac{(ICC - I(charge) \times t(boot)}{UVLO\ hysteresis}$$

For many applications, the following approximations can be used:

ICC = 10 mA

I(charge) = 1.5 mA

t(boot) = 10 ms (one-half cycle at 50 Hz)

UVLO hysteresis = 5 volts

V(turn-on) = 15V

A standard 15 uF electrolytic with an adequate voltage rating (35V once derated) is used.

PROGRAMMING THE ON-TIME

The maximum switch on-time must be calculated to program the UC3852 oscillator. This maximum occurs when the line voltage, VP is at its minimum and the output power is at its maximum. This is more commonly known as the low line, full load condition.

t(on)max = 4*Pout(max)*L / Vp(min)^2

The UC3852 on-time is programmed by R/C components and uses two of the IC pins. A resistor from the ISET pin to ground programs the charging current into the RAMP pin. The Iset pin has an output voltage of approximately 5 volts, so the ISET is 5 volts divided by Rset. Typical charging current should range between 100 and 600 microamps.

The RAMP pin is used as one input to the Pulse Width Modulator of the UC3852. Internally, the RAMP voltage is compared to the error amplifier output (COMP) voltage to determine the exact on-time. The RAMP pin has a maximum amplitude of approximately 9 volts, and begins charging from approximately 0.2 volts, or an 8.8 volt swing.

The RAMP capacitor value is selected to program the maximum switch on-time as it charges from 0.2 to 9 volts by Iset. It can be calculated from the capacitor charge equation, shown below.

C = (I * dt) / dV

C(RAMP) = [Iset * t(on)max] / 8.8 V

The RAMP capacitor should be selected first from a list of standard values within the 100pF to 1nF range. The resulting ISET programming resistor selection is much easier as standard values with an initial tolerance of one percent (1%) are readily available.

$$RSET = \frac{5 \times t(on)max}{8.8 \times C(RAMP)}$$

or

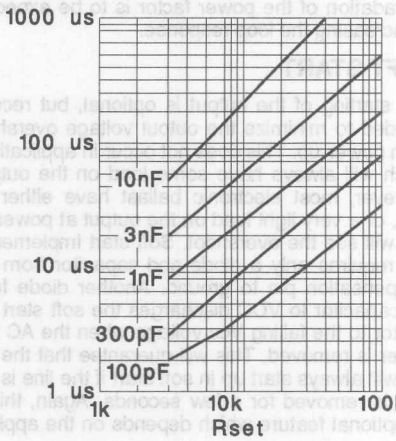
RSET = 0.568 * t(on)max / C(RAMP)

t(on)max = [RSET*C(RAMP)] / 0.568

UC3852 ON-TIME vs. RSET & C(RAMP)

ERROR AMPLIFIER COMPENSATION

Power Factor Correction using the ZCS controlled on-time technique requires a very low bandwidth voltage loop to deliver high power factor (). This is necessary to keep the switch on-time constant during any one line cycle. Other advantages to this approach are high noise immunity, and simplicity,



Max On-Time vs Rset and Ct
Fig. 6

since no squarer, multiply or divide circuitry is needed.

Configuration of the compensation circuitry is shown in the UC3852 PFC application schematic. First, the PFC preregulator output voltage (Vout) is accurately divided down to 5.0 volts to interface with the error amplifier. Three standard one-half watt resistors are used to avoid needing more expensive, high voltage rated resistors for this application. This signal goes through a 20K ohm input resistor to the error amplifier inverting input. Feedback components are a 1 meg ohm resistor and a 0.1 uF capacitor in parallel from the E/A output to the inverting input.

This recommended amplifier compensation delivers one low frequency pole in the loop response at 1.6 Hz, as programmed by 1 meg ohm and 0.1 uF components. Low frequency gain is determined by the 20 K ohm input resistor, the output voltage divider resistance and the 5.0 reference voltage seen at the amplifiers (internal) noninverting input.

Many other compensation arrangements are possible.

Using this compensation network, a low frequency gain of approximately 34 dB is achieved. This rolls off with a single pole (-20 dB/decade) response centering at 1.6 Hz. The gain curve will intersect zero dB at about 120 Hz and result in excellent power factor correction. Better dynamic response and less overshoot of the output voltage can be obtained by adjusting the 20 K ohm input resistor to increase low frequency gain and move the zero dB crossing out to a higher frequency. Some slight degradation of the power factor is to be expected by increasing the loop response.

SOFT START

Soft starting of the output is optional, but recommended to minimize the output voltage overshoot upon power-up. This does not occur in applications which will always have some load on the output. However, most electronic ballast have either no load, or a very light load on the output at power-up and will see the overshoot. Soft start implementation requires only a diode and capacitor from the compensation pin to ground. Another diode from the capacitor to VCC discharges the soft start capacitor to the falling Vcc voltage when the AC line power is removed. This will guarantee that the circuit will always start up in soft start if the line is AC plug is removed for a few seconds. Again, this is an optional feature which depends on the application.

One "trick" to significantly reduce the size of the soft start capacitor is to replace the diode with a cheap PNP transistor. A capacitance multiplier can be obtained by connecting the PNP emitter to the error amplifier output and soft start capacitor from the base to ground. The collector of the transistor is connected to ground. This adaptation will scale the capacitance value up by beta of the transistor at the amplifier output. A 2N2907 or equivalent is a popular choice and will reduce the capacitance value by a factor of approximately 50.

A 1N914 or 1N4148 signal diode should be used from the base to emitter to prevent negative base-emitter voltages from damaging the transistor. Additionally, this transistor can easily be interfaced with any optional fault protection schemes to soft start the controller following a fault.

SOFT START IMPLEMENTATION

CURRENT SENSE

Current in the PFC design is sensed in the return line of the preregulator circuitry at the AC input bridge rectifiers. One side of the current sense resistor is referenced to the UC3852 "ground" connection. The other end of the resistor develops the current sense voltage which is equivalent to minus IL(t) * Rsense. The UC3852 zero current detection circuitry incorporates two comparators, one for zero current detection and another for over current protection.

ZERO CURRENT DETECTION

The zero current detection circuitry uses a negative 10 millivolt (-10mV) threshold as its reference. This negative threshold guarantees that there are no

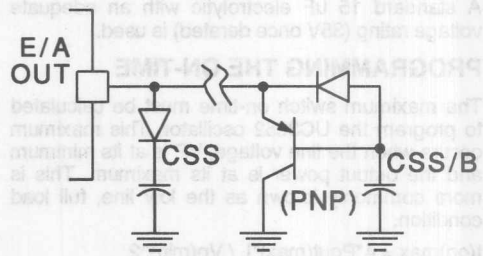


Figure 7.

startup problems since this input must be pulled below ground for normal operation. Whenever the zero detect input is raised above the minus ten millivolt threshold, the comparator is triggered and the next switching cycle begins.

Inductor current can be sensed by a current sense resistor which develops minus 400mV maximum during an overcurrent condition. This should only occur at a twenty percent overload, or 1.2 * IL(pk).

R(shunt) = 0.4 V / (1.2 * IL(pk))

Power dissipated in the shunt can be calculated by using the RMS component of the line current. The peak input current (IP) is one half of the peak inductor current (IL(max). The RMS component of the line current (IP(rms)) is obtained by dividing the peak line current (IP) by the square root of two (1.41).

IP(rms) = [IL(pk) / (2 * 1.414)]

P (R(sense)) = IP(rms)^2 * R(sense)

Standard value, low resistance (1 ohm or less) one-eighth to one-quarter watt resistors can used alone or paralleled to obtain the exact value. Carbon composition or film resistors exhibit low series inductance and will work best.

A small R/C filter can be added in the current sense circuitry to filter out switching noise caused by circuit parasitics. This delay will minimally effect the precise two-to-one ratio of the peak to average

duce the amount of EMI/RFI filtering required by minimizing the rectifier recovery noise. For best results, the filter delay time should match the rectifiers recovery time. A ten ohm resistor and a one nanoFarad (1 nF) capacitor are good starting values.

OVERCURRENT FAULT PROTECTION

The UC3852 contains and overcurrent comparator (-400mV) which quickly terminates the PWM output. This comparator also drives circuitry connected to the ISET pin which raises its normal 5 volt amplitude to 9 volts during the overcurrent condition. In addition to programming the ramp capacitor charging current, the ISET pin can be used to drive external fault protection circuits. A resistor in series with a 5.6 volt zener diode to the ISET pin will develop approximately 3.4 volts across the resistor when an overcurrent fault is detected. This signal can be used to trigger external shutdown or hiccup circuitry.

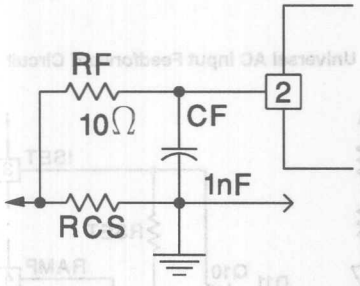


Figure 8.

GATE DRIVE

The UC3852 PWM output section is MOSFET compatible and rated for a one amp peak current. This totem pole design also features a twelve volt (12V) clamped output voltage to prevent excessive gate voltage when used with unregulated (Vcc) supply voltages. A twelve ohm resistor between the UC3852 and the MOSFET switch gate will limit the peak output current to its one amp maximum during normal operation.

Additionally, the UC3852 self biasing active low totem-pole design holds the MOSFET gate low during undervoltage lockout, preventing catastrophic problems at power-up and removal of the AC input.

inductor current and have an insignificant impact on power factor. However, this modification can re

ADVANCED PROTECTION CIRCUITRY

Certain applications of the UC3852 control IC may require sophisticated protection features. Some examples of these options are overvoltage protection and restart delay, soft start or latch-off following a fault. Each of these features can be added to the control circuit with a minimal amount of external parts, and often combined using shared components.

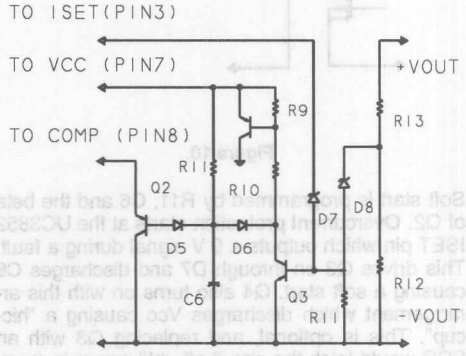


Figure 9.

LIST OF COMPONENTS

C6 = 1 uF, 35V
D5,6 = IN4148
D7 = 6.2 V ZENER
D8 = 40 V ZENER
Q2,4 = 2N2907
Q3 = 2N2222
R9,10 = 10 K
R11 = 1 MEG
R12 = 24 K
R13 = Calculate for OVP
R14 = 1 K

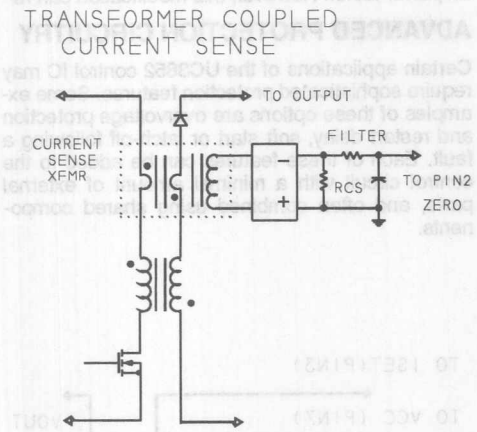


Figure 10.

Soft start is programmed by R11, C6 and the beta of Q2. Overcurrent protection starts at the UC3852 ISET pin which outputs a 9 V signal during a fault. This drives Q3 on through D7 and discharges C6 causing a soft start. Q4 also turns on with this arrangement which discharges Vcc causing a "hiccup". This is optional, and replacing Q3 with an SCR would latch the circuit off until power is reset. Overvoltage protection is attained via R11, R12, R13 and zener diode D8. When enough current flows through the zener (D8), R11 biases transistor Q3. Protection is similar to the overcurrent condition.

Regulated Auxiliary Bias Circuit

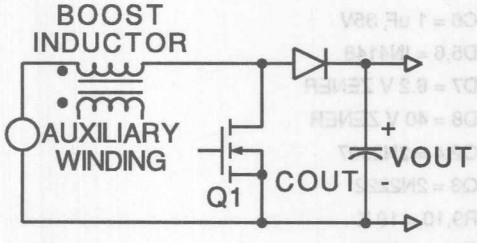


Figure 11.

CURRENT SENSE TRANSFORMERS

A transformer can be used to sense current in most of the UC3852 applications for higher efficiency. Two primary windings are needed to sense each component of the switched current. These may also be unequal in number of turns, depending on the input and output currents (or voltages). A single secondary winding and bridge rectification recreates the total inductor current. A small R/C filter network may be required to smoothen out spikes caused by the leakage inductance.

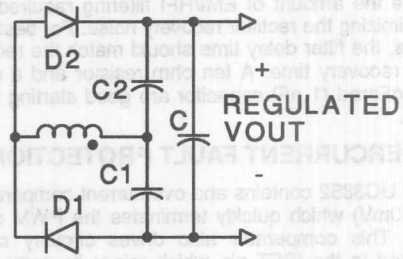


Fig. 12

Universal AC Input Feedforward Circuit

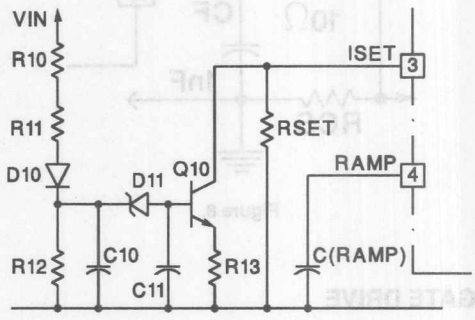


Figure 13.

REGULATED BOOTSTRAP SUPPLY

A regulated auxiliary supply is obtainable with a slight modification to the bootstrap interface and two inexpensive components. This circuit is advantageous in applications which incorporate other control ICs for the main converter or ballast drive sections. A regulated auxiliary voltage is NOT needed for the UC3852 which features a clamped twelve volt (typical) gate drive output voltage. This insures proper drive amplitude for power MOSFETs with an unregulated IC supply voltage to 30 volts.

Dual AC Input Range (110/220 VAC)
Feedforward Circuit

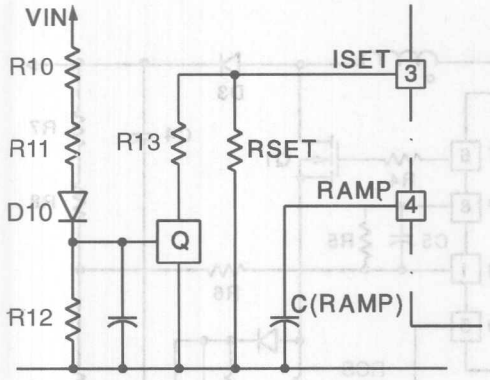


Figure 14.

OTHER PFC APPLICATIONS

The basic PFC schematic of Figure 1 can be used as a template for other PFC applications with different input voltage ranges and output power levels. A majority of the changes will be to accommodate higher (or lower) voltages and currents. Once familiar with the complete design procedure as outlined in this application note, designers are encouraged to recalculate the values for their applications using the same guidelines.

UNIVERSAL AC INPUT RANGE

The UC3852 controlled-on time, zero current switched PFC technique can be used to accommodate wide AC input voltages with the addition of a simple feedforward circuit. This external circuitry is required to cancel out the line dependent changes in the switch on-time over the three-to-one input range from 85 to 264 volts. Otherwise, the approximate nine-to-one control range of the UC3852 on-time would be fully used for line regulation allowing no accommodation for load changes.

CIRCUIT OPERATION

The rectified input voltage is applied across the network consisting of R10 through R12, D10 and C10. Capacitor C10 charges to the peak of the divided input voltage and is large enough to maintain this level over one line cycle. Diode D11 serves as an offset to bypass the range extender circuitry until a sufficient minimum line voltage has been established, typically 80 VAC. Capacitor C11, a small filter capacitor and the base of transistor Q10 reach a voltage of V(C10) minus the Zener forward voltage drop of diode D11. As this voltage rises, the emitter of Q10 and voltage across resistor R13 follows, offset by the base-emitter diode drop of Q10. This increasing bias pulls more current from the UC3852 ISET pin which sits at a fixed voltage. The current in both resistor R13 and resistor RSET is pulled from the UC3852 ISET output. Within the UC3852, the ISET current is mirrored to the RAMP capacitor (Cramp) which is compared to the error amplifier output to determine the ON-time. As the input voltage increases bias to Q10, more current is pulled from ISET thus increasing the RAMP charging current. For a fixed output load, this circuit performs the function of voltage feedforward and can keep the error amplifier output voltage fixed regardless of AC input voltage. This allows the full use of the ICs ON-time control range to accommodate load variations.

FEEDFORWARD CIRCUIT DESIGN

LOW LINE:

ISET= 5V/RSET

t(on)max=8.8*Cramp / ISET

HIGH LINE:

ISET= 5V/(RSET || R13)

GENERAL:

V(C10)=1.41*VIN*R12/(R10+R11+R12)

NOTE:V(C10)MAX=5V+Vzener

ISET(MIN)=5V/RSET

ISET(MAX)=ISET(MIN)+5V/R13

FEEDFORWARD BEGINS WHEN :

V(C10)-Vzener-Vbe(Q10) 0V

COMPONENTS:

C10=22uF/16V Q10=2N2222

C11=1nF/16V R10,11=100K

D10=1N4148 R12,13=5.1K

D11=1N5221(2.4V) RSET=51K

CONTINUOUS CURRENT PFC BOOST CONVERTER

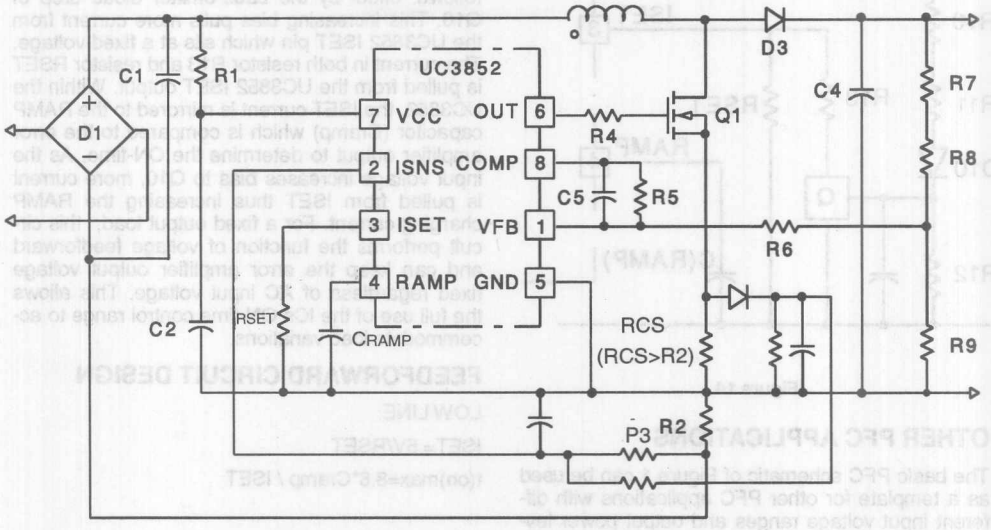


Figure 15.

CONTINUOUS PFC CURRENT IMPLEMENTATION

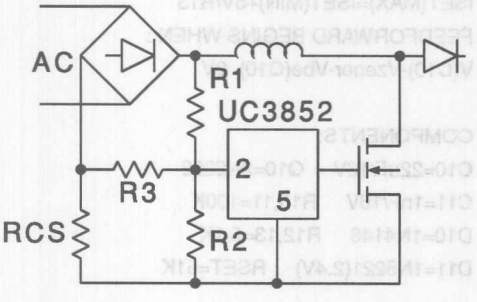


Figure 16.

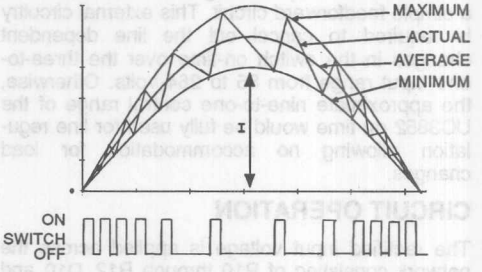


Figure 17.

UC3852 CONTROLLED PFC FLYBACK CONVERTER

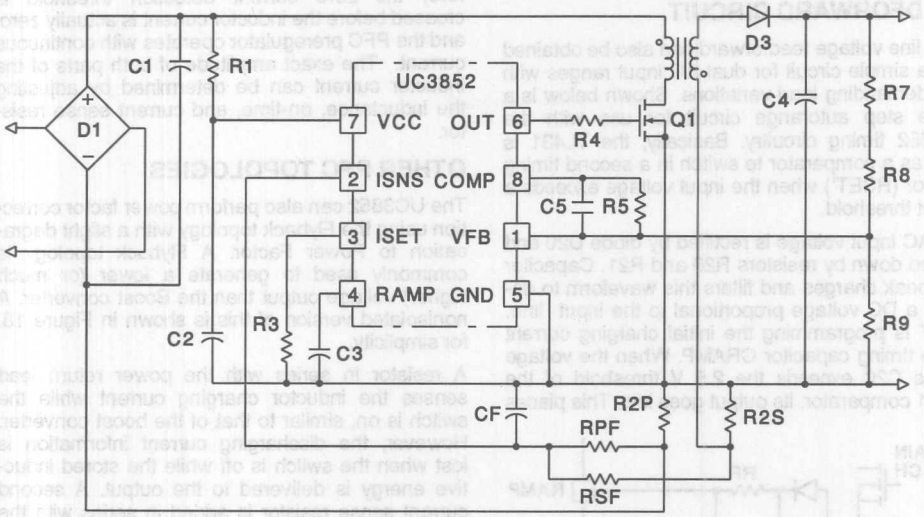


Figure 18.

UC3852 AS A CAPACITIVE DISCHARGE DRIVER

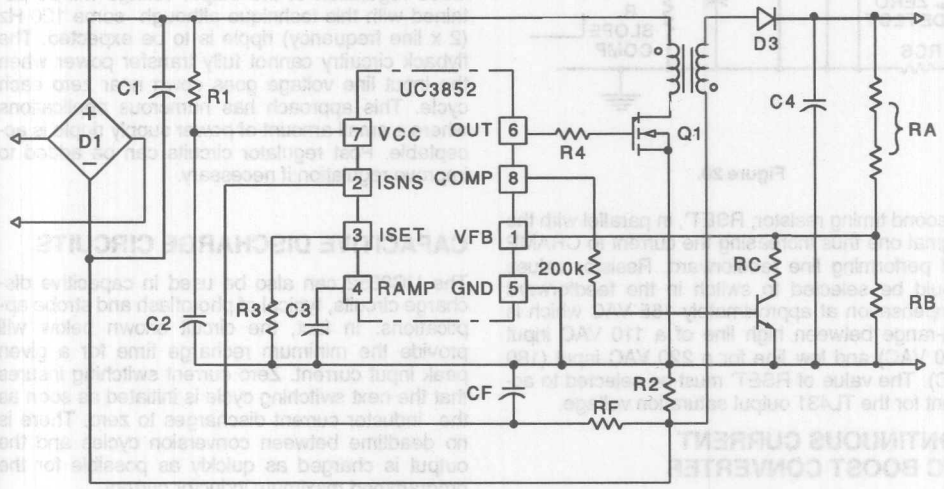


Figure 19.

AUTORANGE (110/220) VOLTAGE FEEDFORWARD CIRCUIT

Input line voltage feedforward can also be obtained with a simple circuit for dual AC input ranges with less demanding load variations. Shown below is a single step autorange circuit for use with the UC3852 timing circuitry. Basically, the TL431 is used as a comparator to switch in a second timing resistor (RSET') when the input voltage exceeds a preset threshold.

The AC input voltage is rectified by diode D20 and divided down by resistors R20 and R21. Capacitor C20 peak charges and filters this waveform to develop a DC voltage proportional to the input line. RSET is programming the initial charging current to the timing capacitor CRAMP. When the voltage across C20 exceeds the 2.5 V threshold of the TL431 comparator, its output goes low. This places

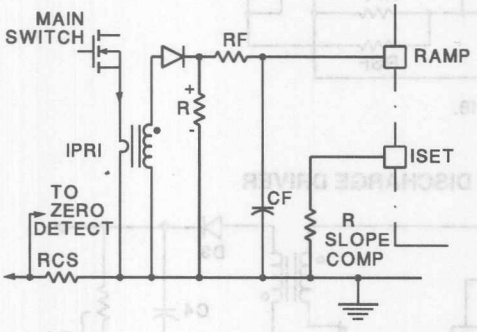


Figure 20.

a second timing resistor, RSET', in parallel with the original one thus increasing the current to CRAMP and performing line feedforward. Resistor values should be selected to switch in the feedforward compensation at approximately 155 VAC which is mid-range between high line of a 110 VAC input (130 VAC) and low line for a 220 VAC input (180 VAC). The value of RSET' must be selected to account for the TL431 output saturation voltage.

CONTINUOUS CURRENT PFC BOOST CONVERTER

The zero current switched PFC technique can also be modified to operate in the continuous inductor current mode. A positive amplitude, small offset signal is derived from the input voltage waveform. It gets added to the normal current sense signal which is negative with respect to ground. Summing these two signals to the ZEROinput biases the actual inductor current sense more positive. Therefore, the zero current detection threshold is crossed before the inductor current is actually zero, and the PFC preregulator operates with continuous current. The exact amplitude of both parts of the inductor current can be determined by adjusting the inductance, on-time, and current sense resistor.

OTHER PFC TOPOLOGIES

The UC3852 can also perform power factor correction using the Flyback topology with a slight degradation to Power Factor. A Flyback topology is commonly used to generate a lower (or much higher) voltage output than the Boost converter. A nonisolated version of this is shown in Figure 18. for simplicity.

A resistor in series with the power return lead senses the inductor charging current while the switch is on, similar to that of the boost converter. However, the discharging current information is lost when the switch is off while the stored inductive energy is delivered to the output. A second current sense resistor is added in series with the secondary winding as shown to recover this information. A small amount of filtering may be necessary to smoothen out switching noise spikes while summing the current sense signals.

Good regulation of the output voltage will be obtained with this technique although some 120 Hz (2 x line frequency) ripple is to be expected. The flyback circuitry cannot fully transfer power when the input line voltage goes down near zero each cycle. This approach has numerous applications where a small amount of power supply ripple is acceptable. Post regulator circuits can be added to improve regulation if necessary.

CAPACITIVE DISCHARGE CIRCUITS

The UC3852 can also be used in capacitive discharge circuits, typical of photoflash and strobe applications. In fact, the circuit shown below will provide the minimum recharge time for a given peak input current. Zero current switching insures that the next switching cycle is initiated as soon as the inductor current discharges to zero. There is no deadtime between conversion cycles and the output is charged as quickly as possible for the programmed maximum inductor current.

Regulation is achieved by using a burst mode of operation where the UC3852 stops delivering output pulses when the output voltage setpoint is reached. Operation will begin again when the output voltage drops below the lower programmed threshold. Both of these thresholds are pro-

grammed by Ra, Rb and Rc according to the following formulas.

Vout(max) = (5*(Ra+Rx))/Rx

Vout(min) = (5*(Ra+Rb))/Rb

where Rx=(Rb*Rc)/(Rb+Rc)

NON PFC APPLICATIONS USING VARIABLE FREQUENCY OPERATION

Conventional PWM (non PFC) applications using a variable frequency control techniques can also be implemented with the UC3852. This applies to both current mode and variable ON-Time control methods. Typical examples of these are discontinuous current boost and flyback converters. Variable frequency operation is popular in numerous applications as it can minimize the peak current in comparison to fixed frequency designs. The zero current detection and switching technique of the UC3852 should be used in its standard configuration with current sensed below ground, although a current transformer can be introduced.

IMPLEMENTING CURRENT MODE

The ICs RAMP input will be used as the current sense input to be compared to the error amplifier output for current mode control. A current transformer is recommended to fully utilize the 9 volt compliance of this pin. This implementation allows for a wide load swing with maximum noise immunity. The RAMP pin gets discharged by internal IC logic to 0.2 V at the end of each ON-time. Therefore, some series impedance to the current sense resistor is recommended to keep load current outside of the IC. Any filter capacitor to suppress the switch leading edge noise spike will also get discharged. The ramp pin does not need a programming resistor, but one could be used to introduce optional slope compensation via the filter capacitor.

VARIABLE ON-TIME CONTROL

The switch ON-Time can also be controlled by comparing a sawtooth ramp to the error amplifier output. Configuration of this is basically identical to the standard PFC application using a RAMP capacitor and resistor to program the maximum ON-Time. Error amplifier compensation is likely to be much different and utilize a much higher loop crossover frequency than its PFC counterpart. The ICs error amplifier is similar to a '741 type general purpose OP-AMP and is programmed accordingly.

REFERENCES and ADDITIONAL INFORMATION:

1. ANDREYCAK, W. : "Controlled ON-Time, Zero Current Switched Power Factor Correction Technique"; UNITRODE Power SUpply Design Manual SEM-800.

2. AHMED, SAEED, : "Controlled On-time Power FActor Correction Circuit with Input Filter"; Thesis, Virginia Polytechnic Institute.

3. MAMMANO,BOB and DIXON,LLOYD: "Designing High Power Factor Systems - Choosing the Optimum Circuit Topology", PCIM Magazine, March 1991.

PERFORMANCE EVALUATION

The UC3852 controlled PFC circuit shown in Figure 1 was constructed using the list of materials provided for this application. Power Factor and Total Harmonic Distortion to the 50th harmonic were measured using a VOLTEC PM- 3000 AC power analyzer. Test results indicated a power factor of 0.998 and T.H.D. below 6% at nominal line and full load. Very similar readings were obtained over the complete input voltage range and a moderate load change. Zero Current Switching (ZCS) facilitates high overall efficiency with this PFC technique.

UC3852 PFC TEST CIRCUIT

SPECIFICATIONS:

VIN = 85 TO 135 VAC

VOUT = 350 VDC

POUT = 86 W

MEASURED PERFORMANCE :

P.F. = 0.998

T.H.D. = 5.81 %

TEST CONDITIONS:

(nominal line)

VIN = 115.7 VAC

IIN = 0.799 AAC

PIN = 92.13 W

VA IN = 91.84

INRUSH Ipk = 17.7 A

VOUT = 355.6 VDC

IOUT = 0.242 ADC

POUT = 86.1 W

EFFICIENCY = 93.45 %

CURRENT WAVEFORM :

HARMONIC CONTENT

1st : 0.775 Amp

3rd : 3.91 %

5th : 0.82 %

7th : 0.38 %

9th : 0.35 %

11th : 1.30 %

13th : 0.21 %

LIST OF MATERIALS

CAPACITORS

C2 = 0.47 uF / 200 V

C3 = 82 uF / 400 V

C4 = 22 uF / 35 V

C5 = 0.1 uF / 35 V

C6 = 1 nF / 16 V

C7 = 0.1 uF / 16 V

DIODES

D1-4 = 1N4004, 1 A / 400V

D5 = 1N4937, 1 A / 600V

trr = 200ns

D6 = 1N4148, 0.2 A / 50 V

INDUCTORS

L2 = 1 mH Boost inductor

L3 = Several turns on L2 to provide 20 VDC supply voltage

RESISTORS

R1 = 100 k ohms 1 Watt

R2 = 0.1 ohm 1 W non-inductive

R3 = 18.2 k ohms 1% 1/2 W

R4 = 1 meg ohm 1/4 W

R5 = 330 k ohms 1% 1/2 W

R6 = 390 k ohms 1% 1/2 W

R7 = 10 k ohms 1% 1/4 W

R8 = 20 k ohms 1/4 W

R9 = 10 ohms 1/2 W non-inductive

TRANSISTOR

Q1 = IRF830 500 V / 4 A

INTEGRATED CIRCUIT

U1 = UC 3852

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

UNITRODE

UCC 3800/1/2/3/4/5 BiCMOS CURRENT MODE CONTROL ICs

BILL ANDREYCAK

INTRODUCTION

Power supply design has become increasingly more challenging as engineers confront the difficulties of obtaining higher power density, improved performance and lower cost. The control for many of these switchmode supplies was revolutionized with two significant introductions; an advance technique known as current mode control, and a novel PWM solution, the UC3842 controller. This IC contained several innovative features for general purpose current mode controlled applications. Included were high speed circuitry, undervoltage lockout, an op-amp type error amplifier, fast overcurrrent protection, a precision reference and a high current totem-pole output.

The popular UC3842 control circuit architecture has been recently improved upon to deliver even higher levels of protection and performance. Advanced circuitry such as leading edge blanking of the current sense signal, soft-start and full cycle restart have been built-in to minimize external parts count. Additionally, these integrated circuits have been developed on a BiCMOS wafer fabrication process geared to virtually eliminate supply power and propagation delays in comparison to the bipolar UC3842 devices. These sophisticated new BiCMOS controllers, the UCC3800 through UCC3805 pulse width modulators address the challenges presented by the upcoming generations of power supply designs. This application note will highlight the features incoporated into this new generation of PWM controllers in addition to realizeable enhancements in typical applications. The specific differences between members of the UCC3800/1/2/3/4/5 family are reflective of their maximum duty cycle, undervoltage lockout thresholds and reference voltage which are summarized in the following table.

Unitrode Part #	Max Duty Cycle	VRef (V)	UVLO Turn-On	UVLO Turn-Off
UCC3800	100%	5.0	7.2	6.9
UCC3801	50%	5.0	9.4	7.4
UCC3802	100%	5.0	12.5	8.4
UCC3803	100%	4.0	4.1	3.6
UCC3804	50%	5.0	12.5	8.4
UCC3805	50%	4.0	4.1	3.6

UCC3800/1/2/3/4/5 PWM FEATURES

A. Low start-up current
B. Undervoltage lockout
C. Low operating current
D. Internal soft start
E. Self biasing output during UVLO
F. Leading Edge Blanking
G. Self regulating Vcc supply
H. Full cycle restart after fault
I. Clamped gate drive amplitude
J. Reduced propagation delays
K. 5 Volt operation (UCC3803 & 05)

IN-CIRCUIT ADVANTAGES vs. UC3842

- Greatly reduced power requirements
- Eliminates bootstrap supply
- Fewer external components
- Lower junction temperature
- Reduced stress during faults
- No current sense R/C filter network
- Faster response to fault
- Higher frequency operation
- Higher maximum duty cycles

UCC3800/1/2/3/4/5 DEVICE OVERVIEW

The BiCMOS UCC3800/1/2/3/4/5 devices have similar standard features and pinouts to the bipolar UC3842/3/4/5 PWMs and are enhanced replacements in many applications. There are a few important differences however which may require minor modifications to existing applications.

APPLICATION DIFFERENCES

1. Maximum supply voltage from a low impedance source: 12V versus 30V
2. Undervoltage lockout thresholds
3. Start-up current
4. Operating current
5. Oscillator timing component values
6. Reference voltage (UCC3803 and 05)
7. Vcc supply self clamping zener voltage
8. Internal soft start
9. Internal full cycle restart
10. Clamped gate drive voltage
11. Current loop gain
12. E/A reference voltage ('03 & '05)

UCC3800/1/2/3/4/5 BLOCK DIAGRAM

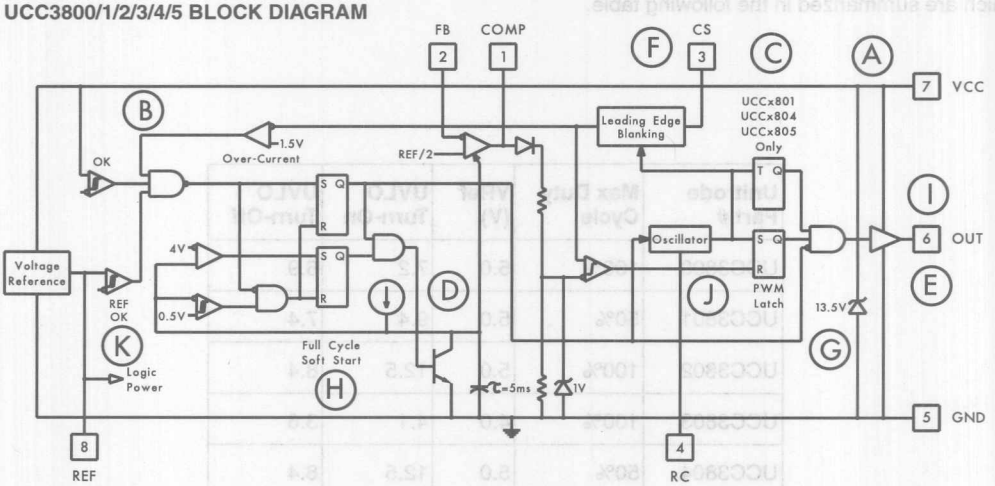


Figure 1.

SUPPLYING POWER

An internal Vcc shunt regulator is incorporated in each member of the UCC3800/1/2/3/4/5 PWMs to regulate the supply voltage at approximately 13.5 volts. A series resistor from Vcc to the input supply source is required with inputs above 12 volts to limit the shunt regulator current as shown in figure 2. A maximum of 10 milliamps can be shunted to ground by the internal regulator.

The internal regulator in conjunction with the device's low startup and operating current can greatly simplify powering the device and may eliminate the need for a regulated bootstrap auxiliary supply and winding in many applications. The supply voltage is MOSFET gate level compatible and needs no external zener diode or regulator protection with a current limited input supply. The UVLO start-up threshold is 1.0 volts below the shunt regulator level on the '02 and '04 devices to guarantee start-up.

It is important to bypass the ICs supply (Vcc) and reference voltage (Vref) pins with a 0.1uF to 1uF ceramic capacitor to ground. The capacitors should be located as close to the actual pin connections as possible for optimal noise filtering. A second, larger filter capacitor may also be required in off-line applications to hold the supply voltage (Vcc) above the UVLO turn-off threshold during start-up.

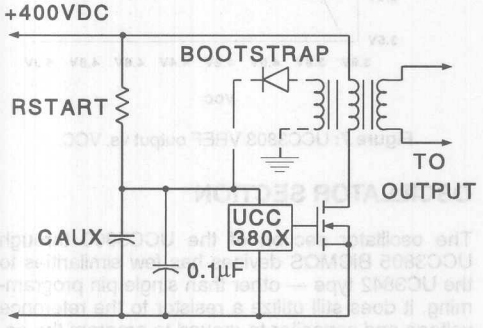


Figure 2. Powering the UCC3802.

UNDERVOLTAGE LOCKOUT

The UCC3800/1/2/3/4/5 devices feature undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. Both the supply voltage (Vcc) and the reference voltage (Vref) are monitored by the UVLO circuitry. An active low, self biasing totem pole output during UVLO design is also incorporated for enhanced power switch protection.

Undervoltage lockout thresholds for the UCC 3802/3/4/5 devices are different from the previous generation of UC3842/3/4/5 PWMs. Basically, the thresholds are optimized for two groups of applications; off-line power supplies and DC-DC converters. The UCC3802 and UCC3804 feature typical UVLO thresholds of 12.5V for turn-on and 8.3V for turn-off, providing 4.3V of hysteresis. For low voltage inputs which include battery and 5V applications, the UCC3803 and UCC3805 turn on at 4.1V and turn off at 3.6V with 0.5V of hysteresis. The UCC3800 and UCC3801 have UVLO thresholds optimized for automotive and battery applications.

During UVLO the IC draws approximately 100 microamps of supply current. Once crossing the turn-on threshold the IC supply current increases typically to about 500 microamps, over an order of magnitude lower than bipolar counterparts.

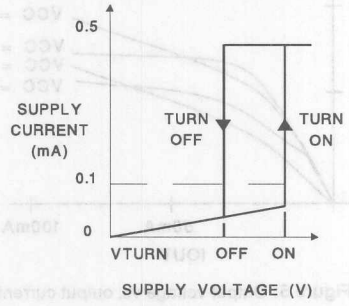


Figure 3. During Undervoltage Lockout

Device	Vton	Vtoff
UCC3800	7.2	6.9
UCC3801	9.4	7.4
UCC3802, 4	12.5	8.3
UCC3803, 5	4.1	3.6

SELF BIASING, ACTIVE LOW OUTPUT

The self biasing, active low clamp circuit shown eliminates the potential for problematic MOSFET turn on. As the PWM output voltage rises while in UVLO, the P device drives the larger N type switch ON which clamps the output voltage low. Power to this circuit is supplied by the externally rising gate voltage, so full protection is available regardless of the ICs supply voltage during undervoltage lockout.

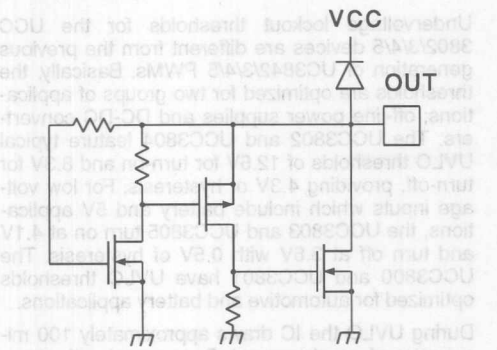


Figure 4: Internal circuit which holds output low during UVLO.

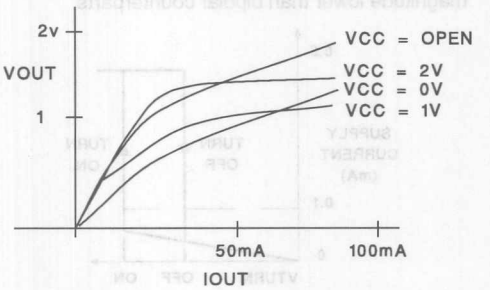


Figure 5: Output voltage vs. output current during UVLO.

REFERENCE VOLTAGE

The traditional 5.0V amplitude bandgap reference voltage of the UC3842 family can be also found on the UCC3800,1,2 and UCC3804 devices. However, the reference voltage of the UCC3803 and UCC3805 device is 4.0 volts. This change was necessary to facilitate operation with input supply voltages below five volts. Many of the reference voltage specifications are similar to the UC3842 devices although the test conditions have been changed, indicative of lower current PWM applications. Similar to their bipolar counterparts, the BiCMOS devices internally pull the reference voltage low during UVLO which can be used as a UVLO status indication.

REFERENCE DIFFERENCES

Note that the 4V reference voltage on the UCC3803 and UCC3805 is derived from the supply voltage (Vcc) and requires about 0.5V of headroom to maintain regulation. Whenever Vcc is below approximately 4.5V, the reference voltage also will drop outside of its specified range for normal operation. The relationship between Vcc and Vref during this excursion is shown in Figure 7.

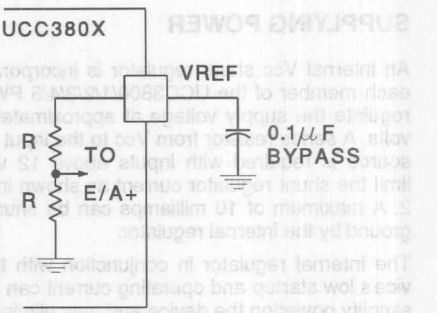


Figure 6: Required reference bypass.

The noninverting input to the error amplifier is tied to one-half of the PWMs reference voltage, Vref. Note that this input is 2.0V on the UCC3803 and UCC3805 and 2.5V on the higher reference voltage parts, the UCC3800, UCC3801, UCC3802 and UCC3804.

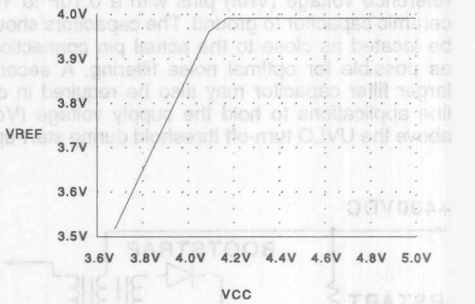


Figure 7: UCC3803 VREF output vs. VCC.

OSCILLATOR SECTION

The oscillator section of the UCC3800 through UCC3805 BiCMOS devices has few similarities to the UC3842 type — other than single pin programming. It does still utilize a resistor to the reference voltage and capacitor to ground to program the oscillator frequency up to 1 MHz. Timing component values will need to be changed since a much lower charging current is desirable for low power operation.

Several characteristics of the oscillator have been optimized for high speed, noise immune operation. The oscillator peak to peak amplitude has been increased to 2.45V typical versus 1.7V on the UC 3842 family. The lower oscillator threshold has been dropped to approximately 0.2 volts while the upper threshold remains fairly close to the original 2.8 volts at approximately 2.65V.

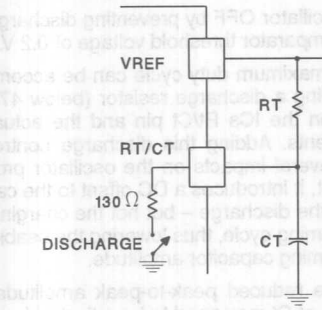


Figure 8: Oscillator equivalent circuit.

Discharge current of the timing capacitor has been increased to nearly 20 milliamps peak as opposed to roughly 8mA. As shown, this can be represented by approximately 130 ohms in series with the discharge switch to ground. A higher current was necessary to achieve brief deadtimes and high duty cycles with high frequency operation. Practical applications can utilize these new ICs to a 1 MHz switching frequency.

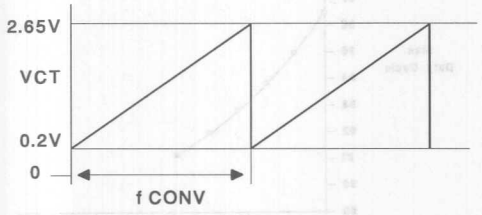


Figure 9: OSC Waveform

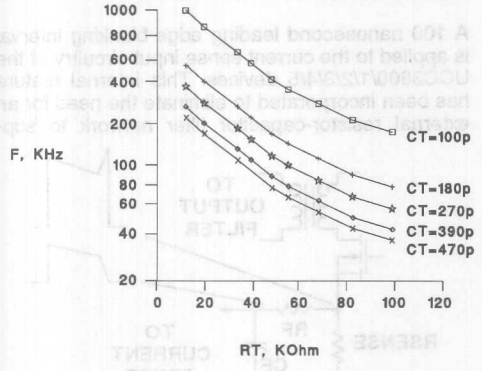


Figure 10: Oscillator frequency vs. RT for several CT.

SYNCHRONIZATION

Synchronization of these PWM controllers is best obtained by the universal technique shown in figure 12. The ICs oscillator is programmed to free run at a frequency about 20% lower than that of the synchronizing frequency. A brief positive pulse is applied across the 50Ω resistor to force synchronization. Typically, a one volt amplitude pulse of 100 nanoseconds width is sufficient for most applications.

The ICs can also be synchronized to a pulse train input directly to the oscillator Rt/Ct pin. Note that the IC will internally pull low at this node once the upper oscillator threshold is crossed. This 130 ohm impedance to ground remains active until the pin is lowered to approximately 0.2 V. External synchronization circuits should accommodate these conditions.

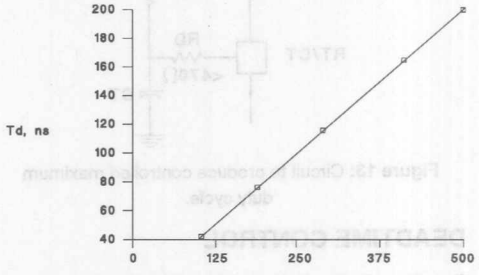


Figure 11: Minimum dead time vs. CT.

PWM SECTION : MAXIMUM DUTY CYCLE

Maximum duty cycle is higher for these devices than for their UC3842/3/4/5 predecessors. This is primarily due to the higher ratio of timing capacitor discharge to charge current which can exceed one-hundred to one in a typical BiCMOS application. **Attempts to program the oscillator maximum duty cycle much below the specified range by adjusting the timing component values of Rt and Ct should be avoided.** There are two reasons to refrain from this design practice. First, the ICs high discharge current would necessitate higher charging currents than necessary for programming,

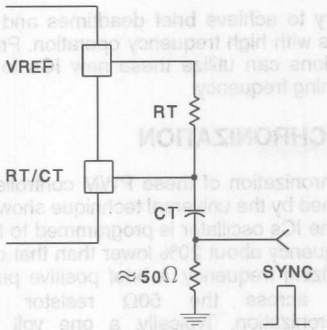


Figure 12: Synchronizing the oscillator.

defeating the purpose of low power operation. Secondly, a low value timing resistor will prevent the capacitor from discharging to the lower threshold and initiating the next switching cycle.

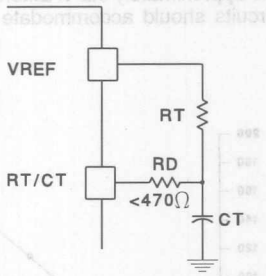


Figure 13: Circuit to produce controlled maximum duty cycle.

DEADTIME CONTROL

Deadtime is the term used to describe the guaranteed OFF time of the PWM output during each oscillator cycle. It is used to insure that even at maximum duty cycle, there is enough time to reset the magnetic circuit elements, and prevent saturation.

The deadtime of the UCC380x PWM family is determined by the internal 130 Ohm discharge impedance and the timing capacitor value. Larger capacitance values extend the deadtime whereas smaller values will result in higher maximum duty cycles for the same operating frequency. A curve for deadtime versus timing capacitor values is provided in figure 11.

Increasing the deadtime is possible by adding a resistor between the Rt/Ct pin of the IC and the timing components. The deadtime increases with the discharge resistor value to about 470 Ohms as indicated from the curve. Higher resistances should be avoided as they can decrease the deadtime and reduce the oscillator peak-to-peak amplitude. Sinking too much current (1 mA) by reducing Rt will "freeze" the oscillator OFF by preventing discharge to the lower comparator threshold voltage of 0.2 V.

Reducing the maximum duty cycle can be accomplished by adding a discharge resistor (below 470 Ohms) between the ICs Rt/Ct pin and the actual Rt/Ct components. Adding this discharge control resistor has several impacts on the oscillator programming. First, it introduces a DC offset to the capacitor during the discharge – but not the charging portion of the timing cycle, thus lowering the usable peak-to-peak timing capacitor amplitude.

Because of the reduced peak-to-peak amplitude, the exact value of Ct may need to be adjusted from UC3842 type designs to obtain the correct initial oscillator frequency. One alternative is keep the same value timing capacitor and adjust both the timing and discharge resistor values since these are readily available in finer numerical increments.

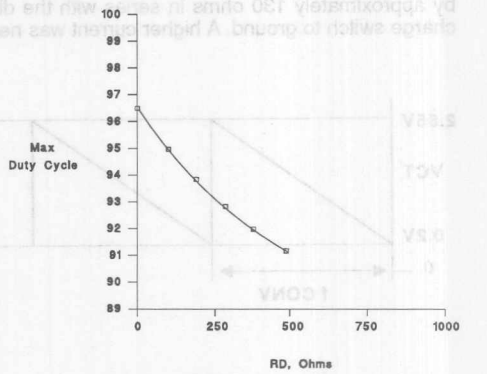


Figure 14: Maximum duty cycle vs. RD for RT = 20k.

LEADING EDGE BLANKING

A 100 nanosecond leading edge blanking interval is applied to the current sense input circuitry of the UCC3800/1/2/3/4/5 devices. This internal feature has been incorporated to eliminate the need for an external resistor-capacitor filter network to sup-

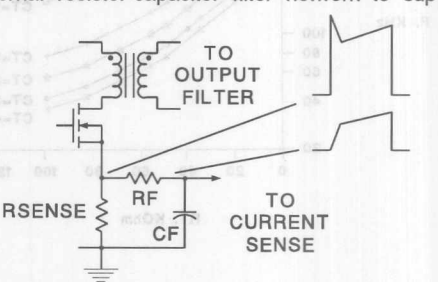


Figure 15: Current sense filter required with older PWM ICs.

press the switching spike associated with turn-on of the power MOSFET. This 100 nanosecond period should be adequate for most switchmode designs but can be lengthened by adding an external R/C filter.

Note that the 100 ns leading edge blanking is also applied to the cycle-by-cycle current limiting function in addition to the overcurrent fault comparator.

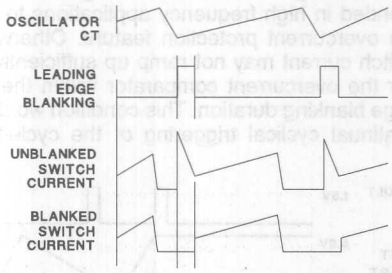


Figure 16: Current sense waveforms with leading edge blanking.

MINIMUM PULSE WIDTH

The leading edge blanking circuitry can lead to a minimum pulse width equal to the blanking interval under certain conditions. This will occur when the error amplifier output voltage (minus a diode drop and divided by 1.65) is lower than the current sense input. However, the amplifier output voltage must also be higher than a diode forward voltage drop of about 0.5V. It is only during these conditions that a minimum output pulse width equal to the blanking duration can be obtained.

Note that the PWM comparator has two inputs; one is from the current sense input. The other PWM input is the error amplifier output which has a diode and two resistors in series to ground. The diode in this network is used to guarantee that zero duty cycle can be reached. Whenever the E/A output falls below a diode forward voltage drop, no current flows in the resistor divider and the PWM input goes to zero, along with pulse width.

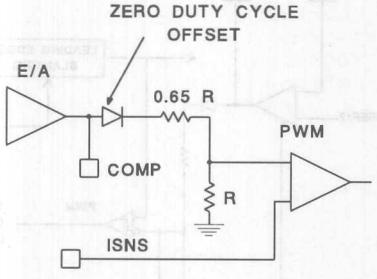


Figure 17.

Zero duty cycle is achievable by forcing the error amplifier output below the zero duty cycle threshold of one diode voltage drop.

PROTECTION CIRCUITRY: CURRENT LIMITING

A 1.0 volt (typical) cycle-by-cycle current limit threshold is incorporated into the UCC3800 family. Note that the 100 nanosecond leading edge blanking pulse is applied to this current limiting circuitry. The blanking overrides the current limit comparator output to prevent the leading edge switch noise from triggering a current limit function.

Propagation delay from the current limit comparator to the output is typically 70 nanoseconds. This high speed path minimizes power semiconductor dissipation during an overload by abbreviating the on time.

CURRENT SENSE OFFSET CIRCUITRY

For increased efficiency in the current sense circuitry, the circuit shown in figure 18 can be used. Resistors RA and RB bias the actual current sense resistor voltage up, allowing a small current sense amplitude to be used. This circuitry provides current limiting protection with lower power loss current sensing.

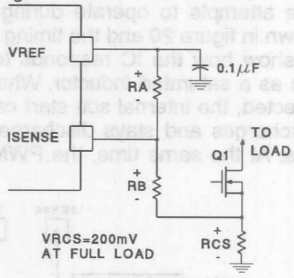


Figure 18: Biasing Isense for lower current sense voltage.

The example shown uses a 200 millivolt full scale signal at the current sense resistor. Resistor Rb biases this up by approximately 700 mV to mate with the 0.9V minimum specification of the current limit comparator of the IC. The value of resistor Ra changes with the specific IC used, due to the different reference voltages. The resistor values should be selected for minimal power loss. For example, a 50 uA bias sets Rb = 13k ohms, Ra=75 k ohms (UCC3800,1,2,4) or Ra=56k ohms with the UCC3803 and UCC3805 devices.

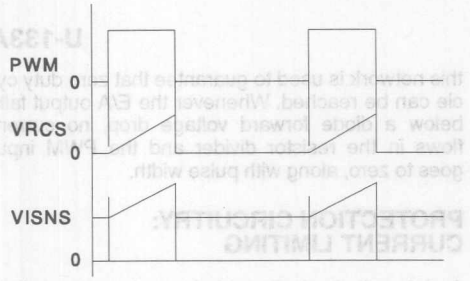


Figure 19.

OVERCURRENT PROTECTION AND FULL CYCLE RESTART

A separate overcurrent comparator within the UCC 3800/1/2/3/4/5 devices handles operation into a short circuited or severely overloaded power supply output. This overcurrent comparator has a 1.5 volt threshold and is also gated by the leading edge blanking signal to prevent false triggering. Once triggered, the overcurrent comparator uses the internal soft start capacitor to generate a delay before retry is attempted. Often referred to as "hiccup", this delay time is used to significantly reduce the input and dissipated power of the main converter and switching components.

Full Cycle Soft Start insures that there is a predictable delay of greater than 3 milliseconds between successive attempts to operate during fault. The circuit shown in figure 20 and the timing diagram in figure 21 show how the IC responds to a severe fault, such as a saturated inductor. When the fault is first detected, the internal soft start capacitor instantly discharges and stays discharged until the fault clears. At the same time, the PWM output is turned off and held off. When the fault clears, the capacitor will slowly charge and will allow the error amp output (COMP) to rise. When COMP gets high enough to enable the ouput, another fault occurs, latching off the PWM output, but the soft start capacitor still continues to rise to 4V before being discharged and permitting start of a new cycle. This means that for a severe fault, sucessive retries will be spaced by the time required to fully charge the soft start capacitor.

Low leakage transformer designs are recommended in high frequency applications to activate the overcurrent protection feature. Otherwise, the switch current may not ramp up sufficiently to trigger the overcurrent comparator within the leading edge blanking duration. This condition would cause continual cyclical triggering of the cycle-by-cycle

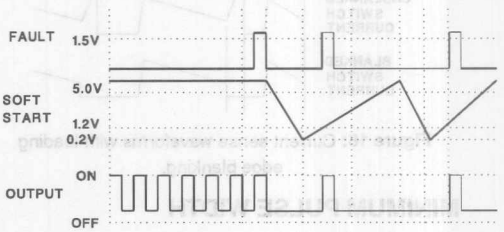


Figure 21.

current limit comparator but not the overcurrent comparator. This would result in brief high power dissipation durations in the main converter at the switching frequency. The intent of the overcurrent comparator is to reduce the effective retry rate under these conditions to a few milliseconds, thus significantly lowering the short circuit power dissipation of the converter.

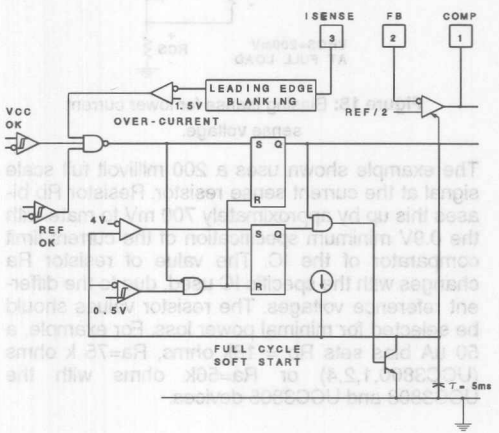


Figure 20.

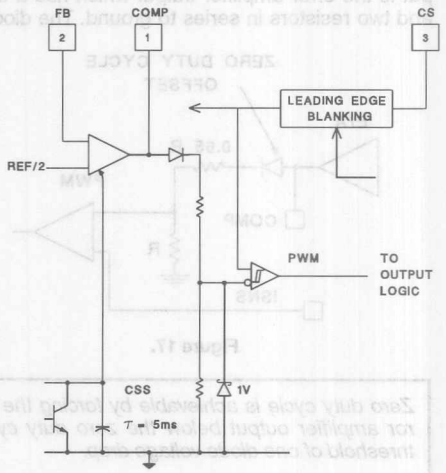


Figure 22.

SOFT START

Internal soft starting of the PWM output is accomplished by gradually increasing error amplifier (E/A) output voltage. When used in current mode control, this implementation slowly raises the peak switch

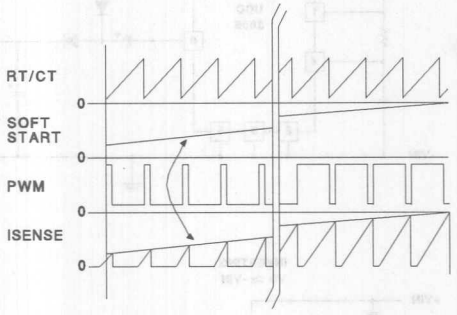


Figure 23.

current each PWM cycle in comparison, forcing a controlled start-up. In voltage mode (duty cycle) control, this feature continually widens the pulse width.

The soft start capacitor (Css) is discharged following an undervoltage lockout transition or if the reference voltage is below a minimum value for normal operation. Additionally, discharge of Css occurs whenever the overcurrent protection comparator is triggered by a fault.

Soft start is performed within the UCC3800/-1/2/3/4/5 devices by clamping the E/A amplifier output to an internal soft start capacitor (Css) which is charged by a current source. The soft start clamp circuitry is overridden once Css charges above the voltage commanded by the error amplifier for normal PWM operation.

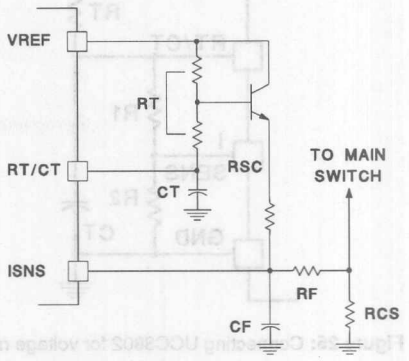


Figure 24: Adding slope compensation.

APPLICATIONS SECTION: CURRENT MODE CONTROL

Peak current mode control is obtained by feeding the converters switch current waveform into the current sense (Isens) input of a UCC3800/1/2/3/4/5 device. The sense resistor should be selected to develop a 0.9 V peak amplitude at full load, including slope compensation. Because of the internal 100 ns typical leading edge blanking, the traditional resistor-capacitor (Rf/Cf) filter to suppress the turn-on noise spike may not be needed.

SLOPE COMPENSATION

Slope compensation can be added in all current mode control applications to cancel the peak to average current error. Slope compensation is neces-

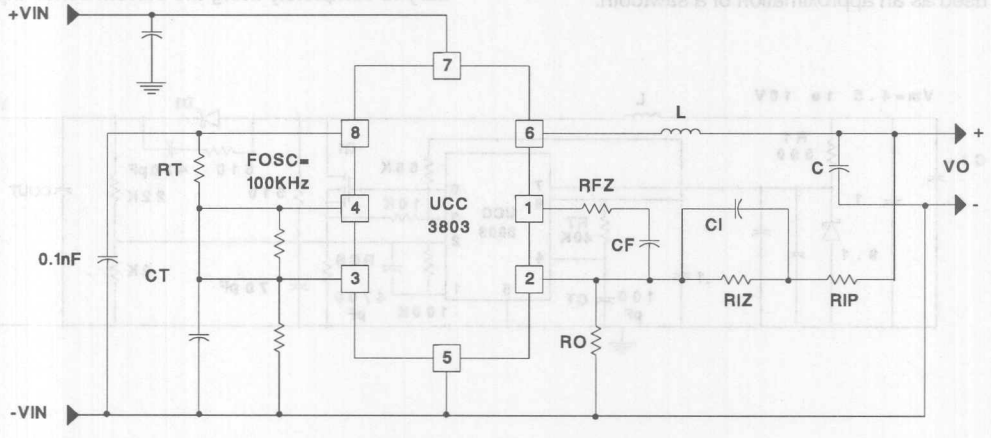


Figure 27: Low-power buck PWM example using on-chip power FETs.

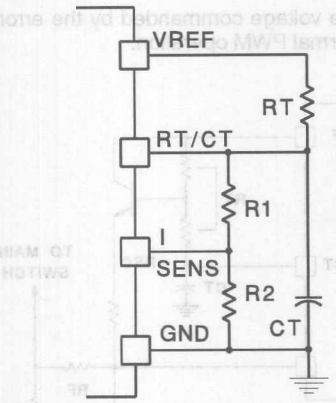


Figure 25: Connecting UCC3802 for voltage mode.

sary with applications with duty cycles exceeding 50%, but also improves performance in those below 50%.

Primary current is sensed using resistor Rcs in series with the converter switch. The timing resistor can be broken up into two series resistors to bias up the NPN follower. This is needed to provide ample compliance for slope compensation at the beginning of a switching cycle, especially with continuous current converters. A NPN voltage follower drives the slope compensating programming resistor (Rsc) to provide a slope compensating current into Cf.

VOLTAGE MODE OPERATION

Any current mode control IC can be used as a direct duty cycle control (voltage mode) by applying a sawtooth ramp to the current sense input. The exponential charging of the timing capacitor (Ct) is used as an approximation of a sawtooth.

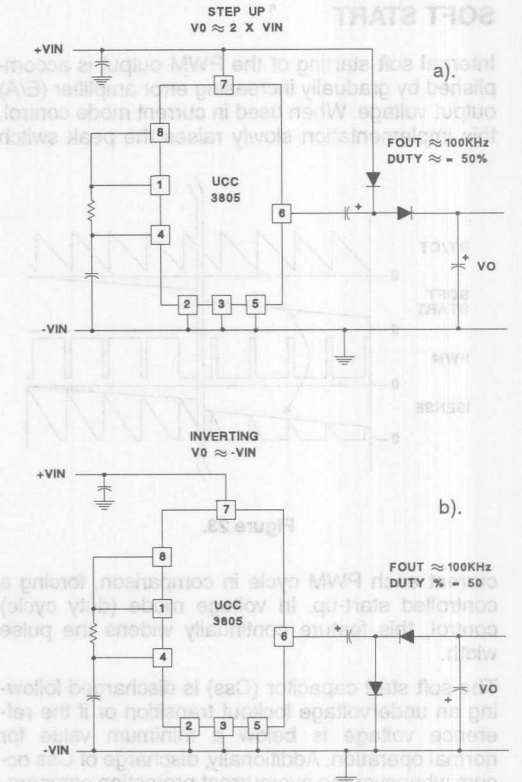


Figure 26: a) Using the UCC3805 to double VIN.
b). Using the UCC3805 to create Vo = –VIN.

The oscillator waveform is resistively divided down by R1 and R2 to a 0.9V maximum amplitude and fed into the current sense input for duty cycle control. A small capacitor across R1 might be necessary to completely bring the current sense input to

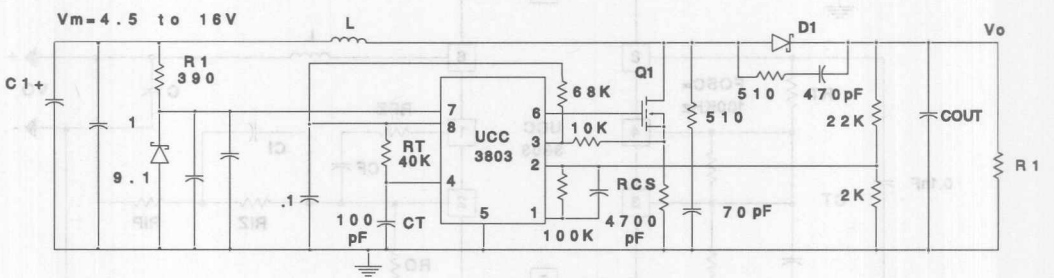


Figure 28: A practical boost PWM example.

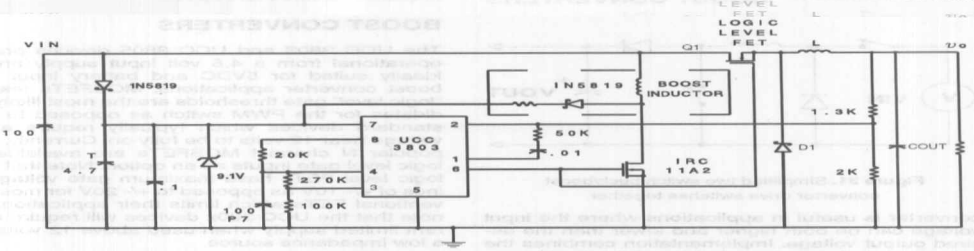


Figure 29: A practical buck PWM that runs with VIN ≥ 4.1V.

zero volts at the beginning of each PWM cycle. Current in the divider network should be kept around 50 microamps, a compromise between low power consumption and good noise immunity. A 15K ohm and 30 K ohm are used in the example.

This circuit can also be used to program the PWM maximum duty cycle. Values should be calculated to attain the 0.9V current sense voltage at the desired maximum duty cycle.

LOW POWER DC/DC CONVERTERS CHARGE PUMP CONVERTERS

Charge pump converters are popular for simple, low power applications. The two basic applications are free running step-up and inverting switchers which use few external components as shown in figure 26.

LOW POWER BUCK REGULATOR

For voltage step down applications, the UCC 380x totem pole output can be used as both the switch and commutating diode of the buck regulator (see figure 27). Power dissipation and the one amp peak current rating of the IC's output stage limit the range of applications to less than 1 amp of output current. High frequency operation permits the use of small and inexpensive surface mount components.

BUCK-BOOST CONVERTER for VOLTAGE STEP-UP and/or STEP-DOWN APPLICATIONS

A two-switch buck-boost converter can be controlled by the UCC380x family of PWMs. This specific

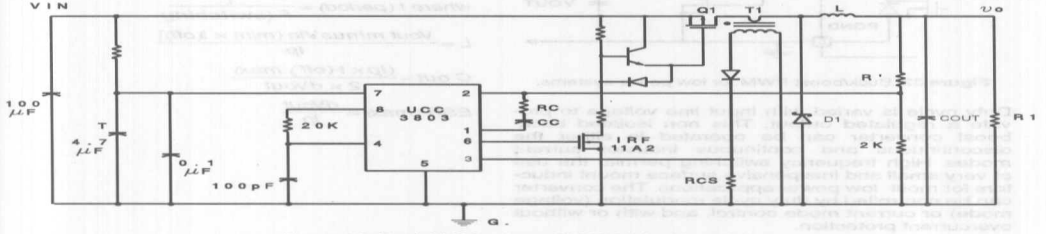


Figure 30: Buck PWM using a PMOS high-side switch.

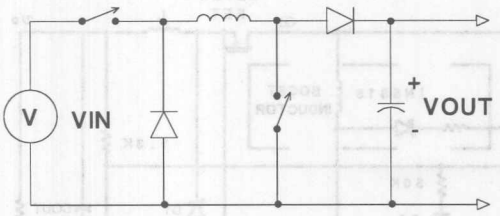


Figure 31. Simplified two switch buck/boost converter drive switches together.

converter is useful in applications where the input voltage can be both higher and lower than the desired output voltage. Implementation combines the voltage step-down characteristic of the buck regulator with the voltage step-up of the boost converter. Both switches are driven simultaneously with this adaptation to simplify the control algorithm. Note that the PWM output of the IC will be used directly for the high side switch in a low power application thus requiring only one external switch. Also, the body diode of the lower side totem-pole output is used as one of the commutating rectifiers, further reducing complexity. As shown in figure 31, this approach is ideal for low voltage, low power DC to DC applications. Higher voltage and higher power applications will require the use of discrete semiconductors for the high side switch and lower diode.

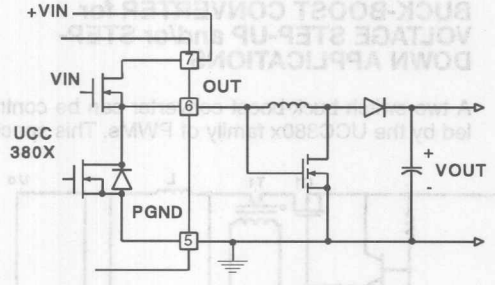


Figure 32. Buck/boost PWM for low power systems.

Duty cycle is varied with input line voltage to provide a regulated output. This non isolated buck-boost converter can be operated in either the discontinuous and continuous inductor current modes. High frequency switching permits the use of very small and inexpensive surface mount inductors for most low power applications. The converter can be controlled by duty cycle modulation (voltage mode) or current mode control, and with or without overcurrent protection.

BOOST CONVERTERS

The UCC 3803 and UCC 3805 devices are fully operational from a 4.5 volt input supply and are ideally suited for 5VDC and battery input PWM boost converter applications. MOSFETs featuring "logic level" gate thresholds are the most likely candidates for the PWM switch as opposed to using standard devices which typically require a gate voltage near 12 volts to be fully on. Currently, many popular N channel MOSFETs are available with logic level gate inputs as an option. Note that many logic level FETs have maximum gate voltage ratings of +/- 10V as opposed to +/- 20V for most conventional FETs which limits their application. Also note that the UCC 380x devices will require a current limited supply when used above 12 volts from a low impedance source.

A basic current mode controlled boost converter application circuit is shown in figure 28. Typical component values for 250 kHz operation are listed in the following tables for a 12V and 24V output applications. The boost converter design equations are summarized below.

BOOST DESIGN SUMMARY:

(Discontinuous inductor current)

$$Vout = Vin \times \left(\frac{t(on)}{t(off)} + 1 \right)$$

$$Iin = Iout \times \left(\frac{t(on)}{t(off)} + 1 \right)$$

$$Ip = 2 \times Iin \times \frac{t(period)}{t(on)}$$

$$Ip = \frac{2 \times t(period) \times Iout \times (t(on) + t(off))}{[t(on) \times t(off)]}$$

$$where\ t(period) = \frac{1}{F(switching)}$$

$$L = \frac{Vout\ minus\ Vin(min) \times t(off)]}{Ip}$$

$$C\,out = \frac{(Ip \times t(off))\ max}{2 \times dVout}$$

$$ESR(max) = \frac{dVout}{Ip}$$

VIN = 4.5 to 10 VDC

VOUT = 12 VDC

IOUT = 0.2, 0.4, 1 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	3W	6W	12W
D1	1A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	12uH	6.8uH	1.8uH
PCH-	27-123	27-682	27-182
Cout	100uF	300uF	500uF
Rcs(ohm)	0.1	0.05	0.033
Q1*	2A/50V RFL2NO5L	IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 2

VIN = 4.5 to 10 VDC

VOUT = 24 VDC

IOUT = 0.1, 0.2, 0.5 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	3W	6W	12W
D1	1A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	12uH	6.8uH	3.9uH
PCH-	27-123	27-682	27-392
Cout	100uF	200uF	500uF
Rcs(ohm)	0.1	0.05	0.033
Q1*	2A/50V RFL2NO5L	8A/50V IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

VOUT = 24 VDC

IOUT = 0.1, 0.2, 0.5 ADC

DISCONTINUOUS I MODE

F(SWITCHING) = 250kHz

POUT	3W	6W	12W
D1	1A/40V 1N5819	3A/40V 1N5822	6A/45V 6TQ045
L	22uH	12uH	3.9uH
PCH-	27-223	27-123	27-392
Cout	100uF	200uF	500uF
Rcs(ohm)	0.2	0.1	0.066
Q1*	3A/60V IRFF113	3A/60V IRFF113	IRFF133

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

BUCK REGULATOR

The buck regulator is a more difficult design challenge than the boost converter due to the high side switch. A transformer coupled gate drive is typically required to deliver drive pulses to the switch, which requires about ten volts above the input voltage for proper drive. Current mode control further complicates the design by requiring a current transformer to level shift the high side current sense signal down to the ground based input of the IC. In many applications, direct duty cycle control (voltage mode) can be used to simplify the design although overcurrent protection is lost with common ground applications.

Several examples of common buck regulator application circuits are shown in figures 29 and 30. Direct duty cycle control is used for simplicity, however current mode control can be easily adapted as shown in the example. Tables listing component values and typical part numbers have been included.

DESIGN EQUATIONS:

$Vout = Vin * D$ (duty cycle)

$$where\ D = \frac{T(on)}{T(period)}$$

$$L = Vout \times \frac{t(off)}{d\ Io}$$

where: Delta Io is the inductor ripple current and equal to one-half of the minimum output current. Minimum output current has been selected as 10% of the full load current

$$Ipk = Io + \frac{d\ Io}{2}$$

$Iin(DC) = Iout * D$

$$Cout = \frac{d\ Io}{(8 \times F \times d\ Vout)}$$

where F is the switching frequency and Δ Vout is the output ripple voltage

BUCK REGULATOR DESIGN TABLES

TABLE 4

VIN = 4.5 to 10 VDC

VOUT = 3.3 VDC

IOUT = 1, 3 and 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	1A	3A	5A
D1	3A/20V 1N5820	6A/40V 6TQ045	12A/45V 12TQ045
L	39uH	22uH	6.8uH
PCH-	27-393	45-223	45-682
Cout	2uF	4.7uF	10uF
Q1*	8A/60V IRLZ14	8A/60V IRLZ14	IRLZ14

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 5

VIN = 10 to 18 VDC

VOUT = 5 VDC

IOUT = 1, 3 and 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	1A	3A	5A
D1	3A/40V 1N5822	6A/40V 6TQ045	12A/40V 12TQ045
L	120uH	39uH	22uH
PCH-	27-1243	45-393	45-223
Cout	2uF	5uF	10uF
Q1*	4A/50V IRF9Z12	8A/50V IRF9Z22	12A/50V IRF9Z30

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

TABLE 6

VIN = 10 to 18 VDC

VOUT = 9 VDC

IOUT = 1, 3, 5 ADC

CONTINUOUS I MODE

F(SWITCHING) = 250kHz

Iout(min) = Iout(max)/10

IOUT	1A	3A	5A
D1	3A/40V 1N5822	6A/40V 6TQ045	12A/40V 12TQ045
L	39uH	12uH	6.9uH
PCH-	27-293	27-123	27-682
Cout	1uF	3uF	5uF

NOTE 1: Coilcraft inductor part number.
NOTE 2: Cout must be low ESR and ESI.
NOTE 3: MOSFET ratings and part number.
LOGIC LEVEL gate threshold.

OFF-LINE APPLICATIONS: FORWARD AND FLYBACK CONVERTERS

Several benefits can be realized in off-line applications by using the low current, UC380x BiCMOS PWM controllers. First, the IC can be powered from a resistor to the rectified input voltage source, eliminating the bootstrap winding. This applies to most low frequency applications (50kHz) where the DC supply current required for the gate drive is low. Soft start of the power supply and delayed restart following a fault requires no external parts. The internal leading edge blanking eliminates filtering of the current sense signal. Also, the ICs undervoltage lockout thresholds, internal Vcc shunt regulator and active low totem pole output eliminate any problematic gate drive operation.

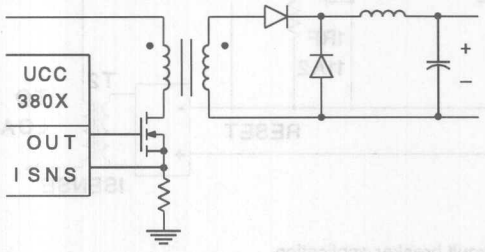


Figure 33. Forward Converter

The basic schematic of a forward converter is shown in figure 33, and a flyback is shown in figure 34. In each, the UCC3804 limits the maximum duty cycle to 50% by internal logic, allowing time for the main transformer to reset. Applications which utilize higher maximum duty cycles, for example 65%, should use the UCC 3802 device without the internal toggle flip flop.

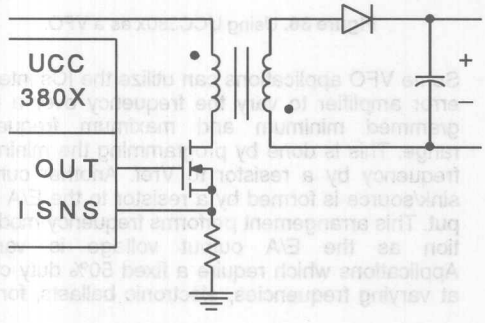


Figure 34. Flyback Converter

UCC380X OTHER APPLICATIONS: UNIVERSAL SYNC GENERATOR

The UCC3803 can be used as a synchronization (SYNC) pulse generator and driver for a variety of applications. Basically, one circuit shown uses the leading edge blanking duration as the SYNC output pulse width. The current limit input is biased at 1.25 volts to terminate the output pulse immediately after the ICs internal blanking pulse width.

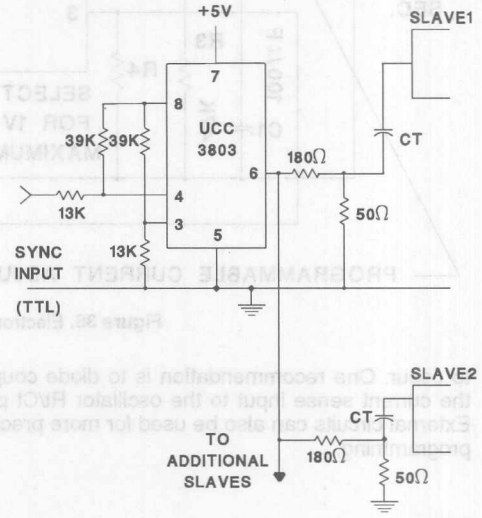


Figure 35. Synchronization Circuit

The oscillator is resistively programmed to a DC level of 1.25 volts also, midway between its upper and lower thresholds. When a TTL compatible SYNC pulse is injected, the amplitude at the oscillator input is raised above its upper threshold. This turns on the internal discharge circuitry which pulls the pin to about 0.2 volts, crossing the lower oscillator threshold. Once this occurs, the discharge transistor is turned off and the ICs output is turned on, generating the SYNC pulse. Note that the current sense input is biased to turn the ICs output off following the leading edge blanking duration, which is used to program the SYNC output pulse width. This 100 nanosecond duration is ideal for synchronizing most PWMs used today with the technique shown.

This circuit can be adapted to generate other width pulses with minor modifications. A capacitor can be added across the lower resistor in the divider network to the current sense input for extending the pulse width. Note that the voltage must be limited below 1.4 volts or a full cycle soft start will be incurred. Also, this capacitor must be discharged before the beginning of each pulse for proper timing

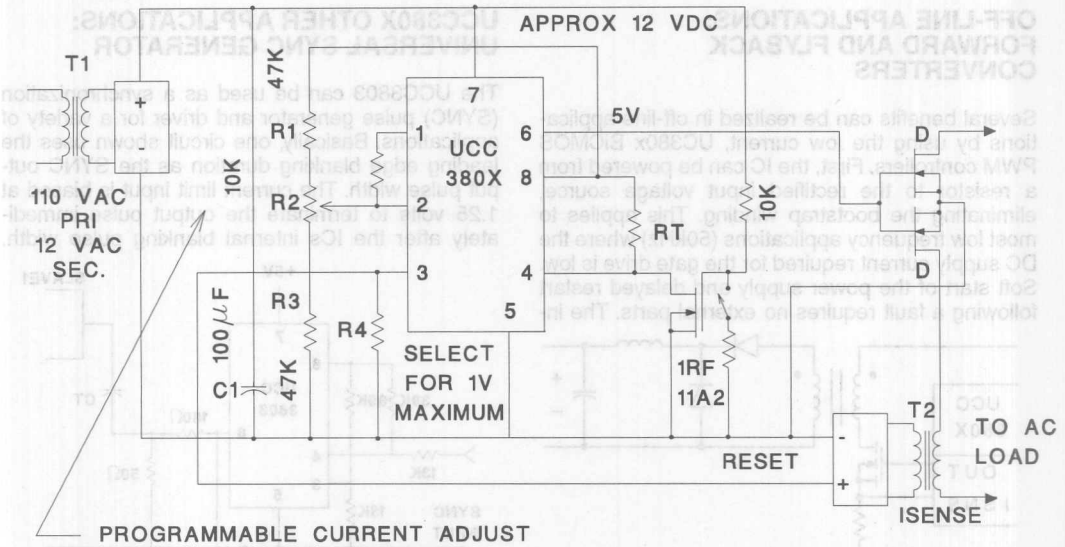


Figure 36. Electronic circuit breaker application.

to occur. One recommendation is to diode couple the current sense input to the oscillator Rt/Ct pin. External circuits can also be used for more precise programming.

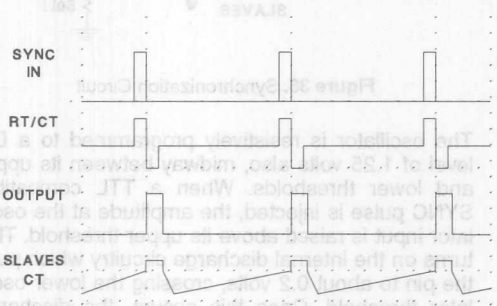


Figure 37. Synchronization Circuit Waveforms

VFO APPLICATIONS

Members of the UCC380x family of devices are adaptable for use in variable frequency applications. The most direct means of accomplishing this is to vary the charging current to the oscillator timing capacitor. Note that the minimum compliance voltage of the current source must exceed the upper oscillator threshold of approximately 2.7 volts. The VFO current source can be generated by an external op-amp for general purpose applications as shown.

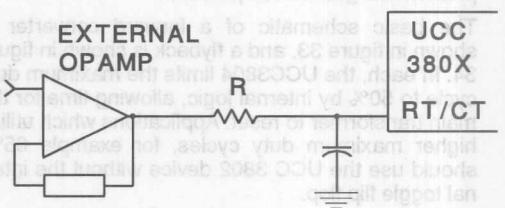


Figure 38. Using UCC380x as a VFO.

Some VFO applications can utilize the ICs internal error amplifier to vary the frequency over a programmed minimum and maximum frequency range. This is done by programming the minimum frequency by a resistor to Vref. Another current sink/source is formed by a resistor to the E/A output. This arrangement performs frequency modulation as the E/A output voltage is varied. Applications which require a fixed 50% duty cycle at varying frequencies, electronic ballasts, for ex-

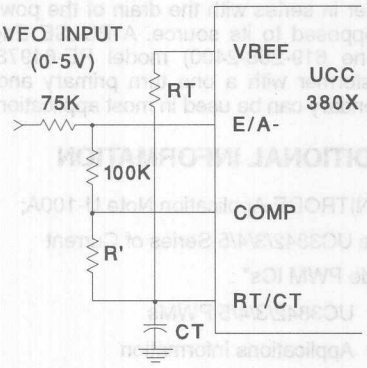


Figure 39: Using the error amplifier to make a simple VFO.

ample, should use the UCC3804 or UCC3805 devices. Output frequency from these will be one-half of the ICs oscillator due to the internal divide-by-two gating circuitry.

FIXED OFF-TIME APPLICATIONS

Obtaining a fixed off-time, variable on-time control technique is easily implemented with the UCC380x family. The oscillator Rt/Ct timing components are used to generate the off-time rather than the operating frequency. Implementation is shown in the corresponding figure 40.

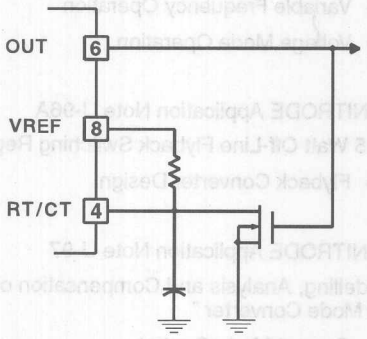


Figure 40: Fixed off-time control.

FULL DUTY CYCLE APPLICATIONS

Any of the UCC380x PWM controllers can be used at full (100%) duty cycle. This mode of operation may be required in certain applications, including DC switch drivers. Implementation requires "freezing" the oscillator so that the output stays high until it is time to turn off. Switch Q1 insures that the PWM output is high when switch Q2 is activated to stop the oscillator. Current limiting can still be accomplished by using the current sense feature of the IC, in addition to modulating the peak current via the error amplifier.

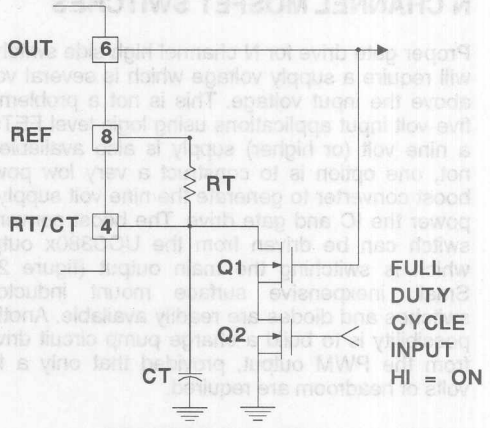


Figure 41. 100% Duty Cycle Circuit

HIGH SPEED, PROGRAMABLE ELECTRONIC CIRCUIT BREAKER

A high speed, programmable electronic circuit breaker can be built using the UCC380x family to perform the control and MOSFET drive functions. Basically, back-to-back power MOSFETS are used as the switching element although an SCR, TRIAC or bipolar switch can also be used. The MOSFETS are connected with the sources tied together to simplify the gate drive while providing a blocking path to current in either direction. Current limiting for an AC supply requires a current transformer, also shown, which can be simplified to a resistor for use in DC input applications. The current sense input to the IC can either be biased up for lower power loss in the current sense network, or programmed by adjusting the error amplifier output voltage to yield a similar result.

SWITCHING COMPONENT NOTES: P CHANNEL MOSFET SWITCHES

Logic level P channel MOSFETs are unavailable today which limits the use of P channel MOSFETs to those with input voltages greater than about ten volts for proper gate drive. The P channel switch will also require a small N channel device to invert its gate drive command, due to the active high output of the PWM (figure 30). High speed PNP transistors are also a suitable choice for some applications.

N CHANNEL MOSFET SWITCHES

Proper gate drive for N channel high side switches will require a supply voltage which is several volts above the input voltage. This is not a problem in five volt input applications using logic level FETs if a nine volt (or higher) supply is also available. If not, one option is to construct a very low power boost converter to generate the nine volt supply to power the IC and gate drive. The boost converter switch can be driven from the UCC380x output which is switching the main output (figure 29). Small, inexpensive surface mount inductors, switches and diodes are readily available. Another possibility is to build a charge pump circuit driven from the PWM output, provided that only a few volts of headroom are required.

GATE DRIVE TRANSFORMER

Higher input voltage applications using high-side switches will require a gate drive transformer due to 12 volt maximum supply rating of the UCC 380x IC family. A small ferrite toroid with two windings and minimal insulation is typically used. A capacitor is placed in series with the primary and is needed for proper reset of the core. The DC offset introduced by the capacitor will effect the primary to secondary turns ratio of the transformer which is dependant on the application. A PULSE Engineering (phone 619-268-2400) model PE-64973 can be employed in most Buck regulator designs.

CURRENT SENSE TRANSFORMER

A current sense transformer is required in the buck regulator application for current mode control. This transformer is used to level shift the current signal from the high side input supply to the ground referenced PWM circuitry. A high turns ratio should be incorporated to reduce power dissipation. Parasitic noise can be minimized by inserting the transformer in series with the drain of the power switch as opposed to its source. A PULSE Engineering (phone 619-268-2400) model PE-64978 current transformer with a one turn primary and 50 turn secondary can be used in most applications.

ADDITIONAL INFORMATION

1. UNITRODE Application Note U-100A;

" The UC3842/3/4/5 Series of Current Mode PWM ICs" :

- UC3842/3/4/5 PWMs
- Applications Information

2. UNITRODE Application Note U-111;

" Practical Considerations in Current Mode Power Supplies" ;

- Fixed OFF-Time Implementation
- Full Duty Cycle
- Paralleling Power Supplies
- Shutdown Techniques
- Slope Compensation (implementation)
- Soft Start
- Synchronization
- Variable Frequency Operation
- Voltage Mode Operation

3. UNITRODE Application Note U-96A

"A 25 Watt Off-Line Flyback Switching Regulator":

- Flyback Converter Design

4. UNITRODE Application Note U-97

"Modelling, Analysis and Compensation of the Current Mode Converter "

- Current Mode Control
- Slope Compensation

5. UNITRODE Design Note DN-42

"Design Considerations for Transitioning from UC3842 to the New UCC3802 Family"

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UNITRODE
APPLICATION NOTE

UC3854 Controlled Power Factor Correction Circuit Design

PHILIP C. TODD

ABSTRACT

This Application Note describes the concepts and design of a boost preregulator for power factor correction. This note covers the important specifications for power factor correction, the boost power circuit design and the UC3854 integrated circuit which controls the converter. A complete design procedure is given which includes the tradeoffs necessary in the process. This design procedure is directly applicable to the UC3854A/B as well as the UC3854. The recommendations in Unitrode Design Note DN-39 cover other areas of the circuit and, while not discussed here, must be considered in any design. This application note supersedes Application Note U-125 "Power Factor Correction With the UC3854."

INTRODUCTION

The objective of active power factor correction is to make the input to a power supply look like a simple resistor. An active power factor corrector does this by programming the input current in response to the input voltage. As long as the ratio between the voltage and current is a constant the input will be resistive and the power factor will be 1.0. When the ratio deviates from a constant the input will contain phase displacement, harmonic distortion or both and either one will degrade the power factor.

The most general definition of power factor is the ratio of real power to apparent power.

$$PF = \frac{P}{(Vrms \times Irms)} \quad \text{or} \quad PF = \frac{Watts}{V.A.}$$

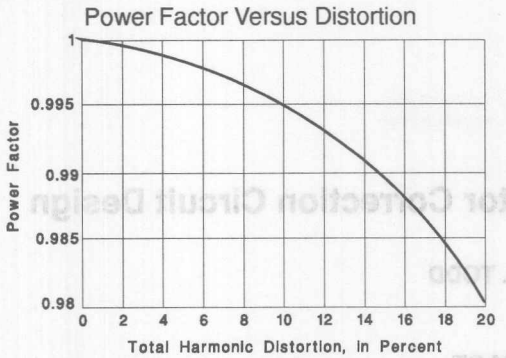
Where P is the real input power and Vrms and Irms are the root mean square (RMS) voltage and current of the load, or power factor corrector input in this case. If the load is a pure resistance the real power and the product of the RMS voltage and current will be the same and the power factor will be 1.0. If the load is not a pure resistance the power factor will be below 1.0.

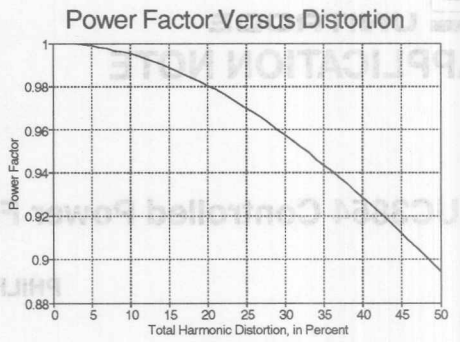
Phase displacement is a measure of the reactance of the input impedance of the active power factor corrector. Any amount of reactance, either inductive or capacitive will cause phase displacement of the input current waveform with respect to the input voltage waveform. The phase displacement of the voltage and current is the classic definition of power factor which is the cosine of the phase angle between the voltage and current sinusoids.

$$PF = \text{Cos}\ \theta$$

The amount of displacement between the voltage and current indicates the degree to which the load is reactive. If the reactance is a small part of the impedance the phase displacement will be small. An active power factor corrector will generate phase displacement of the input current if there is phase shift in the feedforward signals or in the control loops. Any filtering of the AC line current will also produce phase displacement.

Harmonic distortion is a measure of the non-linearity of the input impedance of the active power factor corrector. Any variation of the input impedance as a function of the input voltage will cause distortion of the input current and this distortion is the other contributor to poor power factor. Distortion increases the RMS value of the current without increasing the total power being drawn. A non-linear load will therefore have a poor power factor because the RMS value of the current is high but the total power delivered is small. If the non-linearity is small the harmonic distortion will be low. Distortion in an active power factor corrector comes from





Harmonic Order	Permissible current	Maximum permissible current
n	mA/W	A
Odd harmonics		
3	3.4	2.30
5	1.9	1.14
7	1.0	0.78
9	0.5	0.40
11	0.35	0.33
13	0.3	0.21
15 up	3.85/n	$0.15 \times \frac{15}{n}$
Even harmonics		
2	1.8	1.08
4	0.7	0.42
6	0.5	0.30
>8	$\frac{3}{n}$	$\frac{1.80}{n}$

Table 1

several sources: the feedforward signals, the feedback loops, the output capacitor, the inductor and the input rectifiers.

An active power factor corrector can easily achieve a high input power factor, usually much greater than 0.9. But power factor is not a sensitive measure of the distortion or the displacement of the current waveform. It is often more convenient to deal with these quantities directly rather than with the power factor. For example, 3% harmonic distortion alone has a power factor of 0.999. A current with 30% total harmonic distortion still has a power factor of 0.95. A current with a phase displacement of 25 degrees from the voltage has a power factor of 0.90.

The trend among the world standards organizations responsible for power quality is to specify maximum limits for the amount of current allowed at each of the harmonics of the line frequency. IEC 555-2 specifies each harmonic up through and beyond the 15th and the amount of current permissible at each. Table 1 lists the requirements for IEC 555-2 as of the time of this writing. There are two parts to the specification, a relative distortion and an absolute distortion maximum. Both limits apply to all equipment. This table is included here as an example of a line distortion specification. It is not intended to be used for design purposes. The IEC has not finalized the requirements of IEC 555 at this time and major changes are possible.

Active Power Factor Correction

A boost regulator is an excellent choice for the power stage of an active power factor corrector because the input current is continuous and this produces the lowest level of conducted noise and the best input current waveform. The disadvantage of the boost regulator is the high output voltage required. The output voltage must be greater than the highest expected peak input voltage.

The boost regulator input current must be forced or programmed to be proportional to the input voltage waveform for power factor correction. Feedback is necessary to control the input current and either

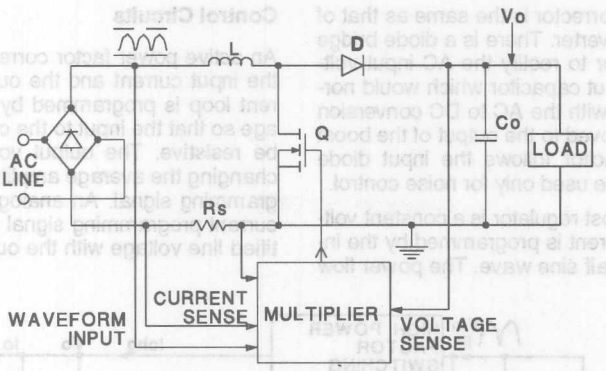


Figure 1

Basic Configuration of High Power Factor Control Circuit

peak current mode control or average current mode control may be used. Both techniques may be implemented with the UC3854. Peak current mode control has a low gain, wide bandwidth current loop which generally makes it unsuitable for a high performance power factor corrector since there is a significant error between the programming signal and the current. This will produce distortion and a poor power factor.

Average current mode control is based on a simple concept. An amplifier is used in the feedback loop around the boost power stage so that input current tracks the programming signal with very little error. This is the advantage of average current mode control and it is what makes active power factor correction possible. Average current mode control is relatively easy to implement and is the method described here.

A block diagram of a boost power factor corrector circuit is shown in Figure 1. The power circuit of a

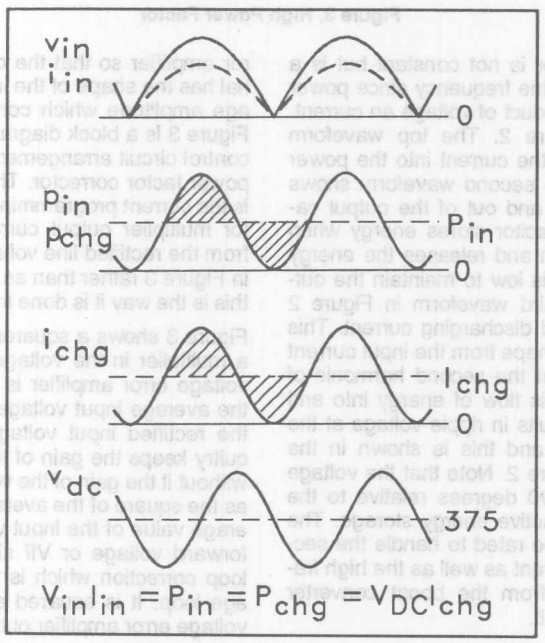


Figure 2. Preregulator Waveforms

boost power factor corrector is the same as that of a dc to dc boost converter. There is a diode bridge ahead of the inductor to rectify the AC input voltage but the large input capacitor which would normally be associated with the AC to DC conversion function has been moved to the output of the boost converter. If a capacitor follows the input diode bridge it is a small one used only for noise control.

The output of the boost regulator is a constant voltage but the input current is programmed by the input voltage to be a half sine wave. The power flow into the output capacitor is not constant but is a sine wave at twice the line frequency since power is the instantaneous product of voltage an current. This is shown in Figure 2. The top waveform shows the voltage and the current into the power factor corrector and the second waveform shows the flow of energy into and out of the output capacitor. The output capacitor stores energy when the input voltage is high and releases the energy when the input voltage is low to maintain the output power flow. The third waveform in Figure 2 shows the charging and discharging current. This current has a different shape from the input current and is almost entirely at the second harmonic of the AC line voltage. This flow of energy into and out of the capacitor results in ripple voltage at the second harmonic also and this is shown in the fourth waveform in Figure 2. Note that the voltage ripple is displaced by 90 degrees relative to the current since this is reactive energy storage. The output capacitor must be rated to handle the second harmonic ripple current as well as the high frequency ripple current from the boost converter switch which modulates it.

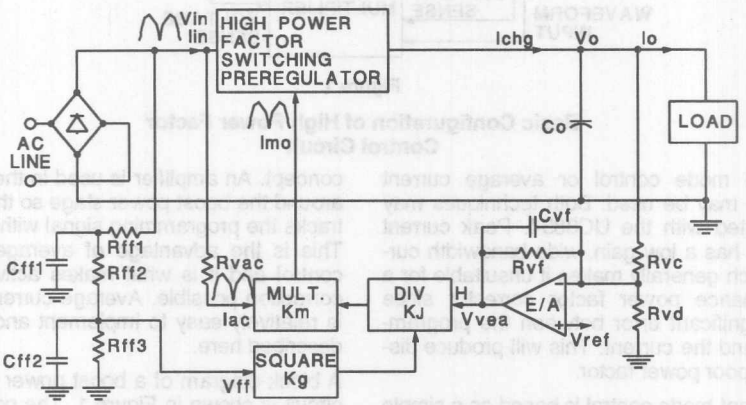


Figure 3. High Power Factor

Control Circuits

An active power factor corrector must control both the input current and the output voltage. The current loop is programmed by the rectified line voltage so that the input to the converter will appear to be resistive. The output voltage is controlled by changing the average amplitude of the current programming signal. An analog multiplier creates the current programming signal by multiplying the rectified line voltage with the output of the voltage error amplifier so that the current programming signal has the shape of the input voltage and an average amplitude which controls the output voltage. Figure 3 is a block diagram which shows the basic control circuit arrangement necessary for an active power factor corrector. The output of the multiplier is the current programming signal and is called Imo for multiplier output current. The multiplier input from the rectified line voltage is shown as a current in Figure 3 rather than as a voltage signal because this is the way it is done in the UC3854.

Figure 3 shows a squarer and a divider as well as a multiplier in the voltage loop. The output of the voltage error amplifier is divided by the square of the average input voltage before it is multiplied by the rectified input voltage signal. This extra circuitry keeps the gain of the voltage loop constant, without it the gain of the voltage loop would change as the square of the average input voltage. The average value of the input voltage is called the feedforward voltage or Vff since it provides an open loop correction which is fed forward into the voltage loop. It is squared and then divided into the voltage error amplifier output voltage (Vvea).

The current programming signal must match the rectified line voltage as closely as possible to maximize the power factor. If the voltage loop bandwidth were large it would modulate the input current to keep the output voltage constant and this would distort the input current horribly. Therefore the voltage loop bandwidth must be less than the input line frequency. But the output voltage transient response must be fast so the voltage loop bandwidth must be made as large as possible. The squarer and divider circuits keep the loop gain constant so the bandwidth can be as close as possible to the line frequency to minimize the transient response of the output voltage. This is especially important for wide input voltage ranges.

The circuits which keep the loop gain constant make the output of the voltage error amplifier a power control. The output of the voltage error amplifier actually controls the power delivered to the load. This can be seen easily from an example. If the output of the voltage error amplifier is constant and the input voltage is doubled the programming signal will double but it will be divided by the square of the feedforward voltage, or four times the input, which will result in the input current being reduced to half its original value. Twice the input voltage times half the input current results in the same input power as before. The output of the voltage error amplifier, then, controls the input power level of the power factor corrector. This can be used to limit the maximum power which the circuit can draw from the power line. If the output of the voltage error amplifier is clamped at some value that corresponds to some maximum power level, then the active power factor corrector will not draw more than that amount of power from the line as long as the input voltage is within its range.

Input Distortion Sources

The control circuits introduce both distortion and displacement into the input current waveform. These errors come from the input diode bridge, the multiplier circuits and ripple voltage, both on the output and on the feedforward voltage.

There are two modulation processes in an active power factor corrector. The first is the input diode bridge and the second is the multiplier, divider, squarer circuit. Each modulation process generates cross products, harmonics or sidebands between the two inputs. The description of these mathematically can be quite complex. Interestingly enough, however, the two modulators interact and one becomes a demodulator for the other so that the result is quite simple. As shown later, virtually all of the ripple voltages in an active power factor corrector are at the second harmonic of the line frequency. When these voltages go through the multiplier and get programmed into the input current and then go through the input diode bridge the second harmonic voltage amplitude results in two frequency components. One is at the third harmonic of the line frequency and the other is at the fundamental. Both of these components have an amplitude which is half of the amplitude of the original second harmonic voltage. They also have the same phase as the original second harmonic. If the ripple voltage is 10% of the line voltage amplitude and is phase shifted 90 degrees the input current will have a third harmonic which is 5% of the fundamental and is shifted 90 degrees and a fundamental component which is 5% of the line current and is displaced by 90 degrees.

The feedforward voltage comes from the rectified AC line which has a second harmonic component that is 66% of the amplitude of the average value. The filter capacitors of the feedforward voltage divider greatly attenuate the second harmonic and effectively remove all of the higher harmonics but some of the second harmonic is still present at the feedforward input. This ripple voltage is squared by the control circuits as shown in Figure 3. This doubles the amplitude of the ripple since it is riding on top of a large DC value. The divider process is transparent to the ripple voltage so it passes on to the multiplier and eventually becomes third harmonic distortion of the input current and a phase displacement. The doubling action of the squarer means that the amplitude of the input current distortion in percent is the same as the amplitude of the ripple voltage, in percent, at the feedforward input.

Needless to say, the feedforward ripple voltage must be kept small to achieve a low distortion input current. The ripple voltage could be made small with a single pole filter with a very low cutoff frequency. However, fast response to changes of the input voltage is also desirable so the response time of the filter must be fast. These two requirements are, of course, in conflict and a compromise must be found. A two pole filter on the feedforward input has a faster transient response than a single pole filter for the same amount of ripple attenuation. Another advantage of the two pole filter has is that the phase shift is twice that of the single pole filter. This results in 180 degrees of phase shift of the second harmonic and brings both the resulting third harmonic and the displacement component of the input current back in phase with the voltage. A second harmonic ripple voltage of 3% at the feedforward input results in a 0.97 power factor just from the displacement component if a single pole filter is used for the feedforward voltage. With a two pole filter there is no displacement component to the power factor because it is in

phase with the input current. The third harmonic component of the input current resulting from the second harmonic at the feedforward input will have the same amplitude as the second harmonic ripple voltage. If 3% second harmonic is present on the feedforward voltage the line current waveform will contain 3% third harmonic distortion.

The output voltage has ripple at the second harmonic due to the ripple current flowing through the output capacitor. This ripple voltage is fed back through the voltage error amplifier to the multiplier and, like the feedforward voltage, programs the input current and results in second harmonic distortion of the input current. Since this ripple voltage does not go through the squarer the amplitude of the distortion and displacement are each half of the amplitude of the ripple voltage. The ripple voltage at the output of the voltage error amplifier must be in phase with the line voltage for the displacement component to be in phase. The voltage error amplifier must shift the second harmonic by 90 degrees so that it will be in phase with the line voltage.

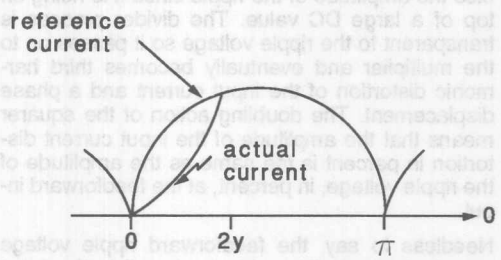


Figure 4. Cusp Distortion

The voltage loop of a boost converter with average current mode control has a control to output transfer function which has a single pole roll off characteristic so it could be compensated with a flat gain error amplifier. This produces a very stable loop with 90 degrees of phase margin. However, it provides less than optimum performance. The ripple voltage on the output capacitor is out of phase with the input current by 90 degrees. If the error amplifier has flat gain at the second harmonic frequency the distortion and displacement generated in the input current will be 90 degrees out of phase with the rectified AC line. The power factor can be improved by introducing phase shift into the voltage error amplifier response. This shifts the displacement component of the power factor back into alignment with the input voltage and increases the power factor. The amount of phase shift which can be added is determined by the need to keep the voltage loop stable. If the phase margin is reduced to 45 degrees the phase at the second harmonic will be very close to 90 degrees and this brings the displacement component back in phase with the input voltage.

The bandwidth of the voltage control loop is determined by the amount of input distortion to be contributed by the output ripple voltage. If the output capacitor is small and the distortion must be low then the bandwidth of the loop will be low so that the ripple voltage will be sufficiently attenuated by the error amplifier. Transient response is a function of the loop bandwidth and the lower the bandwidth the slower the transient response and the greater the overshoot. The output capacitor may need to be large to have both fast output transient response and low input current distortion.

The technique used to design the loop compensation is to find the amount of attenuation of the output ripple voltage required in the error amplifier and then work back into the unity gain frequency. The loop will have the maximum bandwidth when the phase margin is the smallest. A 45 degree phase margin is a good compromise which will give good loop stability and fast transient response and which is easy to design. The voltage error amplifier response which results will have flat gain up to the loop unity gain frequency and will have a single pole roll off above that frequency. This gives the maximum amount of attenuation at the second harmonic of the line frequency from a simple circuit, gives the greatest bandwidth and provides a 45 degree phase margin.

Cusp Distortion

Cusp distortion occurs just after the AC line input has crossed zero volts. At this point the amount of current which is required by the programming signal exceeds the available current slew rate. When the input voltage is near zero there is very little voltage across the inductor when the switch is closed so the current cannot ramp up very quickly so the available slew rate is too low and the input current will lag behind the desired value for a short period of time. Once the input current matches the programmed value the control loop is back in operation and the input current will follow the programming signal. The length of time that the current does not track the programmed value is a function of the inductor value. The smaller the inductor value the better the tracking and the lower the distortion but the smaller inductor value will have higher ripple current. The amount of distortion generated by this condition is generally small and is mostly higher order harmonics. This problem is minimized by a sufficiently high switching frequency.

UC3854 Block Diagram

A block diagram of the UC3854 is shown in Figure 5 and is the same as the one in the device data sheet. This integrated circuit contains the circuits necessary to control a power factor corrector. The UC3854 is designed to implement average current mode control but is flexible enough to be used for a wide variety of power topologies and control methods.

The top left corner of Figure 5 contains the under voltage lock out comparator and the enable comparator. The output of both of these comparators must be true to allow the device to operate. The inverting input to the voltage error amplifier is connected to pin 11 and is called Vsens. The diodes shown around the voltage error amplifier are intended to represent the functioning of the internal circuits rather than to show the actual devices. The diodes shown in the block diagram are ideal diodes and indicate that the non-inverting input to the error amplifier is connected to the 7.5Vdc reference voltage under normal operation but is also used for the slow start function. This configuration lets the voltage control loop begin operation before the output voltage has reached its operating point and eliminates the turn-on overshoot which plagues many power supplies. The diode shown between pin 11 and the inverting input of the error amplifier is also an ideal diode and is shown to eliminate confusion about whether there might be an extra diode drop added to the reference or not. In the actual device we do it with differential amplifiers. An internal current source is also provided for charging the slow start timing capacitor.

The output of the voltage error amplifier, Vvea, is available on pin 7 of the UC3854 and it is also an input to the multiplier. The other input to the multiplier is pin 6, Iac, and this is the input for the programming wave shape from the input rectifiers. This pin is held at 6.0 volts and is a current input. The feedforward input, Vff, is pin 8 and its value is squared before being fed into the divider input of the multiplier. The Iset current from pin 12 is also used in the multiplier to limit the maximum output current. The output current of the multiplier is Imo and it flows out of pin 5 which is also connected to the non-inverting input of the current error amplifier.

The inverting input of the current amplifier is connected to pin 4, the Isens pin. The output of the current error amplifier connects to the pulse width modulation (PWM) comparator where it is compared to the oscillator ramp on pin 14. The oscillator and the comparator drive the set-reset flip-flop which, in turn, drives the high current output on pin 16. The output voltage is clamped internally to the UC3854 at 15 volts so that power MOSFETs will not have their gates over driven. An emergency peak current limit is provided on pin 2 and it will shut the output pulse off when it is pulled slightly below ground. The reference voltage output is connected to pin 9 and the input voltage is connected to pin 15.

DESIGN PROCESS

Power Stage Design

This analysis of the power stage design makes use of a 250W boost converter as an example. The control circuit for a boost power factor corrector does not change much with the power level of the converter. A 5000 watt power factor corrector will have almost the same control circuits as a 50 watt

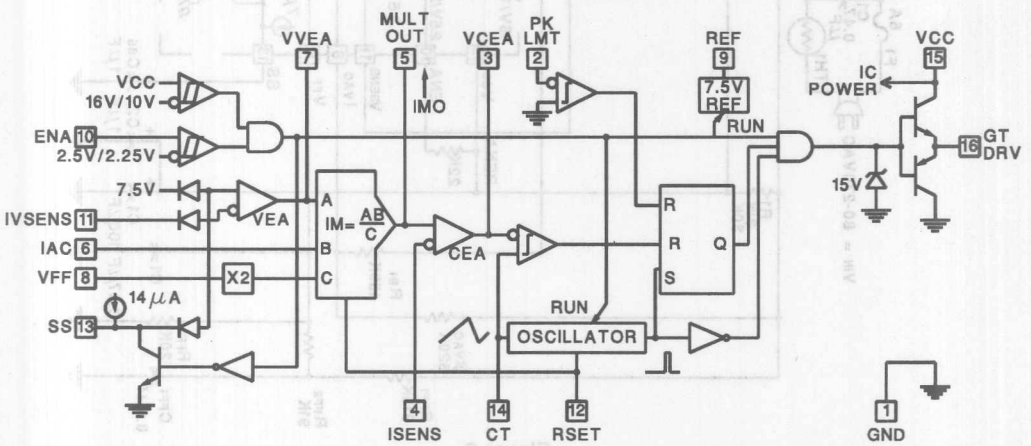


Figure 5. UC3854 Block Diagram

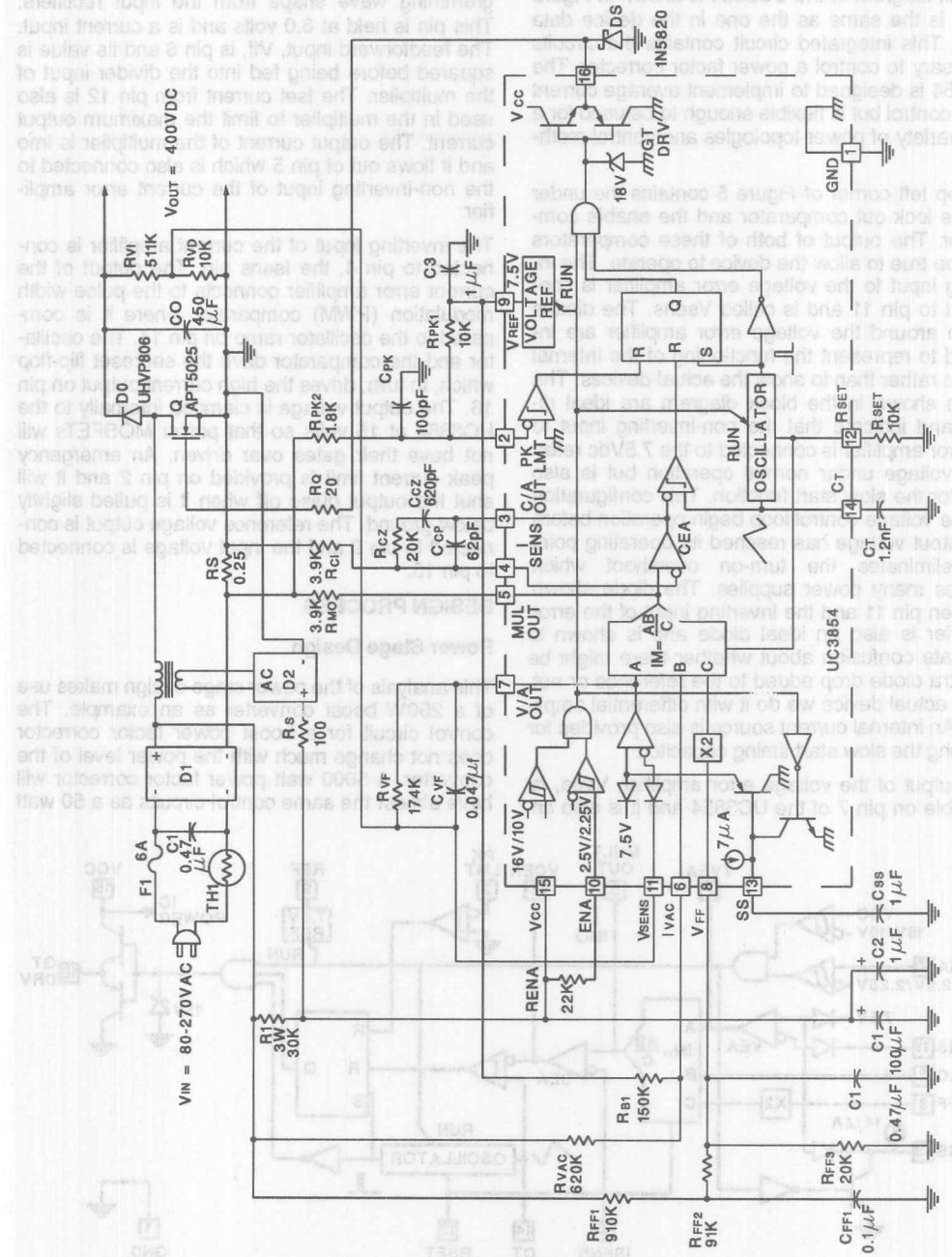


Figure 6.
Complete Schematic of 250W Power Factor Preregulator

corrector. The power stage will be different but the design process will remain the same for all power factor corrector circuits. Since the design process is the same and the power stage is scalable a 250 watt corrector serves well as an example and it can be readily scaled to higher or lower output levels. Figure 6 is the schematic diagram of the circuit. Please refer to this schematic in the discussion of the design process which follows.

Specifications

The design process starts with the specifications for the converter performance. The minimum and maximum line voltage, the maximum output power, and the input line frequency range must be specified. For the example circuit the specifications are:

Maximum power output: 250W

Input voltage range: 80-270Vac

Line frequency range: 47-65Hz

This defines a power supply which will operate almost anywhere in the world. The output voltage of a boost regulator must be greater than the peak of the maximum input voltage and a value 5% to 10% higher than the maximum input voltage is recommended so the output voltage is chosen to be 400Vdc.

Switching Frequency

The choice of switching frequency is generally somewhat arbitrary. The switching frequency must be high enough to make the power circuits small and minimize the distortion and must be low enough to keep the efficiency high. In most applications a switching frequency in the range of 20KHz to 300KHz proves to be an acceptable compromise. The example converter uses a switching frequency of 100KHz as a compromise between size and efficiency. The value of the inductor will be reasonably small and cusp distortion will be minimized, the inductor will be physically small and the loss due to the output diode will not be excessive. Converters operating at higher power levels may find that a lower switching frequency is desirable to minimize the power losses. Turn-on snubbers for the switch will reduce the switching losses and can be very effective in allowing a converter to operate at high switching frequency with very high efficiency.

Inductor Selection

The inductor determines the amount of high frequency ripple current in the input and its value is chosen to give some specific value of ripple current. Inductor value selection begins with the peak

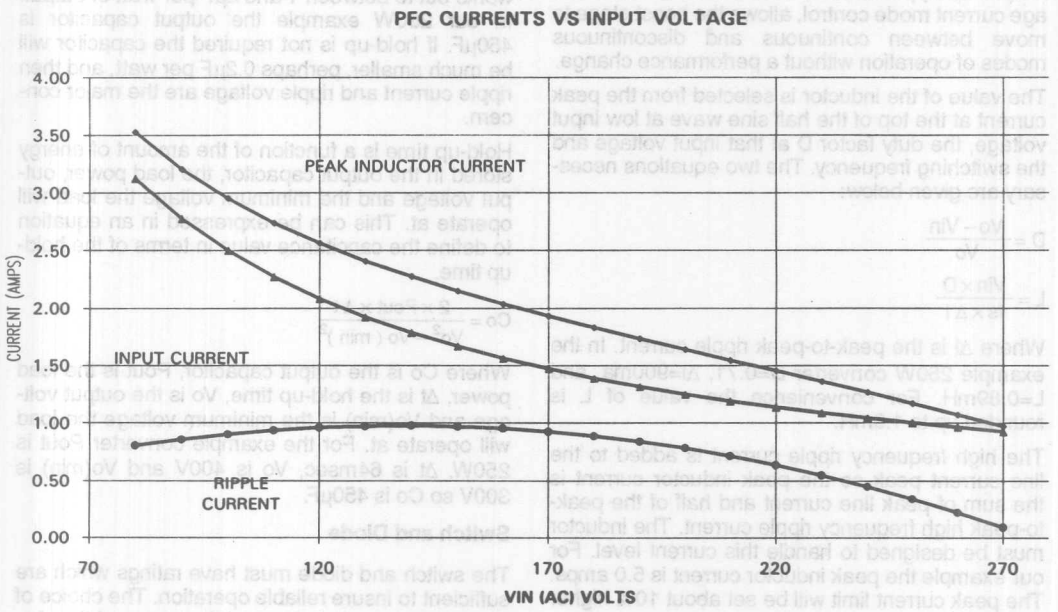


Figure 7

current of the input sinusoid. The maximum peak current occurs at the peak of the minimum line voltage and is given by:

$$I\,line\,(pk) = \frac{\sqrt{2} \times P}{Vin\,(min)}$$

For the example converter the maximum peak line current is 4.42 amps at a Vin of 80Vac.

The maximum ripple current in a boost converter occurs when the duty factor is 50% which is also when the boost ratio M=Vo/Vin=2. The peak value of inductor current generally does not occur at this point since the peak value is determined by the peak value of the programmed sinusoid. The peak value of inductor ripple current is important for calculating the required attenuation of the input filter. Figure 7 is a graph of the peak to peak ripple current in the inductor versus input voltage for the example converter.

The peak-to-peak ripple current in the inductor is normally chosen to be about 20% of the maximum peak line current. This is a somewhat arbitrary decision since this is usually not the maximum value of the high frequency ripple current. A larger value of ripple current will put the converter into the discontinuous conduction mode for a larger portion of the rectified line current cycle and means that the input filter must be larger to attenuate more high frequency ripple current. The UC3854, with average current mode control, allows the boost stage to move between continuous and discontinuous modes of operation without a performance change.

The value of the inductor is selected from the peak current at the top of the half sine wave at low input voltage, the duty factor D at that input voltage and the switching frequency. The two equations necessary are given below:

$$D = \frac{Vo - Vin}{Vo}$$

$$L = \frac{Vin \times D}{fs \times \Delta I}$$

Where ΔI is the peak-to-peak ripple current. In the example 250W converter D=0.71, ΔI=900ma, and L=0.89mH. For convenience the value of L is rounded up to 1.0mH.

The high frequency ripple current is added to the line current peak so the peak inductor current is the sum of peak line current and half of the peak-to-peak high frequency ripple current. The inductor must be designed to handle this current level. For our example the peak inductor current is 5.0 amps. The peak current limit will be set about 10% higher at 5.5 amps.

Output Capacitor

The factors involved in the selection of the output capacitor are the switching frequency ripple current, the second harmonic ripple current, the DC output voltage, the output ripple voltage and the hold-up time. The total current through the output capacitor is the RMS value of the switching frequency ripple current and the second harmonic of the line current. The large electrolytic capacitors which are normally chosen for the output capacitor have an equivalent series resistance which changes with frequency and is generally high at low frequencies. The amount of current which the capacitor can handle is generally determined by the temperature rise. It is usually not necessary to calculate an exact value for the temperature rise. It is usually adequate to calculate the temperature rise due to the high frequency ripple current and the low frequency ripple current and add them together. The capacitor data sheet will provide the necessary ESR and temperature rise information.

The hold-up time of the output often dominates any other consideration in output capacitor selection. Hold-up is the length of time that the output voltage remains within a specified range after input power has been turned off. Hold-up times of 15 to 50 milliseconds are typical. In off-line power supplies with a 400Vdc output the hold-up requirement generally works out to between 1 and 2µF per watt of output. In our 250W example the output capacitor is 450µF. If hold-up is not required the capacitor will be much smaller, perhaps 0.2µF per watt, and then ripple current and ripple voltage are the major concern.

Hold-up time is a function of the amount of energy stored in the output capacitor, the load power, output voltage and the minimum voltage the load will operate at. This can be expressed in an equation to define the capcitance value in terms of the hold-up time.

$$Co = \frac{2 \times Pout \times \Delta t}{Vo^2 - Vo\,(min)^2}$$

Where Co is the output capacitor, Pout is the load power, Δt is the hold-up time, Vo is the output voltage and Vo(min) is the minimum voltage the load will operate at. For the example converter Pout is 250W, Δt is 64msec, Vo is 400V and Vo(min) is 300V so Co is 450µF.

Switch and Diode

The switch and diode must have ratings which are sufficient to insure reliable operation. The choice of these components is beyond the scope of this Application Note. The switch must have a current rating at least equal to the maximum peak current in

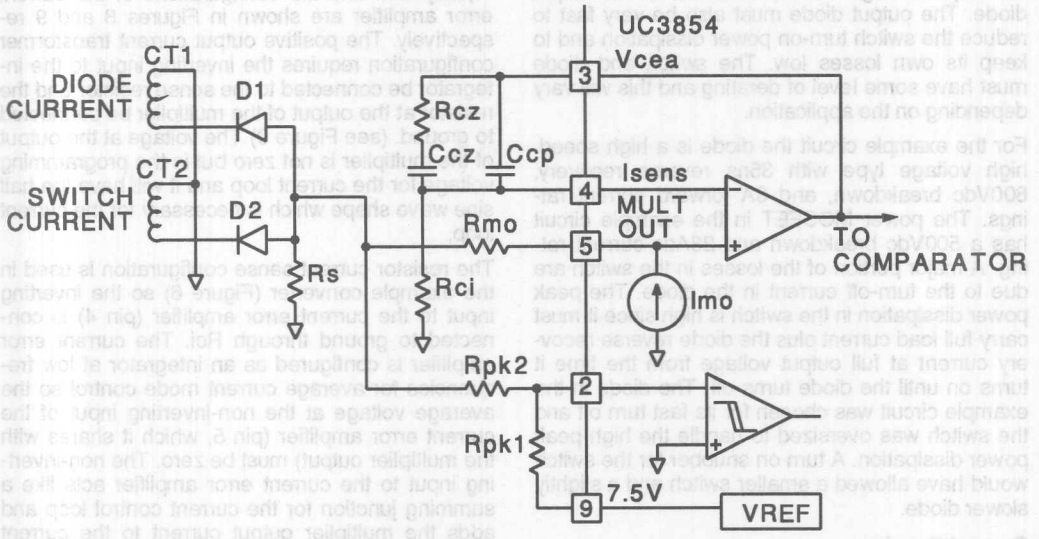


Figure 8.
Current Transformers Used with Negative Output

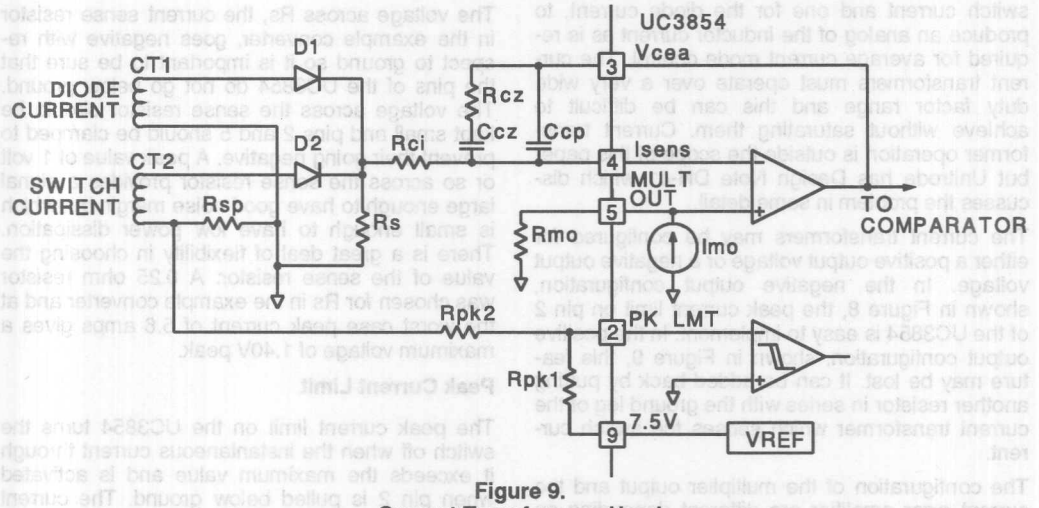


Figure 9.
Current Transformers Used with Positive Output

the inductor and a voltage rating at least equal to the output voltage. The same is true for the output diode. The output diode must also be very fast to reduce the switch turn-on power dissipation and to keep its own losses low. The switch and diode must have some level of derating and this will vary depending on the application.

For the example circuit the diode is a high speed, high voltage type with 35ns reverse recovery, 600Vdc breakdown, and 8A forward current ratings. The power MOSFET in the example circuit has a 500Vdc breakdown and 23Adc current rating. A major portion of the losses in the switch are due to the turn-off current in the diode. The peak power dissipation in the switch is high since it must carry full load current plus the diode reverse recovery current at full output voltage from the time it turns on until the diode turns off. The diode in the example circuit was chosen for its fast turn off and the switch was oversized to handle the high peak power dissipation. A turn on snubber for the switch would have allowed a smaller switch and a slightly slower diode.

Current Sensing

There are two general methods for current sensing, a sense resistor in the ground return of the converter or two current transformers. The sense resistor is the least expensive method and is most appropriate at low power or current levels. The power dissipation in the resistor may become quite large at higher current levels and in that case the current transformers are more appropriate. Two current transformers are required, one for the switch current and one for the diode current, to produce an analog of the inductor current as is required for average current mode control. The current transformers must operate over a very wide duty factor range and this can be difficult to achieve without saturating them. Current transformer operation is outside the scope of this paper but Unitrode has Design Note DN-41 which discusses the problem in some detail.

The current transformers may be configured for either a positive output voltage or a negative output voltage. In the negative output configuration, shown in Figure 8, the peak current limit on pin 2 of the UC3854 is easy to implement. In the positive output configuration, shown in Figure 9, this feature may be lost. It can be added back by putting another resistor in series with the ground leg of the current transformer which senses the switch current.

The configuration of the multiplier output and the current error amplifier are different depending on whether a resistor is used for current sensing or whether current transformers with positive output voltages are used for current sensing. Both work equally well and the configurations of the current error amplifier are shown in Figures 8 and 9 respectively. The positive output current transformer configuration requires the inverting input to the integrator be connected to the sense resistor and the resistor at the output of the multiplier be connected to ground. (see Figure 9) The voltage at the output of the multiplier is not zero but is the programming voltage for the current loop and it will have the half sine wave shape which is necessary for the current loop.

The resistor current sense configuration is used in the example converter (Figure 6) so the inverting input to the current error amplifier (pin 4) is connected to ground through Rci. The current error amplifier is configured as an integrator at low frequencies for average current mode control so the average voltage at the non-inverting input of the current error amplifier (pin 5, which it shares with the multiplier output) must be zero. The non-inverting input to the current error amplifier acts like a summing junction for the current control loop and adds the multiplier output current to the current from the sense resistor (which flows through the programming resistor Rmo). The difference controls the boost regulator. The voltage at the inverting input of the current error amplifier (pin 4) will be small at low frequencies because the gain at low frequencies is large. The gain at high frequencies is small so relatively large voltages at the switching frequency may be present. But, the average voltage on pin 4 must be zero because it is connected through Rci to ground.

The voltage across Rs, the current sense resistor in the example converter, goes negative with respect to ground so it is important to be sure that the pins of the UC3854 do not go below ground. The voltage across the sense resistor should be kept small and pins 2 and 5 should be clamped to prevent their going negative. A peak value of 1 volt or so across the sense resistor provides a signal large enough to have good noise margin but which is small enough to have low power dissipation. There is a great deal of flexibility in choosing the value of the sense resistor. A 0.25 ohm resistor was chosen for Rs in the example converter and at the worst case peak current of 5.6 amps gives a maximum voltage of 1.40V peak.

Peak Current Limit

The peak current limit on the UC3854 turns the switch off when the instantaneous current through it exceeds the maximum value and is activated when pin 2 is pulled below ground. The current limit value is set by a simple voltage divider from the reference voltage to the current sense resistor.

The equation for the voltage divider is given below:

$$Rpk2 = \frac{Vrs \times Rpk1}{Vref}$$

Where Rpk1 and Rpk2 are the resistors of the voltage divider, Vref is 7.5 volts on the UC3854, and Vrs is the voltage across the sense resistor Rs at the current limit point. The current through Rpk2 should be around 1mA. The peak current limit in the example circuit is set at 5.4 amps with an Rpk1 of 10K and Rpk2 of 1.8K. A small capacitor, Cpk, has been added to give extra noise immunity when operating at low line and this also increases the current limit slightly.

Multiplier Set-up

The multiplier/divider is the heart of the power factor corrector. The output of the multiplier programs the current loop to control the input current to give a high power factor. The output of the multiplier is therefore a signal which represents the input line current.

Unlike most design tasks where the design begins at the output and proceeds to the input the design of the multiplier circuits must begin with the inputs. There are three inputs to the multiplier circuits: the programming current Iac (pin 6), the feedforward voltage Vff from the input (pin 8), and the voltage error amplifier output voltage Vvea (pin 7). The multiplier output current is Imo (pin 5) and it is related to the three inputs by the following equation:

$$Imo = \frac{Km \times Iac \times (Vvea - 1)}{Vff^2}$$

Where Km is a constant in the multiplier and is equal to 1.0, Iac is the programming current from the rectified input voltage, Vvea is the output of the voltage error amplifier and Vff is the feedforward voltage.

Feedforward Voltage

Vff is the input to the squaring circuit and the UC3854 squaring circuit generally operates with a Vff range of 1.4 to 4.5 volts. The UC3854 has an internal clamp which limits the effective value of Vff to 4.5 volts even if the input goes above that value. The voltage divider for the Vff input has three resistors (Rff1, Rff2 and Rff3 - see Figure 6) and two capacitors (Cff1 and Cff2) and so it filters as well as providing two outputs. The resistors and capacitors of the divider form a second order low pass filter so the DC output is proportional to the average value of the input half sine wave. The average value is 90% of the RMS value of a half sine wave. If the RMS value of the AC input voltage is 270Vac the average value of a half sine will be 243Vdc and the peak will be 382V.

The Vff voltage divider has two DC conditions to meet. At high input line voltage Vff should not be greater than 4.5 volts. At this voltage the Vff input clamps so the feedforward function is lost. The voltage divider should be set up so that Vff is equal to 1.414 volts when Vin is at its low line value and the upper node of the voltage divider, Vffc, should be about 7.5 volts. This allows Vff to be clamped as described in Unitrode Design Note DN-39B. There is an internal current limit which holds the multiplier output constant if the Vff input goes below 1.414 volts. The Vff input should always be set up so that Vff is equal to 1.414 volts at the minimum input voltage. This may cause Vff to clip on the high end of the input voltage range if there is an extremely wide AC line voltage input range. However, it is preferable to have Vff clip at the high end rather than to have the multiplier output clip on the low end of the range. If Vff clips the voltage loop gain will change but the effect on the overall system will be small whereas the multiplier clipping will cause large amounts of distortion in the input current waveform.

The example circuit uses the UC3854 so the maximum value of Vff is 4.5 volts. If Rff1, the top resistor of the divider, is 910K and Rff2, the middle resistor, is 91K and Rff3, the bottom resistor, is 20K the maximum value of Vff will be 4.76 volts when the input voltage is 270Vac RMS and the DC average value will be 243 volts. When the input voltage is 80Vac RMS the average value is 72 volts and Vff is 1.41Vdc. Also at Vin=80Vac the voltage at the upper node on the voltage divider, Vffc, will be 7.83 volts. Note that the high end of the range goes above 4.5 volts so that the low end of the range will not go below 1.41 volts.

The output of the voltage error amplifier is the next piece of the multiplier setup. The output of the voltage error amplifier, Vvea, is clamped inside the UC3854 at 5.6 volts. The output of the voltage error amplifier corresponds to the input power of the converter. The feedforward voltage causes the power input to remain constant at given Vvea voltage regardless of line voltage changes. If 5.0V is established as the maximum normal operating level then 5.6V gives an overload power limit which is 12% higher.

The clamp on the output of the voltage error amplifier is what sets the minimum value of Vff at 1.414 volts. This can be seen by plugging these values into the equation for the multiplier output current given above. When Vff is large the inherent errors of the multiplier are magnified because Vvea/Vff becomes small. If the application has a wide input voltage range and if a very low harmonic distortion

is required then Vff may be changed to the range of 0.7 to 3.5 volts. To do this an external clamp MUST be added to the voltage error amplifier to hold its output below 2.00 volts. In general, however, this is not a recommended practice.

Multiplier Input Current

The operating current for the multiplier comes from the input voltage through Rvac. The multiplier has the best linearity at relatively high currents, but the recommended maximum current is 0.6mA. At high line the peak voltage for the example circuit is 382Vdc and the voltage on pin 6 of the UC3854 is 6.0Vdc. A 620K value for Rvac will give an Iac of 0.6mA maximum. For proper operation near the cusp of the input waveform when Vin=0 a bias current is needed because pin 6 is at 6.0Vdc. A resistor, Rb1, is connected from Vref to pin 6 to provide the small amount of bias current needed. Rb1 is equal to Rvac/4. In the example circuit a value of 150K for Rb1 will provide the correct bias.

The maximum output of the multiplier occurs at the peak of the input sine wave at low line. The maximum output current from the multiplier can be calculated from the equation for Imo, given above, for this condition. The peak value of Iac will be 182 microamps when Vin is at low line. Vvea will be 5.0 volts and Vff will be 2.0. Imo will then be 365 microamps maximum. Imo may not be greater than twice Iac so this represents the maximum current available at this input voltage and the peak input current to the power factor corrector will be limited accordingly.

The Iset current places another limitation on the multiplier output current. Imo may not be larger than 3.75 / Rset. For the example circuit this gives Rset = 10.27K maximum so a value of 10K is chosen.

The current out of the multiplier, Imo, must be summed with a current proportional to the inductor current to close the voltage feedback loop. Rmo, a resistor from the output of the multiplier to the current sense resistor, performs the function and the multiplier output pin becomes the summing junction. The average voltage on pin 5 will be zero under normal operation but there will be switching frequency ripple voltage which is amplitude modulated at twice the line frequency. The peak current in the boost inductor is to be limited to 5.6 amps in the example circuit and the current sense resistor is 0.25 ohms so the peak voltage across the sense resistor is 1.4 volts. The maximum multiplier output current is 365 microamps so the summing resistor, Rmo, must be 3.84K and a 3.9K resistor is chosen.

Oscillator Frequency

The oscillator charging current is Iset and is determined by the value of Rset and the oscillator frequency is set by the timing capacitor and the charging current. The timing capacitor is determined from:

$$Ct = \frac{1.25}{Rset \times fs}$$

Where Ct is the value of the timing capacitor and fs is the switching frequency in Hertz. For the example converter fs is 100KHz and Rset is 10K so Ct is 0.00125µF.

Current Error Amplifier Compensation

The current loop must be compensated for stable operation. The boost converter control to input current transfer function has a single pole response at high frequencies which is due to the impedance of the boost inductor and the sense resistor (Rs) forming a low pass filter. The equation for the control to input current transfer function is:

$$\frac{Vrs}{Vcea} = \frac{Vout \times Rs}{Vs \times sL}$$

Where Vrs is the voltage across the input current sense resistor and Vcea is the output of the current error amplifier. Vout is the DC output voltage, Vs is the peak-to-peak amplitude of the oscillator ramp, sL is the impedance of the boost inductor (also jwL), and Rs is the sense resistor (with a current transformer it will be Rs/N). This equation is only valid for the region of interest between the resonant frequency of the filter (LCo) and the switching frequency. Below resonance the output capacitor dominates and the equation is different.

The compensation of the current error amplifier provides flat gain near the switching frequency and uses the natural roll off of the boost power stage to give the correct compensation for the total loop. A zero at low frequency in the amplifier response gives the high gain which makes average current mode control work. The gain of the error amplifier near the switching frequency is determined by matching the down slope of the inductor current when the switch is off with the slope of the ramp generated by the oscillator. These two signals are the inputs of the PWM comparator in the UC3854.

The downslope of the inductor current has the units of amps per second and has a maximum value when the input voltage is zero. In other words, when the voltage differential between the input and output of the boost converter is greatest. At this point (Vin=0) the inductor current is given by the ratio of the converter output voltage and the inductance (Vo/L). This current flows through the current sense resistor Rs and produces a voltage

with the slope VoRs/L (with current sense transformers it will be VoRs/NL). This slope, multiplied by the gain of the current error amplifier at the switching frequency, must be equal to the slope of the oscillator ramp (also in volts per second) for proper compensation of the current loop. If the gain is too high the slope of the inductor current will be greater than the ramp and the loop can go unstable. The instability will occur near the cusp of the input waveform and will disappear as the input voltage increases.

The loop crossover frequency can be found from the above equation if the gain of the current error amplifier is multiplied with it and it is set equal to one. Then rearrange the equation and solve for the crossover frequency. The equation becomes:

$$fci = \frac{Vout \times Rs \times Rcz}{Vs \times 2\pi L \times Rci}$$

Where fci is the current loop crossover frequency and Rcz/Rci is the gain of the current error amplifier. This procedure will give the best possible response for the current loop.

In the example converter the output voltage is 400Vdc and the inductor is 1.0mH so the down slope of inductor current is 400mA per microsecond. The current sense resistor is 0.25 ohms so the input to the current error amplifier is 100mV per microsecond. The oscillator ramp of the UC3854 has a peak to peak value of 5.2V and the switching frequency is 100KHz so the ramp has a slope of 0.52 volts per microsecond. The current error amplifier must have a gain of 5.2 at the switching frequency to make the slopes equal. With an input resistor (Rci) value of 3.9K the feedback resistance (Rcz) is 20K to give the amplifier a gain of 5.2. The current loop crossover frequency is 15.9KHz.

The placement of the zero in the current error amplifier response must be at or below the crossover frequency. If it is at the crossover frequency the phase margin will be 45 degrees. If the zero is lower in frequency the phase margin will be greater. A 45 degree phase margin is very stable, has low overshoot and has good tolerance for component variations. The zero must be placed at the crossover frequency so the impedance of the capacitor at that frequency must be equal to the value of Rcz. The equation is: $Ccz = 1 / (2\pi \times fci \times Rcz)$. The example converter has Rcz=20K and fci=15.9KHz so Ccz=500pF. A value of 620pF was chosen to give a little more phase margin.

A pole is normally added to the current error amplifier response near the switching frequency to reduce noise sensitivity. If the pole is above half the switching frequency the pole will not affect the frequency response of the control loop. The example converter uses a 62pF capacitor for Ccp which gives a pole at 128KHz. This is actually above the switching frequency so a larger value of capacitor could have been used but 62pF is adequate in this case.

Voltage Error Amplifier Compensation

The voltage control loop must be compensated for stability but because the bandwidth of the voltage loop is so small compared to the switching frequency the requirements for the voltage control loop are really driven by the need to keep the input distortion to a minimum rather than by stability. The loop bandwidth must be low enough to attenuate the second harmonic of the line frequency on the output capacitor to keep the modulation of the input current small. The voltage error amplifier must also have enough phase shift so that what modulation remains will be in phase with the input line to keep the power factor high.

The basic low frequency model of the output stage is a current source driving a capacitor. The power stage and the current feedback loop compose the current source and the capacitor is the output capacitor. This forms an integrator and it has a gain characteristic which rolls off at a constant 20dB per decade rate with increasing frequency. If the voltage feedback loop is closed around this it will be stable with constant gain in the voltage error amplifier. This is the technique which is used to stabilize the voltage loop. However, its performance at reducing distortion due to the second harmonic output ripple is miserable. A pole in the amplifier response is needed to reduce the amplitude of the ripple voltage and to shift the phase by 90 degrees. The distortion criteria is used to define the gain of the voltage error amplifier at the second harmonic of the line frequency and then the unity gain crossover frequency is found and is used to determine the pole location in the voltage error amplifier frequency response.

The first step in designing the voltage error amplifier compensation is to determine the amount of ripple voltage present on the output capacitor. The peak value of the second harmonic voltage is given by:

$$Vopk = \frac{Pin}{2\pi fr \times Co \times Vo}$$

Where Vopk is the peak value of the output ripple voltage (the peak to peak value will be twice this), fr is the ripple frequency which is the second harmonic of the input line frequency, Co is the value of the output capacitance and Vo is the DC output voltage. The example converter has a peak ripple voltage of 1.84Vpk.

The amount of distortion which the ripple contributes to the input must be decided next. This deci-

sion is based on the specification for the converter. The example converter is specified for 3% THD so 0.75% THD is allocated to this component. This means that the ripple voltage at the output of the voltage error amplifier is limited to 1.5%. The voltage error amplifier has an effective output range (ΔVvea) of 1.0 to 5.0 volts so the peak ripple voltage at the output of the voltage error amplifier is give by Vvea(pk) = %Ripple x ΔVvea. The example converter has a peak ripple voltage at the output of the voltage error amplifier of 60mVpk.

The gain of the voltage error amplifier, Gva, at the second harmonic ripple frequency is the ratio of the two values given above. The peak ripple voltage allowed on the output of the voltage error amplifier is divided by the peak ripple voltage on the output capacitor. For the example converter Gva is 0.0326.

The criteria for the choice of Rvi, the next step in the design process, are reasonably vague. The value must be low enough so that the opamp bias currents will not have a large effect on the output and it must be high enough so that the power dissipation is small. In the example converter a 511K resistor was chosen for Rvi and it will have power dissipation of about 300mW.

Cvf, the feedback capacitor sets the gain at the second harmonic ripple frequency and is chosen to give the voltage error amplifier the correct gain at the second harmonic of the line frequency. The equation is simply:

$$Cvf = \frac{1}{2\pi fr \times Rvi \times Gva}$$

The example converter has a Cvf value of 0.08μF. If this value is rounded down to Cvf=0.047μF the phase margin will be a little better with only a little more distortion so this value was chosen.

The output voltage is set by the voltage divider Rvi and Rvd. The value of Rvi is already determined so Rvd is found from the desired output voltage and the reference voltage which is 7.50Vdc. In the example Rvd=10K will give an output voltage of 390Vdc. This could be trimmed up to 400VDC with a 414K resistor in parallel with Rvd but for this application 390Vdc is acceptable. Rvd has no effect on the AC performance of the active power factor corrector. Its only effect is to set the DC output voltage.

The frequency of the pole in the voltage error amplifier can be found from setting the gain of the loop equation equal to one and solving for the frequency. The voltage loop gain is the product of the error amplifier gain and the boost stage gain, which can be expressed in terms of the input power. The multiplier, divider and squarer terms can all be lumped into the power stage gain and their effect is to transform the output of the voltage error amplifier into a power control signal as was noted earlier. This allows us to express the transfer function of the boost stage simply in terms of power. The equation is:

$$Gbst = \frac{Pin \times Xco}{\Delta Vvea \times Vo}$$

Where Gbst is the gain of the boost stage including the multiplier, divider and squarer, Pin is the average input power, Xco is the impedance of the output capacitor, ΔVvea is the range of the voltage error amplifier output voltage (4 volts on the UC3854) and Vo is the DC output voltage.

The gain of the error amplifier above the pole in its frequency response is given by:

$$Gva = \frac{Xcf}{Rvi}$$

Where Gva is the gain of the voltage error amplifier, Xcf is the impedance of the feedback capacitance and Rvi is the input resistance.

The gain of the total voltage loop is the product of Gbst and Gva and is given by the this equation:

$$Gv = \frac{Pin \times Xco \times Xcf}{\Delta Vvea \times Vo \times Rvi}$$

Note that there are two terms which are dependent on f, Xco and Xcf. This function has a second order slope (-40dB per decade) so it must be a function of frequency squared. To solve for the unity gain frequency set Gv equal to one and rearrange the equation to solve for fvi. Xco is replaced with 1/(2πfCo) and Xcf is replaced with 1/(2πfCvf).

The equation becomes:

$$fvi^2 = \frac{Pin}{\Delta Vvea \times Vo \times Rvi \times Co \times Cvf \times (2\pi)^2}$$

Solving for fvi in the example converter gives fvi=19.14Hz. The value of Rvf can now be found by setting it equal to the impedance of Cvf at fvi. The equation is: Rvf=1/(2πfviCvf).

In the example converter a value of 177K is calculated and 174K is used.

Feedforward Voltage Divider Filter Capacitors

The percentage of second harmonic ripple voltage on the feedforward input to the multiplier results in the same percentage of third harmonic ripple current on the AC line. The capacitors in the feedforward voltage divider (Cff1 and Cff2) attenuate the ripple voltage from the rectified input voltage. The

second harmonic ripple is 66.2% of the input AC line voltage. The amount of attenuation required, or the "gain" of the filter, is simply the amount of third harmonic distortion allocated to this distortion source divided by 66.2% which is the input to the divider. The example circuit has an allocation of 1.5% total harmonic distortion from this input so the required attenuation is Gff = 1.5 / 66.2 = 0.0227.

The recommended divider string impliments a second order filter because this gives a much faster response to changes in the RMS line voltage. Typically, it is about six times faster. The two poles of the filter are placed at the same frequency for the widest bandwidth. The total gain of the filter is the product of the gain of the two filter section so the gain of each section is the square root of the total gain. The two sections of the filter do not interact much because the impedances are different so they can be treated separately. In the example converter the gain of each filter section at the second harmonic frequency is 0.0227 or 0.15 for each section. This same relationship holds for the cutoff frequency which is needed to find the capacitor values. These are simple real poles so the cutoff frequency is the section gain times the ripple frequency or:

$$fc = \sqrt{Gff} \times fr$$

The example converter has a filter gain of 0.0227 and a section gain of 0.15 and a ripple frequency of 120Hz so the cutoff frequency is fc=0.15x120=18Hz.

The cutoff frequency is used to calculate the values for the filter capacitors since, in this applivation, the impedance of the capacitor will equal the impedance of the load resistance at the cutoff frequency. The two equations given below are used to calculate the two capacitor values.

$$Cff1 = \frac{1}{2\pi \times fp \times Rff2}$$

$$Cff2 = \frac{1}{2\pi \times fp \times Rff3}$$

In the example converter Rff2 is 91K and Rff3 is 20K; so,

Cff1=1/2πx18x91K=0.1μF;

Cff2=1/2πx18x20K=0.44μF;

so choose Cff2=0.47μF.

This completes the design of the major circuits of an active power factor corrector.

DESIGN PROCEDURE SUMMARY

This section contains a brief, step-by-step summary of the design procedure for an active power factor corrector. The example circuit used above is repeated here.

1. Specifications: Determine the operating requirements for the active power factor corrector.

   Example:

   Pout (max): 250W
   Vin range: 80-270Vac
   Line frequency range: 47-65Hz
   Output voltage: 400Vdc

2. Select switching frequency:

   Example:

   100KHz

3. Inductor selection:

   A. Maximum peak line current. Pin ≈ Pout(max)

   $$Ipk = \frac{\sqrt{2} \times Pin}{Vin\ (min)}$$

   Example:

   Ipk=1.41x250/80=4.42 amps

   B. Ripple current.

   $$\Delta I = 0.2 \times Ipk$$

   Example:

   ΔI=0.2x4.42= 0.9 amps peak to peak

   C. Determine the duty factor at Ipk where Vin(peak) is the peak of the rectified line voltage at low line.

   $$D = \frac{Vo - Vin\ (peak)}{Vo}$$

   Example:

   D=(400-113)/400=0.71

   D. Calculate the inductance. fs is the switching frequency.

   $$L = \frac{Vin \times D}{fs \times \Delta I}$$

   Example:

   L=(113x.71)/(100,000x0.9)=0.89mH

   Round up to 1.0mH.

4. Select output capacitor. With hold-up time, use the equation below. Typical values for Co are 1μF to 2μF per watt. If hold-up is not required use the second harmonic ripple voltage and total capacitor power dissipation to determine minimum size of the capacitor. Δt is the hold-up time in seconds and V1 is the minimum output

capacitor voltage.

$$Co = \frac{2 \times Pout \times \Delta t}{Vo^2 - V1^2}$$

Example:

Co=(2x250x34msec)/(400-350)=450µF

5. Select current sensing resistor. If current transformers are used then include the turns ratio and decide whether the output will be positive or negative relative to circuit common. Keep the peak voltage across the resistor low. 1.0V is a typical value for Vrs.

A. Find $Ipk(max) = Ipk + \frac{\Delta I}{2}$

Example:

Ipk(max)=4.42+0.45 ≈ 5.0amps peak

B. Calculate sense resistor value.

$$Rs = \frac{Vrs}{Ipk(max)}$$

Example:

Rs=1.0/5.0=0.20 ohms. Choose 0.25ohms

C. Calculate the actual peak sense voltage.

$$Vrs(pk) = Ipk(max) \times Rs$$

Example:

Vrs(pk)=5.0x0.25=1.25V

6. Set independent peak current limit. Rpk1 and Rpk2 are the resistors in the voltage divider. Choose a peak current overload value, Ipk(ovld). A typical value for Rpk1 is 10K.

$$Vrs(ovld) = Ipk(olvd) \times Rs$$

Example:

Vrs(ovld)=5.6x0.25=1.4V

$$Rpk2 = \frac{Vrs(ovld) \times Rpk1}{Vref}$$

Example:

Rpk2=(1.4x10K)/7.5=1.87K. Choose 1.8K

7. Multiplier setup. The operation of the multiplier is given by the following equation. Imo is the multiplier output current, Km=1, Iac is the multiplier input current, Vff is the feedforward voltage and Vvea is the output of the voltage error amplifier.

$$Imo = \frac{Km \times Iac \times (Vvea - 1)}{Vff^2}$$

A. Feedforward voltage divider. Change Vin from RMS voltage to average voltage of the rectified input voltage. At Vin(min) the voltage at Vff should be 1.414 volts and the voltage at Vffc, the other divider node, should be about 7.5 volts. The average value of Vin is given by the following equation where Vin(min) is the RMS value of the AC input voltage:

$$Vin(av) = Vin(min) \times 0.9$$

The following two equations are used to find the values for the Vff divider string. A value of 1 Megohm is usually chosen for the divider input impedance. The two equations must be solved together to get the resistor values.

$$Vff = 1.414V = \frac{Vin(av) \times Rff3}{Rff1 + Rff2 + Rff3}$$

$$Vnode \approx 7.5V = \frac{Vin(av) \times (Rff2 + Rff3)}{Rff1 + Rff2 + Rff3}$$

Example:

Rff1=910K, Rff2=91K, and Rff3=20K

B. Rvac selection. Find the maximum peak line voltage.

$$Vpk(max) = \sqrt{2} \times Vin(max)\}$$

Example:

Vpk(max)=1.414x270=382Vpk

Divide by 600 microamps, the maximum multiplier input current.

$$Rvac = \frac{Vpk(max)}{600E-6}$$

Example:

Rvac=(382)/6E-4=637K. Choose 620K

C. Rb1 selection. This is the bias resistor. Treat this as a voltage divider with Vref and Rvac and then solve for Rb1. The equation becomes:

$$Rb1 = 0.25\ Rvac$$

Example:

Rb1=0.25Rvac=155K. Choose 150K

D. Rset selection. Imo cannot be greater than twice the current through Rset. Find the multiplier input current, Iac, with Vin(min). Then calculate the value for Rset based on the value of Iac just calculated.

$$Iac(min) = \frac{Vin(pk)}{Rvac}$$

Example:

Iac(min)=113/620K=182µA

$$Rset = \frac{3.75}{2 \times Iac(min)}$$

Example:

Rset=3.75V/(2x182μA)=10.3Kohms.

Choose 10Kohms

E. Rmo selection. The voltage across Rmo must be equal to the voltage across Rs at the peak current limit at low line input voltage.

$$Rmo = \frac{Vrs(pk) \times 1.12}{2 \times Iac(min)}$$

Example:

Rmo=(1.25x1.12)/(2x182E-6)=3.84K.

Choose 3.9Kohms

8. Oscillator frequency. Calculate Ct to give the desired switching frequency.

$$Ct = \frac{1.25}{Rset \times fs}$$

Example:

Ct=1.25/(10K x 100K)=1.25nF.

9. Current error amplifier compensation.

A. Amplifier gain at the switching frequency. Calculate thevoltage across the sense resistor due to the inductor current downslope and then divide by the switching frequency. With current transformers substitute (Rs/N) for Rs. The equation is:

$$\Delta Vrs = \frac{Vo \times Rs}{L \times fs}$$

Example:

ΔVrs=(400x0.25)/(0.001x100,000)=1.0Vpk

This voltage must equal the peak to peak amplitude of Vs, the voltage on the timing capacitor (5.2 volts). The gain of the error amplifier is therefore given by:

$$Gca = \frac{Vs}{\Delta Vrs}$$

Example:

Gca=5.2/1.0=5.2

B. Feedback resistors. Set Rci equal to Rmo.

Rci = Rmo

Rcz = Gca x Rci

Example:

Rcz=5.2x3.9K=20Kohms

C. Current loop crossover frequency.

$$fci = \frac{Vout \times Rs \times Rcz}{Vs \times 2\pi L \times Rci}$$

Example:

fci=(400x0.25x20K)/(5.2x2πx0.001x3.9K)

=15.7KHz

D. Ccz selection. Choose a 45 degree phase margin. Set the zero at the loop crossover frequency.

$$Ccz = \frac{1}{2\pi \times fci \times Rcz}$$

Example:

Ccz=1/(2πx15.7Kx20K)=507pF.

Choose 620pF

E. Ccp selection. The pole must be above fs/2.

$$Ccp = \frac{1}{2\pi \times fs \times Rcz}$$

Example:

Ccp=1/(2πx100Kx20K)=80pf.

Choose 62pF

10. Harmonic distortion budget. Decide on a maximum THD level. Allocate THD sources as necessary. The predominant AC line harmonic is third. Output voltage ripple contributes ½% third harmonic to the input current for each 1% ripple at the second harmonic on the output of the error amplifier. The feedforward voltage, Vff, contributes 1% third harmonic to the input current for each 1% second harmonic at the Vff input to the UC3854.

Example:

3% third harmonic AC input current is chosen as the specification. 1.5% is allocated to the Vff input and 0.75% is allocated to the output ripple voltage or 1.5% to Vvao. The remaining 0.75% is allocated to miscellaneous nonlinearities.

11. Voltage error amplifier compensation.

A. Output ripple voltage. The output ripple is given by the following equation where fr is the second harmonic ripple frequency:

$$Vo(pk) = \frac{Pin}{2\pi fr \times Co \times Vo}$$

Example:

Vo(pk)=250/(2π120x450E-6x400)=1.84Vac

B. Amplifier output ripple voltage and gain. Vo(pk) must be reduced to the ripple voltage allowed at the output of the voltage error amplifier. This sets the gain of the voltage error amplifier at the second harmonic frequency. The equation is:

$$Gva = \frac{\Delta Vvao \times \%Ripple}{Vo(pk)}$$

For the UC3854 Vvao is 5-1=4V

Example:

Gva=(4x0.015)/1.84=0.0326

C. Feedback network values. Find the component values to set the gain of the voltage error amplifier. The value of Rvi is reasonably arbitrary.

Example:

Choose Rvi=511K

$$Cvf = \frac{1}{2\pi \times fr \times Rvi \times Gva}$$

Example:
Cvf=1/(2πx120x511Kx0.0326)=0.08μF.

Choose 0.047μF

D. Set DC output voltage.

$$Rvd = \frac{Rvi \times Vref}{Vo - Vref}$$

Example:

Rvd=(511Kx7.5)/(400-7.5)=9.76K.

Choose 10.0K

E. Find pole frequency. fvi = unity gain frequency of voltage loop.

$$fvi^2 = \frac{Pin}{\Delta Vvao \times Vo \times Rvi \times Co \times Cvf \times (2\pi)^2}$$

Example:

$$fvi = \sqrt{(250/(4x400x511Kx450E{-}6x47E{-}9x39.5))} =$$

19.1 Hz

F. Find Rvf.

$$Rvf = \frac{1}{2\pi \times fvi \times Cvf}$$

Example:

Rvf=1/(2πx19.1x47E-9)=177K. Choose 174K

12. Feedforward voltage divider capacitors. These capacitors determine the contribution of Vff to the third harmonic distortion on the AC input current. Determine the amount of attenuation needed. The second harmonic content of the rectified line voltage is 66.2%. %THD is the allowed percentage of harmonic distortion budgeted to this input from step 10 above.

$$Gff = \frac{\%THD}{66.2\%}$$

Example:

Gff=1.5/66.2=0.0227

Use two equal cascaded poles. Find the pole frequencies. fr is the second harmonic ripple frequency.

$$fp = \sqrt{Gff} \times fr$$

Example:

fp=0.15x120=18Hz

Select Cff1 and Cff2.

$$Cff1 = \frac{1}{2\pi \times fp \times Rff2}$$

$$Cff2 = \frac{1}{2\pi \times fp \times Rff3}$$

Example:

Cff1=1/(2πx18x91K)=0.097μF. Choose 0.10μF

Cff2=1/(2πx18x20K)=0.44μF. Choose 0.47μF

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The UC3848 Average Current Mode Controller Squeezes Maximum Performance from Single Switch Converters

by JOHN A. O'CONNOR

ABSTRACT

This application note describes the UC3848 average current mode PWM controller. The unique features of this controller are discussed, which make primary side average current mode control practical for isolated converters. The UC3848 employs a current waveform synthesizer which monitors switch current and simulates the inductor current down slope, generating a complete current waveform without actual secondary side measurement. Primarily intended for single ended converters, several additional features such as accurate duty-cycle and volt-second limiting allow maximum transformer and switch utilization. A three output, 200 watt off-line design example is presented which also features planar magnetics and a coupled output inductor.

INTRODUCTION

The UC3848 represents a significant advance in the control of single switch forward converters. Generally considered simple and reliable, but non-optimum in transformer and switch utilization, the single switch forward has previously been reserved for less demanding applications. Upon careful examination however, it is apparent that many of the perceived limitations actually result from the control circuitry rather than the converter topology itself.

The advantages that an inner current loop brings to power supply design and performance are well known [1]. Current mode control is usually preferred over direct duty cycle control because of the superior input supply rejection and simplified voltage loop closure. Average current feedback provides additional advantages over the more common peak current feedback. Major benefits include inherent slope compensation, better noise rejection, and the ability to operate with both continuous and discontinuous inductor current. Additionally, average current feedback provides significantly better closed current loop accuracy. This further improves input supply rejection and current limit accuracy. Average current feedback is detailed in the references [2,3,4].

Maximum power component utilization requires carefully defined and controlled operating mode boundaries. While this can be said of many converter topologies, it is particularly critical with the single switch forward because of the transformer reset mechanism. Energy in the transformer leakage and magnetizing inductance must be removed after each energy transfer cycle. Above all, the control circuit must insure that this condition is achieved. Total losses are generally minimized by bringing the peak power transfer as close to the average as possible. This indicates that improvements in efficiency and component utilization are obtainable by maximizing duty-cycle. Unfortunately, maximizing duty-cycle conflicts with assuring transformer reset, traditionally requiring an overly conservative design to assure reliability.

Previously, these characteristics have limited the single switch converter to low-power, low-end applications. The UC3848 Average Current Mode PWM Controller allows operation beyond conventional limitations by employing highly accurate circuitry to provide programmable operating boundaries, and by implementing an inner average current feedback loop for improved control characteristics and accuracy. This control circuit advance capitalizes on unique, patented circuitry, and the precision achievable with Unitrode's thin-film resistor process.

The UC3848 Average Current Mode PWM Controller

The block diagram of the UC3848 shown in figure 1, illustrates a number of unique functions. Although the IC can certainly be used for flyback,

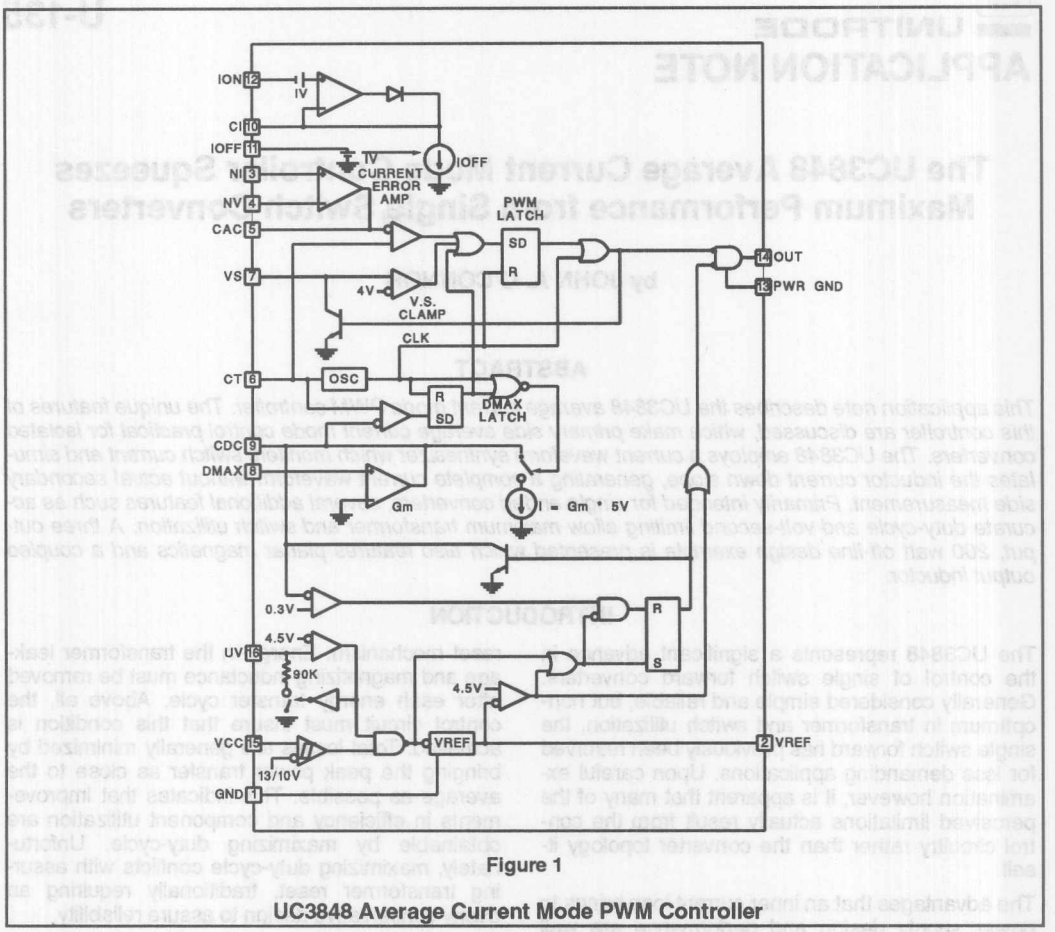


Figure 1

UC3848 Average Current Mode PWM Controller

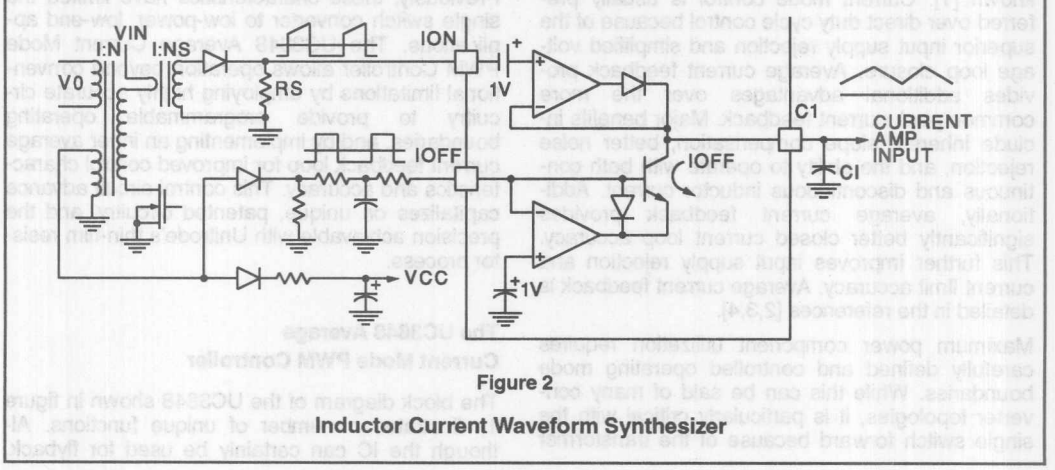


Figure 2

Inductor Current Waveform Synthesizer

boost, as well as other buck derived converters [4], the UC3848 has been optimized for forward converter use. The UC3848s precision functions bring switching power supply control to a new level:

- Average Current Mode Control
- Average Current Sense Signal Synthesizer
- Programmable Maximum Duty-Cycle and Volt-Second Control
- Under Voltage Lockout (UVLO) monitors Vcc, Vin, and Vref
- 2 Amp peak MOSFET Driver with Active Low During UVLO
- 8MHz gain-bandwidth Current Error Amplifier
- Latched PWM comparator
- Practical Operation up to 1MHz
- Low Start-Up Current (500uA)
- Precision Reference (1% @ 5V)

The sophistication and performance of the UC3848 may at first appear contradictory to simple forward converter design. A truly simple implementation however, is best achieved by maintaining simple power circuitry, and placing the complexity and precision in the control circuitry where it can be integrated into a single IC.

Average Current Mode Control

Average current loop implementation first requires an average current signal for the control variable. This immediately presents a problem with isolated converters since this signal is entirely on the secondary side. A current sense transformer cannot be used to directly sense output inductor current with buck derived converters since the inductor normally has a continuous DC component. A potentially complex and expensive solution is avoided with the realization that output inductor current is directly reflected to the primary during the switch on time. Simply scaling the switch current by the transformer turns ratio provides the rising portion of the inductor current waveform. When the switch is off, the inductor current decays at V_{OUT}/L. This information can be used to synthesize an analog of the actual output inductor current without any secondary connections.

Inductor current is synthesized by the UC3848 with a circuit that behaves similar to a track and hold amplifier, as shown in figure 2. While the switch is on, a unity gain buffer charges an external capacitor (C_I), essentially following the rising input current waveform. A one volt offset is also added to provide sufficient headroom for the buffer's output stage. When the switch turns off, a programmable current sink discharges the capacitor, simulating the actual inductor current decay. Several techniques are available for setting the discharge current, depending on the required accuracy of the current sense signal. If good short-circuit accuracy is required, an analog of the output voltage is required to control the synthesizer capacitor discharge rate. There are two simple ways to derive this signal on the primary side.

The first method uses a transformer bootstrap winding voltage as shown in figure 2. The average value of the rectified output and bootstrap winding voltages are directly proportional. By adding a separate rectifier and filter to this winding, the capacitor discharge current can be programmed to track V_{OUT}. Typically, a bootstrap winding is employed with off-line converters to power the control circuitry after initial start-up, so the raw signal is usually present at no additional cost. Note that an error is present during transients since the filter creates a lag between the output and the filtered bootstrap voltages.

If the transient error is unacceptable, the technique shown in figure 3 can be used. A secondary winding on the output inductor provides a voltage directly proportional to the output without filtering. While the switch is off, V_{OUT} is across the output inductor. Any other winding on the inductor will have a voltage proportional to V_{OUT} by the turns

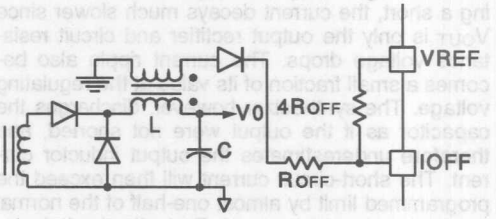


Figure 3
IOFF Generation using Second Inductor Winding

ratio of the two windings. The sense winding rectifier drop cancels the output rectifier drop when the turns ratio is 1:1, yielding excellent signal accuracy. While this approach is simple and accurate, it does come at additional expense since this winding is not normally required. Additionally, high voltage agency approved isolation is required for off-line converters, adding further cost and manufacturing complexity to the inductor.

With either of these techniques, an offset current may be added to compensate for the synthesizer's

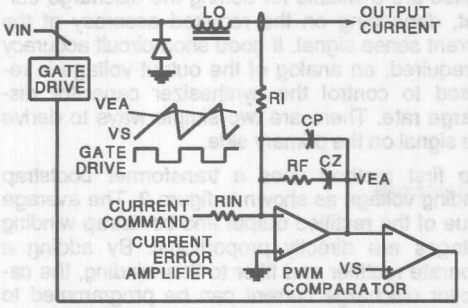


FIGURE 4. AVERAGE CURRENT FEEDBACK LOOP

Figure 4

Average Current Feedback Loop

one volt offset. Connecting a resistor with a value four times the I_{OFF} input resistor between the V_{REF} and I_{OFF} pins cancels the offset.

Often, a fixed discharge current is acceptable. This is programmed by connecting a resistor between the V_{REF} and I_{OFF} pins. The synthesized current waveform is quite accurate when the output voltage is near the regulating value, however an error exists during start-up and output short-circuit. During a short, the current decays much slower since V_{OUT} is only the output rectifier and circuit resistance voltage drops. The current ripple also becomes a small fraction of its value at the regulating voltage. The synthesizer however, discharges the capacitor as if the output were not shorted, and therefore underestimates the output inductor current. The short-circuit current will then exceed the programmed limit by almost one-half of the normal peak-to-peak ripple current. Typically, the inductor ripple current is 20% to 30% of the maximum DC value, corresponding to a short circuit current 10% to 15% higher than the maximum output current available at normal output voltage.

The current error amplifier has sufficient gain to use a current sense resistor directly in most applications. A current sense transformer however, results in better performance by allowing a larger amplitude, lower noise signal. Ideally, the current sense signal is scaled to 4 volts at the maximum current level. The current transformer load resistance is then:

$$R_S = 4V \times N \times \frac{N_S}{I_L} \qquad (1)$$

where N = transformer turns ratio
N_S = current transformer ratio
I_L = maximum load current

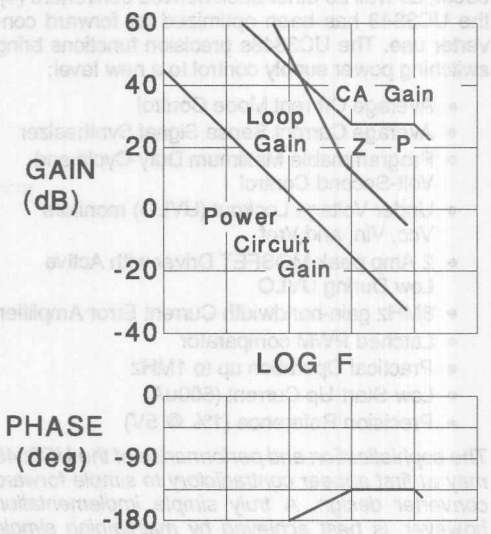


Figure 5

Open Current Loop Response

With multiple secondaries, normalize all other loads to the main output through the turns ratio directly. Note that for these calculations, output inductors and their effect on ripple current is not considered, since the UC3848 controls average, not peak current. Output inductances must be normalized to the main output through the turns ratio squared however, when calculating peak current and current ripple.

The recommended nominal I_{OFF} current is 100µ A, leaving C_I the remaining current synthesizer component.

$$C_I = \frac{(100\mu A \times N \times N_S \times L_{NORM})}{(Rs \times V_{OUT}(nom))} \qquad (2)$$

where L_{NORM} = normalized output inductance

Figure 4 shows the average current feedback loop. This inner loop is analogous to direct duty-cycle or voltage-mode control except that the control variable is output inductor current rather than output voltage. Properly compensated, the open loop gain is comparable to peak current-mode's at high frequency, and becomes orders of magnitude higher as frequency decreases. The open current loop response shown in figure 5 illustrates this behavior. This high open loop gain translates into high

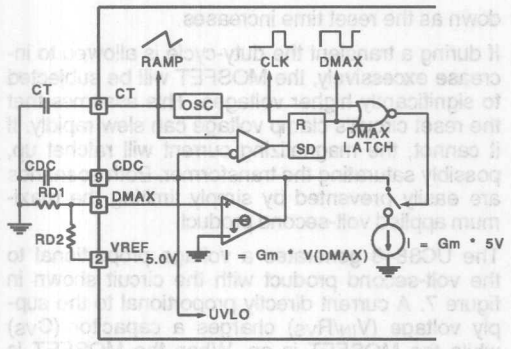


Figure 6

Duty-Cycle Limit Programming

closed loop accuracy. In comparison, peak current mode relies entirely on it's transfer function accuracy, and has no means by which to reduce errors. This characteristic difference from peak current-mode is attributed to the current error amplifier's compensation, and is key to the resulting performance enhancements.

The increased gain at low frequency provides excellent closed current loop accuracy, even when the inductor current becomes discontinuous. High open loop gain also allows greater filtering of the current sense signal with no degradation in closed loop accuracy. It is this characteristic, along with the larger amplitude signals that provides significantly reduced noise susceptibility in comparison to peak current-mode control.

PWM Oscillator

Oscillator programming is simplified by providing internally set charge and discharge currents. Excellent initial accuracy and temperature stability are assured by precision thin-film resistors. Since only a timing capacitor (C_T) is required to set the frequency, external component error contribution is minimal. The precision high speed oscillator combined with short propagation delay through the PWM circuitry allows practical operation up to 1MHz.

A 200µA charge current and a 1800µA discharge current generates a sawtooth waveform with a well defined rise/fall relationship and accurate frequency. During discharge, the output driver is disabled, limiting the maximum duty-cycle to 90%. Note that this maximum can be reduced by the accurate, duty-cycle limit and the volt-second product limit circuits, which are explained in following sections. Oscillator frequency is programmed by:

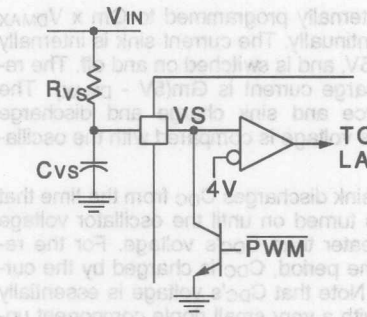


Figure 7

Volt-Second Clamp

$$F = \frac{1}{(10k \times C_T)} \quad (3)$$

If greater frequency accuracy is required, a trim resistor in parallel with C_T can be added to lower the frequency. The trim resistor should not be less than 40kΩ, limiting the maximum trim range to 25% below nominal. Frequency decrease as a function of trim resistance is shown on the UC3848 data sheet.

Duty-Cycle Limiting and Soft Start

The conventional single switch forward converter design usually limits the maximum duty-cycle to 50%. This limit however, is only required if a one-to-one clamp winding is employed to facilitate transformer core reset. While some designers still use this technique, a resistor/capacitor/diode (RCD) clamp has become more prevalent. The RCD clamp eliminates a transformer winding and potentially offers a wider duty-cycle range. Currently, a 50% duty-cycle limit is primarily used because it can be accurately derived from a toggle flip-flop. To exploit a wider duty-cycle, an accurate, programmable duty-cycle clamp is required.

The UC3848 employs a unique, patented technique to limit the maximum duty-cycle to a value programmed by a resistive divider. The circuit utilizes a capacitor (C_{DC}) for integration only, and does not rely on its absolute value for maximum duty-cycle accuracy. The absolute value of C_{DC} does set the soft-start time constant, although high precision is not normally required for this function.

Internally, the UC3848 capitalizes on the excellent matching characteristics achievable on an IC to implement a charge balanced loop. A matched transconductance source and sink form a precision integrator circuit, as shown in figure 6. The current

source is externally programmed to Gm x V_{DMAX} and is on continually. The current sink is internally set at Gm x 5V, and is switched on and off. The resulting discharge current is Gm(5V - $_{DMAX}$). The current source and sink charge and discharge C_{DC}, while its voltage is compared with the oscillator voltage.

The current sink discharges C_{DC} from the time that the switch is turned on until the oscillator voltage becomes greater than C_{DC}'s voltage. For the remainder of the period, C_{DC} is charged by the current source. Note that C_{DC}'s voltage is essentially a DC level with a very small ripple component unless it is a particularly small value. C_{DC} maintains a constant voltage only if the average applied charge is zero. The charge balanced loop therefore forces $I_{DISCHARGE}$ x $T_{ON(max)}$ to equal I_{CHARGE} x $T_{OFF(min)}$. A large offset voltage between C_T and C_{DC} may be observed when measuring an actual circuit. This offset contributes negligible error since high DC loop gain reduces its effect by several orders of magnitude.

While the circuit's operation may seem complicated, it couldn't be easier to apply. A voltage divider from V_{REF} to D_{MAX} as shown if figure 6 sets the maximum duty-cycle. The circuit inherently provides soft-start at initial power-up as C_{DC} charges to it's steady state value. Increasing C_{DC} extends the loop settling time, and hence the soft-start time constant, with no effect on the programmed maximum duty-cycle. Note that the single pole loop response avoids overshoot, regardless of the integrating capacitor value. Soft-start after fault is explained in the under-voltage lockout section. Maximum duty-cycle and soft-start are programmed by the following relationships:

$$D_{MAX} = \frac{R_{D1}}{(R_{D1} + R_{D2})} \quad (4)$$

$$\tau_{ss} = 20k \times C_{DC} \quad (5)$$

Volt-Second Product Limit

During transients it may be desirable to limit the duty-cycle below the programmed maximum value. For example, active transformer reset circuits vary the clamp voltage inversely proportional to the input supply voltage [5]. During steady state operation the peak MOSFET voltage varies much less than with passive clamp circuits. Unless the input voltage range is large, the peak MOSFET voltage will be fairly constant. This occurs because the applied volt-second product remains constant over the entire operating duty-cycle range during steady state. Thus as the input voltage goes up and the duty-cycle decreases, the clamp voltage goes down as the reset time increases.

If during a transient the duty-cycle is allowed to increase excessively, the MOSFET will be subjected to significantly higher voltages. This assumes that the reset circuit's clamp voltage can slew rapidly. If it cannot, the magnetizing current will ratchet up, possibly saturating the transformer. Both scenarios are easily prevented by simply limiting the maximum applied volt-second product.

The UC3848 generates a voltage proportional to the volt-second product with the circuit shown in figure 7. A current directly proportional to the supply voltage (V_{IN}/R_{VS}) charges a capacitor (C_{VS}) while the MOSFET is on. When the MOSFET is turned off, the capacitor is discharged. Volt-second limiting is accomplished by comparing the capacitor's voltage to a 4 volt reference, and terminating the pulse width for the remainder of the switching period. Normally, the worst case MOSFET voltage occurs during maximum input voltage at the volt-second limited duty-cycle. However, high turns ratio designs which allow a very wide duty-cycle may actually generate the highest MOSFET voltage during low-line at the volt-second limited duty-cycle.

Since the volt-second product is constant it can be calculated at any input voltage. The effectiveness

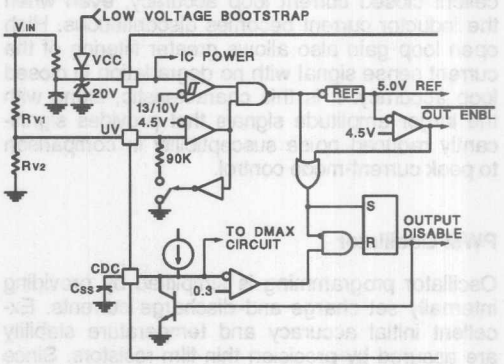


Figure 8

Under Voltage Lockout

of the volt-second limit however, should be analyzed at minimum and maximum input voltage, in addition to a few more typical voltages. The volt-second product clamp is programmed by:

$$V_{IN} \times T_{ON} = 4.0V \times R_{VS} \times C_{VS} \quad (6)$$

Under Voltage Lockout

Programmable under voltage lockout (UVLO) further defines operating mode boundaries. V_{CC}, V_{IN},

and V_{REF} are monitored to insure that the chip supply, main input supply, and reference are within specification before enabling the output stage. Figure 8 shows the block diagram of the UVLO circuitry.

The V_{CC} comparator monitors the chip supply voltage. Hysteretic thresholds at 13V and 10V insure that sufficient voltage is available to power the chip and fully turn on the MOSFET. The V_{IN} comparator monitors the input supply through a resistive divider. A small capacitor from UV to ground is usually required to filter noise from this high impedance node. Both the thresholds and the hysteresis are programmed by the divider values with the relationships:

$$V_{IN(ON)} = 4.5V \times \left(1 + \frac{R_{V1}}{R_{V2'}}\right) \quad (7)$$

$$V_{IN(OFF)} = 4.5V \times \left(1 + \frac{R_{V1}}{R_{V2}}\right) \quad (8)$$

where $R_{V2'} = R_{V2} \parallel 90k$

$$V_{IN(HYS)} = 4.5V \times \frac{R_{V1}}{90k} \quad (9)$$

When either the V_{CC} or the V_{IN} comparator are low, the bias circuitry to the rest of the chip is off. The quiescent current (I_{CC}) is nominally 500µ A to facilitate off-line applications. Once both V_{CC} and V_{IN} are within specification, the bias circuitry for the rest of the chip is activated. The output driver and C_{DC} pin are still held low until V_{REF} exceeds the 4.5V threshold of the V_{REF} comparator. When the V_{REF} comparator goes high, control of the output driver transfers to the PWM circuitry and C_{DC} is allowed to charge, soft-starting the supply.

If any of the three monitored voltages falls below their threshold during start-up or normal operation, the UVLO latch is set, the output driver is held low, and C_{DC} is discharged. This state is maintained until C_{DC} is fully discharged, at which point operation is as described above.

Output Driver

High current transistors enable the output driver to deliver 2 amps peak allowing direct interface to any MOSFET typically used in single ended converters. The driver also incorporates self-biasing circuitry that maintains a low impedance to ground during UVLO. This assures that high dv/dt at V_{IN} during power-up cannot inadvertently turn on the MOSFET through its miller capacitance.

The combination of high peak current, stray circuit inductance, and capacitive gate load result in reflections back to the driver, which if left unclamped, will cause erratic chip behavior. External schottky diodes from the output to V_{CC} and ground will divert the reflected current and assure reliable operation. A well designed layout with typical circuit values will normally require 1A, 20V schottky clamp diodes. Looser layouts, longer gate drive traces, and lower gate resistor values all place greater demand on the output clamping circuit, and may necessitate higher current diodes.

Voltage Reference and Error Amplifier

Since the UC3848 is intended for primary side control, the voltage reference (V_{REF}) does not affect output voltage stability. It does however, affect current limiting and the other precision circuits previously mentioned, and has therefore been designed for good initial accuracy and temperature drift. The reference should be capacitively bypassed to reduce high frequency output impedance and noise susceptibility.

To facilitate wide bandwidth current loops, the error amplifier has an 8Mhz gain bandwidth product. Even with small current feedback signals such as from a current sense resistor, loop bandwidth will almost always be limited by external circuit characteristics rather than error amplifier limitations. The amplifier's 8 V/s slew rate assures that even during large signal transients, external components will determine circuit behavior.

Design Example

A 200 watt off-line supply utilizing the UC3848 is shown in figure 9. It delivers a regulated +5V at 20A, and a semi-regulated +/-15V at 3.3A. The conversion frequency is 260kHz, which was determined to be a reasonable compromise between size and efficiency. A coupled output inductor improves dynamic cross regulation and steers some of the +5V ripple current to the +/-15V filter capacitors [9]. This results in minimal total output capacitor volume. A bridge/doubler input rectifier allows operation over an input range of 85 to 265VAC. For simplicity and cost, an RCD clamp is employed to facilitate transformer reset. This common configuration is typical of many commercial applications.

The transformer turns ratio is selected to minimize MOSFET stress. Ideally, the maximum duty-cycle should be as large as possible, allowing the highest turns ratio and lowest reflected load current. This must be balanced against the peak MOSFET voltage developed during transformer reset.

Since the UC3848 can accurately define operating mode boundaries, any practical duty-cycle range can be used. This allows maximum utilization of both current and voltage capability of a particular

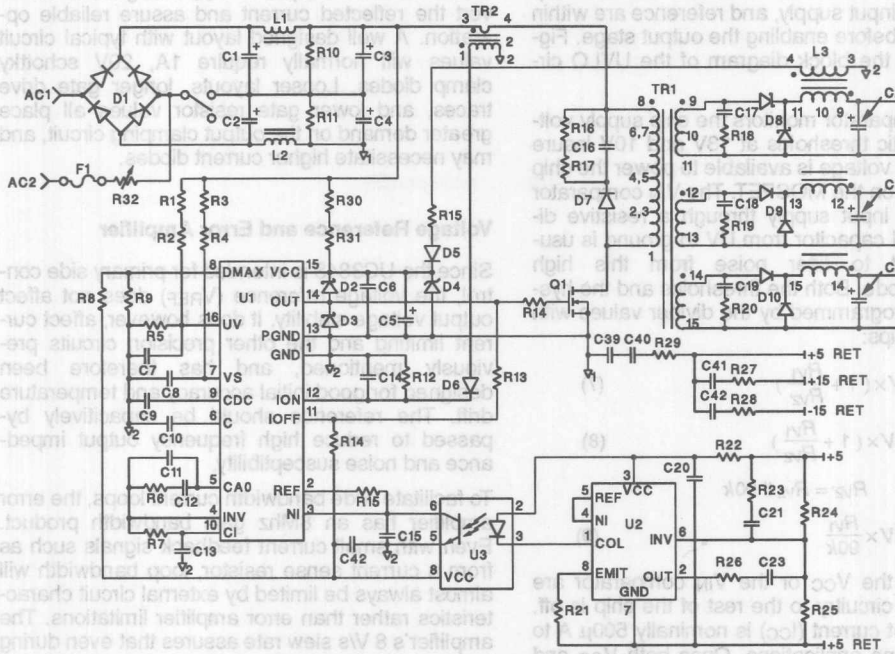


Figure 9

200W 3 OUTPUT FORWARD CONVERTER

MOSFET. The RCD clamp allows some trade-off in dissipation versus peak MOSFET voltage. Turns ratio and clamp optimization requires a good estimation of leakage inductance, switch capacitance, and transformer interwinding capacitance, since energy stored in these parasitics will be transferred or dissipated each switching cycle. RCD clamp optimization is covered in detail in reference [6].

The design example transformer uses a 16:1 turns ratio (primary to 5 volt), allowing a wide input supply range and reliable use of an 800V MOSFET. The MOSFET, an APT801R2BN from Advanced Power Technology [7], is rated at 800V and has 1.2Ω maximum on resistance at 25°C. A planar transformer and coupled output inductor from Signal Transformer Co. [8] are used, which offer several advantages over custom wound components. Planar construction provides tighter parameter tolerance. Compact, low profile magnetics help achieve high power density. Their standard design provides agency approved insulation and known performance characteristics, greatly reducing the number of iterations to produce a good power supply design.

The duty-cycle is limited to 0.6, maintaining regulation down to approximately 160 VDC in. With the switching frequency programmed for 260 kHz, the nominal volt-second product is 345 Vs. The volt-second clamp is programmed to 425 Vs to allow for tolerances and large signal transients.

A current transformer senses switch current resulting in minimal loss and good signal quality. A 1000pF capacitor shunts the high frequency turn-on spike before feeding the current sense signal to the UC3848s current waveform synthesizer. A fixed I_{OFF} value renders an acceptable short circuit current for this application. Average short circuit losses are kept low by the hiccup action which occurs as the boot-strap supply colapses and the supply restarts. Highly accurate short circuit current is most advantageous when a continuous supply is available for the control circuit such as in low voltage DC to DC converter applications.

When the MOSFET is on, the current synthesizer's I_{OFF} current is increased through a resistor connected to the gate driver output (R13). This allows C_I's voltage to better follow rectifier reverse recovery spikes present in the current waveform. This technique allows minimal filtering of the current

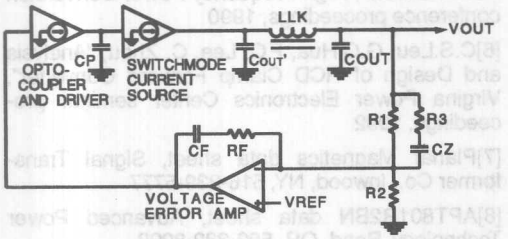


Figure 10

Voltage Feedback Loop

sense signal, and thus preserves accuracy.

The coupled output inductor provides good dynamic cross regulation, and steers some of the 5 volt ripple current to the +/-15 volt outputs where it is more efficiently filtered. Although this technique minimizes size and complexity, it does negate two major advantages of average current mode control. The average current loop maintains excellent regulation down to zero load for the fully regulated output. Unfortunately, the semi-regulated outputs will degrade quickly as the inductor current becomes discontinuous, forcing minimum loads for reasonable output voltage tolerance. Also, stray and leakage inductance between the secondary circuits introduces parasitic tank circuits, which if underdamped, will cause output ringing and instability. Generally, electrolytic output capacitors, low coupled inductor leakage inductance, and tight layout will allow successful implementation, although loop bandwidth must usually be compromised to maintain stability. Coupled output inductor design and application is detailed in reference [9].

Without the additional output circuitry parasitics, a single output supply with average current feedback has excellent regulation and transient response from zero to full load. There is also much less restriction on output capacitor type, allowing small ceramic or film capacitors in many applications. Although the design example's closed loop bandwidth is not as high as would be achievable with a single output, the electrolytic output capacitors store enough energy to provide good transient response and low output impedance.

Control Loops

A block diagram of the voltage feedback loop is shown in figure 10. For clarity, the inner average current feedback loop is shown as a transconductance amplifier, and is identical to figure 4. Current loop compensation is best described in the references [2,3], as a number of subtleties must be considered for optimal performance. The basic approach is easily summarized:

To avoid subharmonic oscillation of a single pole system, the amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input. This puts an upper limit on the current amplifier gain, and indirectly sets the loop gain crossover frequency. As derived in [2], the resulting unity gain crossover frequency will be:

$$f_C = \frac{(f_S V_{IN})}{(2\pi V_{OUT})} = \frac{f_S}{(2\pi D)} \quad (10)$$

The crossover frequency must be reduced in a practical system to account for tolerances and additional waveform slope injected by output voltage ripple through the voltage error amplifier. For the design example, f_C is approximately 50kHz at the maximum duty-cycle.

At the switching frequency, the average current loop's behavior is similar to peak current mode control. Placing a zero at one-half the crossover frequency increases the loop gain with decreasing frequency, providing high closed current loop accuracy. To further reduce noise susceptibility, a pole is placed at the switching frequency. While such a low frequency filter is completely unacceptable with peak sensing, the high gain at low frequency assures accurate current limiting. It is these fundamental differences from peak current mode which provide the performance enhancements.

The voltage loop reference and error amplifier reside on the secondary side as typically configured in off-line power supplies. A UC19432 incorporates a high precision reference, voltage error amplifier, and programmable transconductance amplifier for accurate opto-coupled feedback. Voltage loop compensation is normally the same as with peak current mode control and is described in detail in the references [2,9,10]. As previously noted, an additional LC pole resulting from leakage and stray inductance requires additional compensation. Ultimately, this parasitic restricts the bandwidth of this coupled inductor design example, although transient response is still quite good. The same control configuration with a single output supply provides optimal performance and allows simpler compensation.

Summary

The UC3848 clearly demonstrates the next level of switching power supply control achievable with improved techniques and precision circuitry. High

performance and high power density objectives coupled with the need for simplicity and low cost have called for further refinement of single switch conversion. The UC3848 answers that call combining precision circuitry, average current mode control and function flexibility, allowing optimal power component utilization and performance.

References:

[1]V. Holland, "Modelling, Analysis and Compensation of the Current-Mode Converter" Unitrode application note U-97

[2]L. Dixon, "Control Loop Design", Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM800, 1991

[3]L. Dixon, "Average Current Mode Control of Switching Power Supplies", Unitrode application note U-140

[4]B. Mammano, "Average Current-Mode Control Provides Enhanced Performance for a Broad Range of Power Topologies", PCIM conference proceedings, 1992

[5]B. Carsten, "Design Techniques for Transformer Active Reset Circuits at High Frequencies and Power Levels", High Frequency Power Conversion conference proceedings, 1990

[6]C.S.Leu, G.C.Hua, F.C. Lee, C. Zhou, "Analysis and Design of RCD Clamp Forward Converter", Virgina Power Electronics Center seminar proceedings, 1992

[7]Planar Magnetics data sheet, Signal Transformer Co., Inwood, NY, 516-239-5777

[8]APT801R2BN data sheet, Advanced Power Technology, Bend, OR, 503-382-8028

[9]L. Dixon, "Coupled Filter Inductors in Multi-Output Buck Regulators", Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM800, 1991

[10]L. Dixon, "Closing the Feedback Loop", Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM700, 1990

Unitrode Data Sheets:

UC3848
UC19432

PARTS LIST FOR 200W CONVERTER

R1, 2	825k	1%
R3, 4	243k	1%
R5	42.2k	1%
R6, 7	10k	
R8	10.0k	1%
R9	15.0k	1%
R10, 11	62k	1w
R12	68	
R13	36k	
R14	39k	
R15,23	2k	
R16, 17	15k	3w
R18	10	2w
R19, 20	33	1/2w
R21	33	
R22	200	
R24	18.7k	1%
R25	6.49k	1%
R26	1k	
R27, 28	20	
R29	100	
R30, 31	120k	1/2w
R32	5ΩNTC	thermistor

C1-C4	390µF	20%	200V
C5	100µF	20%	25V
C6, 20, 31, 32, 35, 38	1µF		
C7, 14	1nF		
C8	220pF	5%	
C9	47nF		
C10	390pF	5%	
C11	22pF		
C12	330pF		
C13	220pF		
C15	10nF		
C16	2.2nF		
C17	4.7nF		100V
C18, 19	470pF		500V
C21, 23	3.3nF		
C24-C30	1000µF	20%	10V
C32, 33, 36, 37	330µF	20%	25V
C39, 40	2.2nF	20%	500V
	class x/y		
C41, 42	100nF	20%	100V

D1	MB106-ND	(Diodes, Inc.)
D2, 3	1N5820	
D3	1N4745A	
D4, 5	1N4148	
D6	10DF8	(International Recifier)
D7	40CPQ060	(International Recifier)
D9, 10	10CTF20	(International Recifier)
Q1	APT801R2BN	(Advanced Power Technology)
L1, 2	RL-1160-1.0	(Renco)
L3	SHFI-2515	(Signal Transformer Co.)
TR1	SHF-2525-16	(Signal Transformer Co.)
TR2	PE64978	(Pulse Engineering)
U1	UC3848	
U2	UC19432	

NOTE: All resistors 5%, 1/4 watt unless noted
All capacitors 10%, 50V unless noted

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UNITRODE

APPLICATION NOTE

PHASE SHIFTED, ZERO VOLTAGE TRANSITION DESIGN CONSIDERATIONS and the UC3875 PWM CONTROLLER

BILL ANDREYCAK

ABSTRACT

This Application Note will highlight the design considerations incurred in a high frequency power supply using the Phase Shifted Resonant PWM control technique. An overview of this switching technique including comparisons to existing fixed frequency non-resonant and variable frequency Zero Voltage Switching is included. Numerous design equations and associated voltage, current and timing waveforms supporting this technique will be highlighted. A general purpose Phase Shifted converter design guide and procedure will be introduced to assist in weighing the various design tradeoffs. An experimental 500 Watt, 48 volt at 10.5 amp power supply design operating from a preregulated 400 volt DC input will be presented as an example. Considerations will be given to the details of the magnetic, power switching and control circuitry areas. A summary of comparative advantages, differences and tradeoffs to other conversion alternatives is included.

UC3875 CONTROL CIRCUIT SCHEMATIC

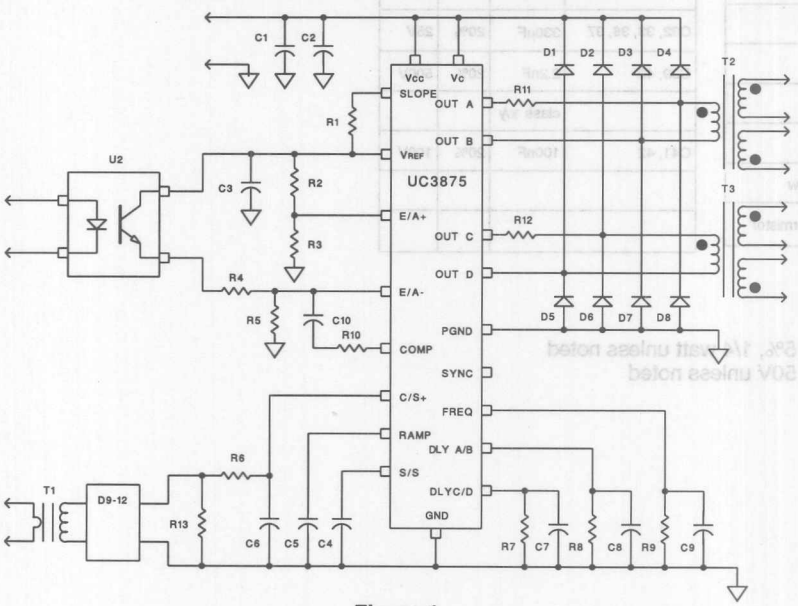


Figure 1

INTRODUCTION

The merits of lossless transitions using Zero Voltage Switching techniques have already been established in power management applications. [1-5] Effects of the parasitic circuit elements are used advantageously to facilitate the resonant transitions as opposed to being dissipatively snubbed. This resonant tank functions to position zero voltage across the switching device prior to turn-on, eliminating any power loss due to the simultaneous overlap of switch current and voltage at each transition. High frequency converters operating from high voltage input sources stand to gain significant improvements in efficiency with this technique. The full bridge topology as shown in figure 2. will be the specific focus of this presentation, with an emphasis placed on the fixed frequency, phase shifted mode of operation.

Full Bridge Topology - General Circuit

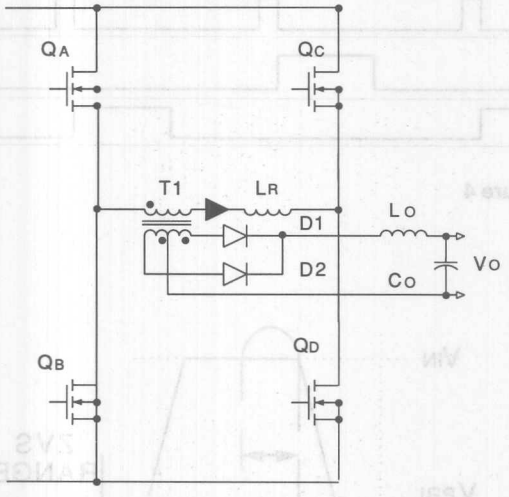


Figure 2

SWITCH DRIVE COMMANDS

The diagonal bridge switches are driven together in a conventional full bridge converter which alternately places the transformer primary across the input supply, Vin, for some period of time, t(on) as shown in figure 3.

Power is only transferred to the output section during the ON times of the switches which corresponds to a specific duty cycle when operated at fixed frequency. Additionally, the complete range of required duty cycles is unique to the application, and can be estimated from the power supply input and output voltage specifications.

Conventional Full Bridge PWM Waveforms

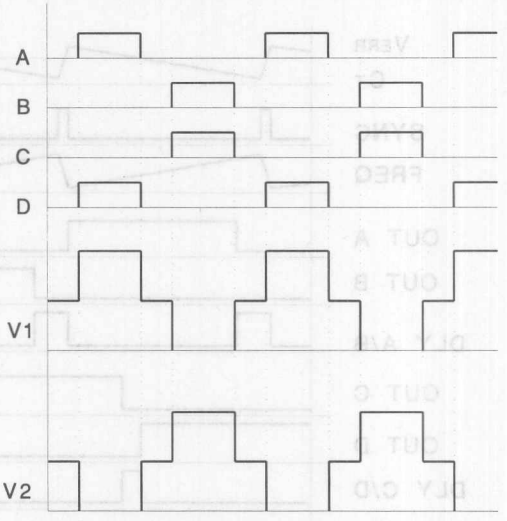


Figure 3

Rather than driving both of the diagonal full bridge switches together, a deliberate delay will be introduced between their turn-on commands with the Phase Shifted approach. This delay will be adjusted by the voltage loop of the control circuitry, and essentially results as a phase shift between the two drive signals. The effective duty cycle is controlled by varying the phase shift between the switch drive commands as shown in figure 4.

Unique to this Phase Shifted technique, two of the switches in series with the transformer can be ON, yet the applied voltage to the transformer is zero. These are not diagonal switches of the full bridge converter, but either the two upper or two lower switches. In this mode the transformer primary is essentially short circuited and clamped to the respective input rail. Primary current is maintained at its previous state since there is no voltage available for reset to take place. This deadband fills the void between the resonant transitions and power transfer portion of the conversion cycle. Switches can be held in this state for a certain period of time which corresponds to the required off time for that particular switching cycle.

When the correct one of these switches is later turned off, the primary current flows into the switch output capacitance (Coss) causing the switch drain voltage to resonate to the opposite input rail. This aligns the opposite switch of the particular bridge "leg" with zero voltage across it enabling Zero Voltage Switching upon its turn ON.

Phase Shifted PWM Control Waveforms

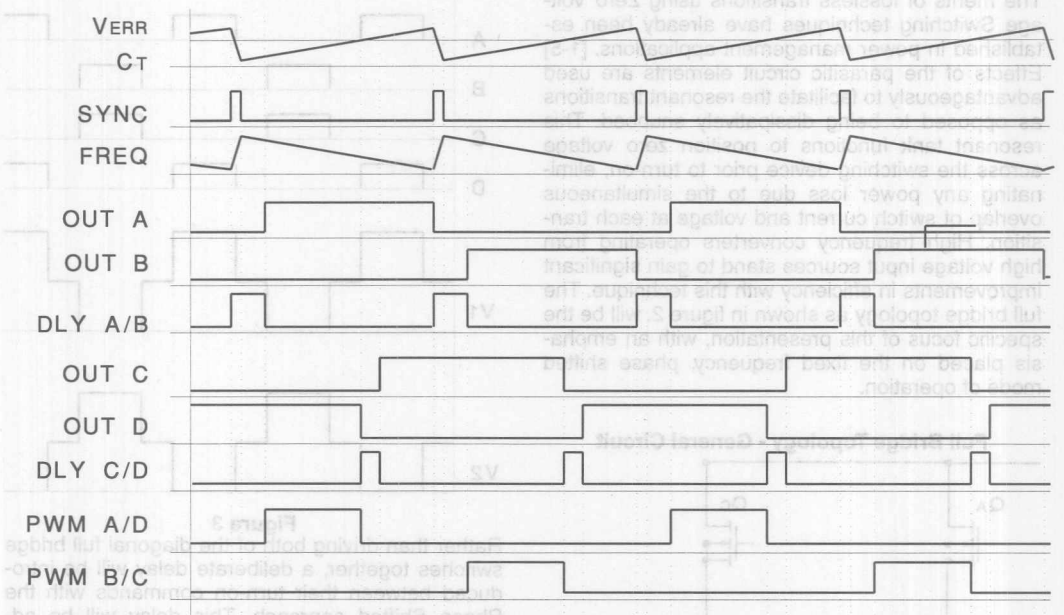


Figure 4

ZVS FUNDAMENTALS

An intentional dead-time can be introduced in the power conversion cycle whereby the switch remains off and is clamped at zero voltage by the resonant tank. Rather then turn the switch on instantly when zero voltage is attained, the switch is held off while the primary current circulates into the shorted primary through the body diode and the opposite leg switch, which is still on. This off time is used to fill in the voids between the point where zero voltage has been reached where the switch needs to turned on to achieve fixed frequency operation.

Fixed frequency operation is obtainable over an identified range of input voltages and output currents. For reference purposes, the variable frequency ZVS technique has similar limitations for proper operation which occur at minimum output load and maximum input line as shown in figure 5.

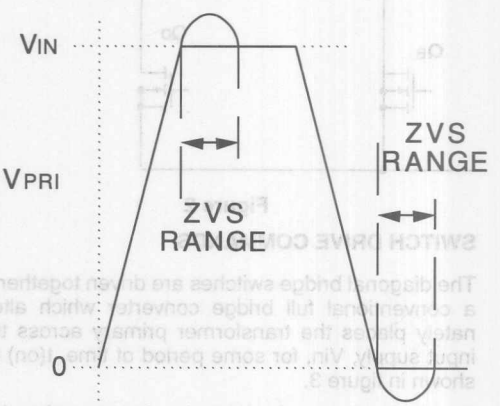


Figure 5

ZVS Limitations

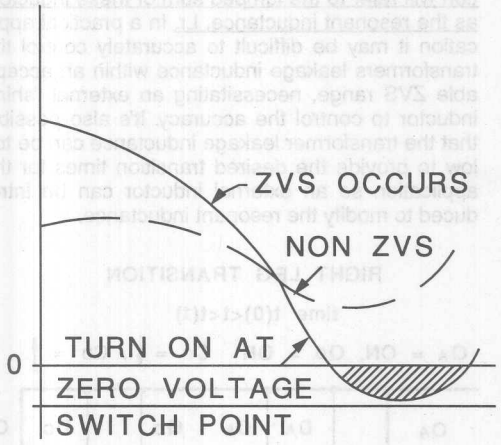


Figure 6

Phase Shifted PWM Switch Orientation

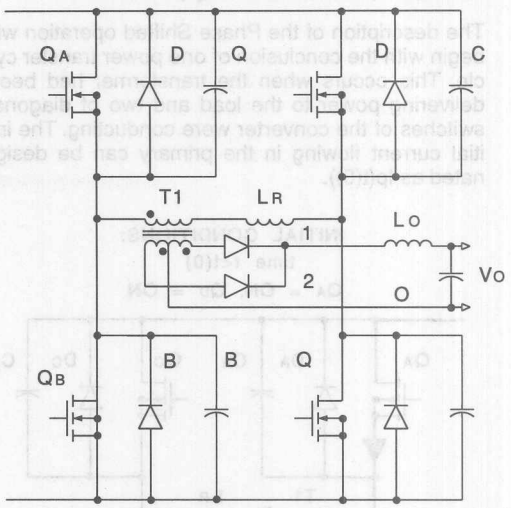


Figure 7

PHASE SHIFTED FUNDAMENTALS

Switches within the Phase Shifted full bridge converter will be utilized differently than those of its nonresonant counterpart. Instrumental to this technique is the use of the parasitic elements of the MOSFET switch's constructuin. The internal body diode and output capacitance (Coss) of each device (in conjunction with the primary current) become the principal components used to accomplish and commutate the resonant transitions.

CIRCUIT SCHEMATIC AND DESCRIPTION

Detailed operation of the Phase Shifted Converter operation will begin following a description of the circuit elements. The circuit schematic of this technique is shown in figure 7. including voltage and current designations.

The basic circuit is comprised of four switches labeled QA through QD and is divided up into two "legs", the right and left hand legs. Each switch is shown shunted by its body diode (DA through DD) and parasitic output capacitance, (CA through CD). These have been identified separately to clarify the exact elements and current paths during the conversion interval.

A detailed model of the transformer primary section is presented which separately indicates the leakage and magnetizing inductances and currents of the primary. The reflected secondary contributors to primary current are also shown for completeness, and divided into two components. The DC primary current (IP) is the secondary DC output current divided by the transformer turns ratio (N). The secondary AC current should also accounted for by multiplying the output inductance by the turns ratio squared (N^2), or dividing the secondary AC ripple current Isec(ac) by the turns ratio (N) as shown in figure 8.

Primary Magnetic Components

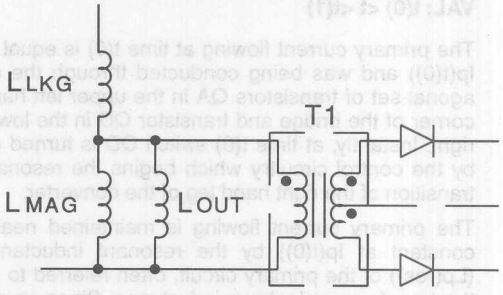


Figure 8

INITIAL CONDITIONS : t = t(0)

The description of the Phase Shifted operation will begin with the conclusion of one power transfer cycle. This occurs when the transformer had been delivering power to the load and two of diagonal switches of the converter were conducting. The initial current flowing in the primary can be designated as Ip(t(0)).

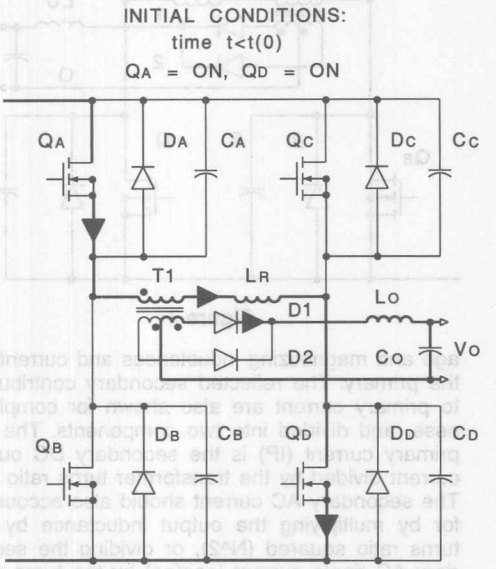


Figure 9

RIGHT LEG RESONANT TRANSITION : INTERVAL: t(0) <t <t(1)

The primary current flowing at time t(0) is equal to Ip(t(0)) and was being conducted through the diagonal set of transistors QA in the upper left hand corner of the bridge and transistor QD in the lower right. Instantly, at time t(0) switch QD is turned off by the control circuitry which begins the resonant transition of the right hand leg of the converter.

The primary current flowing is maintained nearly constant at Ip(t(0)) by the resonant inductance (Lp(res)) of the primary circuit, often referred to as the transformers leakage inductance. Since an external series inductance can be added to alter the effective leakage inductance value, this presentation will refer to the lumped sum of these inductors as the resonant inductance, Lr. In a practical application it may be difficult to accurately control the transformers leakage inductance within an acceptable ZVS range, necessitating an external "shim" inductor to control the accuracy. It's also possible that the transformer leakage inductance can be too low to provide the desired transition times for the application so an external inductor can be introduced to modify the resonant inductance.

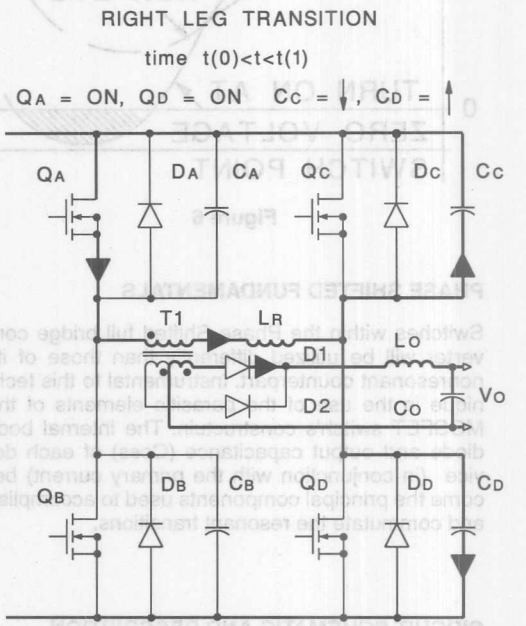


Figure 10

With switch QD turned off, the primary current continues to flow using the switch output capacitance, Coss to provide the path. This charges the switch capacitance of QD from essentially zero volts to the upper voltage rail, Vin+. Simultaneously, the transformer capacitance (Cxfmr) and the output capacitance of switch QC is discharged as its source voltage rises from the lower to the upper rail voltage. This resonant transition positions switch QC with no drain to source voltage prior to turn-on and facilitates lossless, zero voltage switching.

The primary current causing this right leg transition can be approximated by the full load primary current of IP(t(0)). The small change due to the barely resonant circuit contribution is assumed to be negligible in comparison to the magnitude of the full load current.

During this right leg transition the voltage across the transformers primary has decreased fom Vin to zero. At some point in the transition the primary voltage drops below the reflected secondary voltage, Vout*N. When this occurs the primary is no longer supplying full power to the secondary and the output inductor voltage changes polarity. Simultaneously, energy stored in the output choke begins supplementing the decaying primary power until the primary contribution finally reaches zero.

Once the right leg transition has been completed there is no voltage across the transformer primary. Likewise, there is no voltage across the transformers secondary winding and no power transferred, assuming ideal conditions. Note that the resonant transition not only defines the rate of change in primary and secondary voltages dV/dt, but also the rate of change in current in the output filter network, dI/dt.

CLAMPED FREEWHEELING INTERVAL
Time t(1) <t <t(2)

Once the right leg transition is complete the primary current free wheels through transistor QA and the body diode of switch QC. The current would remain constant until the next transition occurs assuming that the components were ideal. Switch QC can be turned on at this time which shunts the body diode with the FET Rds(on) switch impedance thus lowering conduction losses. Although current is flowing opposite to the normal convention (source to drain) the channel of QC will conduct and divide the current between the switch and body diode.

LEFT LEG TRANSITION :
Time t(2) <t <t(3)

At time t(2) a residual current was flowing in the primary of the transformer which is slightly less than IP(t(0)) due to losses. Switch QC has been previously turned ON and switch QA will now be turned OFF. The primary current will continue to

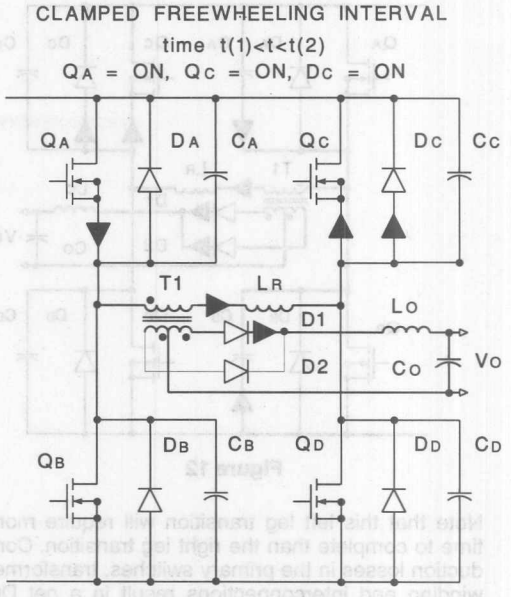


Figure 11

flow but the path has changed to the output capacitance (Coss) of switch QA instead of its channel. The direction of current flowing causes the drain to source voltage of switch QA to increase and lowers its source from the upper to lower rail voltage. Just the opposite conditions have occurred to switch QB which previously had the full input across its terminals. The resonant transition now aligns switch QB with zero voltage across it, enabling lossless switching to occur.

Primary current continues to flow and is clamped by the body diode of switch QB, which is still OFF. This clamping into a short circuit is a necessary condition for fixed frequency, zero voltage switching. Once switch QB is turned ON, the transformer primary is placed across the input supply rails since switch QC is already ON and will begin to transfer power. Although zero voltage switching has already been established, turning ON switch QB the instant it reaches zero voltage will cause variable frequency operation.

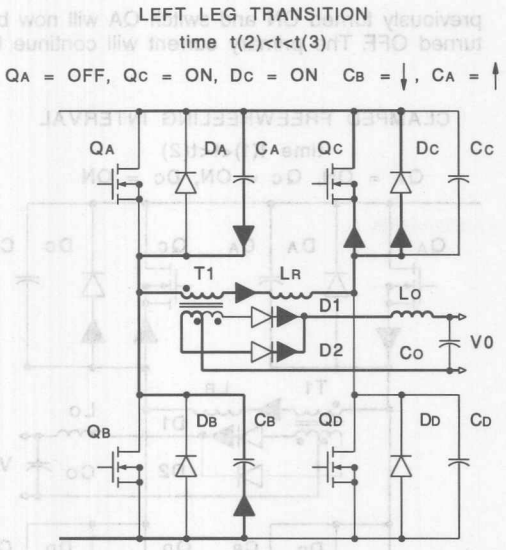


Figure 12

Note that this left leg transition will require more time to complete than the right leg transition. Conduction losses in the primary switches, transformer winding and interconnections result in a net DC voltage drop due to the flowing primary current. Energy stored in the series resonant inductor and magnetizing inductance is no longer ideally clamped to zero voltage. This loss, in addition to the losses incurred during the previous transition, reduce the primary current below its initial (IP(t(0)) value, thus causing a longer left leg transition time than the right leg.

Unlike conventional power conversion, one transistor in the diagonal pair of the phase shifted full bridge converter is ON just before power is transferred which simplifies the gate drive. An additional benefit is realized by designating these commutating switches as the high side switches of the converter, usually far more difficult to drive than their lower side counterparts.

POWER TRANSFER INTERVAL
Time t(3) <t <t(4)

This interval of the phase shifted cycle is basically identical to that of conventional square wave power convesion. Two diagonal switches are ON which applies the full input voltage across the transformer primary. Current rises at a rate determined by Vin and the series primary inductance, however starts at a negative value as opposed to zero. The current will increase to a DC level equal to the output current divided by the turns ratio, Iout/N. The two time variant contributors to primary current are the magnetizing current (Imag) and the output inductor magnetizing contribution reflected to the primary, Lout/N^2. The exact switch ON time is a function of Vin, Vout and N the transformer turns ratio, just as with conventional converters.

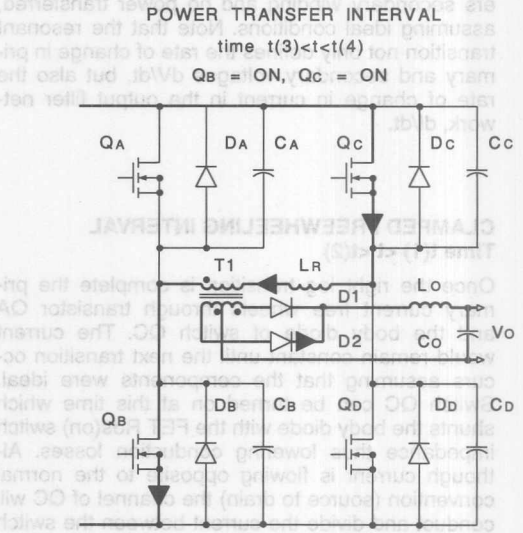


Figure 13

SWITCH TURN OFF; TIME t(4)

One switching cycle is concluded at time t(4) when QC the upper right hand corner switch is turned OFF. Current stops flowing in QC's semiconductor channel but continues through the parasitic output capacitance, Coss. This increases the drain-to-source voltage from essentially zero to the full input supply voltage, Vin. The output capacitance of the lower switch in the left hand leg (QD) is simultaneously discharged via the primary current. Transistor QD is then optimally positioned for zero voltage switching with no drain-to-source voltage.

The current during this interval is assumed to be constant, simplifying the analysis. In actuality, it is slightly resonant as mentioned in the right leg transition, but the amplitude is negligible in comparison to the full load current. The power conversion interval is concluded at this point and an identical analysis occurs as for the opposite diagonal switch set which has thoroughly been described for the switch set QA and QD.

OPERATIONAL WAVE FORMS

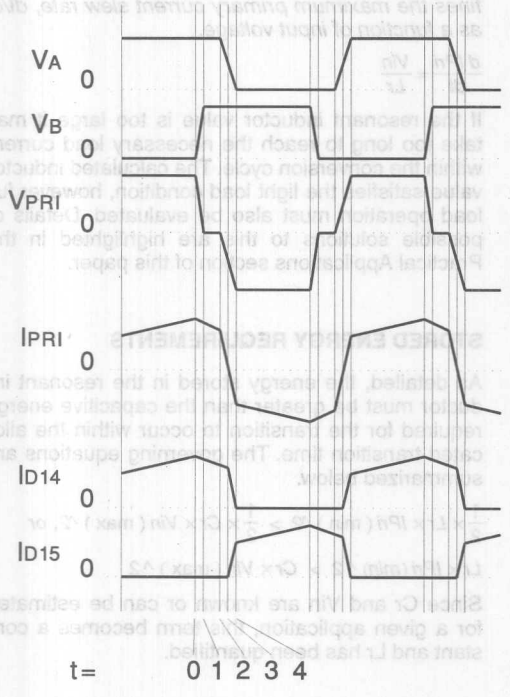


Figure 14

RESONANT TANK CONSIDERATIONS

The design of the resonant tank begins with the selection of an acceptable switching frequency; one selected to meet the required power density. Second, the maximum transition time must also be established based on achievable duty cycles under all operating conditions. Experience may provide the best insight for acceptable results.

The maximum transition time will occur during the converters left leg transition operating at the minimum output load current.

RESONANT CIRCUIT LIMITATIONS

Two conditions must be met by the resonant circuit at light load, and both relate to the energy stored in the resonant inductor. One, there must be enough inductive energy stored to drive the resonant capacitors to the opposite supply rail. Two, this transition must be accomplished within the allocated transition time. Lossy, non-zero voltage switching will result if either, or both are violated. The first condition will always be met when the latter is used as the resonant circuit limitation.

Designers can argue that some switching loss may be of little consequence in a practical application at very light loads - especially considering that there is a significant benefit at heavy loads. While this may be a pragmatic approach in many applications, and a valid concern, this presentation will continue using the fully lossless mode as the ultimate design goal.

The stored inductive energy requirement and specified maximum transition time have also defined the resonant frequency (Wr) of the tank circuit. Elements of this tank are the the resonant inductor (Lr) and capacitor (Cr), formed by the two switch output capacitors, also in parallel with the transformer primary capacitance Cxfmr. The maximum transition time cannot exceed one-fourth of the self resonant period, (four times the self resonant frequency) to satisfy the zero voltage switching condition.

The resonant tank frequency, Wr :

$$Wr = \frac{1}{(Lr \times Cr)\,\hat{}\,0.5}$$

$$t(max)\ transition = \frac{\pi}{2 \times Wr}$$

Coss, the specified MOSFET switch output capacitance will be multiplied by a 4/3 factor to accommodate the increase caused by high voltage operation. During each transition, two switch capacitances are driven in parallel, doubling the total capacitance to 8/3 * Coss. Transformer capacitance (Cxfmr) must also be added as it is **NOT** negligible in many high frequency applications.

The capacitive energy required to complete the transition , W(Cr) is:

$$W(Cr) = \frac{1}{2} \times Cr \times VPri^2$$

This energy can also be expressed as:

$$W(Cr) = [(\frac{4}{3} \times Coss) + Cxfmr] \times Vin^2$$

STORED INDUCTIVE ENERGY

The energy stored in the resonant inductance must be greater than the energy required to charge and discharge the FET output and transformer capacitances of the leg in transition within the maximum transition time.

Inside the transformer, all of the energy is stored in the leakage inductance since the secondary current has clamped the transformers primary voltage to essentially zero. This causes high circulating primary current (as shown in figure 8) in the physical winding but has no effect on the stored energy used to perform the ZVS transition. More detail about the tradeoffs and design optimization is presented in the Design Procedure.

The energy stored in the resonant inductor, Lr:

$$W(Lr) = \frac{1}{2} \times Lr \times Ipri^2$$

RESONANT CIRCUIT SUMMARY

There are several ways to arrive at the solutions for the resonant inductor value and minimum primary current required for any application. Each of these is based upon the following fundamental relationships.

The resonant tank frequency must be at least four times higher than the transition time to fully resonate within the maximum transition time t(max) at light load.

$$Tres = 4 \times t(\max)$$

$$Fres = \frac{1}{T(res)} \quad or$$

$$where \quad Wr = 2 \times \pi \times Fres$$

$$Wr = \frac{2 \times \pi}{T(res)}$$

$$\left[(4 \times t(\max))\right]$$

$$Wr = \frac{\pi}{(2 \times t(\max))}$$

The resonant radian frequency (Wr) is related to the resonant components by the equation:

$$Wr = \frac{1}{(Lr \times Cr)^2}$$

Both sides of this can be squared to simplify the calculations and reorganized to solve for the exact resonant inductor value.

$$Lr = \frac{1}{(Wr^2 \times Cr)}$$

Previously outlined relationships for Wr and Cr can be introduced to result in the following specific equation.

$$Lr = \frac{1}{\left[\frac{\pi}{(2 \times t(\max))}\right]^2 \times \left[(\frac{8}{3} \times Coss) + Cxfmr\right]}$$

Note that this figure indicates the exact resonant inductor value required to satisfy only the task of resonant transitions. This resonant inductor is in series with the transformer primary hence also defines the maximum primary current slew rate, dI/dt as a function of input voltage.

$$\frac{d\,IPri}{dt} = \frac{Vin}{Lr}$$

If the resonant inductor value is too large it may take too long to reach the necessary load current within the conversion cycle. The calculated inductor value satisfies the light load condition, however full load operation must also be evaluated. Details of possible solutions to this are highlighted in the Practical Applications section of this paper.

STORED ENERGY REQUIREMENTS

As detailed, the energy stored in the resonant inductor must be greater than the capacitive energy required for the transition to occur within the allocated transition time. The governing equations are summarized below.

$$\frac{1}{2} \times Lr \times IPri(\min)^2 > \frac{1}{2} \times Cr \times Vin(\max)^2, \; or$$

$$Lr \times IPri(min)^2 > Cr \times Vin(\max)^2$$

Since Cr and Vin are known or can be estimated for a given application, this term becomes a constant and Lr has been quantified.

MINIMUM PRIMARY CURRENT

The minimum primary current required for the phase shifted application can now be determined by reorganizing the previous equation.

$$IPri\,(\min) = \left[\frac{(Cr \times Vin\hat{}2)}{Lr}\right]\hat{}0.5$$

This value can be supported by the calculating the average current required to slew the resonant capacitor to the full rail voltage. Although this figure will be lower that IP(min) it can be used as a confirmation of the mathematics.

$$IR\,(average) = Cr \times \frac{Vin}{t\,(\max)}$$

Obtaining the necessary amount of primary current can be done in several ways. The most direct approach is to simply limit the minimum load current to the appropriate level. One alternative, however, is to design the transformer magnetizing inductance accordingly. Also assisting the magnetizing current is the reflected secondary inductor current contribution which is modeled in parallel. Any duty cycle variations modifying the peak charging current must also be taken into account.

Generally the magnetizing current alone is insufficient in many off-line high frequency converters. The transformer is usually cores loss limited which means numerous primary turns and a high magnetizing inductance. Shunting the transformer primary with an external inductor to develop the right amount of primary current is one possibility. Incorporating the output filter inductor magnetizing current to assist resonance on the primary side is also an alternative.

PHASE SHIFTED PWM CONTROL CIRCUITRY

Probably the most critical control aspect in the phase shifted PWM technique is the ability to span the full 0 to 180 degree phase shift range. Falling short of performance on either end of the spectrum can place unnecessary burdens on the fault protection circuitry or primary switches. Loss of control at either extreme will result in catastrophic consequences by simultaneously turning on both transistors in a given "leg" of the converter. The UC3875 Phase Shifted controller features the required circuitry to deliver both zero and effectively full duty cycle - effortlessly. Additionally, the UC3875 controller is utilized to perform the necessary control, decoding, protection and drive functions for this application. Peak current mode control is implemented for this example although the IC is equally suited for conventional voltage mode control, with or without input voltage feed forward. When used in current mode, the IC accepts a zero to 2.7 volt amplitude maximum current senses input and makes adding slope compensation a simple function.

UC3875 Block Diagram

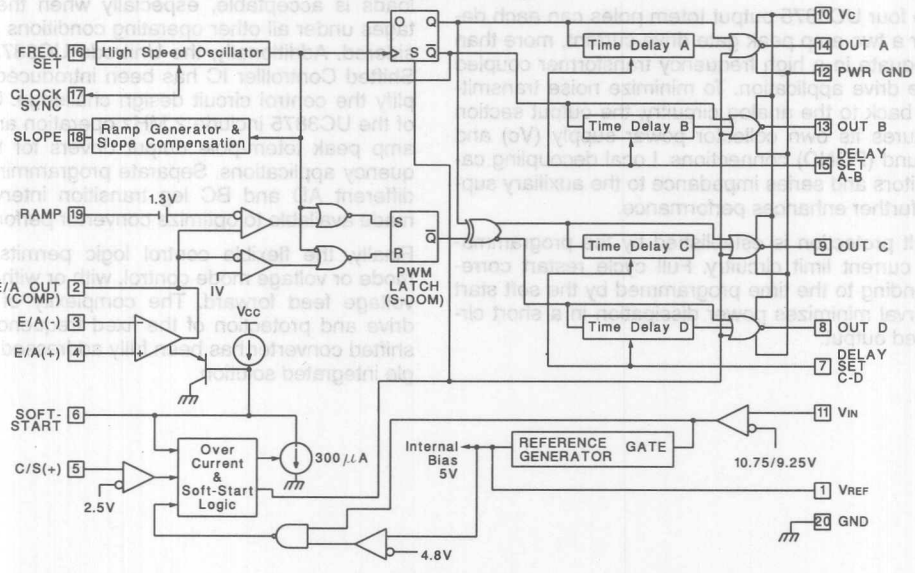


Figure 16

UNITRODE UC3875 PHASE SHIFTED PWM CONTROL IC - BLOCK DIAGRAM

A synchronizable oscillator is programmed by a resistor capacitor network from the frequency set pin to ground. Synchronization is performed by driving the SYNC pin from another UC3875 or external circuitry. The precision 5.0 volt bandgap reference is available to program the noninverting input of the error amplifier as well as optional external functions. Output regulation is achieved using the 7 MHz gain-band width on-board error amplifier which feeds the high speed PWM circuitry. Soft starting is accomplished with a capacitor to ground which gradually increases the error amplifier output, corresponding to pulse width, phase shift or peak current, depending on the exact implementation. This signal is compared to the Ramp input of the IC having a usable input range from zero to 2.7 volts.

Delays between the output drive commands to facilitate Zero Voltage Switching are programmed at the Delay Set inputs. One unique feature of the UC3875 is the ability to separately program the A-B output delays differently from the C-D outputs. This capability accommodates the different primary currents during one switching cycle which cause and result in different resonant transition times between the leading and falling edges. Inability to program each of these durations will generally result in lossy, non-zero voltage switching of the full bridge converters switches under some operating conditions.

The four UC3875 output totem poles can each deliver a two amp peak gate drive current, more than adequate in a high frequency transformer coupled gate drive application. To minimize noise transmitted back to the analog circuitry, the output section features its own collector power supply (Vc) and ground (PGND) connections. Local decoupling capacitors and series impedance to the auxiliary supply further enhances performance.

Fault protection is established by the programmable current limit circuitry. Full cycle restart corresponding to the time programmed by the soft start interval minimizes power dissipation in a short circuited output.

TYPICAL APPLICATION CIRCUIT SCHEMATIC SUMMARY

The fixed frequency phase shifted control technique of the full bridge converter offers numerous performance advantages over the conventional approach. switching losses due to the simultaneous overlapof voltage and current disappear along with the dissipative discharge of the FET output capacitance. EMI/RFI is significantly lower, also due to the "soft" switching characteristics which incorporate parasitic elements of the power stage acvantageously. For most applications, there is little reason to consider the traditional square wave counterpart of theis phase shifted PWM technique for future designs.

Very high frequency operation of this technique, beyond 500 KHz, is probable above the optimal operating point. Transition times quickly erode the usable duty cycle to a point where the transformer turns ratio has been compromised. This could result in unreasonably high primary currents and repower loss in the switches. Any incremental gains in cost or power density by reducting the size of the output filter are probably nullified by the needs for larger MOSFETs and heatsinks. This phase shifted PWM technique does excel in the overall majority of mid to high power, off-line applications. Peak efficiency will be obtained in applications with moderate load ranges, however excellent results can also be obtained in most designs with load ranges of ten-to one. A subgroup of applications may exist where non ZVS operation extremely light loads is acceptable, especially when the advantages under all other operating conditions are considered. Additionally, the Unitrode UC3875 Phase Shifted Controlller IC has been introduced to simplify the control circuit design challenge. Features of the UC3875 include 2 MHz operation and four 2 amp peak totem-pole output drivers for high frequency applications. Separate programming of the different AD and BC leg transition intervals has made available to optimize converter performance.

Finally, the flexible control logic permits current mode or voltage mode control, with or without input voltage feed forward. The complexity of control, drive and protection of the fixed frequency phase shifted converter has been fully addressed in a single integrated solution.



UC3875 Phase Shifted PWM Converter Control and Output Circuit Schematic

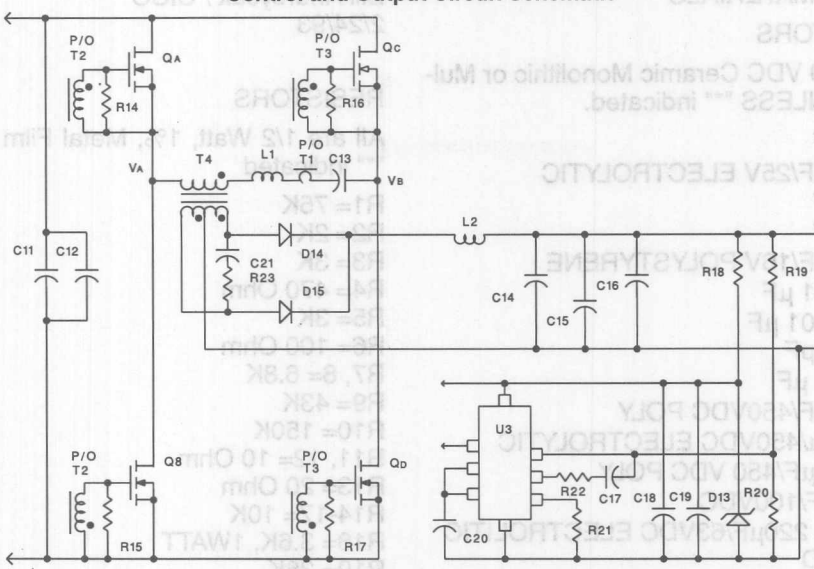


Figure 17

UC 3875 Phase Shifted PWM Converter Control and Drive Circuit Schematic

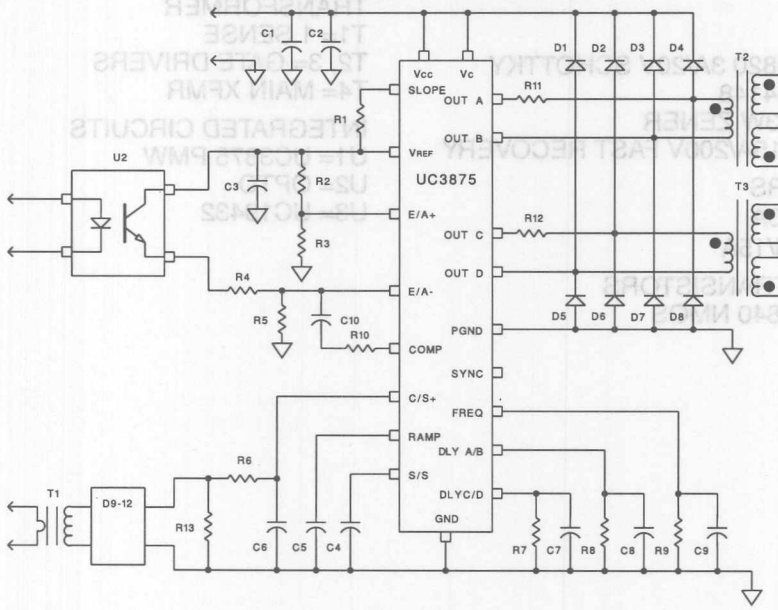


Figure 18

2/24/93

CAPACITORS

All are 20 VDC Ceramic Monolithic or Multilayer UNLESS "*" indicated.

C1= 1 µF
C2= 47 µF/25V ELECTROLYTIC
C3= 1 µF
C4= 1 µF
C5= 75 pF/16V POLYSTYRENE
C6= 0.001 µF
C7, 8= 0.01 µF
C9= 470 pF
C10= 0.1 µF
C11= 1 µF/450VDC POLY
C12= 47µ/450VDC ELECTROLYTIC
C13= 1.2µF/450 VDC POLY
C14= 1µF/100VDC
C15, 16= 220µF/63VDC ELECTROLITIC
C17= TBD
C18= 1µF
C19= 22 µF/25VDC ELECTROLITIC
C20= 1 µF
C21= 2.7 nF/200V POLY/low ESL&ESR

DIODES
D1-8= 1N5820 3A/20V SCHOTTKY
D9-12= 1N4148
D13= 12V 3W ZENER
D14, 15= 15A/200V FAST RECOVERY

INDUCTORS
L1= 47µH/3A
L2= 100µH/15A

MOSFET TRANSISTORS
QA-D=IRF840 NMOS

RESISTORS

All are 1/2 Watt, 1%, Metal Film UNLESS "*" indicated

R1= 75K
R2= 2K
R3= 3K
R4= 470 Ohm
R5= 3K
R6= 100 Ohm
R7, 8= 6.8K
R9= 43K
R10= 150K
R11, 12= 10 Ohm
R13= 20 Ohm
R14-17= 10K
R18= 3.6K, 1WATT
R19= 36K
R20= 1K
R21= TBD
R22= TBD
R23= 110 Ohms/5W Carbon

TRANSFORMER
T1= 1 SENSE
T2, 3= GATE DRIVERS
T4= MAIN XFMR

INTEGRATED CIRCUITS
U1= UC3875 PMW
U2= OPTO
U3= UC19432

One Switching Cycle

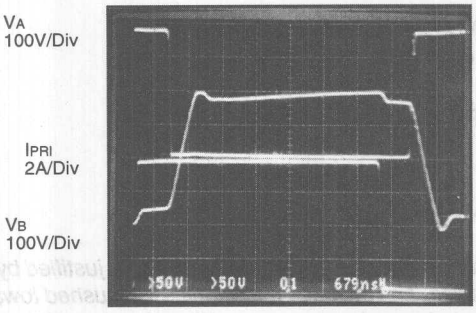


Figure 19

Primary Waveforms

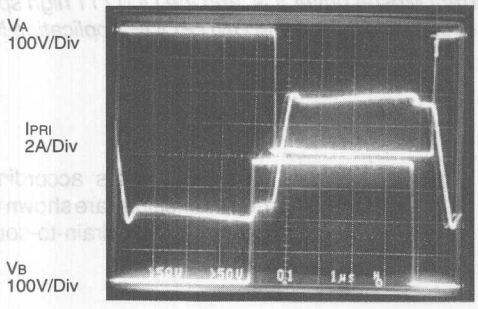


Figure 20

Secondary Waveforms

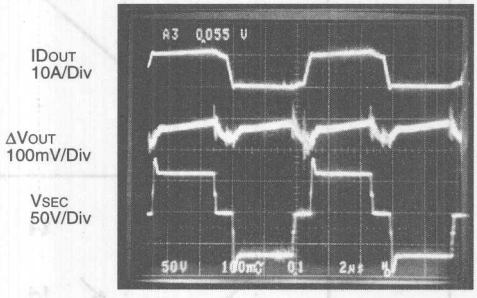


Figure 21

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APPLICATION NOTE

PRACTICAL CONSIDERATIONS IN HIGH PERFORMANCE MOSFET, IGBT and MCT GATE DRIVE CIRCUITS

BILL ANDREYCAK

INTRODUCTION

The switchmode power supply industry's trend towards higher conversion frequencies is justified by the dramatic improvement in obtaining higher power densities. And as these frequencies are pushed towards and beyond one megahertz, the Mosfet transition periods can become a significant portion of the total switching period. Losses associated with the overlap of switch voltage and current not only degrade the overall power supply efficiency, but warrant consideration from both a thermal and packaging standpoint. Although brief, each of the Mosfet switching transitions can be further reduced if driven from from a high speed, high current totem-pole driver - one designed exclusively for this application. This paper will highlight three such devices; the UC1708 and UC1710 high current Mosfet driver ICs, and the UC1711 high speed driver. Other Mosfet driver ICs and typical application circuits are featured in UNITRODE Application Note U-118.

EFFECTIVE GATE CAPACITANCE

The Mosfet input capacitance (Ciss) is frequently misused as the load represented by a power mosfet to the gate driver IC. In reality, the effective input capacitance of a Mosfet (Ceff) is much higher, and must be derived from the manufacturers' published total gate charge (Qg) information. Even the specified maximum values of the gate charge parameter do not accurately reflect the driver's instantaneous loads during a given switching transition. Fortunately, FET manufacturers provide a curve for the gate-to-source voltage (Vgs) versus total gate charge in their datasheets. This will be segmented into four time intervals of interest per switching transition. Each ofthese will be analyzed to determine the effective gate capacitance and driver requirements for optimal performance.

Inadequate gate drive is generally the result of underestimating the effective load of a power mosfet to its driver.

TOTAL GATE CHARGE (Qg)

First, a typical high power Mosfet "Gate Charge versus Gate-to-Source Voltage" curve will be examined. An IRFP460 device has been selected and this curve is applicable to most other Fet devices by adjusting the gate charge numbers accordingly. Both turn-on and turn-off trasnsitions are shown with the respective drain currents and drain-to-source voltages.

TURN-ON WAVEFORMS
Gate voltage vs time

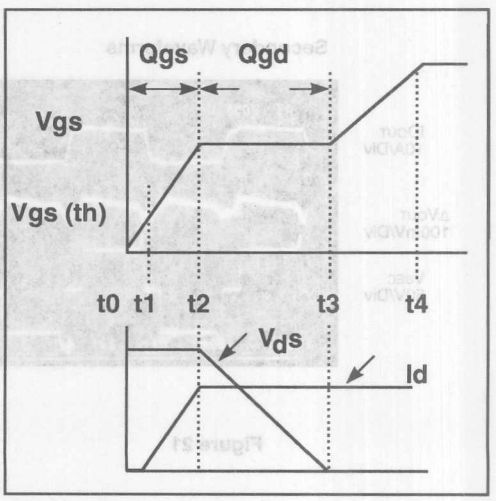


Figure 1.

INTERVAL t0-t1

The time required to bring the gate voltage from zero to its threshold Vgs(th) can be expressed as a delay time. Both the voltage across the switching device and current through it are uneffected during this interval.

INTERVAL t1-t2

This period starts at time t1 when the gate voltage has reached Vgs(th) and drain current begins to flow. Current continues to rise until essentially reaching its final value at time t2. While this occured, the gate to source voltage had also been increasing. The drain-to-source voltage remains unchanged at Vds(off). Power in the Mosfet is wasted by the simultaneous overlap of voltage and current.

INTERVAL t2-t3

Beginning at time t2 the drain-to-source voltage starts to fall which introduces the "Miller" capacitance effects (Cgd) from the drain to the Mosfet gate. The result is the noticeable plateau in the gate voltage waveform from time t2 until t3 while a charge equal to Qgd is admitted. It is here that most drive circuits are taxed to their limits. The interval concludes at time t3 when the drain voltage approaches its minimum.

INTERVAL t3-t4

During this final interval of interest the gate voltage rises from the plateau of the prior region up to its final drive voltage. This increasing gate voltage decreases Rds(on), the Mosfet drain-to-source resistance. Bringing the gate voltage above 10 to 12 volts, however, has little effect on further reducing Rds(on).

SUMMARY OF INTERVAL WAVEFORMS AND DRIVER LIMITATIONS

INTERVAL	Vgs(t)	ID(t)	Vds(t)	DRIVER LIMITATIONS
t0-t1	0-threshold	0	Vds(off)	Slew rate (dv/dt)
t1-t2	thrs-plateau	rising	Vds(off)	Slew rate (dv/dt)
t2-t3	V(plateau)	Ion(dc)	falling	Peak current I(max)
t3-t4	rising	Ion(dc)	Ion*Rds(t)	Peak I & dv/dt

TURN-OFF WAVEFORMS

Gate voltage vs time

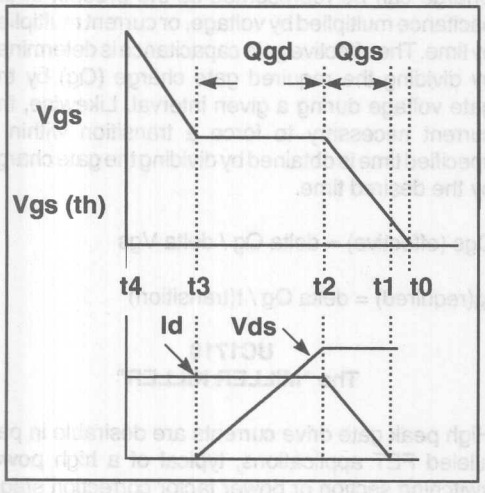


Figure 2

The intervals during turn-off are basically the same as those described for turn-on, however the sequence and corresponding waveforms are reversed.

INTERVAL t4-t3

The beginning of the turn-off cycle can be described as a delay from the final drive voltage (Vgs(on)) the the plateau region. Both the drain voltage and current waveforms remain unchanged while the devices effective resistance (Rds(on)) increases as the gate voltage decreases.

INTERVAL t3-t2

Once the plateau is reached at time t3, the gate voltage remains constant until time t2. Gate charge due to the Miller effect is being removed, an amount equal to Qgd. The drain voltage rises to its off state amplitude, Vds(off), while the drain current continues to flow and equals I(on). This lossy transition ends at time t2.

INTERVAL t2-t1

Once the Miller charge is completely removed, the gate voltage is reduced from the plateau to the threshold voltage causing the drain current to fall from I(on) to zero. Transition power loss ends at time t1 when the gate threshold is crossed.

INTERVAL t1-t0

This brief period is of little interest in the turn-off sequence since the device is off at time t1.

SUMMARY OF INTERVAL WAVEFORMS AND DRIVER LIMITATIONS

INTERVAL	Vgs(t)	ID(t)	Vds(t)	DRIVER LIMITATIONS
t4-t3	falling	Ion(dc)	Ion* Rds(t)	Peak I and dv/dt
t3-t2	V(plateau)	Ion(dc)	falling	Peak Current I (max)
t2-t1	Vplat-thrsh	falling	Vds(off)	Slew rate (dv/dt)
t1-t0	thrsh-0	0	Vds(off)	Slew rate (dv/dt)

FET Transition Power Loss

During each of the FET turn-on and turn-off sequences power is lost due to the switching device's simultaneous overlap of drain - source voltage and drain current. Since both the FET voltage and current are externally controlled by the application, the driver IC can only reduce the power losses by making the transition times as brief as possible. Minimization of these losses simply requires a competant driver IC, one able to provide high peak currents with high voltage slew rates.

A review of the prior transition waveforms indicates that power is lost between the times of t1 and t3. While t2 serves as the pivot point for which waveform is rising or falling, as the equations show its irrelavent in the power loss equation. For the purpose of brevity, the waveform of interest can be approximated as a triangle while the other waveform is constant. The duration between times t1 and t3 can now be defined as the net transition time, t(tran), with a conversion period of t(period)

During the two intervals from t1 to t3:

$$Ploss = \frac{0.5 * I(on) * Vds(off) * t(2\text{-}1)}{t(period)}$$

$$Ploss = \frac{0.5 * Vds(off) * I(on) * t(3\text{-}2)}{t(period)}$$

Combininig the two equations with t(tran) = t3-1 results in a net loss of :

$$Ploss = \frac{0.5 * Vds(off) * I(on) * t(trans)}{t(period)}$$

Since these loses are incurred twice percycle, first at turn-on and then again at turn-off, the net result is a doubling of the power loss.

Ploss = Vds(off)*I(on)*t(trans)/t(period)

This relationship displays the need for fast transitions at any switching frequency, and is of significant concern at one megaHertz. Minimization of the FET transition power loss can be achieved with high current drivers.

GATE CHARGE

Each division of the transition interval has an associated gate charge which can be derived from the FET manufacturers datasheets. Since there are three basic shapes to the Vgs curve, the interval from t0 to t1 can be lumped together with that of the t1 to t2 period. For most large FET geometries, the amount of charge in the t0 to - t1 span is negligible anyway. This simplification allows an easy calculation of the effective gate capacitance for each interval along with quantifying the peak current required to traverse in a given amount of time.

Charge can be represented as the product of capacitance multiplied by voltage, or current multiplied by time. The effective gate capacitance is determined by dividing the required gate charge (Qg) by the gate voltage during a given interval. Likewise, the current necessary to force a transition within a specified time is obtained by dividing the gate charge by the desired time.

Cgs (effective) = delta Qg / delta Vgs

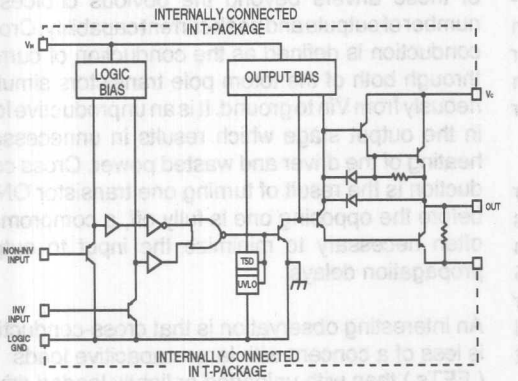
Ig(required) = delta Qg / t(transition)

UC1710
The "MILLER KILLER"

High peak gate drive currents are desirable in paralleled FET applications, typical of a high power switching section or power factor correction stage. Dubbed as "the Miller Killer", the UC1710 boasts a guaranteed 6 amp peak output current. This hefty driver current minimizes the FET parasitic "Miller" effects which would otherwise result in poor transi-

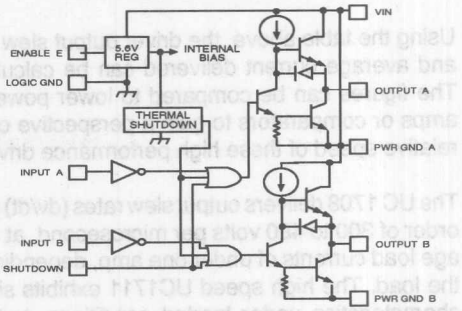
tion performance. Higher currents are possible with this driver, however the limiting factor soon becomes the parasitic series inductance of the FET package (15 nH) and the layout interconnection of 20 nH/inch. An RF type arrangement of the PC board layout is an absloute **MUST** to realize this device's full potential.

UC 1710 BLOCK DIAGRAM



The UC1710 has "no-load" rise and fall times of 20 nanoseconds (or less) which do not change significantly with any loads under 3 nanoFarads. It's also specified into a load capacitance of 30 nanoFarads, roughly equivalent to what is represented by three paralleled "size 6" FET devices. Propagation delays are brief with typical values specified at 35 nanoseconds from either input to a ten percent change in output voltage.

UC 1708 BLOCK DIAGRAM



The UC1708 is a unique blend of the high speed attributes of the UC1711 along with the higher peak current capability of the UC1710. This dual noninverting driver accepts positive TTL/CMOS logic from control circuits and provides 3 amp peak outputs from each totem pole.

Propagation delays are under 25 nanoseconds while rise and fall times typically run 35 nonoseconds into 2.2 nanofarads. The output stage design is a "no float" version which incorporates a self biasing technique to hold the outputs low during undervoltage lockout, even with Vin removed.

In the 16 pin DIL package, the device features a remote ENABLE and SHUTDOWN function in addition to seperate signal and power grounds. The ENABLE function places the device in a low current standby mode and the SHUTDOWN circuitry is high speed logic directly to the outputs.

UC1708 / 1710 / 1711 PERFORMANCE COMPARISON
TABLE 1.

PARAMETER	LOAD	UC1708	UC1710	UC1711
Propagation Delay	0	25	30	10
t(plh)	1.0 nF	25	-	15
input to 10% output	2.2 nF	25	30	20
	30 nF	-	30	-
Raise time	0	25	20	12
t(tlh)	1.0 nF	30	-	25
10% to 90% rise	2.2 nF	40	25	40
	30 nF	-	85	-
Propagation Delay	0	25	30	3
t(phl)	1.0 nF	25	-	5
input to 90% output	2.2 nF	25	30	
	30 nF	-	30	-
Fall Time	0	25	15	7
t(thl)	1.0 nF	30	-	25
90% to 10% fall	2.2 nF	40	20	40
	30 nF	-	85	-

TRANSITION PERFORMANCE

Using the table above, the driver output slew rates and average current delivered can be calculated. The figures can be compared to lower power op-amps or comparators to gain a perspective on the relative speed of these high performance drivers.

The UC 1708 delivers output slew rates (dv/dt) in the order of 300 to 480 volts per microsecond, at average load currents of under one amp, depending on the load. The high speed UC1711 exhibits similar characteristics under loaded conditions, but can achieve a no load slew rate of over 1700 volts per microsecond - nearly 2 volts per nanosecond.

For higher power applications, the UC1710 "Miller Killer" will produce an average current of 4.5 amps AT slew rates of 150 volts per microsecond. With lighter loads it will deliver an average current of 1.5 amps at a slew rate of approximately 500 volts per microsecond. In most applications, the UC1710 will easily outperform "homebrew" discrete mosfet transistor totempole drive techniques.

Each device in this new generation of MOSFET drivers is significantly more responsive than the earlier counterparts for a given application - whether it's higher speed (UC1711), higher peak current (UC1710) or a combination of both (UC1708).

DRIVER CONSIDERATIONS

As previously demonstrated, the ideal MOSFET gate drive IC is a unique blend of both high speed switching and high peak current capability. Initially, the high speed is required to bring the gate voltage from zero to the plateau, but the current is low. Once the plateau is intersected, the driver voltage is fairly constant, and the IC must switch modes. Instantly, the driver current snaps to its maximum as charge is injected to overcome the FET's Miller effects. Finally, a combination of both high slew rate and high current is needed to complete the gate drive cycle.

At turn-off this sequence is reversed, first demanding both high slew rate and high current simultaneously. This is followed by the plateau region which is limited only by the maximum driver current. Finally, there is high speed discharge of the gate to zero volts.

Optimization of a driver for this type of application can be difficult. In general, the MOSFET driver IC output stage is designed to switch as fast as the manufacturer's process will allow.

CROSS CONDUCTION

There are numerous tradeoffs involved in the design of these drivers beyond the obvious choices of number of outputs and peak current capability. Cross-conduction is defined as the conduction of current through both of the totem pole transistors simultaneously from Vin to ground. It is an unproductive loss in the output stage which results in unnecessary heating of the driver and wasted power. Cross conduction is the result of turning one transistor ON before the opposing one is fully off, a compromise often necessary to minimize the input to output propagation delays.

An interesting observation is that cross-conduction is less of a concern with large capacitive loads (FETs) than with unloaded or lightly loaded driver outputs. Any capacitive load will reduce the slew of the output stage, slowing down its dv/dt. This causes a portion of the cross conduction current to flow from the load, rather than from the input supply through the driver's opposite output transistor. The power loss associated with a drivers inherent cross-conduction is unchanged with large capacitive loads, however it is not caused by a "shoot-through" of supply current.

DRIVER PERFORMANCE

There are a variety of applications for MOSFET drivers - each with its own unique set of speed and peak current requirements. Most general purpose drivers feature 1.5 amp peak totem-pole outputs which deliver rise and fall times of approximately 40 nanoseconds into 1 nanoFarad. Propagation delays are in the neighborhood of 40 to 50 nanoseconds, making these devices quite adaptable to numerous power supply and motor control applications. These specifications can be used for a comparison to those of a new series of higher speed and higher current devices, specifically, the UC1708, UC1710 and the UC1711 power MOSFET drivers. Each member in this group of "third" generation driver ICs features significant performance improvements over their predecessors with one parameter optimized for a specific set of applications.

MOSFET DRIVER IC FEATURE AND PERFORMANCE OVERVIEW
TABLE 2.

Feature	UC1708	UC1710	UC1711
Number of outputs	2	1	2
Peak output current (per output)	3 A	6 A	1.5 A
Noninverting input-output logic	YES	YES	
Inverting input-output logic		YES	YES
Maximum supply voltage Vcc	35V	20V	40V
Typical supply current Icc (1.)	16ma	30ma	17ma
Remote Enable	YES		
Shutdown Input	YES	YES (2)	
Seperate grounds, signal and power	YES (3)	YES (3)	
Seperate Vin and Vc pins		YES (3)	
8 pin DIL package	YES	YES	YES
16 pin DIL package	YES	YES	YES
5 pin TO-220 package		YES	

Note 1. Typical Vc plus Vcc current measured at 200KHZ, 50 % duty cycle and no load
Note 2. Using the device's other input
Note 3. Package dependant

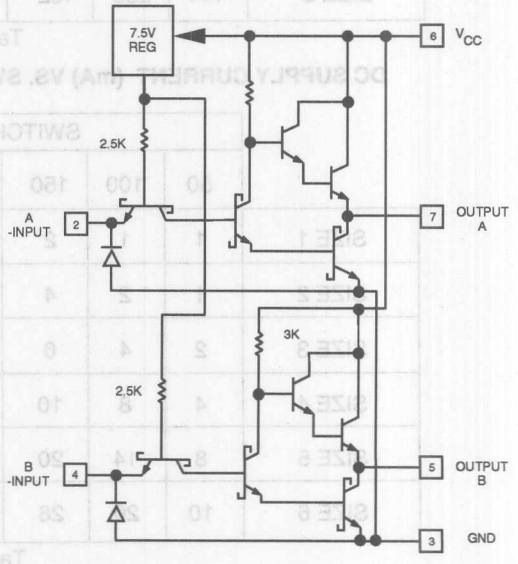
PROPAGATION DELAYS

The power supply industry's trend towards higher power densities has thrust switching frequencies well beyond one megaHertz in many low to medium power systems. With a one microsecond total conversion period, or less, the FET switching transitions should be in the order of low tens of nanoseconds to yield high efficiency. Additionally, the propagation delays from the driver input to output should be around ten nanoseconds for quick response.

UC1711

The UC1711 device features typical propagation delays of three and ten nanoseconds at no load, depending on the transition. Coupled with dual 1.5 amp peak totem-pole outputs, this device is optimized for high frequency FET drive applications. Its all NPN Schottky transistor construction is not only fast, but radiation tolerant as well.

UC1711 BLOCK DIAGRAM



GATE DRIVE POWER CONSIDERATIONS

Perhaps the most popular misconception in the power supply industry is that a FET gates require NO power from the auxiliary supply - that both turn-on and turn-off are miraculously power free. Another fallacy is that the driver consumes all the measured supply current, Icc, and none of it is used to transition the gates. Obviously, both of these statements are false.

In reality, the power required by the gate itself can be quite substantial in high frequency applications. Calculation of this begins by listing the specified total gate charge for the FET device, Qg.

The gate power utilized in charging and discharging a capacitor at frequency "F" is:

$$P(cap) = C * V^2 * F$$

Substituting the gate charge for capacitance multiplied by voltage (Q=C*V) in this equation results in:

$$P(gate) = Qg * V * F$$

The gate power required verses FET size and switching frequencies is tabulated for some common applications in Table 3. Table 4. transforms this power into driver input current at a nominal 12 volt bias.

GATE POWER (mW) VS. SWITCHING FREQUENCY AND FET SIZE

FET SIZE	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	10	18	28	36	46	90	136	180
SIZE 2	16	30	46	60	76	153	226	300
SIZE 3	28	54	82	108	136	275	406	504
SIZE 4	48	96	144	192	240	480	720	960
SIZE 5	100	200	300	400	550	1W	1.5W	2W
SIZE 6	144	288	432	576	720	1.4W	2W	>2W

Table 3.

DC SUPPLY CURRENT (mA) VS. SWITCHING FREQUENCY AND FET SIZE

	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	1	1	2	4	5	6	10	12
SIZE 2	1	2	4	5	6	10	16	20
SIZE 3	2	4	6	8	10	16	26	36
SIZE 4	4	8	10	12	16	32	48	64
SIZE 5	8	14	20	26	32	66	100	130
SIZE 6	10	20	28	38	48	96	144	190

Table 4.

The driver output stage can be modelled as a resistance to the respective auxiliary supply rail driving an ideal FET capacitor. All of the power used to charge and discharge the MOSFET gate capacitor is completely transferred into heat by the driver. This gate power loss adds to the driver's own power loss - resulting in a net driver power dissipation equal to it's input voltage, Vcc, multiplied by the sum of the gate and driver currents, Ig + Icc. This can be calculated or determined empirically by measuring the driver DC input voltage and current.

THERMAL CONSIDERATIONS

Proper IC package selection and/or device heatsinking is the only method available to insure a safe operating junction temperature, tj. All IC's are specified and graded for various junction temperature ranges, and priced accordingly. As a precaution, it should be noted that using a device outside its tested temperature range can result in poor performance, parameters which run outside their specifications, and quite possibly - no operation at all.

JUNCTION TEMPERATURE

The junction temperature of the driver IC is obtained by first calculating the device's thermal rise above the ambient temperature. This is obtained by multiplying the average input power (Vin*Iin) by the device's thermal impedance to air, theta JA (Oja). This term is then added to the ambient temperature to yield the resulting junction temperature, Tj.

If the driver is thermally attached to a heatsink or "cold plate", then the thermal impedance from the device junction to it's package case, theta JC (Ojc), is used to determine the thermal rise. Likewise, this thermal rise is added to the heatsink temperature to determine the junction temperature. In either case, the maximum junction temperature (tj(max)) should be determined and checked against the device's absolute maximum specification.

Average supply currents for each of the three drivers of interest varies primarily with the switching frequency. Rather than listing each driver independantly, an rough approximation of 25 milliamps will be used as the driver current, regardless of the specific device utilized and switching frequency. In addition, a typical supply voltage of 12 volts results in a power dissipation by the driver itself of 300 milliwatts.

The calculated gate power of Table 5. has been added to the estimated 300mW of device power to formulate Table 6. - the driver total power dissipation. This is of particular interest in selecting a driver package (8 pin, TO-220, etc) and heatsink determination for a specific maximum junction temperature, or rise. Typical junction temperature rises vs. frequency and FET size for a IC package, and recommendations are shown in table 7.

AVERAGE POWER DISSIPATION (mW) VS. FREQUENCY AND FET SIZE

FET SIZE	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	310	318	3 28	336	346	390	436	480
SIZE 2	316	330	346	360	376	452	526	600
SIZE 3	328	354	382	408	436	570	706	840
SIZE 4	348	396	444	492	540	780	1.0W	1.3W
SIZE 5	400	500	600	700	800	900	1.7W	2.4W
SIZE 6	444	588	732	876	1.0W	1.7W	2.5W	3.1W

Table 5.

PACKAGE RECOMMENDATIONS

	SWITCHING FREQUENCY (kHz)							
	50	100	150	200	250	500	750	1MEG
SIZE 1	A	A	B	B	B	C	D	D
SIZE 2	A	B	B	B	C	D	D	D
SIZE 3	B	B	C	D	D	D	E	F
SIZE 4	B	C	D	D	D	F	F	F
SIZE 5	C	D	D	E	F	F	F	F
SIZE 6	D	D	E	F	F	F	F	F

For P(diss) = or < 500mW
A: 8 pin DIL, <40 C rise
B: 8 pin DIL, <45 C rise
C: 8 pin DIL, <50 C rise

For P(diss) = or > 500mW (using heatsink)
D: 8 pin DIL, <40 C rise
E: 8 pin DIL, <50 C rise

For P (diss) > 500mW
F: TO-220 recommended

Table 6.

HIGH POWER APPLICATIONS

Most high power applications require the use of "monster" MOSFETs or several large FETs in parallel for each switch. Generally, these are low to medium frequency applications (less than 200kHz) where obtaining a low Rds(on) is of primary concern to minimize the DC switch loss. It is not uncommon to find two, three and even four large devices used in parallel, although some of these combinations are unlikely from a cost versus performance standpoint.

Table seven displays the individual FET device characteristics and several popular parallel arrangements. Listed in descending order is Rds (on) at room temperature and the total gate charge required. This will ultimately be used to determine the gate drive current in Table 8., total power dissipation in Table 9., and driver IC recommendation in Table 10 for various applications.

PARALLELED MOSFET CHARACTERISTICS - TABLE 7.

MOSFET ARRANGEMENT	Rds (on) effective	Qg (nC) total	MOSFET ARRANGEMENT	Rds (on) effective	Qg (nC) total
1 X SIZE 4	0.85	63	2 X SIZE 5	0.200	260
1 X SIZE 5	0.40	130	2 X SIZE 6	0.135	380
1 X SIZE 6	0.27	190	3 X SIZE 5 (1)	0.133	390
2 X SIZE 4 (1)	0.425	126	4 X SIZE 5 (1)	0.100	520
3 X SIZE 4 (1)	0.283	189	3 X SIZE 6 (2)	0.090	570
4 X SIZE 4 (1)	0.213	252	4 X SIZE 6 (2)	0.068	760

1. Consider another selection 2. Consider a "Monster" FET

AVERAGE SUPPLY CURRENT (mA) VS. FREQUENCY AND FET SELECTION

FET ARRANGEMENT	Rds mohm	SWITCHING FREQUENCY (kHz)					
		25	50	75	100	150	200
2 X SIZE 5	200	31	39	45	51	65	77
2 X SIZE 6	135	35	45	53	63	83	101
3 X SIZE 6	90	39	53	69	73	91	139
4 X SIZE 6	68	45	63	82	101	139	177

*Includes 25mA of driver supply current

Table 8

POWER DISSIPATION (mW) VS. FREQUENCY AND APPLICATION

FET ARRANGEMENT	Rds mohm	SWITCHING FREQUENCY (kHz) 25	50	75	100	150	200
2 X SIZE 5	200	372	468	540	612	780	924
2 X SIZE 6	135	420	540	636	756	1.0W	1.2W
3 X SIZE 6	90	468	636	828	876	1.1W	1.7W
4 X SIZE 6	68	540	756	984	1.2W	1.7W	2.1W

* Includes 300mW of driver dissipation

Table 9.

DRIVER IC AND PACKAGE SELECTION GUIDE

Selection Guide for < 50 C rise

A: 8 pin DIL or 20 pin PLCC
B: 8 pin DIL with heatsink. or TO-220.
C: TO-220 with heatsink

FET ARRANGEMENT	Rds mohm	SWITCHING FREQUENCY (kHz) 25	50	75	100	150	200
2 X SIZE 5	200	A	B	C	C	C	C
2 X SIZE 6	135	B	C	C	C	C	C
3 X SIZE 6	90	B	C	C	C	C	C
4 X SIZE 6	68	C	C	C	C	C	C

Table 10.

UC1710 DRIVER PERFORMANCE

Although capacitive in nature, the FET "Miller" effects and demands on the driver differ significantly than a true capacitor load as previously described.

Table 11. shows the typical response of the UC1710 "Miller Killer" driving a single APT5025BN (size 6) device and paralleled MOSFET combinations for reference.

UC1710 RISE, FALL AND DELAY TIMES VS. LOADS

TEST CONDITIONS		Tp LH	Tt LH	Tp HL	Tt HL	Tp +Tt LH	Tt +Tp HL
NO LOAD	VDS	28	12	36	12	40	50
ONE	0	28	26	38	30	54	68
APT5025	350	28	35	40	30	63	70
TWO	0	28	38	40	36	66	76
APT5025	350	28	48	42	38	76	80
THREE	0	28	48	42	48	76	90
APT5025	350	28	60	44	58	88	92

Table 11.

PERFORMANCE COMPARISONS

"HOMEBREW" TOTEM-POLES VS INTEGRATED CIRCUIT DRIVERS

The prior lack of "off-the-shelf" high current or high speed drivers had prompted many to design their own gate drive circuits. Traditionally, an NPN-PNP emitter follower arrangement had been used in lower frequency applications as shown in Figure 7.

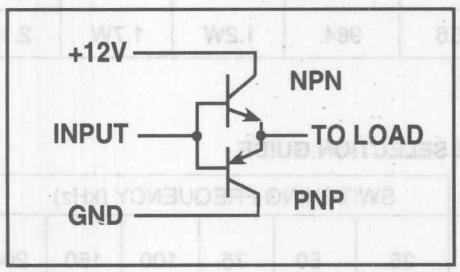


Figure 7

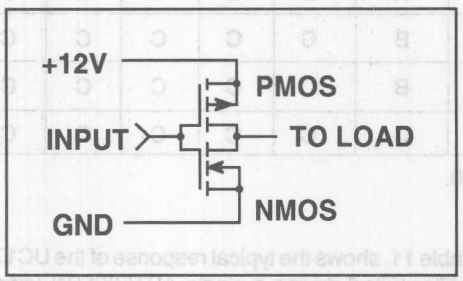


Figure 8

For higher speed applications, a P and N channel FET pair can be used as shown in figure 8. The circuit is configured with the P channel MOS as the upper side switch to simplify the auxiliary bias. Otherwise, a gate drive potential of ten volts above the auxiliary bias would required.

Unfortunately, this configuration has a few drawbacks. First, it leads to an inverting logic flow from the driver input to its output, complicating matters especially during power-up and power-down sequences. Without a clever undervoltage lockout circuit the main power switch will tend to be ON as the auxiliary supply voltage is raised or lowered while the PWM is OFF.

Cross conduction of both FETs is unavoidable with this configuration due to the difference between the gate threshold voltages of each device. Both P and N channel devices are cross conducting while their input drive waveform is above Vgs(th) of the N device and below that of the P device. One technique to minimize the cross conduction peak current is to add some resistance between the FETs. While this does minimize the "shoot-through" current, it also limits the peak current available to the load. This somewhat defeats the purpose of using the MOSFETs in the first place to deliver high currents. The resistor serves an additional purpose of damping the gate drive oscillations during the transitions. In a practical application, two resistors can be used in the place of one with the center-tap connecting to the FET gate,or load as shown in figure 9.

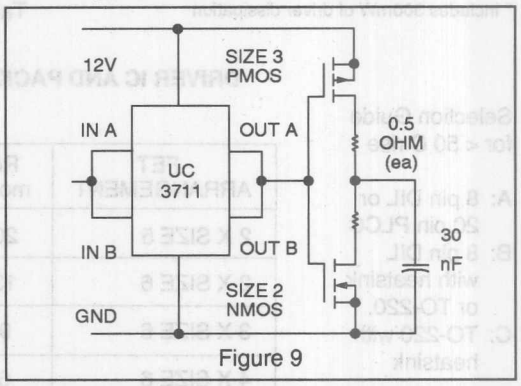
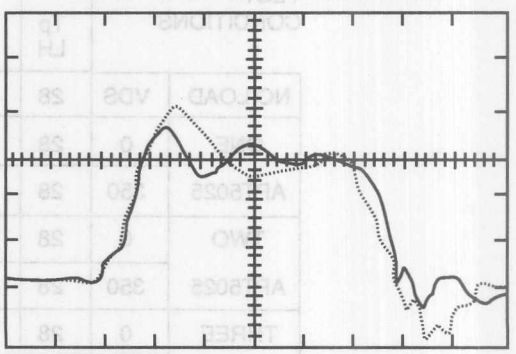


Figure 9

The performance of the circuit in figure 9 was evaluated and compared to that of the UC1710 driver into a 30 nanoFarad load. A size three P type FET and a size two N channel device were connected in series with two one-half ohm resistors to limit the shoot-through current. These FETs were driven from the UC1711 dual driver which can deliver 3 Amp peak gate drive currents for rapid transitions. The results of this test are shown in figure 10.

Driver Performance into 30nF load

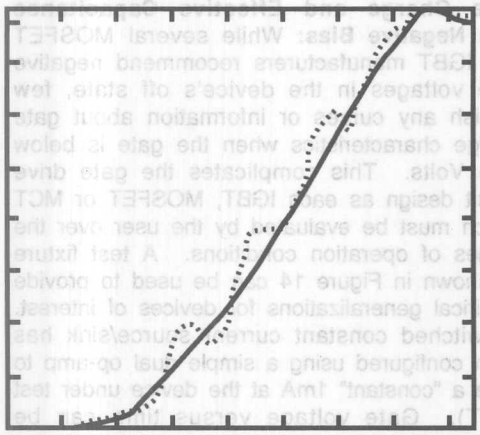


Lines: solid=UC3710, dashed=discrete
Figure 10. - VERT: 5V/DIV: HORIZ: 50 nS/DIV

The test results indicate very similar performance into this load from either technique. Obviously, the "homebrew" approach utilizes a total of three devices in comparison to a single UC1710 driver to obtain essentially the same high speed performance. Additionally, the cost of the P channel FET alone may exceed the price of the UC1710 device, not to mention the difference in PC board real estate. As a final note, the discrete FET approach required over 10 milliamps more supply current than the single UC1710 driver or a increase in supply current of twenty percent. Results of this test shown in figures 11 and 12.

RISE AND FALL TRANSITION PERFORMANCE INTO 30 nF

RISE TIMES (Fig 11.)



FALL TIMES (Fig 12.)

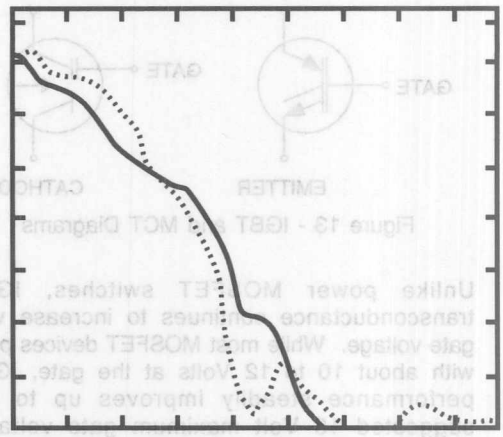


PHOTO SCALES (BOTH): VERT=2V/DIV, HORIZ=10 nS/DIV
LINES: SOLID = UC3710; DASHED = DISCRETE CIRCUIT OF FIGURE 9.

POWER DEVICES

IGBTs and MCTs: While existing generations of power MOSFETs continue to be enchanced for lower RDS(on) and faster recovery internal diodes, alternative new devices have also been introduced. Among the most popular, and viable for high voltage high power applications are IGBTs (Insulated Gate Bipolar transistors) and MCTs (MOS Controlled Thyristors). Although frequently drawn as an NPN structure, the IGBT actually resembles a PNP bipolar transistor with an internal MOS device to control the base drive. Indicative by its description, the MCT is essentially an SCR structure also utilitzing a MOS drive stage. Both devices offer significant cost advantages over MOSFETs for a given power capability.

MOSFET, IGBT and MCT Gate Drives: There are numerous reasons for driving the MOSFET gate to a negative potential during the device's off state. Degradation of the gate turn-on threshold over time and especially following high levels of irradiation are amongst the most common. However, with IGBTs, the important concern is the ability to keep the device off following turn-off with a high drain current flowing. On larger IGBT's with ratings up to 300 Amps, inductive effects caused by the device's package alone can "kick" the effective gate-to-emitter voltage positive by several Volts at the die - even with the gate shorted to the emitter at the package terminals. Actually, this is the result of the high current flowing in the emitter lead (package) inductance which can less than 1nH. The corresponding voltage drop changes polarity at turn off, thus pulling the emitter below the gate, or ground. If high enough, a fast turn off will be followed by a parasitic turn-on of the

switch, and potential destruction of the semiconductor. Applying the correct amplitude of negative gate voltage can insure proper operation under these high current turn-off conditions. Also, the negative bias protects against turn-on from high dv/dt related changes that could couple into the gate through the "Miller" capacitance.

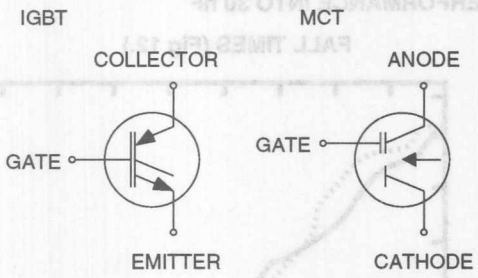


Figure 13 - IGBT and MCT Diagrams

Unlike power MOSFET switches, IGBT transconductance continues to increase with gate voltage. While most MOSFET devices peak with about 10 to 12 Volts at the gate, IGBT performance steadily improves up to the suggested 16 Volt maximum gate voltage. Typically, most IGBT manufacturers recommend a negative drive voltage between -5 and -15V. Generally, it is most convenient to derive a negative voltage equal in amplitude to the positive supply rail, and ±15V is common.

The gate charge required by an IGBT (for a given voltage and current rating) is noticeably less than that of a MOSFET. Part of this is due to the better utilization of silicon which allows the IGBT die to be considerably smaller than its FET counterpart. Additionally, the IGBT (being a bipolar transistor) does not suffer from the severe "Miller" effects of the MOS devices, easing the drive requirements in a given application. However, because of their advantages, most available IGBTs have fairly high gate charge demands - simply because of their greater power handling capability.

In contrast, MCTs (MOS Controlled Thyristors) exhibit the highest silicon utilization level among power switching devices. While relatively new to the market, these devices are quickly gaining acceptance in very high power (above several kilowatts) applications because of their high voltage (1000V) and high current (to 1000A) capability. Recently introduced parts boast maximum ratings to one megawatt, ideal for large industrial motor drives and high power distribution—even at the substation level. These devices are essentially MOS controlled SCRs and are intended for low frequency switchmode conversion. They will most likely replace high power discrete transistors, Darlingtons and SCRs because of their higher efficiency and lower cost.

Gate Charge and Effective Capacitance with Negative Bias: While several MOSFET and IGBT manufacturers recommend negative gate voltages in the device's off state, few publish any curves or information about gate charge characteristics when the gate is below zero Volts. This complicates the gate drive circuit design as each IGBT, MOSFET or MCT switch must be evaluated by the user over the ranges of operation conditions. A test fixture as shown in Figure 14 can be used to provide empirical generalizations for devices of interest. A switched constant current source/sink has been configured using a simple dual op-amp to drive a "constant" 1mA at the device under test (DUT). Gate voltage versus time can be monitored which provides the exact gate charge requirements for a given device. Any application specific requirements can also be accommodated by modifying the test circuit with external circuitry.

Negative Gate Charge - Empirical Data: Several MOSFET, IGBT and MCT gate charge measurements were taken to establish the general characteristics with negative gate charge and effective capacitance during this third quadrant operation was calculated and compared to of the first quadrant specifications from the manufacturers data sheets. Figure 15 demonstrates the general relationships of gate charges for comparison.

Both the IGBT and MCT have similar negative bias gate charge requirements as with an applied positive bias. The MOSFET, however, exhibits a slightly reduced gate charge in its negative bias region, somewhere between 70 and 75 percent of its positive bias charge. The MOSFET's more significant "Miller" effect in the first quadrant is responsible for this since the higher effective capacitance during the plateau region does not occur with negative bias.

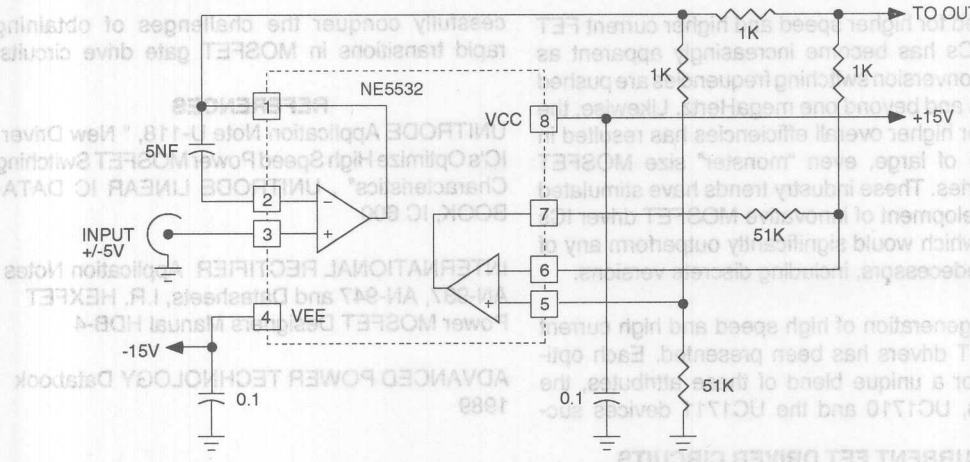


Figure 14 - Gate Charge Test Circuit

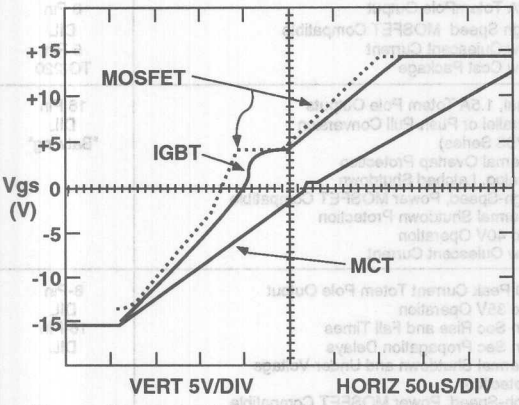


Figure 15 - Gate Charge Comparison Low to High Transition

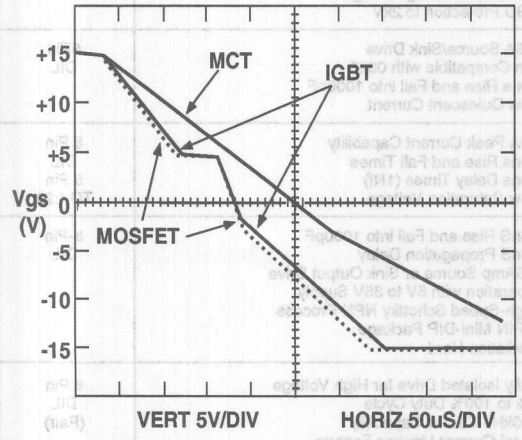


Figure 16 - Gate Drive Comparison High to Low Transition

Total Gate Power - Negative Drive Voltage Applications: All of the previously presented gate power equations still apply, however they must be modified to include the additional charge requirements of the negative supply voltage. For the sake of simplicity, a multiplication factor can be used for recalculation of the exact figures. When identical amplitudes of positive and negative supply voltages are used, for example ±15V, then the gate power utilized can be simply multiplied by a factor of two. This completes the process for the IGBTs and MCTs. The total MOSFET gate charge, on the other hand, should only be multiplied by a factor of 1.7 to 1.75 to accommodate the reduced negative bias demands. Additionally, if a negative supply voltage different than the positive rail voltage is used, for example +15 and -5, then the scaling factor must be adjusted accordingly. In this case, the new total gate power would be 1+ (-5/-15) or 1.33 times the initial 0-15V gate power for IGBTs and MCTs. The negative drive voltage scaling factor (-5/-15) would be multiplied by the 70 to 75% index if a MOSFET were used instead of an IGBT or MCT. This would result in a 1.23 to 1.25 times net increase over the initial (0-15V) gate power demand.

SUMMARY

The need for higher speed and higher current FET driver ICs has become increasingly apparent as power conversion switching frequencies are pushed towards and beyond one megaHertz. Likewise, the quest for higher overall efficiencies has resulted in creation of large, even "monster" size MOSFET geometries. These industry trends have stimulated the development of innovative MOSFET driver ICs - ones which would significantly outperform any of their predecessors, including discrete versions.

A new generation of high speed and high current MOSFET drivers has been presented. Each optimized for a unique blend of these attributes, the UC1708, UC1710 and the UC1711 devices successfully conquer the challenges of obtaining rapid transitions in MOSFET gate drive circuits.

REFERENCES

UNITRODE Application Note U-118, " New Driver IC's Optimize High Speed Power MOSFET Switching Characteristics" , UNITRODE LINEAR IC DATA-BOOK, IC 600

INTERNATIONAL RECTIFIER Application Notes AN-937, AN-947 and Datasheets, I.R. HEXFET Power MOSFET Designers Manual HDB-4

ADVANCED POWER TECHNOLOGY Databook 1989

HIGH CURRENT FET DRIVER CIRCUITS

TYPE	DESCRIPTION	KEY FEATURES	PACKAGE
UC1705/3705	High Speed Power Driver (Single ended)	• 1.5A TotemPole Output • High Speed MOSFET Compatible • Low Quiescent Current • Low Cost Package	8 Pin DIL 5 Pin TO-220
UC1706/3706	Dual High Current MOSFET Compatible Output Driver	• Dual, 1.5A Totem Pole Outputs • Parallel or Push-Pull Conversion (1706 Series) • Internal Overlap Protection • Analog, Latched Shutdown • High-Speed, Power MOSFET Compatible • Thermal Shutdown Protection • 5 to 40V Operation • Low Quiescent Current	16 Pin DIL "Batwing"
UC1707/3707	Dual Uncommitted High Current MOSFET Compatible Output Driver		
UC1708/3708	Dual Non-Inverting Power Driver	• 3.0 Peak Current Totem Pole Output • 5 to 35V Operation • 25n Sec Rise and Fall Times • 25n Sec Propagation Delays • Thermal Shutdown and Under-Voltage Protection • High-Speed, Power MOSFET Compatible • Efficient High Frequency Operation • Low-Cross-Conduction Current Spike • Enable and Shutdown Functions • Wide Input Voltage Range • ESD Protection to 2kV	8-Pin DIL 16-Pin DIL
UC1709/3709	Dual High Speed FET Driver	• 1.5A Source/Sink Drive • Pin Compatible with 0026 • 40ns Rise and Fall into 1000pF • Low Quiescent Current	8Pin DIL
UC1710/3710	High Current/Speed FET Driver	• 10A Peak Current Capability • 40ns Rise and Fall Times • 40ns Delay Times (1Nf) • Low Saturation Voltage	8 Pin DIL 5 Pin TO-220
UC1711/3711	Dual Ultra High Speed FET Driver	• 25nS Rise and Fall into 1000pF • 15nS Propagation Delay • 1.5Amp Source or Sink Output Drive • Operation with 5V to 35V Supply • High-Speed Schottky NPN Process • 8-PIN Mini-DIP Package • Radiation Hard	8-Pin DIL
UC3724 UC3725 (PAIR)	Isolated High Side Drive for N-Channel Power MOSFET Gates	• Fully Isolated Drive for High Voltage • 0% to 100% Duty Cycle • 600kHz Carrier Capability • Local Current Limiting Feature	8 Pin DIL (Pair)

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Zero Voltage Switching Resonant Power Conversion

Bill Andreycak

Abstract

The technique of zero voltage switching in modern power conversion is explored. Several ZVS topologies and applications, limitations of the ZVS technique, and a generalized design procedure are featured. Two design examples are presented: a 50 Watt DC/DC converter, and an off-line 300 Watt multiple output power supply. This topic concludes with a performance comparison of ZVS converters to their square wave counterparts, and a summary of typical applications.

Introduction

Advances in resonant and quasi-resonant power conversion technology propose alternative solutions to a conflicting set of square wave conversion design goals; obtaining high efficiency operation at a high switching frequency from a high voltage source. Currently, the conventional approaches are by far, still in the production mainstream. However, an increasing challenge can be witnessed by the emerging resonant technologies, primarily due to their lossless switching merits. The intent of this presentation is to unravel the details of zero voltage switching via a comprehensive analysis of the timing intervals and relevant voltage and current waveforms.

The concept of quasi-resonant, "lossless" switching is not new, most noticeably patented by one individual [1] and publicized by another at various power conferences [2,3]. Numerous efforts focusing on zero current switching ensued, first perceived as the likely candidate for tomorrow's generation of high frequency power converters [4,5,6,7,8]. In theory, the on-off transitions occur at a time in the resonant cycle where the switch current is zero, facilitating zero current, hence zero power switching. And while true, two obvious concerns can impede the quest for high efficiency operation with high voltage inputs.

By nature of the resonant tank and zero current switching limitation, the peak switch current is significantly higher than its square wave counterpart. In fact, the peak of the full load switch current is a minimum of twice that of its square wave kin. In its off state, the switch returns to a blocking a high voltage every cycle. When activated by the next drive pulse, the MOSFET output capacitance (C_{oss}) is discharged by the FET, contributing a significant power loss at high frequencies and high voltages. Instead, both of these losses are avoided by implementing a zero voltage switching technique [9,10].

Zero Voltage Switching Overview

Zero voltage switching can best be defined as conventional square wave power conversion during the switch's on-time with "resonant" switching transitions. For the most part, it can be considered as square wave power utilizing a constant off-time control which varies the conversion frequency, or on-time to maintain regulation of the output voltage. For a given unit of time, this method is similar to fixed frequency conversion which uses an adjustable duty cycle, as shown in Fig. 1.

Regulation of the output voltage is accomplished by adjusting the effective duty cycle, performed by varying the conversion frequency. This changes the effective on-time in a ZVS design. The foundation of this conversion is simply the volt-second product equating of the input and output. It is virtually identical to that of square wave power conversion, and vastly

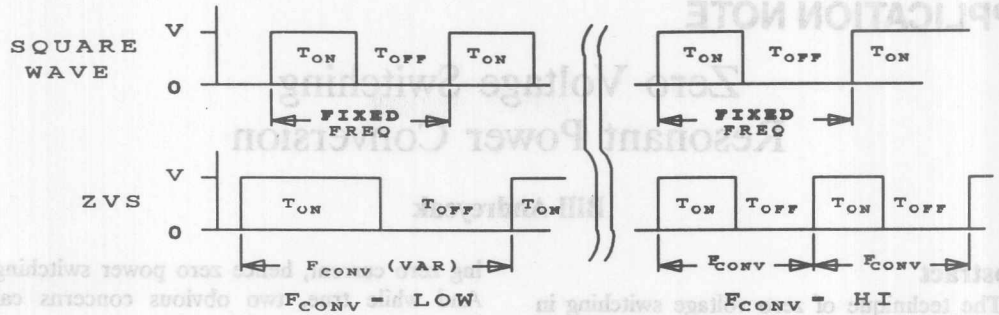


Fig. 1 - Zero Voltage Switching vs. Conventional Square Wave

unlike the energy transfer system of its electrical dual, the zero current switched converter.

During the ZVS switch off-time, the L-C tank circuit resonates. This traverses the voltage across the switch from zero to its peak, and back down again to zero. At this point the switch can be reactivated, and lossless zero voltage switching facilitated. Since the output capacitance of the MOSFET switch (C_{oss}) has been discharged by the resonant tank, it does not contribute to power loss or dissipation in the switch. Therefore, the MOSFET transition losses go to zero - regardless of operating frequency and input voltage. This could represent a significant savings in power, and result in a substantial improvement in efficiency. Obviously, this attribute makes zero voltage switching a suitable candidate for high frequency, high voltage converter designs. Additionally, the gate drive requirements are somewhat reduced in a ZVS design due to the lack of the gate to drain (Miller) charge, which is deleted when V_{DS} equals zero.

The technique of zero voltage switching is applicable to all switching topologies; the buck regulator and its derivatives (forward, half and full bridge), the flyback, and boost converters, to name a few. This presentation will focus on the continuous output current, buck derived topologies, however a list of references describing the others has been included in the appendix.

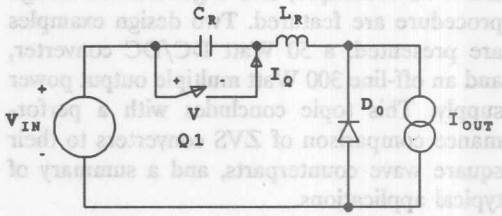


Fig. 2 - Resonant Switch Implementation

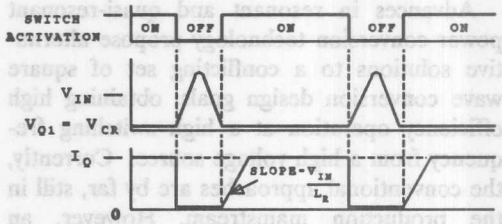


Fig. 3 - General Waveforms

ZVS Benefits

- Zero power "Lossless" switching transitions
- Reduced EMI / RFI at transitions
- No power loss due to discharging C_{oss}
- No higher peak currents, (ie. ZCS) same as square wave systems
- High efficiency with high voltage inputs at any frequency
- Can incorporate parasitic circuit and component *L & C*

- Reduced gate drive requirements (no "Miller" effects)
- Short circuit tolerant

ZVS Differences:

- Variable frequency operation (in general)
- Higher off-state voltages in single switch, unclamped topologies
- Relatively new technology - users must climb the learning curve
- Conversion frequency is inversely proportional to load current
- A more sophisticated control circuit may be required

ZVS Design Equations

A zero voltage switched Buck regulator will be used to develop the design equations for the various voltages, currents and time intervals associated with each of the conversion periods which occur during one complete switching cycle. The circuit schematic, component references, and relevant polarities are shown in Fig. 4.

Typical design procedure guidelines and "shortcuts" will be employed during the analysis' for the purpose of brevity. At the onset, all components will be treated as though they were ideal which simplifies the generation of the basic equations and relationships. As this section progresses, losses and non-ideal characteristics of the components will be added to the formulas. The timing summary will expound upon the equations for a precise analysis.

Another valid assumption is that the output filter section consisting of output inductor L_O and capacitor C_O has a time constant several orders of magnitude larger than any power conversion period. The filter inductance is large in comparison to that of the resonant inductor's value L_R and the magnetizing current ΔI_{Lo} as well as the inductor's DC resistance is negligible. In addition, both the input voltage V_{IN} and output voltage V_O are purely DC, and do not vary during a given conversion cycle. Last, the converter is operating in a closed loop configuration which regulates the output voltage V_O.

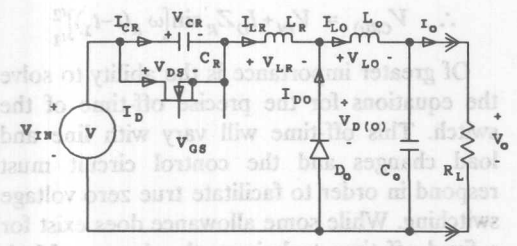


Fig. 4 - Zero Voltage Switched Buck Regulator

Initial Conditions: Time interval < t_0

Before analyzing the individual time intervals, the initial conditions of the circuit must be defined. The analysis will begin with switch Q_1 on, conducting a drain current I_D equal to the output current I_O, and $V_{DS} = V_{CR} = 0$ (ideal). In series with the switch Q_1 is the resonant inductor L_R and the output inductor L_O which also conduct the output current I_O. It has been established that the output inductance L_O is large in comparison to the resonant inductor L_R and all components are ideal. Therefore, the voltage across the output inductor V_{Lo} equals the input to output voltage differential; $V_{Lo} = V_{IN} - V_O$. The output filter section catch diode D_O is not conducting and sees a reverse voltage equal to the input voltage; $V_{Do} = V_1$, observing the polarity shown in Figure 4.

Table I - INITIAL CONDITIONS

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$V_{DS}=V_{CR}=0$; $I_D=I_{LR}=I_{LO}=I_O$
D_O	OFF	$V_{DO}=V_{IN}$; $I_{DO}=0$
L_R		$I_{LR}=I_O$; $V_{LR}=0$
L_O		$V_{LO}=V_{IN}-V_O$; $I_{LO}=0$

Capacitor Charging State: t_0 - t_1

The conversion period is initiated at time t_0 when switch Q_1 is turned OFF. Since the current through resonant inductor L_R and output inductor L_O cannot change instantaneously, and no drain current flows in Q_1 while

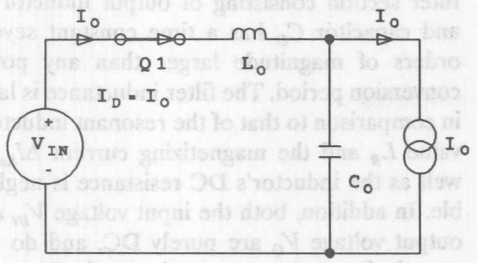


Fig. 5 - Simplified Model

$$V_{CR}(t) = \frac{I_O t}{C_R} \quad ; \quad t_{01} = \frac{C_R V_{IN}}{I_O}$$

$$I_{CR} = I_O \qquad for\ t_0 < t < t_1$$

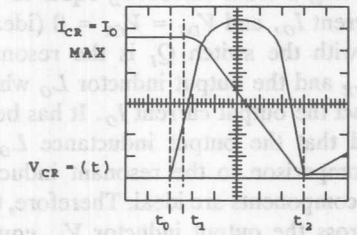


Fig. 6 - Resonant Capacitor Waveforms

it is off, the current is diverted around the switch through the resonant capacitor C_R. The constant output current will linearly increase the voltage across the resonant capacitor until it reaches the input voltage ($V_{CR} = V_{IN}$). Since the current is not changing, neither is the voltage across resonant inductor L_R.

At time t_0 the switch current I_D "instantly" drops from I_O to zero. Simultaneously, the resonant capacitor current I_{CR} snaps from zero to I_O, while the resonant inductor current I_{LR} and output inductor current I_{LO} are constant and also equal to I_O during interval t_{01}. Voltage across output inductor L_O and output catch diode D_O linearly decreases during this interval due to the linearly increasing voltage across resonant capacitor C_R. At time t_1, V_{CR} equals V_{IN}, and D_O starts to conduct.

Table II - CAPACITOR CHARGING: t_0 - t_1

COMP.	STATUS	CIRCUIT VALUES
Q_1	OFF	$I_D = 0$; $V_{DS(t)} = V_{CR(t)}$
C_R	Charging	$I_{CR} = 0$; $V_{CR(t)}$ RISES LINEARLY $V_{CR(t0)} = 0$; $V_{CR(t1)} = V_{IN}$
L_R		$I_{LR(t)} = I_O$; $V_{LR} = 0$
D_O	OFF	$V_{DO(t0)} = V_{IN}$; $V_{DO(t1)} = 0$; DECREASES LINEARLY
L_O		$V_{LO(t0)} = V_{IN} - V_O$; $V_{LO(t1)} = -V_O$ DECREASES LINEARLY ; $I_{LO} = I_O$

Resonant State: t_1 - t_2

The resonant portion of the conversion cycle begins at t_1 when the voltage across resonant capacitor V_{CR} equals the input voltage V_{IN}, and the output catch diode begins conducting. At t_1, current through the resonant components I_{CR} and I_{LR} equals the output current I_O.

The stimulus for this series resonant L-C circuit is output current I_O flowing through the resonant inductor prior to time t_1. The ensuing resonant tank current follows a cosine function beginning at time t_1, and ending at time t_2. At the natural resonant frequency ω_R, each of the *L-C* tank components exhibit an impedance equal to the tank impedance, Z_R. Therefore, the peak voltage across C_R and switch Q_1 are a function of Z_R and I_O.

The instantaneous voltage across C_R and Q_1 can be evaluated over the resonant time interval using the following relationships:

$$V_{CR(t)} = V_{CR(t1)} + \frac{I_O}{\omega_R C_R} \sin\left[\omega_R (t - t_1)\right]_{t_1}^{t_2}$$

$$Z_R = 1/\omega_R C_R \quad ; \quad V_{CR(t1)} = V_{IN}$$

$$\therefore \quad V_{CR(t)} = V_{IN} + I_O Z_R \sin\left[\omega_R (t - t_1)\right]_{t_1}^{t_2}$$

Of greater importance is the ability to solve the equations for the precise off-time of the switch. This off-time will vary with line and load changes and the control circuit must respond in order to facilitate true zero voltage switching. While some allowance does exist for a fixed off time technique, the degree of lati-

tude is insufficient to accommodate typical input and output variations. The exact time is obtained by solving the resonant capacitor voltage equations for the condition when zero voltage is attained.

$$Let\ V_{CR(t)} = 0\ ;\ I_O Z_R\ SIN(\omega_R(t-t_1)) = -V_{IN}$$

The equation can be further simplified by extracting the half cycle (180 degrees) of conduction which is a constant for a given resonant frequency, and equal to π/ω_R.

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R} \arcsin\left[\frac{V_{IN}}{I_O Z_R}\right]_{t1}^{t2}$$

The resonant component current ($I_{CR} = I_{LR}$) is a cosine function between time t_1 and t_2, described as:

$$I_{CR(t)} = I_O \cos\left[\omega_R(t-t_1)\right]_{t_1}^{t2}$$

The absolute maximum duration for this interval occurs when 270 degrees ($3\pi/2\omega_R$) of resonant operation is required to intersect the zero voltage axis. This corresponds to the limit of resonance as minimum load and maximum line voltage are approached.

Contributions of line and load influences on the resonant time interval t_{12} can be analyzed individually as shown in Figs. 7 and 8.

Prior to time t_1, the catch diode D_O was not conducting. Its voltage, V_{DO}, was linearly decreasing from V_{IN} at time t_0 to zero at t_1 while input source V_{IN} was supplying full output current, I_O. At time t_1, however, this situation changes as the resonant capacitor initiates resonance, diverting the resonant inductor current away from the output filter section. Instantly, the output diode voltage, V_{DO}, changes polarity as it begins to conduct, supplementing the decreasing resonant inductor current with diode current I_{DO}, extracted from stored energy in output inductor L_O. The diode current waveshape follows a cosine function during this interval, equalling I_O minus $I_{CR}(t)$.

Also occurring at time t_1, the output filter inductor L_O releases the stored energy required

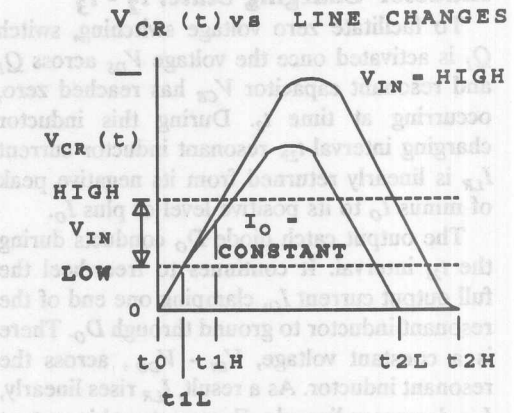


Fig. 7 -- Resonant Capacitor Voltage vs. Line

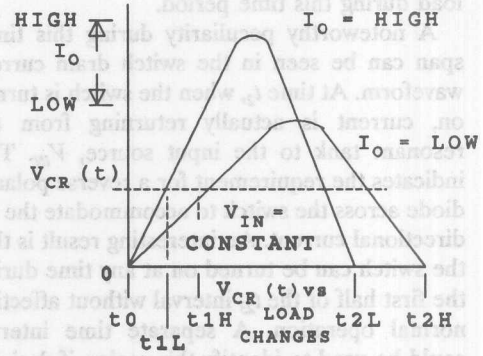


Fig. 8 -- Resonant Capacitor Voltage vs. Load

to maintain a constant output current I_O. Its reverse voltage is clamped to the output voltage V_O minus the diode voltage drop V_{DO} by the convention followed by Figure 4.

Table III - RESONANT INTERVAL: t_1 - t_2

COMP.	STATUS	CIRCUIT VALUES
Q_1	OFF	$V_{DS(t)} = V_{CR(t)}$
C_R	Resonant	$V_{CR(t)} = V_{IN} + (I_O Z_R \sin(\omega_R(t-t_1)))$ $I_{CR(t)} = I_O \cos(\omega_R(t-t_1))$
L_R	Resonant	$V_{LR(t)} = [I_O Z_R \sin(\omega_R(t-t_1))$ $I_{LR(t)} = I_{CR(t)}$
D_O	ON	$I_{DO(t)} = I_O - I_{LR(t)}$
L_O	Discharge	$V_{LO} = -(V_O + V_{DO(fwd)})$

Inductor Charging State: t_2 - t_3

To facilitate zero voltage switching, switch Q_1 is activated once the voltage V_{DS} across Q_1 and resonant capacitor V_{CR} has reached zero, occurring at time t_2. During this inductor charging interval t_{23}, resonant inductor current I_{LR} is linearly returned from its negative peak of minus I_O to its positive level of plus I_O.

The output catch diode D_O conducts during the t_{23} interval. It continues to freewheel the full output current I_O, clamping one end of the resonant inductor to ground through D_O. There is a constant voltage, V_{IN} - V_{DO}, across the resonant inductor. As a result, I_{LR} rises linearly, I_{DO} decreases linearly. Energy stored in output inductor L_O continues to be delivered to the load during this time period.

A noteworthy peculiarity during this time-span can be seen in the switch drain current waveform. At time t_2, when the switch is turned on, current is actually returning from the resonant tank to the input source, V_{IN}. This indicates the requirement for a reverse polarity diode across the switch to accommodate the bi-directional current. An interesting result is that the switch can be turned on at any time during the first half of the t_{23} interval without affecting normal operation. A separate time interval could be used to identify this region if desired.

$$\frac{dI_R}{dt} = \frac{V_{IN}}{L_R} \quad ; \quad dt = dI_R L_R / V_{IN}$$

$$\therefore \; t_{23} = \frac{L_R \Delta I_R}{V_{IN}}$$

$$\text{where } \Delta I_R = -I_O \text{ to } +I_O = 2I_O$$

$$t_{23} = \frac{2L_R I_O}{V_{IN}} \quad \text{and varies with } V_{IN} \text{ and } V_O$$

Power Transfer State: t_3 - t_4

Once the resonant inductor current I_{LR} has reached I_O at time t_3, the zero voltage switched converter resembles a conventional square wave power processor. During the remainder of the conversion period, most of the pertinent waveforms approach DC conditions.

Table IV - INDUCTOR CHARGING: t_2 - t_3

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$I_{D(t)} = -I_O + ((V_{IN} + V_{DO})/L_R)t$
C_R		$V_{CR} = 0$
L_R	Charging	$V_{LR} = V_{IN} + V_{DO}$ $I_{LR(t)} = -I_O + (V_{LR}/L_R)(t\text{-}t2)$
D_O	ON	$I_{DO(t)} = I_O - I_{LR(t)}$
L_O		$I_{LO} = I_O$; $V_{LO} = -(V_O + V_{DO})$

Assuming ideal components, with Q_1 closed, the input source supplies output current , and the output filter inductor voltage V_{LO} equals V_{IN} - V_O. The switch current and resonant inductor current are both equal to I_O, and their respective voltage drops are zero ($V_{DS} = V_{LR} = 0$). Catch diode voltage V_{DO} equals V_{IN}, and $I_{DO} = 0$.

In closed loop operation where the output voltage is in regulation, the control circuit essentially varies the on-time of the switch during the t_{34} interval. Variable frequency operation is actually the result of modulating the on-time as dictated by line and load conditions. Increasing the time duration, or lowering the conversion frequency has the same effect as widening the duty cycle in a traditional square wave converter. For example, if the output voltage were to drop in response to an increased load, the conversion frequency would decrease in order to raise the effective ON period. Conversely, at light loads where little energy is drawn from the output capacitor, the control circuit would adjust to minimize the t_{34} duration by increasing the conversion frequency. In summary, the conversion frequency is inversely proportional to the power delivered to the load.

$$V_O = \frac{V_{IN} t_{34}}{t_{01} + t_{12} + t_{23} + t_{34}} = \frac{V_{IN} t_{34}}{t_{03} + t_{34}}$$

$$t_{34} = \frac{V_O t_{03}}{V_{IN} - V_O}$$

Table V - POWER TRANSFER: t_3 - t_4

COMP.	STATUS	CIRCUIT VALUES
Q_1	ON	$V_{DS}=I_O R_{DS(ON)}$; $I_D=I_O$
C_R		$V_{CR}=0$
L_R		$I_{LR}=I_O$; $V_{LR}=0$
D_O	OFF	$V_{DO}=V_{IN}$
L_O	Charging	$V_{LO}=V_{IN}-V_O$; $I_{LO}=I_O$

V_{IN} = 18 V
V_O = 5 V
I_O = 5 A

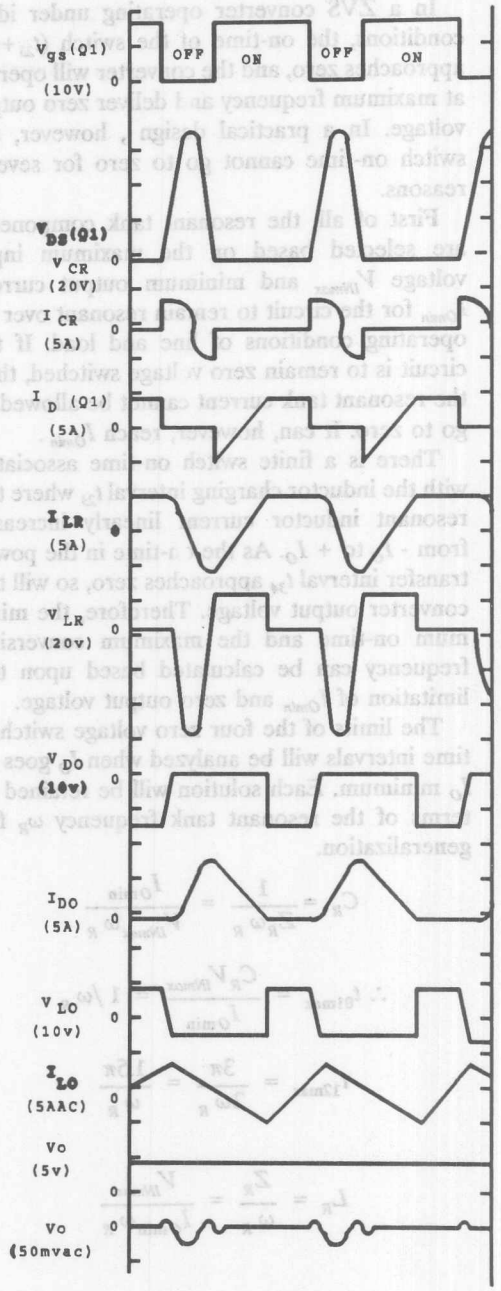


Fig. 9 -- ZVS Buck Regulator Waveforms

ZVS Converter Limitations:

In a ZVS converter operating under ideal conditions, the on-time of the switch ($t_{23}+t_{34}$) approaches zero, and the converter will operate at maximum frequency and deliver zero output voltage. In a practical design , however, the switch on-time cannot go to zero for several reasons.

First of all, the resonant tank components are selected based on the maximum input voltage V_{INmax} and minimum output current I_{Omin} for the circuit to remain resonant over all operating conditions of line and load. If the circuit is to remain zero voltage switched, then the resonant tank current cannot be allowed to go to zero. It can, however, reach I_{Omin} .

There is a finite switch on-time associated with the inductor charging interval t_{23} where the resonant inductor current linearly increases from - I_O to + I_O. As the on-time in the power transfer interval t_{34} approaches zero, so will the converter output voltage. Therefore, the minimum on-time and the maximum conversion frequency can be calculated based upon the limitation of I_{Omin} and zero output voltage.

The limits of the four zero voltage switched time intervals will be analyzed when I_O goes to I_O minimum. Each solution will be retained in terms of the resonant tank frequency ω_R for generalization.

$$C_R = \frac{1}{Z_R \omega_R} = \frac{I_{O\min}}{V_{INmax}\omega_R}$$

$$\therefore t_{01\max} = \frac{C_R V_{INmax}}{I_{O\min}} = 1/\omega_R$$

$$t_{12\max} = \frac{3\pi}{2\omega_R} = \frac{1.5\pi}{\omega_R}$$

$$L_R = \frac{Z_R}{\omega_R} = \frac{V_{INmax}}{I_{O\min}\omega_R}$$

$$\therefore t_{23} = \frac{2L_R I_{O\min}}{V_{INmax}} = \frac{2}{\omega_R}$$

$$t_{34\min} = 0$$

Both the minimum on-time and maximum off-time have been described in terms of the resonant tank frequency , ω_R. Taking this one step further will result in the maximum conversion frequency $f_{CONVmax}$, also as a function of the resonant tank frequency.

Minimum On-Time:

$$t_{23\min} = \frac{2}{\omega_R} = \frac{1}{\pi f_R} = \frac{0.318}{f_R}$$

Maximum Off-Time:

$$t_{01}+t_{12\min} = \frac{1+1.5\pi}{\omega_R} = \frac{0.909}{f_R}$$

The maximum conversion frequency corresponds to the minimum conversion period, $T_{CONVmin}$, which is the sum of the minimum on-time and maximum off-time:

$T_{CONVmin}$:

$$t_{01}+t_{12\min}+t_{23} = \frac{0.909+0.308}{f_R} = \frac{1.227}{f_R}$$

The maximum conversion frequency, $f_{CONVmax} = 1/T_{CONVmin}$, equals

$$F_{CONV\max} = \frac{1}{T_{CONV(\min)}} = \frac{f_R}{1.227}$$

The ratio of the maximum conversion frequency to that of the resonant tank frequency can be expressed as a topology coefficient, K_T. For this zero voltage switched Buck regulator and its derivatives, K_{Tmax} equals:

$$K_{T\max} = \frac{F_{CONVmax}}{f_R} = \frac{f_R/1.227}{f_R} = 0.815$$

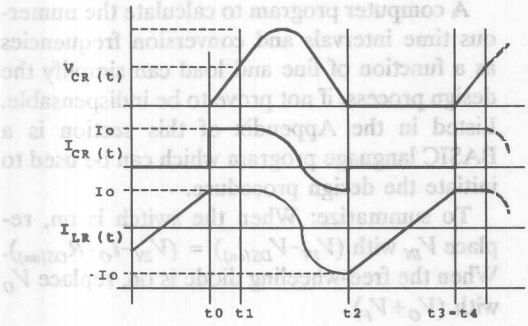


Fig. 10 -- Waveforms at $F_{CONV} = K_T \cdot f_R$

In a realistic application, the output voltage of the power supply is held in regulation at V_O which stipulates that the on-time in the power processing state, t_{34}, cannot go to zero as in the example above. The volt-second product requirements of the output must be satisfied during this period, just as in any square wave converter design. Analogous to minimum duty cycle, the minimum on-time for a given design will be a function of V_{IN}, V_O and the resonant tank frequency, ω_R.

Although small, a specific amount of energy is transferred from the input to the output during the capacitor charging interval t_{01}. The voltage into the output filter section linearly decreases from V_{IN} at time t_0 to zero at t_1, equal to an average value of $V_{IN}/2$. In addition, a constant current equal to the output current I_O was being supplied from the input source. The average energy transferred during this interval is defined as:

$$W_{IN} = \frac{1}{2} V_{IN} I_O t_{01} = \frac{V_{IN} I_O}{2} \frac{C_R V_{IN}}{I_O} = \frac{V_{IN}^2 C_R}{2}$$

The equation can be reorganized in terms of C_R and ω_R as:

$$W_{IN} = \frac{V_{IN}^2 I_{O\min}}{2\omega_R V_{IN\max}}$$

This minimum energy can be equated to minimum output watts by dividing it by its conversion period where t_{34} equals zero. Topology coefficient K_T will be incorporated to define the ratio of the maximum conversion frequency (minimum conversion period) to that of the resonant tank frequency, ω_R.

$$W_{IN} = P_O T_{CONV}, \quad Where\ T_{CONV} = \frac{7.71}{\omega_R}$$

$$W_{IN} = P_{O\min} \frac{7.71}{\omega_R} = \frac{V_{IN}^2 I_{O\min}}{2\omega_R V_{IN\max}}$$

$$P_{O\min} = V_O I_{O\min} = \frac{V_{IN}^2 I_{O\min}}{2(7.71) V_{IN\max}}$$

This demonstrates that a zero power output is **unobtainable** in reality. The same is true for the ability to obtain zero output voltage. The equation can be rewritten as:

$$V_{O\min} = \frac{V_{IN}^2}{2(7.71) V_{IN\max}} = \frac{0.065\, V_{IN}^2}{V_{IN\max}}$$

Solving for the highest minimum output voltage, the worst case for occurs when I_O equals I_{Omin} and V_{IN} is at its maximum, V_{INmax}.

$$V_{O\min} = 0.065\, V_{IN\max} \ ; \ \approx 6.5\%\ V_{IN\max}$$

$$P_{O\min} = 0.065\, V_{IN\max} I_{O\min} \ ; \ \approx 6.5\%\ P_{IN\min}$$

Under normal circumstances the circuit will be operating far above this minimum requirement. In most applications, the amount of power transferred during the capacitor charging interval t_{01} can be neglected as it represents less than seven percent (7%) of the **minimum** input power. This corresponds to less than one percent of the total input power assuming a 10:1 load range.

ZVS Effective Duty Cycles:

A valid assumption is that a negligible amount of power is delivered to the load during the capacitor charging interval t_{01}. Also, no power is transferred during the resonant period from t_{12}. Although the switch is on during period t_{23}, it is only recharging the

resonant and output inductors to maintain the minimum output current, I_{Omin}. In summary, NO output power is derived from V_{IN} during interval t_{03}.

The power required to support V_O at its current of I_O is obtained from the input source during the power transfer period t_{34}. Therefore, an effective "duty cycle" can be used to describe the power transfer interval t_{34} to that of the entire switching period, t_{04}, or T_{CONV}.

ZVS - Effective Duty Cycle Calculations:

$$\text{"Duty Cycle"} = \frac{V_O}{V_{IN}} = \frac{t_{34}}{t_{04}}$$

$$\text{"Duty Cycle"} = \frac{t_{34}}{t_{01}+t_{12}+t_{23}+t_{34}}$$

And can be analyzed over line and load ranges using previous equations for each interval.

Accommodating Losses in the Design Equations:

Equations for zero voltage switching using ideal components and circuit parameters have been generated, primarily to understand each of the intervals in addition to computer modeling purposes. The next logical progression is to modify the equations to accommodate voltage drops across the components due to series impedance, like $R_{DS(on)}$, and the catch diode forward voltage drop. These two represent the most significant loss contributions in the buck regulator model. Later, the same equations will be adapted for the buck derived topologies which incorporate a transformer in the power stage.

The procedure to modify the equations is straightforward. Wherever V_{IN} appears in the equations while the switch is on it will be replaced by $V_{IN}-V_{DS(on)}$, the latter being a function of the load current I_O. The equations can be further adjusted to accept changes of $R_{DS(on)}$ and V_F, etc. with the device junction temperatures. Resonant component initial tolerances, and temperature variations likewise could optionally be evaluated.

A computer program to calculate the numerous time intervals and conversion frequencies as a function of line and load can simplify the design process, if not prove to be indispensable. Listed in the Appendix of this section is a BASIC language program which can be used to initiate the design procedure.

To summarize: When the switch is on, replace V_{IN} with $(V_{IN}-V_{DS(on)}) = (V_{IN}-I_O \cdot R_{DS(on)})$. When the free-wheeling diode is on, replace V_O with (V_O+V_F).

$$t_{01} = \frac{C_R(V_{IN}-I_O R_{DS(on)})}{I_O}$$

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R}\arcsin\left[\frac{V_{IN}-I_O R_{DS(on)}}{I_O Z_R}\right]_{t1}^{t2}$$

$$t_{23} = \frac{2L_R I_O}{V_{IN}-I_O R_{DS(on)}}$$

$$t_{34} = \frac{(V_O+V_F)(t_{01}+t_{12}+t_{23})}{(V_{IN}-I_O R_{DS(on)})-(V_O+V_F)}$$

$$Z_R = \frac{V_{INmax}-R_{DS(on)} I_{O\min}}{I_{O\min}}$$

Transformer Coupled Circuit Equations:

The general design equations for the Buck topology also apply for its derivates; namely the forward, half-bridge, full-bridge and push-pull converters. Listed below are the modifications and circuit specifics to apply the previous equations to transformer coupled circuits.

General Transformer Coupled Circuits. Maintaining the resonant tank components on the primary side of the transformer isolation boundary is probably the most common and simplest of configurations. The design procedure begins by transforming the output voltage and current to the primary side through the turns ratio, N. The prime (') designator will be used to signify the translated variables as seen by the primary side circuitry.

$$N = \frac{Primary\ Turns}{Secondary\ Turns}$$

$I_O' = I_O/N$; $V_O' = V_O \cdot N$; and $Z_O' = Z_O \cdot N^2$

To satisfy the condition for resonance, $I_R < I_O'$

$$I_R \le I_O' = I_O/N \ ; \ Z_R \le \frac{V_{INmax}}{I_{O'\min}} = \frac{V_{INmax} N}{I_O}$$

The resonant tank component equations now become:

$$L_R = \frac{Z_R}{\omega_R} = \frac{V_{INmax} N}{I_{O\min} \omega_R}$$

Note: the calculated resonant inductance value does not include any series inductance, typical of the transformer leakage and wiring inductances.

$$C_R = \frac{1}{Z_R \omega_R} = \frac{I_{O\min}}{N V_{INmax} \omega_R}$$

Note: the calculated resonant capacitor value does not include any parallel capacitance, typical of a MOSFET output capacitance, C_{OSS}, in shunt. Multi-transistor variations of the buck topology should accommodate all switch capacitances in the analysis.

Timing Equations (including N):

$$t_{01} = \frac{C_R V_{IN} N}{I_O}$$

$$t_{12} = \frac{\pi}{\omega_R} + \frac{1}{\omega_R} \arcsin \left[\frac{V_{IN} N}{I_O Z_R} \right]_{t1}^{t2}$$

$$t_{23} = \frac{2 L_R I_O}{V_{IN} N}$$

$$t_{34} = \frac{N V_O (t_{01} + t_{12} + t_{23})}{V_{IN} - N V_O}$$

$$T_{CONV} = t_{01} + t_{12} + t_{23} + t_{34}$$

Determining Transformer Turns Ratio (N): The transformer turns ratio is derived from the equations used to define the power transfer interval t_{34} in addition to the maximum off-time, t_{03}. While this may first seem like an iterative process, it simplifies to the volt-second product relationship described. The general equations are listed below.

The turns ratio N is derived by substituting $N \cdot V_O$ for the output voltage V_O in the power transfer interval t_{34} equation. Solving for N results in the relationship:

$$N V_O / V_{IN} = t_{34} / (t_{01} + t_{12} + t_{23} + t_{34})$$

$$N = \frac{V_{IN\min} t_{34}}{V_O t_{04}}$$

The transformer magnetizing and leakage inductance is part of the resonant inductance. This requires adjustment of the resonant inductor value, or both the resonant tank impedance Z_R and frequency ω_R will be off-target. One

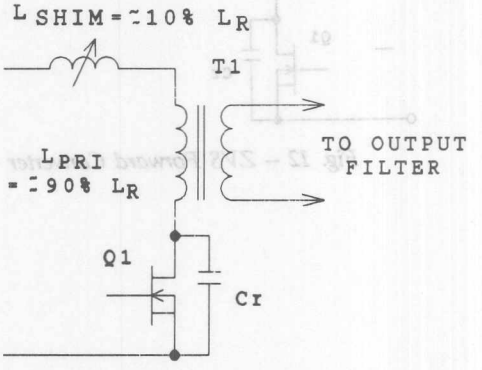


Fig. 11 -- Transformer Inductance "Shim"

option is to design the transformer inductance to be exactly the required resonant inductance, thus eliminating one component. For precision applications, the transformer inductance should be made slightly smaller than required, and "shimmed" up with a small inductor.

Expanding ZVS to Other Topologies

ZVS Forward Converter - Single Ended: The single ended forward converter can easily be configured for zero voltage switching with the addition of a resonant capacitor across the switch. Like the buck regulator, there is a high voltage excursion in the off state due to resonance, the amplitude of which varies with line and load. The transformer can be designed so that its magnetizing and leakage inductance equals the required resonant inductance. This simplifies transformer reset and eliminates one component. A general circuit diagram is shown in Fig. 12 below. The associated waveforms for when L_{PRI} equals L_R are shown in Fig. 13.

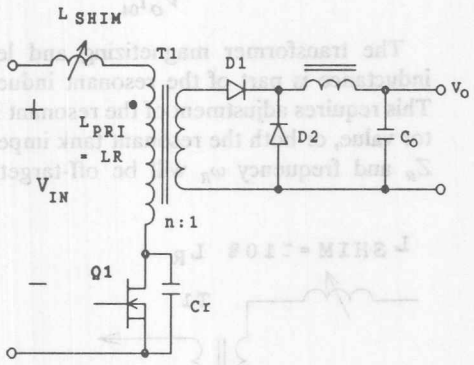


Fig. 12 -- ZVS Forward Converter

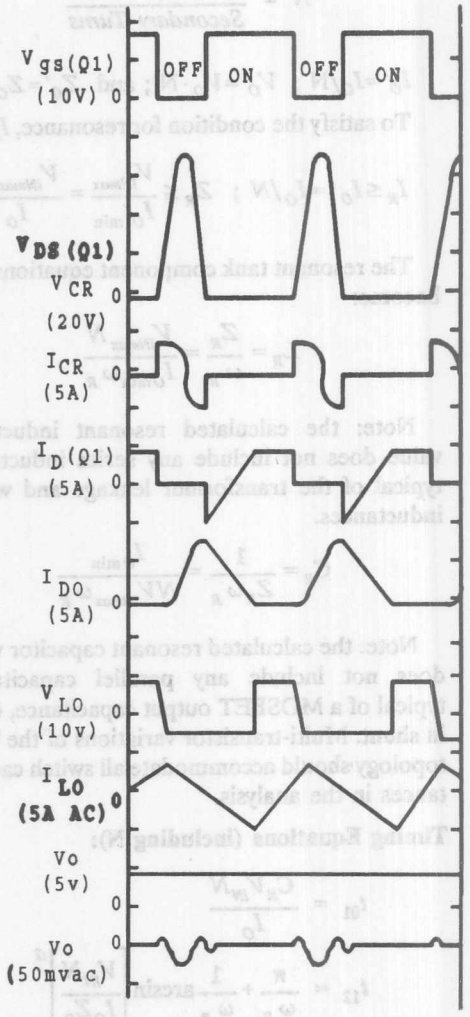


Fig. 13 -- Forward Converter Waveforms

ZVS Clamped Configurations -- Half and Full Bridge Topologies: Zero voltage switching can be extended to multiple switch topologies for higher power levels, specifically the half and full bridge configurations. While the basic operation of each time interval remains similar, there is a difference in the resonant t_{12} interval.

While single switch converters have high off-state voltage, the bridge circuits clamp the switch peak voltages to the DC input rails, reducing the switch voltage stress. This alters the duration of the off segment of the resonant interval, since the opposite switch(es) must be activated long before the resonant cycle is completed. In fact, the opposite switch(es) should be turned on immediately after their voltage is clamped to the rails, where their drain to source voltage equals zero. If not, the resonant tank will continue to ring and return the switch voltage to its starting point, the opposite rail. Additionally, this off period varies with line and load changes.

Examples of this are demonstrated in Figs. 14 and 15. To guarantee true zero voltage switching, it is recommended that the necessary sense circuitry be incorporated.

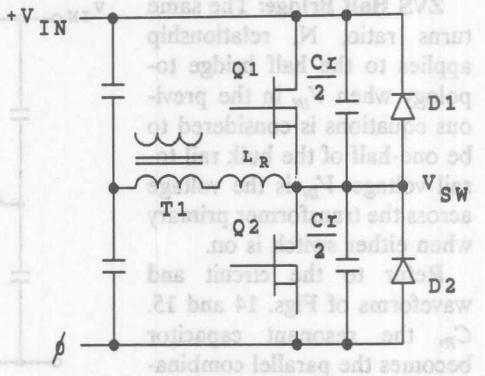


Fig. 14 -- Clamped ZVS Configuration

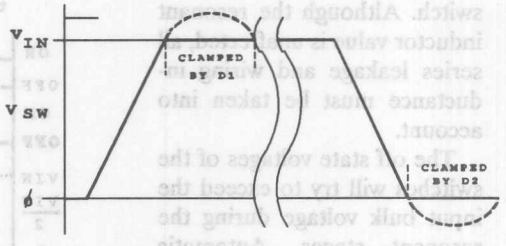


Fig. 15 -- Clamped ZVS Waveforms

ZVS Half Bridge: The same turns ratio, N, relationship applies to the half bridge topology when V_{IN} in the previous equations is considered to be one-half of the bulk rail-to-rail voltage. V_{IN} is the voltage across the transformer primary when either switch is on.

Refer to the circuit and waveforms of Figs. 14 and 15. C_R, the resonant capacitor becomes the parallel combination of the two resonant capacitors, the ones across each switch. Although the resonant inductor value is unaffected, all series leakage and wiring inductance must be taken into account.

The off state voltages of the switches will try to exceed the input bulk voltage during the resonant stages. Automatic clamping to the input bulk rails occurs by the MOSFET body diode, which can be externally shunted with a higher performance variety. Unlike the forward converter which requires a core reset equal to the applied volt second product, the bidirectional switching of the half (and full) bridge topology facilitate automatic core reset during consecutive switching cycles [11,12].

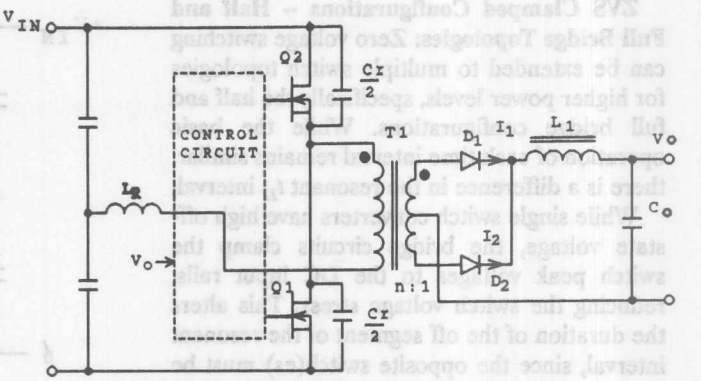


Fig. 16 -- ZVS Half Bridge Circuit

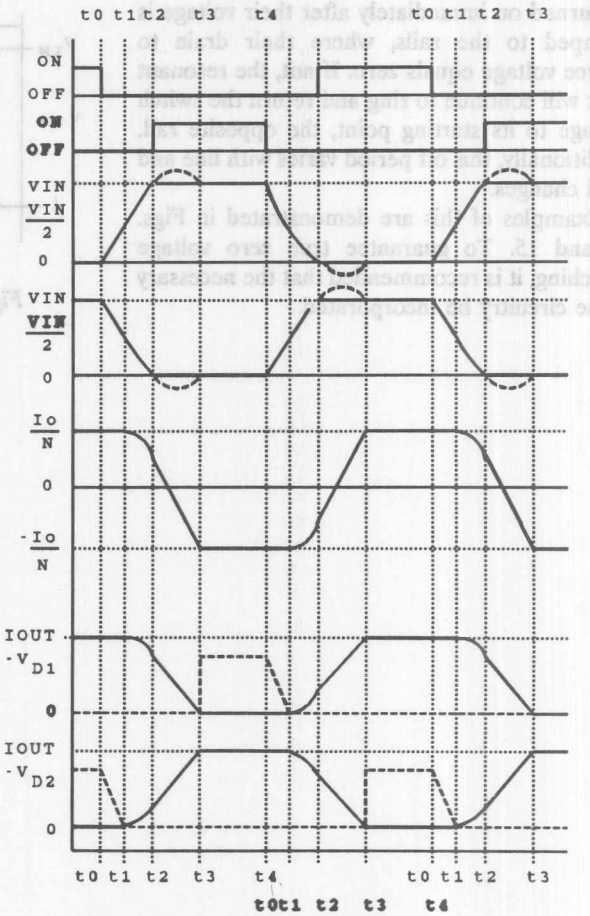


Fig. 17 -- ZVS Half Bridge Waveforms

ZVS Full Bridge: The equations represented for the forward topology apply equally well for one conversion cycle of the full bridge topology, including the transformer turns ratio. Since the resonant capacitors located at each switch are "in-circuit" at all times, the values should be adjusted accordingly. As with the half bridge converter, the resonant capacitors' voltage will exceed the bulk rails, and clamping via the FET body diodes or external diodes to the rails is common [13].

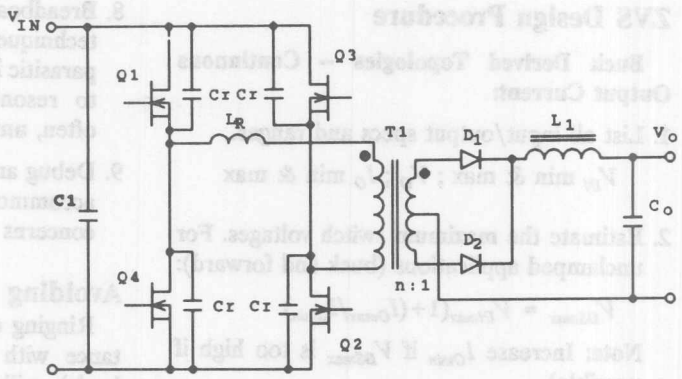


Fig. 18 -- ZVS Full Bridge Circuit

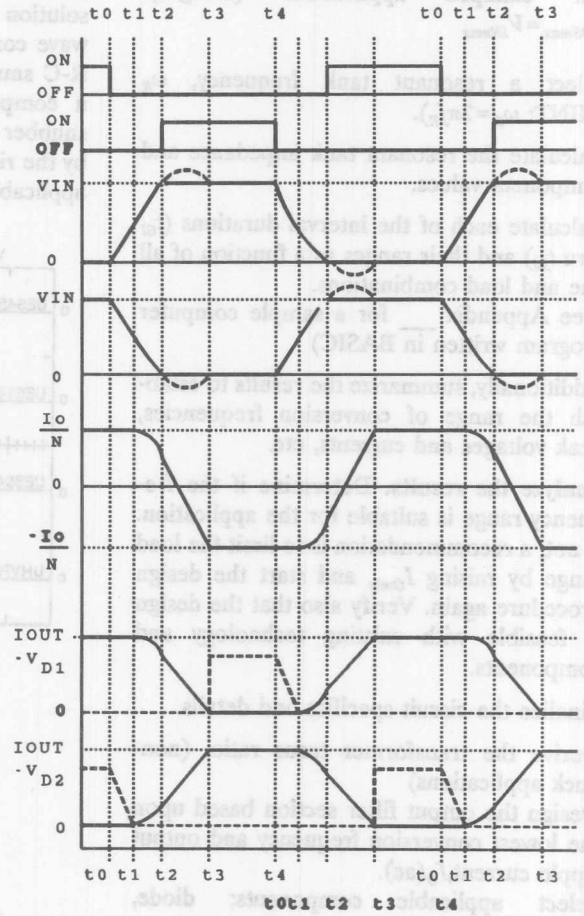


Fig. 19 -- ZVS Full Bridge Waveforms

ZVS Design Procedure

Buck Derived Topologies -- Continuous Output Current:

1. List all input/output specs and ranges.

   V_{IN} min & max ; V_O ; I_O min & max

2. Estimate the maximum switch voltages. For unclamped applications (buck and forward):

   $V_{DSmax} = V_{INmax}(1+(I_{Omax}/I_{Omin})$

   Note: Increase I_{Omin} if V_{DSmax} is too high if possible).

   For clamped applications (bridges): $V_{DSmax}=V_{INmax}$

3. Select a resonant tank frequency, ω_R (HINT: $\omega_R=2\pi f_R$).

4. Calculate the resonant tank impedance and component values.

5. Calculate each of the interval durations (t_{01} thru t_{34}) and their ranges as a function of all line and load combinations.
   (See Appendix ___ for a sample computer program written in BASIC)

   Additionally, summarize the results to establish the range of conversion frequencies, peak voltages and currents, etc.

6. **Analyze the results.** Determine if the frequency range is suitable for the application. If not, a recommendation is to limit the load range by raising I_{Omin} and start the design procedure again. Verify also that the design is feasible with existing technology and components.

7. Finalize the circuit specifics and details.

- ☐ Derive the transformer turns ratio. (non-buck applications)
- ☐ Design the output filter section based upon the lowest conversion frequency and output ripple current,I_O(ac).
- ☐ Select applicable components; diode, MOSFET etc.

8. Breadboard the circuit **carefully** using RF techniques wherever possible. Remember -- parasitic inductances and capacitances prefer to resonate upon stimulation, and quite often, **unfavorably.**

9. Debug and modify the circuit as required to accommodate component parasitics, layout concerns or packaging considerations.

Avoiding Parasitics

Ringing of the catch diode junction capacitance with circuit inductance (and package leads) will significantly degrade the circuit performance. Probably the most common solution to this everyday occurrance in square wave converters is to shunt the diode with an R-C snubber. Although somewhat dissipative, a compromise can be established between snubber losses and parasitic overshoot caused by the ringing. Unsnubbed examples of various applicable diodes are shown in Fig. 20 below.

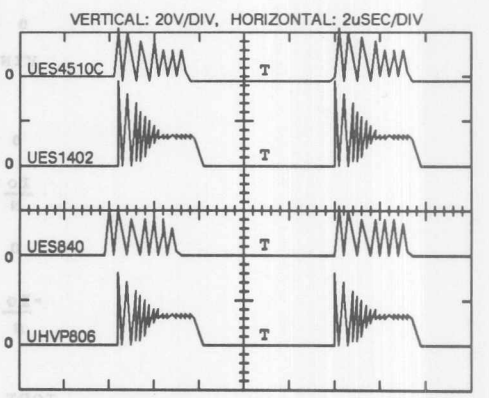


Fig. 20 -- Catch Diode Ringing

Multiresonant ZVS Conversion

Another technique to avoid the parasitic resonance involving the catch diode capacitance is to shunt it with a capacitor much larger than the junction capacitance. Labelled C_D, this element introduces favorable switching characteristics for both the switch and catch diode. The general circuit diagram and associated waveforms are showm below, but will not be explored further in this presentation [14,15].

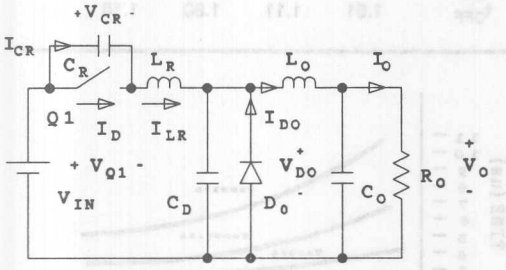


Fig. 21 -- Multiresonant ZVS Circuit

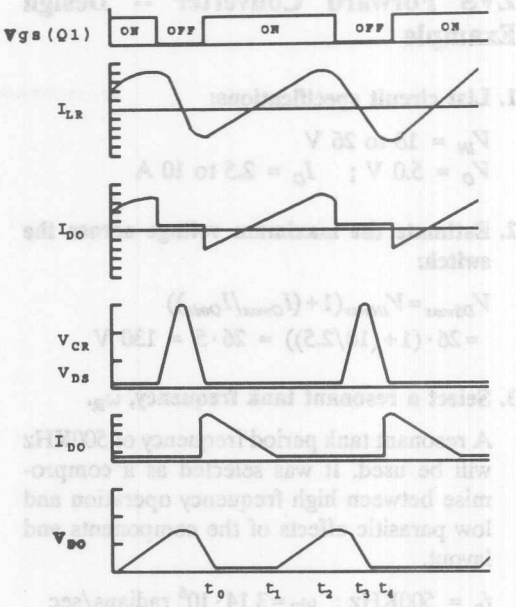


Fig. 22 -- Multiresonant Waveforms

Current Mode Controlled ZVS Conversion

Variable frequency power converters can also benefit from the use of current mode control. Two loops are used to determine the precise ON time of the power switch -- an "outer" voltage feedback loop, and an "inner" current sensing loop. The advantage to this approach is making the power stage operate as a voltage controlled current source. This eliminates the two pole output inductor characteristics in addition to providing enhanced dynamic transient response.

Principles of operation. Two control ICs are utilized in this design example. The UC3843A PWM performs the current mode control by providing an output pulse width determined by the two control loop inputs. This pulse width, or repetition rate is used to set the conversion period of the UC3864 ZVS resonant controller. Rather than utilize its voltage controlled oscillator to generate the conversion period, it is determined by the UC3843A output pulse width.

Zero voltage switching is performed by the UC3864 one-shot timer and zero crossing detection circuitry. When the resonant capacitor voltage crosses zero, the UC3864 output goes high. This turns ON the power switch and recycles the UC3843A to initiate the next current mode controlled period. The UC3864 fault circuitry functions, but its error amplifier and VCO are not used.

ZVS Forward Converter -- Design Example

1. List circuit specifications:

V_{IN} = 18 to 26 V
V_O = 5.0 V ; I_O = 2.5 to 10 A

2. Estimate the maximum voltage across the switch:

$V_{DSmax} = V_{INmax}(1+(I_{Omax}/I_{Omin}))$
$= 26 \cdot (1+(10/2.5)) = 26 \cdot 5 = 130$ V

3. Select a resonant tank frequency, ω_R.

A resonant tank period frequency of 500KHz will be used. It was selected as a compromise between high frequency operation and low parasitic effects of the components and layout.

f_R = 500KHz ; $\omega_R = 3.14 \cdot 10^6$ radians/sec

4. Calculate the resonant tank impedance and component values.

Resonant tank impedance, $Z_R > V_{INmax}/I_{Omin}$

To accommodate the voltage drop across the MOSFET, calculate $V_{DS(on)min}$, which equals $R_{DS(on)}I_{Omin} = 0.8 \cdot 2.5 = 2$V

$Z_R = (V_{INmax} - V_{DSmin})/I_{Omin}$

$Z_R = (26-2)/2.5 = 10\ \Omega$

$C_R = 1/(Z_R\omega_R) = 1/(10 \cdot 3.14 \cdot 10^6) = 32$nF

$L_R = Z_R/\omega_R = 10/3.34 \cdot 10^6 = 3.18\mu$H

5. Calculate each of the interval durations (t_{01} thru t_{34}) and ranges as they vary with line and load changes.

The zero voltage switched buck converter "gain" in kiloHertz per volt of V_{IN} and kHz per amp of I_O can be evaluatated over the specified ranges. A summary of these follows:

Table VI - Interval Durations vs. Line & Load

	V_{IN}=18 I_O=2.5	V_{IN}=18 I_O=10	V_{IN}=26 I_O=2.5	V_{IN}=26 I_O=10
t_{10}	0.217	0.055	0.314	0.078
t_{12}	1.29	1.06	1.49	1.08
t_{23}	0.93	3.72	0.64	2.58
t_{34}	1.39	6.68	0.78	1.78
T_{CONV}	3.83	11.51	3.23	5.52
f_{CONV}	261kHz	87kHz	310kHz	181kHz
Transistor Switch Durations:				
t_{ON}	2.32	10.4	1.42	4.36
t_{OFF}	1.51	1.11	1.80	1.16

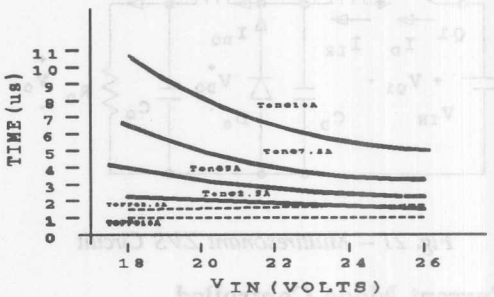


Fig. 23 - Switch Times vs. Line & Load

df_{CONV}/dV_{IN} vs I_O

I_O =	2.5A	5A	7.5A	10A	avg
df/dV =	6.1	11.2	11.9	11.7	10.2

Highest "gain" (11.9 kHz/V) occurs near full load.

df_{CONV}/dI_O vs V_{IN}

V_{IN} =	18	20	22	24	26	avg
df/dV =	23.3	22.1	20.5	18.8	17.3	20.4

Highest "gain" (23.3 kHz/A) occurs at V_{INmin}.

It may be necessary to use the highest gain values to design the control loop compensation for stability over all operating conditions. While this may not optimize the loop transient response for all operating loads, it will guarantee stability over the extremes of line and load.

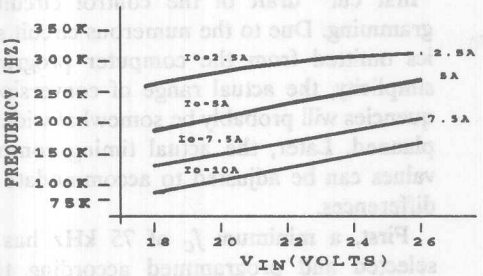


Fig. 24 - Conversion Freq. vs. Line & Load

6. Analyze the results.

The resonant component values, range of conversion frequencies, peak voltage and current ratings seem well within the practical limits of existing components and technology.

7. Finalize the circuit specifics and details based on the information obtained above.

A. Output Filter Section: Select L_O and C_O for operation at the lowest conversion frequency and designed ripple current.

B. Heatsink Requirements: An estimate of the worst case power dissipation of the power switch and output catch diode can be made over line and load ranges.

C. Control Circuit: The UC3861-64 series of controllers will be examined and programmed per the design requirements.

Programming the Control Circuit

One-shot: Accommodating Off-time Variations. The switch off-time varies with line and load by ≈ ± 35% in this design example using ideal components. Accounting for initial tolerances and temperature effects results in an much wider excursion. For all practical purposes, a true fixed off-time technique will *not* work.

Incorporated into the UC3861 family of ZVS controllers is the ability to modulate this off-

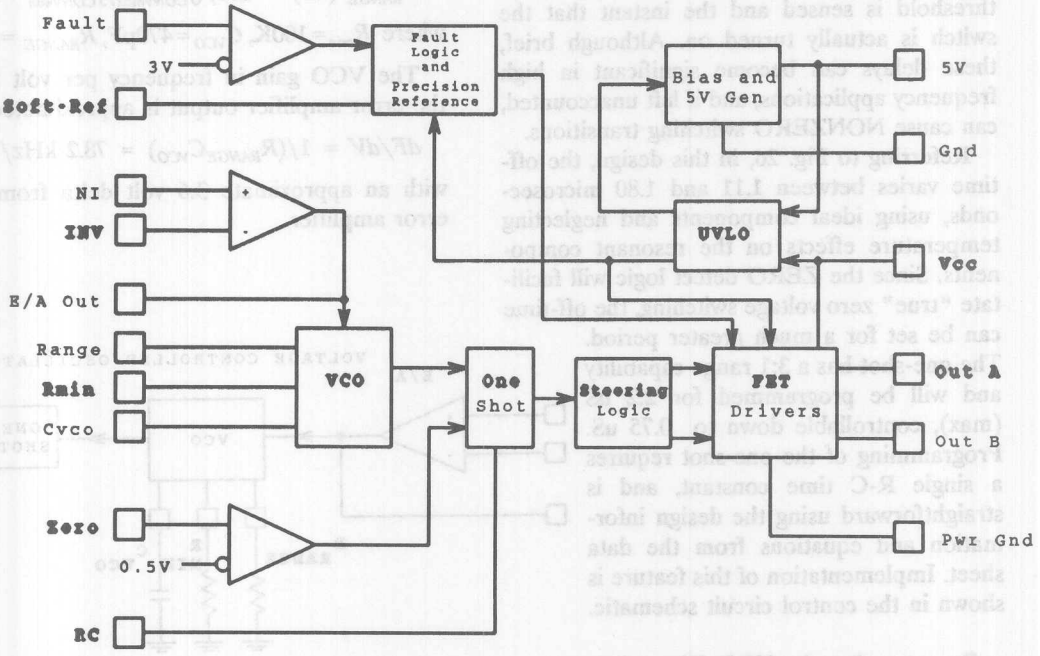


Fig. 25 -- The UC3861-64 ZVS Contollers -- Block Diagram

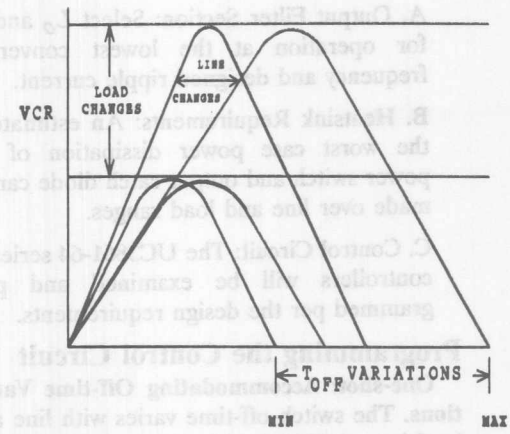


Fig. 26 -- C_R Volts & Off-time vs. Line & Load

time. Initially, the one-shot is programmed for the maximum off-time, and modulated via the ZERO detection circuitry. The switch drain-source voltage is sensed and scaled to initiate turn-on when the precision 0.5V threshold is crossed. This offset was selected to accommodate propogation delays between the instant the threshold is sensed and the instant that the switch is actually turned on. Although brief, these delays can become significant in high frequency applications, and if left unaccounted, can cause NONZERO switching transitions.

Referring to Fig. 26, in this design, the off-time varies between 1.11 and 1.80 microseconds, using ideal components and neglecting temperature effects on the resonant components. Since the ZERO detect logic will facilitate "true" zero voltage switching, the off-time can be set for a much greater period. The one-shot has a 3:1 range capability and will be programmed for 2.2 uS (max), controllable down to 0.75 uS. Programming of the one-shot requires a single R-C time constant, and is straightforward using the design information and equations from the data sheet. Implementation of this feature is shown in the control circuit schematic.

Programming the VCO. The calculated range of conversion frequencies spans 87 to 310 kHz. These values will be used for this "first cut" draft of the control circuit programming. Due to the numerous circuit specifics omitted from the computer program for simplicity, the actual range of conversion frequencies will probably be somewhat wider than planned. Later, the actual timing component values can be adjusted to accommodate these differences.

First, a minimum f_C of 75 kHz has been selected and programmed according to the following equation:

$$F_{VCOmin} = 3.6/(R_{min}C_{VCO})$$

The maximum f_C of 350 kHZ is programmed by:

$$F_{VCOmax} = 3.6/(R_{min} \parallel R_{range}) \cdot C_{VCO}$$

Numerous values of R_{min} and C_{VCO} will satisfy the equations. The procedure can be simplified by letting R_{min} equal 100K.

$$C_{VCO}\ (\mu F) = 0.036/f_{min}\ (\text{kHz})$$

$$R_{RANGE}\ (\text{k}\Omega) = 100/(f_{CONVmax}/f_{CONVmin} - 1)$$

where R_{min}=100K, C_{VCO}=470pF, R_{RANGE} = 27K

The VCO gain in frequency per volt from the error amplifier output is approximated by:

$$dF/dV = 1/(R_{RANGE}C_{VCO}) = 78.2\ \text{kHz/V}$$

with an approximate 3.6 volt delta from the error amplifier.

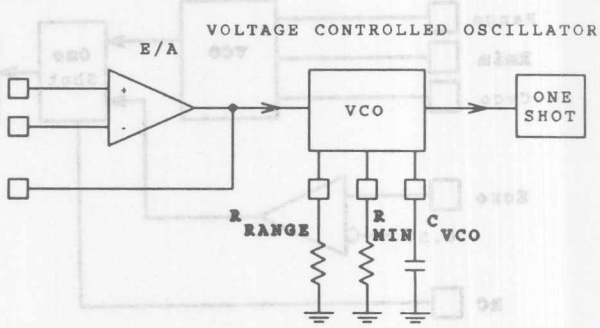


Fig. 27 -- E/A - VCO Block Diagram

Fault Protection - Soft Start & Restart Delay: One of the unique features of the UC 3861 family of resonant mode controllers can be found in its fault management circuitry. A single pin connection interfaces with the soft start, restart delay and programmable fault mode protection circuits. In most applications, one capacitor to ground will provide full protection upon power-up and during overload conditions. Users can reprogram the timing relationships or add control features (latch off following fault, etc) with a single resistor.

Selected for this application is a 1 uF soft-restart capacitor value, resulting in a soft-start duration of 10 ms and a restart delay of approximately 200 ms. The preprogrammed ratio of 19:1 (restart delay to soft start) will be utilized, however the relevant equations and relationships have also been provided for other applications. Primary current will be utilized as the fault trip mechanism, indicative of an overload or short circuit current condition. A current transformer is incorporated to maximize efficiency when interfacing to the three volt fault threshold.

Optional Programming of T_{SS} and T_{RD} :

Soft Start: $T_{SS} = C_{SR} \cdot 10K$

Restart Delay: $T_{RD} = C_{SR} \cdot 190K$

Timing Ratio: $T_{RD}:T_{SS} \approx 19:1$

Gate Drive: Another unique feature of the UC 3861-64 family of devices is the optimal utilization of the silicon devoted to output totem pole drivers. Each controller uses two pins for the A and B outputs which are internally configured to operate in either unison or in an alternating configuration. Typical performance for these 1 Amp peak totem pole outputs shows 30 ns rise and fall times into 1nF.

Loop Compensation -- General Information. The ZVS technique is similar to that of conventional voltage mode square wave conversion which utilizes a single voltage feedback loop. Unike the dual loop system of current mode control, the ZVS output filter section exhibits

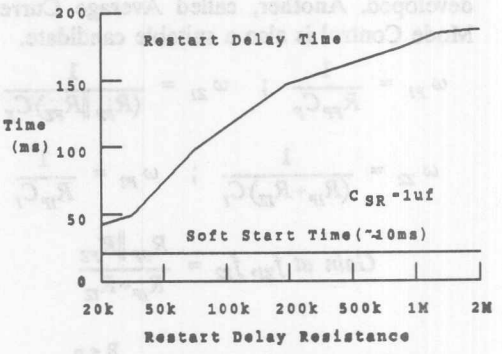


Fig. 28 -- Programming T_{SS} and T_{RD}

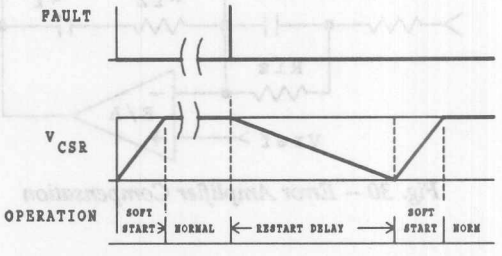


Fig. 29 -- Fault Operational Waveforms

a two pole-zero pair and is compensated accordingly. Generally, the overall loop is designed to cross zero dB at a frequency below one-tenth that of the switching frequency. In this variable frequency converter, the lowest conversion frequency will apply, corresponding to approximately 85 KHz, for a zero crossing of 8.5 KHz. Compensation should be optimized for the highest low frequency gain in addition to ample phase margin at crossover. Typical examples utilize two zeros in the error amplifier compensation at a frequency equal to that of the output filter's two pole break. An additional high frequency pole is placed in the loop to combat the zero due to the output capacitance ESR, assuming adequate error amplifier gain-bandwidth.

A noteworthy alternative is the use of a two loop approach which is similar to current mode control, eliminating one of the output poles. One technique known as Multi-Loop Control for Quasi-Resonant Converters [18] has been

developed. Another, called Average Current Mode Control is also a suitable candidate.

$$\omega_{P1} = \frac{1}{R_{FP}C_F} \; ; \; \omega_{Z1} = \frac{1}{(R_{FP} \| R_{FZ})C_F}$$

$$\omega_{Z2} = \frac{1}{(R_{IP}+R_{IZ})C_I} \; ; \; \omega_{P2} = \frac{1}{R_{IP}C_I}$$

$$Gain\ at\ f_{Z1}, f_{Z2} = \frac{R_{FP} \| R_{FZ}}{R_{IP}+R_{IZ}}$$

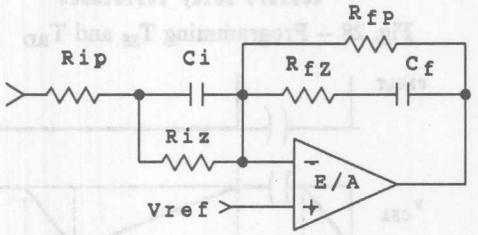


Fig. 30 -- Error Amplifier Compensation

Summary

The zero voltage switched quasi-resonant technique is applicable to most power conversion designs, but is most advantageous to those operating from a high voltage input. In these applications, losses associated with discharging of the MOSFET output capacitance can be significant at high switching frequencies, impairing efficiency. Zero voltage switching avoids this penalty by negating the drain-to-source, "off-state" voltage via the resonant tank.

A high peak voltage stress occurs across the switch during resonance in the buck regulator and single switch forward converters. Limiting this excursion demands limiting the useful load range of the converter as well, an unacceptable solution in certain applications. For these situations, the zero voltage switched multi-resonant approach [14,15] could prove more beneficial than the quasi-resonant ZVS variety.

Significant improvements in efficiency can be obtained in high voltage, half and full bridge ZVS applications when compared to their square wave design complements. Clamping of

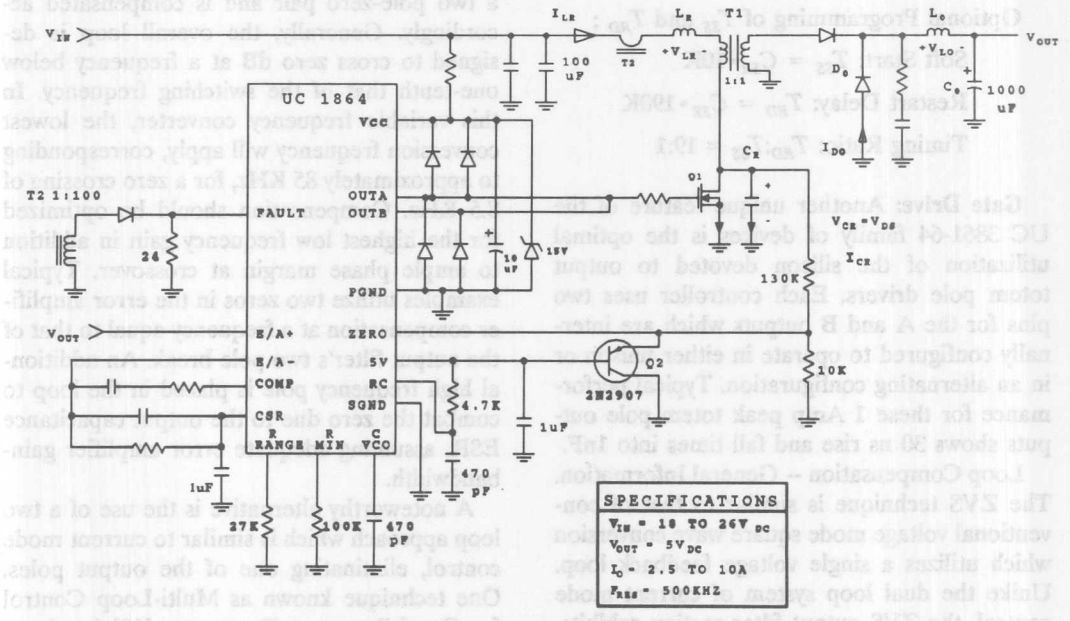


Fig. 31 -- Zero Voltage Switched Forward Converter

the peak resonant voltage to the input rails avoids the high voltage overshoot concerns of the single switch converters, while transformer reset is accomplished by the bidirectional switching. Additionally, the series transformer primary and circuit inductances can beneficial, additives in the formation of the total resonant inductor value. This not only reduces size, but incorporates the detrimental parasitic generally snubbed in square wave designs, further enhancing efficiency.

A new series of control ICs has been developed specifically for the zero voltage switching techniques with a list of features to facilitate lossless switching transitions with complete fault protection. The multitude of functions and ease of programmability greatly simplify the interface to this new generation of power conversion techniques; those developed in response to the demands for increased power density and efficiency.

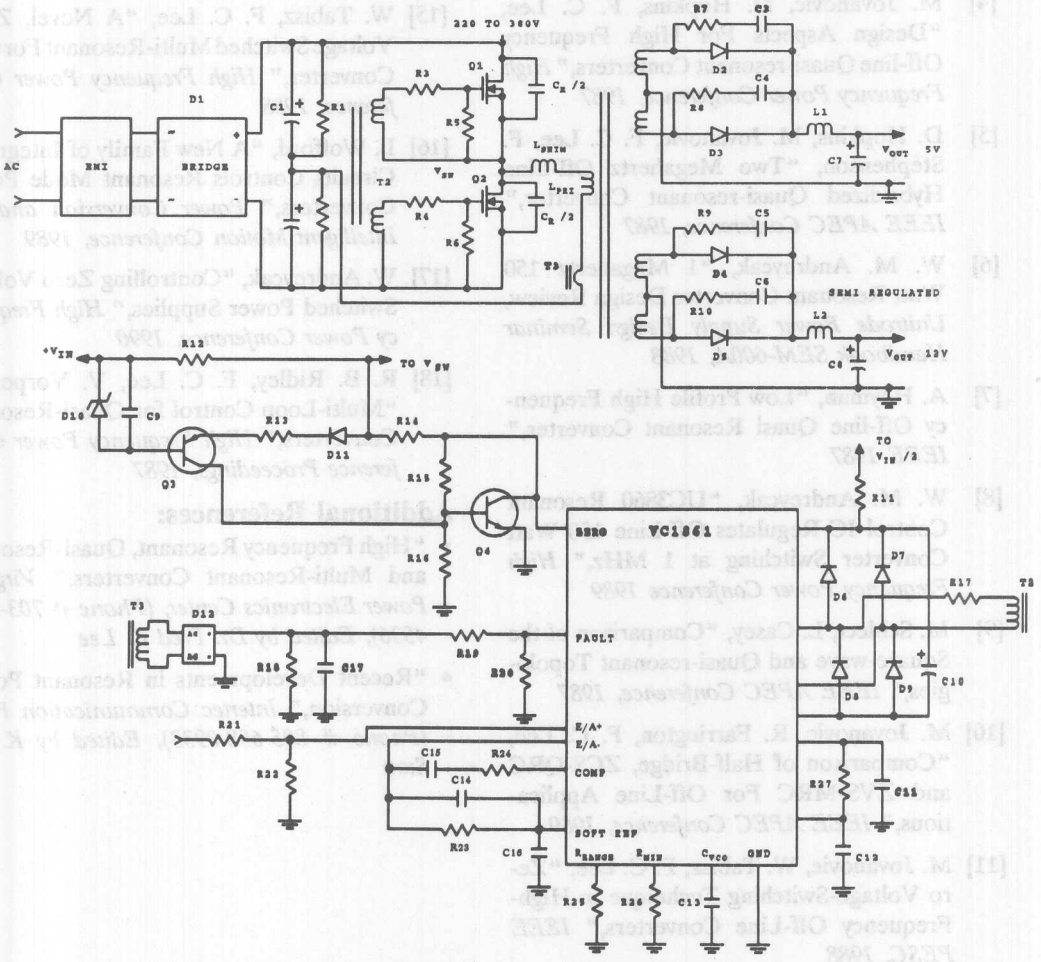


Fig. 32 -- Zero Voltage Switched Half-Bridge Converter

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- "Recent Developments in Resonant Power Conversion," *Intertec Communication Press (Phone # 805-658-0933), Edited by K. Kit Sum*

```
10 ' Zero Voltage Switching Calculations and Equations
20 ' Using the Continuous Current Buck Topology
30 ' in a Typical DC/DC Converter Power Supply Application
40 '
50 PRINTER$ = "lpt1:": ' Printer at parallel port #1 **********
60 '
70 ' Summary of Variables and Abbreviations
80 '
90 ' Cr = Resonant Capacitor
100 ' Lr = Resonant Inductor
110 ' Zr = Resonant Tank Impedance
120 ' Fres = Resonant Tank Frequency (Hz)
130 '
140 ' VImin = Minimum DC Input Voltage
150 ' VImax = Maximum DC Input Voltage
160 ' Vdson = Mosfet On Voltage = Io*Rds
170 ' Rds = Mosfet On Resistance
180 ' Vdsmax = Peak MOSFET Off State Voltage
190 ' Vo = DC Output Voltage
200 ' Vdo = Output Diode Voltage Drop
210 ' Iomax = Maximum Output Current
220 ' Iomin = Minimum Output Current
230 '
240 ' Start with parameters for low voltage dc/dc buck regulator
250 '
260 ' ****Define 5 Vi and 5 Io data points ranging from min to max*****
270 ' (Suggestion: With broad ranges, use logarithmic spread)
280 DATA 18,20,22,24,27 : 'Vi data
290 DATA 2.5,4,6,8,10 : 'Io data
300 FRES = 500000!
310 VO = 5!
320 VDO = .8
330 RDS = .8
340 SAFT = .95
350 '
360 FOR J = 1 TO 5: READ VI(J): NEXT
370 FOR K = 1 TO 5: READ IO(K): NEXT
380 CLS
390 PRINT "For output to screen, enter 'S' or 's',"
400 INPUT "Otherwise output will be sent to printer : ", K$
410 IF K$ = "S" OR K$ = "s" THEN K$ = "scrn:" ELSE K$ = PRINTER$
420 OPEN K$ FOR OUTPUT AS #1: CLS
430 PRINT #1, "================================================"
440 PRINT #1, " Zero Voltage Switching Times (uSec) vs. Vi, Io"
450 PRINT #1, "================================================"
460 '
```

```
470 ' =========HERE GOES==========
480 '
490 VIMAX = VI(5): IOMIN = IO(1): IOMAX = IO(5)
500 ZR = (VIMAX - (RDS * IOMIN)) / (IOMIN * SAFT)
510 WR = 6.28 * FRES
520 CR = 1 / (ZR * WR)
530 LR = ZR / WR
540 '
550 FOR J = 1 TO 5: VI = VI(J)
560   PRINT #1, USING "                Input Voltage = ###.## V"; VI
570   FOR K = 1 TO 5: IO = IO(K)
580     RSIN = (VI / (IO * ZR)):   VDSON = RDS * IO
590 '
600     D(0, K) = IO * .000001:  ' Compensate for later mult. by 10^6
610     D(1, K) = (CR * VI) / IO: 'dt01
620     D(2, K) = (3.14 / WR) + (1 / WR) * ATN(RSIN / (1 - RSIN ^ 2)): 'dt12
630     D(3, K) = (2 * LR * IO) / VI: 'dt23
640     D(6, K) = D(1, K) + D(2, K) + D(3, K): ' dt03
650     D(4, K) = ((VO + VDO) * D(6, K)) / ((VI - VDSON) - (VO + VDO)): 'dt34
660     D(5, K) = D(1, K) + D(2, K) + D(3, K) + D(4, K): 'Tconv
670   NEXT K
680 '
690   PAR$(0) = "Io (A) ="
700   PAR$(1) = "dt01   ="
710   PAR$(2) = "dt12   ="
720   PAR$(3) = "dt23   ="
730   PAR$(4) = "dt34   ="
740   PAR$(5) = "Tconv  ="
750   PAR$(6) = "dt03   ="
760 '
770   FOR P = 0 TO 6
780     PRINT #1, PAR$(P);
790     FOR K = 1 TO 5
800       PRINT #1, USING " ####.###"; D(P, K) * 1000000!;
810     NEXT K: PRINT #1,
820   NEXT P
830 PRINT #1,
840 NEXT J
850 '
860 PRINT #1, "Additional Information:"
870 PRINT #1, "Zr(Ohms) ="; INT(1000! * ZR) / 1000
880 PRINT #1, "wR(KRads)="; INT(WR / 1000)
890 PRINT #1, "Cr(nF)   ="; INT((1000 * CR) / 10 ^ -9) / 1000
900 PRINT #1, "Lr(uH)   ="; INT((1000 * LR) / 10 ^ -6) / 1000
910 PRINT #1, "Vdsmax   ="; VIMAX * (1 + IOMAX / IOMIN)
920 END
```

```
================================================
 Zero Voltage Switching Times (uSec) vs. Vi, Io
================================================
                    Input Voltage =  18.00 V
Io (A) =    2.500     4.000     6.000     8.000    10.000
dt01   =    0.218     0.136     0.091     0.068     0.054
dt12   =    1.290     1.153     1.096     1.070     1.056
dt23   =    0.931     1.490     2.235     2.980     3.725
dt34   =    1.387     1.791     2.682     4.118     6.677
Tconv  =    3.825     4.571     6.103     8.236    11.511
dt03   =    2.439     2.780     3.421     4.118     4.835

                    Input Voltage =  20.00 V
Io (A) =    2.500     4.000     6.000     8.000    10.000
dt01   =    0.242     0.151     0.101     0.076     0.061
dt12   =    1.339     1.175     1.108     1.079     1.062
dt23   =    0.838     1.341     2.011     2.682     3.352
dt34   =    1.150     1.406     1.987     2.852     4.186
Tconv  =    3.569     4.074     5.207     6.688     8.661
dt03   =    2.419     2.667     3.220     3.836     4.475

                    Input Voltage =  22.00 V
Io (A) =    2.500     4.000     6.000     8.000    10.000
dt01   =    0.266     0.166     0.111     0.083     0.067
dt12   =    1.390     1.198     1.120     1.087     1.069
dt23   =    0.762     1.219     1.829     2.438     3.048
dt34   =    0.988     1.153     1.557     2.136     2.958
Tconv  =    3.406     3.737     4.616     5.744     7.141
dt03   =    2.418     2.584     3.060     3.608     4.183

                    Input Voltage =  24.00 V
Io (A) =    2.500     4.000     6.000     8.000    10.000
dt01   =    0.290     0.182     0.121     0.091     0.073
dt12   =    1.442     1.223     1.133     1.096     1.075
dt23   =    0.698     1.117     1.676     2.235     2.794
dt34   =    0.870     0.975     1.268     1.682     2.241
Tconv  =    3.301     3.498     4.199     5.103     6.183
dt03   =    2.431     2.522     2.930     3.421     3.941

                    Input Voltage =  27.00 V
Io (A) =    2.500     4.000     6.000     8.000    10.000
dt01   =    0.327     0.204     0.136     0.102     0.082
dt12   =    0.516     1.264     1.153     1.109     1.085
dt23   =    0.621     0.993     1.490     1.987     2.483
dt34   =    0.442     0.793     0.983     1.253     1.604
Tconv  =    1.906     3.254     3.763     4.451     5.254
dt03   =    1.464     2.461     2.780     3.198     3.650

Additional Information:
Zr(Ohms) = 10.526
WR(KRads)= 3140
Cr(nF)   = 30.254
Lr(uH)   = 3.352
Vdsmax   = 135
```


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Average Current Mode Control of Switching Power Supplies

Lloyd Dixon

Abstract

Current mode control as usually implemented in switching power supplies actually senses and controls peak inductor current. This gives rise to many serious problems, including poor noise immunity, a need for slope compensation, and peak-to-average current errors which the inherently low current loop gain cannot correct. Average current mode control eliminates these problems and may be used effectively to control currents other than inductor current, allowing a much broader range of topological application.

General Perspective

Current mode control is a two-loop system as shown in the simple example of Fig. 1. The switching power supply inductor is "hidden" within the inner current control loop. This simplifies the design of the outer voltage control loop and improves power supply performance in many ways, including better dynamics. The objective of this inner loop is to control the state-space averaged inductor current, but in practice the instantaneous peak inductor current is the basis for control. (Switch current --equal to inductor current during the "on" time--is often sensed.) If the inductor ripple current is small, peak inductor current control is nearly equivalent to average inductor current control.

In a conventional switching power supply employing a buck derived topology, the inductor is in the output. Current mode control then is actually output current control, resulting in many performance advantages. On the other hand, in a high power factor preregulator using the boost topology, the inductor is in the input. Current mode control then controls input current, allowing it to be easily conformed to the desired sinusoidal waveshape.

Peak Current Mode Control Problems

Poor noise immunity. The peak method of inductor current control functions by comparing the upslope of inductor current (or switch current) to a current program level set by the outer loop–see Fig. 1. The comparator turns the power switch off when the instantaneous current reaches the desired level. The current ramp is usually quite small compared to the programming level, especially when V_{IN} is low. As a result, this method is extremely susceptible to noise. A noise spike is generated each time the switch turns on. A fraction of a volt coupled into the control circuit can cause it to turn off immediately, resulting in a subharmonic operating mode with much greater ripple. Circuit layout and bypassing are critically important to successful operation.

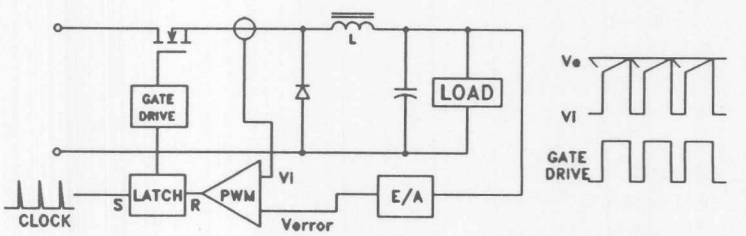


Fig. 1 - Peak Current Mode Control Circuit and Waveforms

Slope compensation required. The peak current mode control method is inherently unstable at duty ratios exceeding 0.5,

resulting in sub-harmonic oscillation. A compensating ramp (with slope equal to the inductor current downslope) is usually applied to the comparator input to eliminate this instability. In a buck regulator the inductor current downslope equals V_O/L. With V_O constant, as it usually is, the compensating ramp is fixed and easy to calculate–but it does complicate the design. With a boost regulator in a high power factor application, the downslope of inductor current equals $(V_{IN}-V_O)/L$ and thus varies considerably as the input voltage follows the rectified sine waveform. A fixed ramp providing adequate compensation will overcompensate much of the time, with resulting performance degradation and increased distortion.

Peak to average current error. The peak to average current error inherent in the peak method of inductor current control is usually not a serious problem in conventional buck-derived power supplies. This is because inductor ripple current is usually much smaller than the average full load inductor current, and because the outer voltage control loop soon eliminates this error.

In high power factor boost preregulators the peak/avg error is very serious because it causes distortion of the input current waveform. While the peak current follows the desired sine wave current program, the average current does not. The peak/avg error becomes much worse at lower current levels, especially when the inductor current becomes discontinuous as the sine wave approaches zero every half cycle. To achieve low distortion, the peak/avg error must be small. This requires a large inductor to make the ripple current small. The resulting shallow inductor current ramp makes the already poor noise immunity much worse.

Topology problems. Conventional peak current mode control actually controls inductor current. As normally used for output current control, it is most effective when applied to a buck regulator where the inductor is in the output. But for flyback or boost topologies the inductor is not in the output, the *wrong* current is controlled, and much of the advantage of current mode control is lost.

Likewise, the boost topology with its inductor at the input is well suited for input current control in a high power factor preregulator, but buck and flyback topologies are not well suited because the inductor is not in the input and the wrong current is controlled.

Average Current Mode Control

Peak current mode control operates by directly comparing the actual inductor current waveform to the current program level (set by the outer loop) at the two inputs of the PWM comparator. This current loop has low gain and so cannot correct for the deficiencies noted above.

Referring to Fig. 2, the technique of average current mode control overcomes these problems by introducing a high gain integrating current error amplifier (*CA*) into the current loop. A voltage across R_P (set by the outer loop) represents the desired current program level. The voltage across current sense resistor R_S represents actual inductor current. The difference, or current error, is amplified and compared to a large amplitude sawtooth (oscillator ramp) at the PWM comparator inputs.

The gain-bandwidth characteristic of the current loop can be tailored for optimum performance by the compensation network around the *CA*. Compared with peak current mode control, the current loop gain crossover frequency, f_C, can be made approximately the same, but the gain will be much greater at lower frequencies.

The result is:

1) Average current tracks the current program with a high degree of accuracy. This is especially important in high power factor preregulators, enabling less than 3% harmonic distortion to be achieved with a relatively small inductor. In fact, average current mode control functions well even when the mode boundary is crossed into the discontinuous mode at low current levels. The outer voltage control loop is oblivious to this mode change.

2) Slope compensation is not required, but

there is a limit to loop gain at the switching frequency in order to achieve stability.

3) Noise immunity is excellent. When the clock pulse turns the power switch on, the oscillator ramp immediately dives to its lowest level, *volts* away from the corresponding current error level at the input of the PWM comparator.

4) The average current mode method can be used to sense and control the current in any circuit branch. Thus it can control input current accurately with buck and flyback topologies, and can control output current with boost and flyback topologies.

Designing the Optimum Control Loop

Gain Limitation at f_S: Switching power supply control circuits all exhibit subharmonic oscillation problems if the slopes of the waveforms applied to the two inputs of the PWM comparator are inappropriately related.

With peak current mode control, slope compensation prevents this instability.

Average current mode control has a very similar problem, but a better solution. The oscillator ramp effectively provides a great amount of slope compensation. One criterion applies in a single pole system: *The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input.* This criterion puts an upper limit on the current amplifier gain at the switching frequency, indirectly establishing the maximum current loop gain crossover frequency, f_C. It is the first thing that needs to be considered in optimizing the average current mode control loop.

In the following examples, we assume that the power circuit design has been completed, and only the *CA* compensation remains to be worked out.

Example 1: Buck Regulator Output Current. The simple buck regulator shown in Fig. 2 has the following operating parameters:

Switching Frequency, f_S = 100 kHz
Input Voltage, V_{IN} = 15 - 30V
Output Voltage, V_O = 12V
Output Current, I_O = 5A (6A O.L.)
Inductance, L = 60 μH
max. ΔI_O @ 30V (100 kHz) = 1.2A
Sense Resistance, R_S = 0.1Ω

C_{FP} is temporarily omitted. Zero $R_F C_{FZ}$ is well below the switching frequency. Near f_S, the amplifier gain is flat. The overall current loop has only one active pole (from the inductor).

The inductor current is sensed through R_S. (How this is accomplished will be discussed later.) The inductor current waveform with its sawtooth ripple component is amplified and inverted through the CA and applied to the comparator. The inductor current downslope (while the switch is off) becomes an upslope, as shown in Fig. 2. To avoid subharmonic oscillation, this off-time CA output slope must not exceed the oscillator ramp slope. In Fig. 2, the off-time CA output slope is much less than the oscillator ramp slope, indicating that the CA gain is less than optimum.

Calculating the slopes:

Inductor Current Downslope = Vo/L
Oscillator Ramp Slope = $Vs/Ts = Vs f_S$

Where V_S is the oscillator ramp p-p voltage, T_S and f_S are the switching period and frequency.

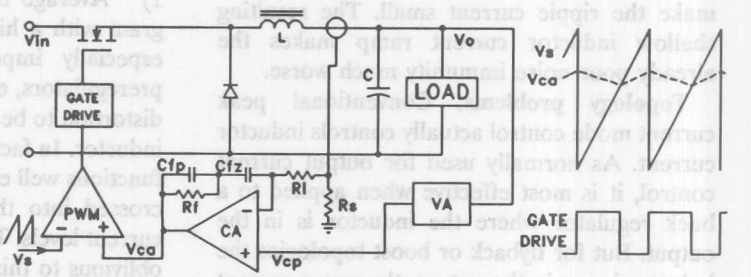


Fig. 2 - Average Current Mode Control Circuit and Waveforms

The inductor current downslope is translated into a voltage across current sense resistor R_S and multiplied by the *CA* gain, G_{CA}. This is set equal to the oscillator ramp slope to determine the *CA* gain allowed at f_S:

$$(V_O/L)R_S G_{CA} = V_S f_S$$

$$\therefore \quad \max \; G_{CA} = \frac{v_{CA}}{v_{RS}} = \frac{V_S f_S L}{V_O R_S} \qquad (1)$$

Applying the values given in the example, and with V_S of 5Vpp, the maximum G_{CA} at the switching frequency is 25 (28dB). The current error amplifier gain at f_S is set to this optimum value by making the ratio $R_F/R_I = 25$.

The small-signal control-to-output gain of the buck regulator current loop power section (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\frac{V_{IN}}{sL} = \frac{1590}{f} \quad (@30V) \qquad (2)$$

The overall open loop gain of the current loop is found by multiplying (1) and (2). The result is set equal to 1 to solve for the loop gain crossover frequency, f_C:

$$\frac{R_S}{V_S}\frac{V_{IN}}{2\pi f_C L}\frac{V_S f_S L}{V_O R_S} = 1$$

$$f_C = \frac{f_S V_{IN}}{2\pi V_O} = \frac{f_S}{2\pi D} \qquad (3)$$

Setting the *CA* gain at the limit found in (1), the crossover frequency will never be less than one sixth of the switching frequency. (This is exactly the same result reported by Middlebrook [1] for peak current mode control with recommended slope compensation.) In this example, f_C is 20 kHz with V_{IN} at 15V (D=.8), and 40 kHz when V_{IN} at 30V (D=.4).

If the error amplifier had a flat gain characteristic, the phase margin at crossover would be 90°–much more than required–and the gain at lower frequencies wouldn't be much better than with peak current mode control. But zero $R_F C_{FZ}$ placed at 10 kHz, below the minimum crossover frequency, reduces the phase margin to 63°, and boosts the low frequency gain dramatically, with an integrator gain of 250K/f. It is this characteristic which causes the current loop to rapidly and accurately home in on the average current called for by the outer loop. Even though the comparator actually turns off the power switch when a *peak* inductor current is reached, this peak current level is adjusted by the current amplifier so that the average current is correct.

Fig. 3 shows the start-up waveforms of the voltages at the PWM comparator inputs and the inductor current with V_{IN} at 30V and full load. Note how the amplified and inverted inductor current downslope virtually coincides with the oscillator ramp, because the CA gain was set at the optimum level according to Equation (1). Note also that if the CA gain is increased further, not only will the off-time slope exceed the oscillator ramp slope, but the positive excursion may reach the CA compliance limit, clipping or clamping the waveform.

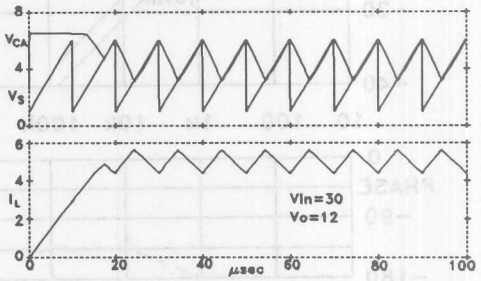


Fig. 3 - Buck Waveforms, Optimized Gain

Pole $R_F C_{FP} C_{FZ}/(C_{FP}+C_{FZ})$ is set at switching frequency f_S (100 kHz). This pole has one purpose–to eliminate noise spikes riding on the current waveform, the nemesis of peak current mode control. The sawtooth CA output waveform is also diminished, especially the higher order harmonics, and shifted in phase as shown in Fig. 4. The pole-zero pair (at 100 kHz and 10 kHz) reduces the phase margin at crossover to a very acceptable 45°–see Fig. 5.

The reduced amplitude and slopes of the CA waveform resulting from the 100 kHz pole might suggest that the *CA* gain could be in-

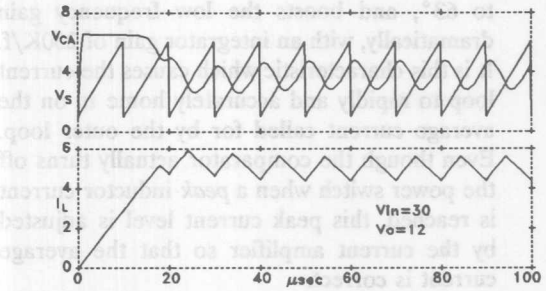


Fig. 4 - Buck with Additional Pole at f_S

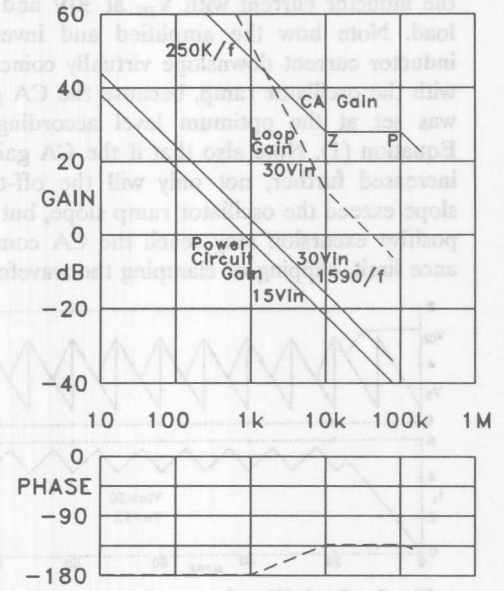


Fig. 5 - Buck Regulator Bode Plot

creased beyond the maximum value from Equation (1), but beware–Eq. (1) is valid only for a system with a single pole response at f_S, but with C_{FP} added there are now two active poles at f_S. Experimentally, increasing G_{CA} may incur subharmonic oscillation.

Discontinuous Operation. When the load current I_O becomes small, the inductor current becomes discontinuous. The current level at the continuous/discontinuous mode boundary is:

$$I_O = I_L = \frac{V_O(V_{IN}-V_O)}{V_{IN}\,2f_S L} \qquad (4)$$

Worst case is at max V_{IN}, when ripple current is greatest. In this example, the mode boundary occurs at I_O ($=I_L$) of 0.2A when V_{IN} is 15V, and at 0.6A when V_{IN} is 30V.

In the discontinuous mode, below the mode boundary, changes in I_O require large duty cycle changes. In other words, the power circuit gain suddenly becomes very low. Also, the single pole characteristic of continuous mode operation with its 90° phase lag disappears, so the power circuit gain is flat–independent of frequency. The current loop becomes more stable, but much less responsive.

With peak current mode control in the discontinuous mode, peak/avg current error becomes unacceptably huge. But with average current mode control, the high gain of the current error amplifier easily provides the large duty cycle changes necessary to accommodate changes in load current, thereby maintaining good average current regulation.

Referring to Fig. 2, when the current loop is closed, the voltage across current sense resistor V_{RS} equals the current programming voltage V_{CP} (from the voltage error amplifier) at frequencies below f_S. The transconductance of the closed current loop is a part of the outer voltage control loop:

$$g = \frac{\hat{i}_L}{\hat{v}_{CP}} = \frac{\hat{v}_{RS}/R_S}{\hat{v}_{CP}} = \frac{1}{R_S} \qquad (5)$$

The closed loop transconductance rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S.

Example 2: Boost Regulator Input Current. A 1 kW off-line preregulator (Fig 6) operates with the following parameters:

Switching Frequency, f_S = 100 kHz
Input Volts, V_{IN} = 90 - 270V rms
Output Volts, V_O = 380Vdc
Max. O.L. I_{IN} (@90V) = 12A rms, 17A pk
L = 0.25mH
ΔI_L, ΔI_{IN} @90V = 3.4A
R_S = 0.05Ω

The max. overload line current at min. V_{IN} corresponds to 1080W input. The max. peak overload 60Hz line current (17A) should–by design–correspond to a limit on the current programming signal, I_{CP}. The max peak 100kHz current through the switch and rectifier is 17A plus one-half ΔI_L: 17 + 3.4/2 = 18.7A

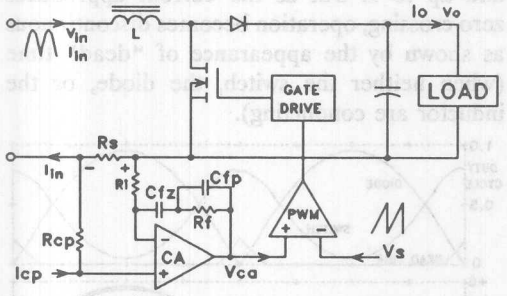


Fig. 6 - Boost Preregulator Circuit

The current downslope occurs when the power switch is off:

$$\textit{Inductor Current Downslope} = (V_O - V_{IN})/L$$
$$\textit{Worst case when } V_{IN} = 0: \quad = V_O/L$$
$$\textit{Oscillator Ramp Slope} = Vs/Ts = Vs f_s$$

Multiply the downslope by R_S and CA gain and set equal to the oscillator ramp slope, then solve for maximum CA gain:

$$(V_O/L)R_S G_{CA} = V_S f_S$$

$$\therefore \quad \max \; G_{CA} = \frac{\hat{v}_{CA}}{\hat{v}_{RS}} = \frac{V_S f_S L}{V_O R_S} \qquad (6)$$

Note the form of Equation (6) is identical to the buck regulator in (1). Using the values for this application, the maximum G_{CA} is 6.58, accomplished by making R_F/R_I = 6.58.

The small-signal control-to-input gain of the current loop power section (from v_{CA} at the CA output, to v_{RS}, the voltage across R_S) is:

$$\frac{\hat{v}_{RS}}{\hat{v}_{CA}} = \frac{R_S}{V_S}\frac{V_O}{sL} = \frac{2420}{f} \qquad (7)$$

Note that (7) is nearly identical to (2) for the buck regulator, except the gain depends on V_O (which is constant), rather than V_{IN}.

The overall current loop gain is found by multiplying (6) and (7). The result is set equal to 1 to solve for the crossover frequency, f_C:

$$\frac{R_S}{V_S}\frac{V_O}{2\pi f_C L}\frac{V_S f_S L}{V_O R_S} = 1$$

$$f_C = \frac{f_S}{2\pi} \qquad (8)$$

With the CA gain at the limit found in (6), the current loop f_C is *fixed* at $f_S/6$ (16.7 kHz).

As with the earlier example, with a flat gain error amplifier the phase margin at crossover is 90°–larger than necessary. So zero $R_F C_{FZ}$ is set at 1/2 of the minimum crossover frequency ($f_C/2 = f_S/12$ = 8.33 kHz), providing a low frequency boost with an integrator gain of 55K/f. Pole $R_F C_{FP} C_{FZ}/(C_{FP}+C_{FZ})$ is set at 6 times the zero frequency (50 kHz) to eliminate noise spikes. Together, the zero at 8.33 kHz and the pole at 50 kHz leave a phase margin at crossover of 40°. Startup waveforms are shown in Fig. 7, and the Bode plot in Fig. 8.

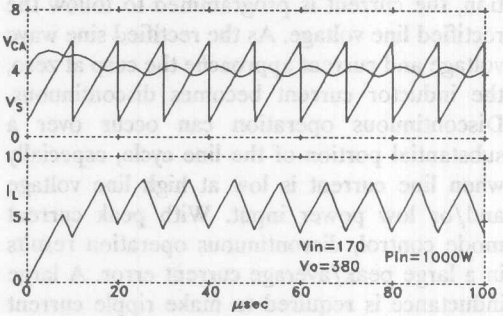


Fig. 7 - Boost Regulator Waveforms

Referring back to Fig. 6 – when the current loop is closed, the voltage across current sense resistor V_{RS} equals the voltage across current programming resistor V_{RCP}. In this case, programmed with a current source I_{CP}, the current gain of the closed current loop is:

$$G = \frac{i_L}{i_{CP}} = \frac{v_{RS}/R_S}{v_{RCP}/R_{CP}} = \frac{R_{CP}}{R_S} \quad (9)$$

The closed loop current gain rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S.

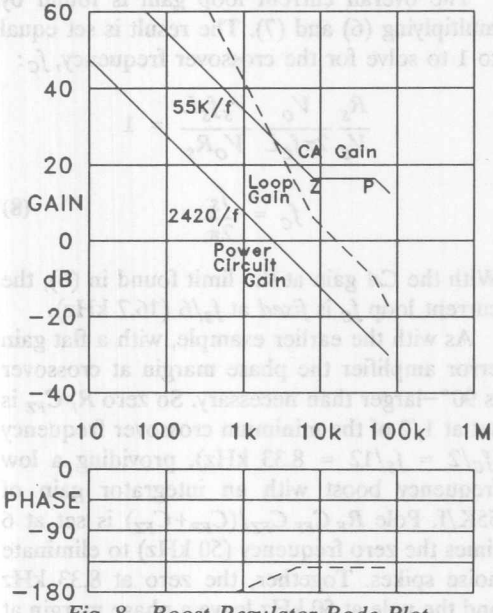


Fig. 8 - Boost Regulator Bode Plot

In a high power factor preregulator application, the current is programmed to follow the rectified line voltage. As the rectified sine wave voltage and current approache the cusp at zero, the inductor current becomes discontinuous. Discontinuous operation can occur over a substantial portion of the line cycle, especially when line current is low at high line voltage and/or low power input. With peak current mode control, discontinuous operation results in a large peak/average current error. A large inductance is required to make ripple current small and put the mode boundary at a low current level. However, average current mode control eliminates the peak/average error. A small inductance can and should be used to reduce cost, size and weight and improve current loop bandwidth.

Figure 9 shows a boost preregulator programmed to follow a 60 Hz (rectified) sine wave input. The lower waveforms show the programmed and actual line current waveforms. (The programmed waveform has been increased by 5% to make the two waveforms visible. The actual waveform leads the programmed waveform by a small amount and has less than 0.5% 3rd harmonic distortion! The upper waveforms show the duty cycles of the switch and diode throughout the line cycle. The inductor current is continuous when the current is high, and the switch and diode duty cycles add up to 1. But as the current approaches zero crossing, operation becomes discontinuous as shown by the appearance of "dead" time (when neither the switch, the diode, or the inductor are conducting).

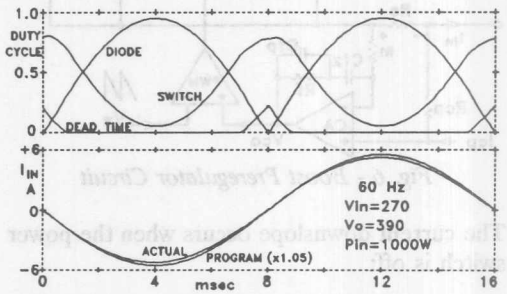


Fig. 9 - Boost 60Hz Sine Wave Input Current

Note that the switch duty cycle does not change as much when operation becomes discontinuous. With the boost (and flyback) topology in the discontinuous mode, average input current tends to follow input voltage at a constant duty cycle. Even though plenty of CA gain is available to change the duty cycle, little change is required for perfect tracking.

Figure 10 shows how the actual input current sine wave tracks the programming signal at 400 Hz. The distortion is worse -- 4.5% 3rd harmonic. This is for two reasons:

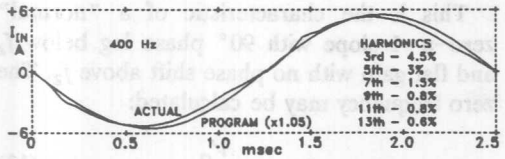


Fig. 10 - Boost 400Hz Sine Wave Input Current

1. The harmonic components of the rectified 400 Hz waveform are at higher frequencies and closer to the current loop crossover frequency where the loop gain is less, compared with the 50 or 60 Hz harmonics.
2. The inductor current has difficulty rising off zero because the input voltage is so very low at that point. So the inductor current lags coming off zero, then catches up and overshoots the programmed level. (This effect is much worse with peak current mode control because of the large inductor required.)

Controlling Average Switch Current

In the previous examples, average current mode control was applied to controlling inductor current (buck output current and boost input current). This is relatively easy because the inductor current is mostly DC with only a small amount of ripple to deal with. But if it is desired to use a buck or flyback topology to control input current in a high power factor application, then the chopped current waveform through the power switch must be averaged, a more difficult task.

Example 3: Flyback Regulator Input Current: A 1000 W off-line preregulator uses a flyback circuit in order to achieve a standard 300V output bus even though the input voltage ranges above and below 300V (Figs. 11,12).

The flyback converter could be designed to operate in the discontinuous inductor current mode in this application. The discontinuous flyback converter is not difficult to control (crudely) by fixing the duty cycle during each line half-cycle, but the peak currents through the power switch and rectifier are nearly twice as high as with continuous mode operation.

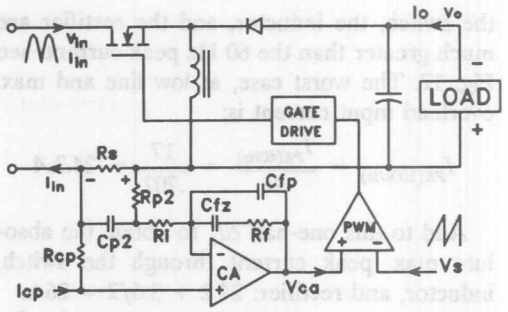


Fig. 11 - Flyback Preregulator Circuit

The high peak current lowers efficiency and requires devices with higher current ratings.

Continuous mode operation suffers the problem that the boundary is crossed into the discontinuous mode at light loads and high input voltage, unless a large filter inductor is used, which hurts the frequency response and the power factor as well as the pocketbook.

This dilemma disappears with average current mode control because it functions well in the discontinuous as well as the continuous mode, enabling the use of a small inductance value. In this example, the flyback converter operates in the continuous mode when it is important do so--at high current levels, to keep the maximum peak current to half that of a strictly discontinuous flyback converter. The operating parameters are:

Switching Frequency, f_S = 100 kHz
Input Volts, V_{IN} = 90 - 270V rms
Output Volts, V_O = 300V dc
Max. O.L. I_{IN} (@90V) = 12A rms, 17A pk
L = 0.25mH
ΔI_L @90V = 3.6A
R_S = 0.025Ω

The max. overload rms line current at min. V_{IN} equates to 1080W input (2160Wpk 60Hz). The max. overload peak 60 Hz line current (17A) should be made to correspond to a limit on the current programming input, I_{CP}. Unlike the boost converter, the flyback input current is chopped, so the peak 100kHz current through

the switch, the inductor, and the rectifier are much greater than the 60 Hz peak current–see Fig. 12. The worst case, at low line and max. overload input current is:

$$I_{PK(100kHz)} = \frac{I_{PK(60Hz)}}{D} = \frac{17}{.702} = 24.2A$$

Add to this one-half ΔI_L to obtain the absolute max. peak current through the switch, inductor, and rectifier: 24.2 + 3.6/2 = 26A.

Compared to the boost converter, the flyback topology requires higher current and higher voltage devices and generates a lot more input noise because of the chopped waveform. In its favor, the flyback converter can operate with any input/output voltage ratio, can provide current limiting, and input/output isolation.

As discussed in the previous example, the boost converter amplifier gain at f_S was limited only by the criteria that the inductor current downslope must not exceed the oscillator ramp slope. The power circuit control-to-input current gain had a simple −1 slope from zero to f_S, making it very easy to compensate.

But with the flyback converter, the chopped switch current waveform will be averaged. This results in a lower crossover frequency, f_C, and lower gain-bandwidth for two reasons:

1. The large amplitude chopped current waveform must be integrated by the CA. The upslope of the resulting triangular waveform at the CA output must not exceed the oscillator ramp slope. (The inductor current downslope is not relevant.)
2. There is a zero (conventional left half-plane) in the control-to-input current gain characteristic. This zero moves with output current level. Loop gain crossover cannot be much higher than the lowest zero frequency.

The small-signal control-to-input gain of the flyback current loop power circuit (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{v_{RS}}{v_{CA}} = \frac{R_S}{V_S}\left(I_L + \frac{V_O}{sL}\right) \quad (10)$$

This is the characteristic of a "normal" zero–a -1 slope with 90° phase lag below f_Z and flat gain with no phase shift above f_Z. The zero frequency may be calculated:

$$f_Z = \frac{V_O}{2\pi L I_L} \quad (11)$$

Note that the zero moves inversely with inductor current and inductance value. This zero has a big effect on loop compensation. To obtain the best loop response, it is important that f_{Zmin} be as high as possible, by making the inductance small. Fortunately, with average current mode control, there is no need to worry about crossing into discontinuous operation. The limit on making the inductance too small is when the inductor ripple current becomes too large, increasing peak switch and rectifier currents an undesirable amount.

Using the specific values of this example, the power circuit gain is:

$$\frac{v_{RS}}{v_{CA}} = \frac{I_L}{200} - j\frac{960}{f}$$

The minimum zero frequency is 8 kHz, which occurs at 24.2A, the max. overload *inductor* current at 90V low line. The gain above f_Z is 0.12 (-18.4dB). The power circuit gain is shown in the Bode plot of Fig. 13.

Turning now to the current error amplifier (Fig. 11), the chopped input (switch) current waveform shown in Fig. 12 flows through R_S. The average value of this waveform, chopped at 100 kHz, is compared to the current program level across R_{CP} and amplified. Assume for the moment that C_{P2} is zero and C_{FZ} is shorted. The CA gain in the vicinity of 100 kHz is determined by integrator $(R_I+R_{P2})C_{FP}$. Averaging is accomplished because the DC gain is high, but the 100 kHz rectangular waveform with its harmonics is amplified relatively little. The rectangular waveform is converted into a triangular wave as shown in Fig. 12.

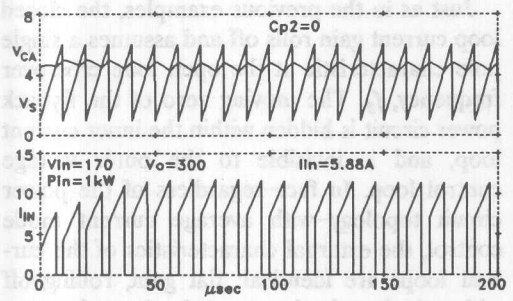


Fig. 12 - Flyback Regulator Waveforms

The optimum CA integrator gain at 100 kHz is the gain at which the maximum CA output upslope equals the oscillator ramp slope. This is the same principle used in the previous two examples, but in those cases the inductor (whose current was being controlled) did most of the averaging. The inductor did the integration to provide the triangular ripple current waveform and the CA gain was flat in the vicinity of f_S. But in this flyback preregulator example, the chopped *switch* current is being controlled so the averaging and the triangular waveshape are achieved by an integrating amplifier.

The upslope of the CA output occurs when the switch is off and the 100 kHz current waveform is at zero. The CA inputs are both at program voltage V_{CP}. V_{CPmax} equates to the max. overload peak 60Hz input current (17A) through R_S. Therefore, during the switch "off" time, the maximum current through $R = (R_I + R_{P2})$ is:

$$I_{RImax} = \frac{V_{CPmax}}{R} = \frac{I_{INpk} R_S}{R}$$

The upslope of the CA output is determined by the current through R_I charging C_{FP}:

$$\text{max } CA \text{ } Upslope = \frac{I_{RImax}}{C_{FP}} = \frac{I_{INpk} R_S}{C_{FP} R_I}$$

$$Oscillator \text{ } Ramp \text{ } Slope = V_S / T_S = V_S f_S$$

Equating the slopes and solving for C_{FP}:

$$\frac{I_{INpk} R_S}{C_{FP} R} = V_S f_S$$

$$C_{FP} = \frac{I_{INpk} R_S}{V_S f_S R} \quad (12)$$

Using the values from this example, and assuming R = 10K (R_I=9K, R_{P2}=1K) :

$$C_{FP} = \frac{17 \times .025}{5 \times 0.1 \times 10^6 \times 10K} = 85\,pF$$

The CA integrator gain may now be calculated and entered in the Bode plot:

$$G_{CA} = \frac{1}{2\pi f R C_{FP}} = \frac{187{,}000}{f} \quad (13)$$

The compensation circuit as designed so far (with C_{P2} zero and C_{FZ} open) has high loop gain and is very stable only when the inductor current is high, maintaining the power circuit zero near the position shown in Fig. 13, so that its gain is flat at f_C. At lower current levels, the power circuit zero slides down to the right and

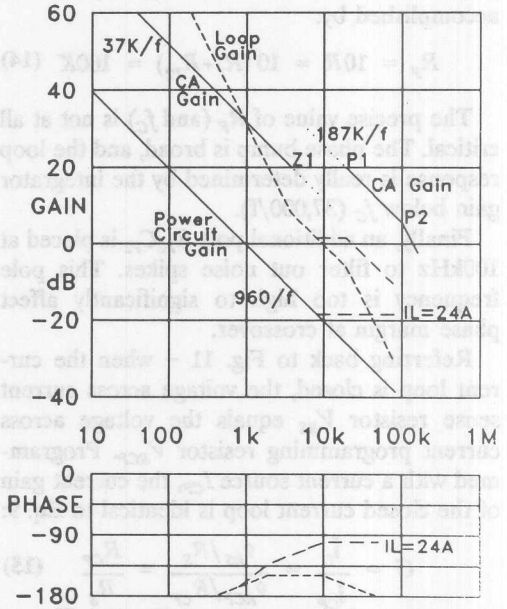


Fig. 13 - Flyback Regulator Bode Plot

the power circuit gain at f_C has a -1 slope. With the -1 slope of the CA gain, the overall current loop gain has a slope of -2 at crossover, and will ring excessively. It is necessary to add a pole-zero pair to the CA gain to reduce the slope to -1 in the vicinity of f_C. Offsetting the integrator gain by a factor of 5, as shown in the Bode plot, provides a phase bump which increases the actual phase margin to 42°, a slightly underdamped condition (the Bode *approximation* is 31°, as shown).

The offset factor of 5 is provided by $C_{FZ} = 4 \cdot C_{FP} = 340\text{pF}$. C_{FZ} and C_{FP} in parallel set the integrator gain at low frequencies to 37,000/f.

The location of the flat portion of the CA gain characteristic is determined by R_F. It is easiest to solve this graphically using the Bode plot. Ideally, Z1 and P1 should bracket the crossover frequency. *Simply slide the flat portion up and down between the integrator slopes until its gain is equal (but opposite in sign) to the power circuit gain at the same frequency as the center of the flat portion.* That frequency is the crossover frequency, f_C. In Fig 13, the CA gain in the flat portion is 10 (20dB). This is accomplished by:

$$R_F = 10R = 10\,(R_1 + R_{P2}) = 100K \quad (14)$$

The precise value of R_F (and f_C) is not at all critical. The phase bump is broad, and the loop response is really determined by the integrator gain below f_C (37,000/f).

Finally, an additional pole $R_{P2}C_{P2}$ is placed at 100kHz to filter out noise spikes. This pole frequency is too high to significantly affect phase margin at crossover.

Referring back to Fig. 11 – when the current loop is closed, the voltage across current sense resistor V_{RS} equals the voltage across current programming resistor V_{RCP}. Programmed with a current source I_{CP}, the current gain of the closed current loop is identical to Eq. 9:

$$G = \frac{\hat{i}_L}{\hat{i}_{CP}} = \frac{\hat{v}_{RS}/R_S}{\hat{v}_{RCP}/R_{CP}} = \frac{R_{CP}}{R_S} \quad (15)$$

Just as in the previous examples, the closed loop current gain rolls off and assumes a single pole characteristic at the open loop crossover frequency, f_S. The moving zero of the flyback power circuit is hidden within the inner current loop, and is invisible to the outer voltage control loop. In fact–regardless of the power circuit topology–with average current mode control, the external characteristics of the current loops are identical: flat gain, rolling off with a single pole characteristic above the open loop crossover frequency.

Example 4: Buck Regulator Input Current: The buck regulator is sometimes used in high power factor preregulator applications. It can only function when V_O is less than V_{IN}, so the output bus voltage must be low. Normally, a low output voltage should be avoided, because the bus filter capacitor becomes large and expensive, but in applications such as telephone or battery charging this is not a problem and/or there is no choice. With 120V line input and 48 volt output bus, the input current will drop to zero for a substantial portion of each line cycle, each time the instantaneous line voltage goes below 48V. Third harmonic distortion will be 7 - 8% at low line, but the power factor of 0.99 is good enough for most applications.

Although the flyback topology might be used in the same low voltage output application, the buck topology operates with lower inductor current and lower peak current through the switch and rectifier. Peak voltages on the switch and rectifier are also much lower. But the flyback topology can provide line isolation in the preregulator by using a flyback transformer instead of simple inductor.

The buck circuit can be almost the same as the flyback circuit of Fig. 11, interchanging the inductor and the rectifier (cathode up).

The control loop design procedure is the same as for the flyback in Example 3. The buck regulator has the same left half-plane zero. In fact, the power circuit control-to-input gain equation is identical to Eq. 10 for the flyback circuit.

Controlling Average Rectifier Current

Peak current mode control has been used with great success in conventional power supplies using buck-derived topologies. It works well because peak current mode control actually controls inductor current, and the inductor is located in the output of all buck topologies. When boost or flyback topologies are used, peak current mode control functions poorly, because the wrong current is controlled–the inductor current is not in the output. Although peak current mode control eliminates the inductor from the small-signal characteristic of the outer loop, the right half-plane zero present in boost and flyback outputs remains to plague outer loop compensation.

In boost or flyback circuits, the diode is in the output side, and ideally the diode current should be controlled, not inductor current. This is no problem for average current mode control. Its integrating current error amplifier can average the rectangular diode current waveform in the same way that it averages the switch current in the input of the buck or flyback preregulators discussed earlier. The right half-plane zero forces a lower current loop crossover frequency, but the RHP zero is "buried" within the current loop. The outer voltage control loop sees only a flat gain characteristic with a single pole roll-off at the crossover frequency–just the same as all the other topologies previously discussed. A flyback circuit using average current mode control is shown in Figure 14.

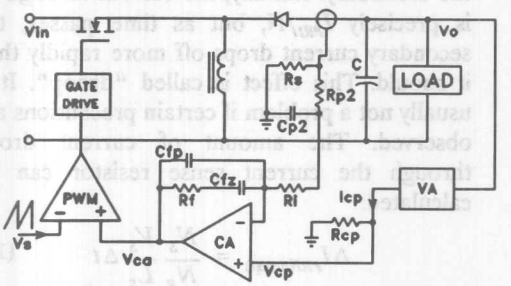


Fig. 14 - Flyback Output Current Control

The circuit is almost identical to the flyback preregulator of Fig. 11, except output current is sensed and controlled.

The small-signal control-to-output gain of the flyback current loop power circuit (from v_{CA} at the *CA* output, to v_{RS}, the voltage across R_S) is:

$$\frac{\hat{v}_{RS}}{\hat{v}_{CA}} = \frac{R_S}{V_S}\left[\frac{V_O}{sL} - I_L\right] \qquad (16)$$

The same equation applies to controlling the output current of a boost circuit. Note the similarity with Eq. 10 for flyback or buck input current control. In Eq. 16, low frequency gain depends on V_{IN} rather than V_O, but more importantly, the inductor current I_L has a minus sign, which represents 180° phase lag above the zero frequency. This is the characteristic of a right half-plane zero, and it makes the loop compensation much more difficult. It is usually necessary to cross over at a frequency one half to one fourth of the RHP zero frequency in order to cross over with adequate phase margin. This results in lower closed loop bandwidth for the current loop than the previous examples. However, once this is accomplished, the RHP zero does not appear in the outer loop.

It is very important to make the inductance small to achieve the highest possible RHP zero frequency. Fortunately, average current mode control allows the mode boundary to be crossed. This permits a much smaller inductance than with peak current mode control, resulting in a much higher RHP zero frequency and higher crossover frequency.

Current Sensing

One important advantage of having a high gain current error amplifier is that it permits a very small current sense resistor value resulting in low power dissipation. The CA can make up for the gain lost with the small resistor.

In many applications, however, using a current sense resistor in the direct path of the current to be measured is not practical. The tiny R_S value may be difficult to implement, and the power dissipation in a practical sense

resistor is too great. Often, the R_S circuit location is at a large potential difference from the control circuit. This is especially a concern when current must be sensed on the other side of the isolation boundary.

A current sense transformer (C.T.) can provide the necessary dielectric isolation and eliminate the need for an extreme low-value resistor. As shown in Fig. 15, this technique

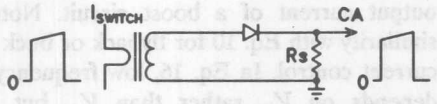


Fig. 15

works well for average current mode control when the current to be sensed and averaged is a pulse which returns to zero within each switching period–such as switch current (buck or flyback input current) or diode current (boost or flyback output current). Although "transformers can't couple DC", a C.T. does couple the entire instantaneous current waveform including its DC component if the core is reset to zero baseline each time the pulse goes to zero.

Total reset requires the same volt-seconds (of opposite sign) that were applied to "set" the core. At duty cycles approaching 1.0–which can occur temporarily with most topologies–the time available for reset may be only a tiny fraction of the switching period. Achieving total reset in a short time requires a large backswing of voltage across the C.T., so don't use low voltage diodes to couple the C.T. to R_S.

With a boost converter controlling input current in a high power factor preregulator application, a current sense resistor easily ties in directly with the control circuit, as shown in Fig. 6. Nevertheless, many designers would prefer to use a current transformer to minimize power loss and allow the use of a much higher R_S value. However, since the input current of a boost converter *is* the inductor current, the input current never goes to zero when operating in the continuous mode. Therefore, a C.T. can't be used to sense input current of a boost converter because the DC value is lost, and the C.T. cannot reset–it will saturate. The same problem occurs in a buck regulator circuit, where the C.T. can't directly sense average output (inductor) current.

The answer to this problem is to use *two* C.T.s–one sensing switch current, the other sensing diode current. By summing their outputs as shown in Fig. 16, the true inductor current is reconstituted. Each C.T. has plenty of time to reset.

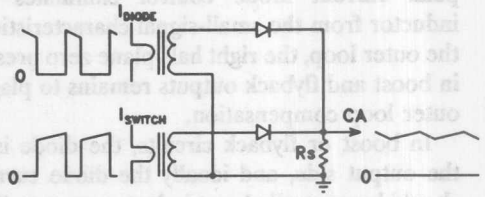


Fig. 16

Using Current Sense Transformers:
It is not difficult to achieve excellent results using low cost commercially available pulse transformers. A current sense "inductor" such as Pulse Engineering 51688 is a toroidal core wound with 200 secondary turns for a secondary inductance of 80 mH. A 0.18" hole is provided to slip the primary wire through.

The pulse voltage across the windings of a current transformer generates a magnetizing current which starts at zero and increases fairly linearly with time. The magnetizing current subtracts from the pulse current delivered to the secondary. Initially, the current through R_S is precisely I_{PRI}/N, but as time passes, the secondary current drops off more rapidly than it should. This effect is called "droop". It is usually not a problem if certain precautions are observed. The amount of current droop through the current sense resistor can be calculated:

$$\Delta I_{PRI(droop)} = \frac{N_S}{N_P}\frac{V_S}{L_S}\Delta t \qquad (17)$$

where N is the turns ratio, V_S the voltage across the secondary, L_S the secondary inductance and Δt is the max. pulse width. As the

equation shows, droop is minimized by maximizing secondary inductance–use the largest you can get. Don't use a large R_S value to obtain a large secondary voltage–its not necessary and makes reset more difficult. Make the turns ratio as low as possible by using two or three primary turns if space allows. Don't reduce the turns ratio by reducing the secondary turns–this is counter-productive because the inductance goes down with the turns *squared*.

For example, consider the flyback input current preregulator of Fig. 11, using a current transformer in series with switch instead of the 0.025Ω sense resistor shown. Using the Pulse Engineering #51688 current sense inductor with one turn primary, the turns ratio is 1:200. Secondary inductance is 80 mH. The 24A max. overload pulse current becomes a 0.12A current pulse on the secondary side. A 10Ω sense resistor will have a max. voltage of 1.3V sent to the CA, and the max. secondary voltage including diode forward drop is 2.0V. The maximum pulse width is 7.02μsec.

Applying these values to Eq. 17:

$$\Delta I_{PRI(droop)} = \frac{200}{1}\,\frac{2.0}{80\times10^{-3}}\,7\times10^{-6} = .035A$$

Only 35mA droop out of 24A isn't bad!

When two C.T.s are used–one on either side of isolation boundary-their turns ratios must be proportioned the same as the power transformer pri/sec turns ratio so that currents through R_S will be equalized.

All of the equations containing R_S given earlier in this paper assume the sense resistor is measuring current directly. When using a current sense transformer, reflect the actual R_S on the C.T. secondary side into the primary by substituting $R_S N_P/N_S$.

References:

[1] S.Hsu, A.Brown, L.Rensink, R.D.Middlebrook, "Modelling and Analysis of Switching DC-to-DC Converters in Constant Frequency Current Programmed Mode, "*IEEE PESC Proceedings,* 1979

[2] R.D.Middlebrook, "Topics in Multiple-Loop Regulators and Current-Mode Programming," *IEEE PESC Proceedings,* June 1985

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APPLICATION NOTES

Resonant Fluorescent Lamp Converter Provides Efficient and Compact Solution

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Abstract - **This paper describes a zero voltage switched (ZVS) resonant converter for driving cold cathode fluorescent lamps. Primarily intended for liquid crystal display (LCD) back-lighting, the circuit features minimal component count and size. A specially designed integrated circuit provides all control functions for a current fed push-pull ZVS converter, and also contains an auxiliary pulse width modulated (PWM) controller to develop a programmable supply voltage for the LCD. Analysis and simulation of the converter, and a complete circuit schematic are presented. The analysis and simulation results are validated by experimental circuit waveforms and critical performance parameters.**

Introduction

The proliferation of laptop and notebook computers places an ever increasing demand on display technology. High resolution and contrast are required to run today's graphics based programs, increasing the conflict between display performance, size and efficiency. The LCD with cold cathode fluorescent back lighting best satisfies this design requirement, however the lamp and its high voltage AC supply still remain the major contributor to battery drain.

The cold cathode fluorescent lamp (CCFL) requires 1-2 kV to fire. Sine wave drive is preferred to minimize RF interference and maximize lamp efficiency over time. Converter efficiency and size are extremely critical. These formidable requirements demand a highly efficient conversion topology and maximum circuit integration.

A zero voltage switched resonant topology will maximize efficiency by eliminating losses associated with charging parasitic capacitances to high voltages. This topology can be controlled using discrete circuitry. The most common implementation is a Royer oscillator modified to provide ZVS operation. While this at first appears to be a good solution, and is commonly used today, it suffers from several limitations.

High voltage DC to AC conversion is only part of the display supply. The average output current must be programmable for lamp intensity control, and the LCD requires a programmable low voltage supply for contrast adjustment. This additional circuitry, implemented discretely or with multiple ICs results in a large number of components, significantly impacting size and reliability. Synchronization is also preferred to eliminate beat frequency effects such as lamp intensity modulation, further complicating the design. Minimizing circuit complexity and bulk are best achieved through integration.

Cold Cathode Lamp Characteristics

The CCFL presents a highly nonlinear load to the converter as illustrated in fig. 1. Initially when the lamp is cold (inoperative for some finite time), the voltage to fire the lamp is typically more than three times higher than the sustaining voltage. The lamp characterized in fig. 1 fires at 1600V and exhibits an average sustaining voltage (V_{FL}) of 300V. Notice that the lamp initially exhibits a positive resistance and then transitions to a negative resistance above 1mA. These characteristics dictate a high output impedance (current source) drive to suppress the negative load resistance's effect and limit current during initial lamp firing. Since the ZVS converter has a low output impedance, an additional "lossless" series impedance such as a coupling capacitor must be added.

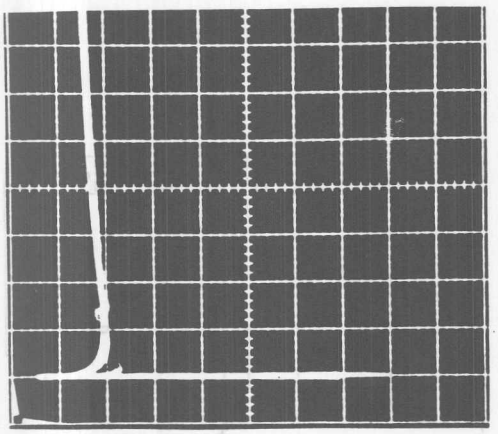


Fig. 1 Cold Cathode Lamp Current as a function of Voltage
Vertical: 2mA/div. Horizontal: 200V/div.

To facilitate analysis, the equivalent CCFL circuit shown in figure 2 is used. V_{FL} is the average lamp sustaining voltage over the operating range. The lamp impedance (R_{FL}) is a complex function but can be considered a fixed negative resistance at the sustaining voltage. Stray lamp and interconnect capacitance are lumped together as C_{FL}.

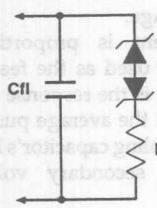


Fig. 2 CCFL equivalent circuit

ZVS Resonant Converter Topology

The current fed push-pull converter shown in fig. 3 is driven at it's resonant frequency to provide ZVS operation. The push-pull output MOSFETS (Q1 & Q2) are alternately driven at 50% duty cycle. Commutation occurs as V1 and V2 resonate through zero thereby insuring zero voltage switching. This virtually eliminates switching losses associated with charging MOSFET output and stray capacitance, and reduces gate drive losses by minimizing gate charge.

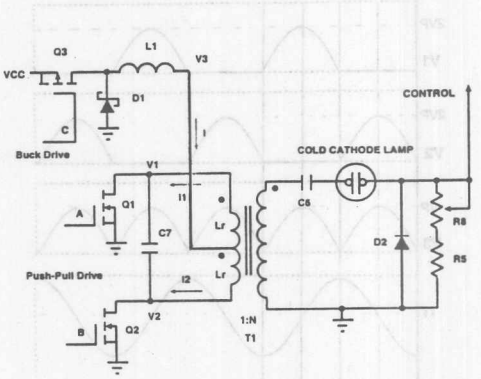


Fig. 3 Current Fed Push-Pull ZVS Resonant Converter

Current is supplied to the push-pull stage by a buck regulator (Q3). The control circuitry forces the average voltage across the current sense resistor (R8+R5) and rectifier (D2) to equal a reference voltage. Adjusted R8 varies the current and the lamp's brightness. The non-linearity introduced by D2 is insignificant since R8 is adjusted for a particular brightness with no concern of the actual current level.

Winding inductance, L_R, and C_R, the combined effective capacitance of C7 and the reflected secondary capacitances make up the resonant tank. The secondary side of the transformer exhibits a symmetrical sine wave voltage varying from about 300V to 1500V peak. Capacitor C6 provides ballasting and insures that the converter is only subjected to positive impedance loads.

Waveform Analysis

Simulated converter voltage and current waveforms are shown in fig. 4. At time t_0, the primary current (I1 & I2) has reached it's peak value. The push-pull drain voltages (V1 & V2) have resonated to zero. The primary voltage (V3) has also resonated to zero, and through the control circuitry commutated Q1 off and Q2 on. The energy stored in L_R is also at it's peak. This energy is transferred from L_R to the effective resonant capacitance (C_R) during time t_0 to t_1, causing C_R's voltage to sinusoidally increase.

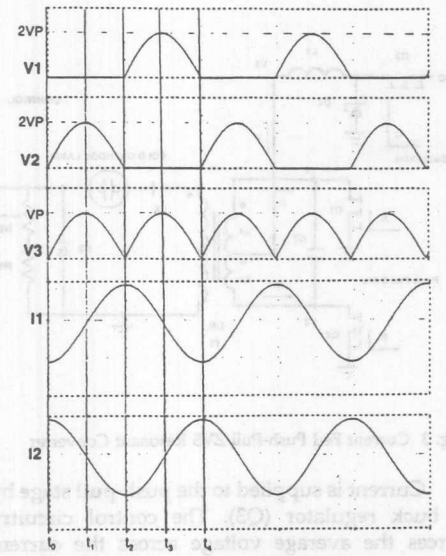


Fig. 4 Converter Voltage and Current Waveforms

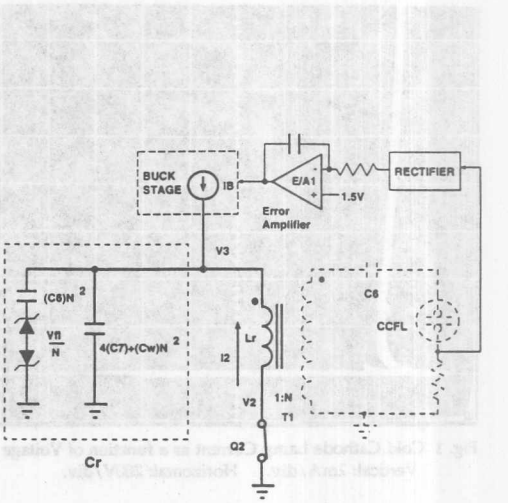


Fig. 5 Simplified converter model

At time t_1, all of the inductive energy in L_R has transferred to C_R, resulting in zero current through L_R and maximum voltage across C_R. From time t_1 to t_2, the energy transfers from C_R back to L_R, decreasing C_R's voltage while L_R's current increases.

The resonant current through L_R at time t_2 is equal and opposite to it's value at t_0. The reflected load current flows during the MOSFET on time, and is observed as a slight current amplitude asymmetry. The voltages at V1, V2, and V3 have resonated back to zero, causing the control circuitry to commutate Q2 off and Q1 on. The cycle continues symmetrically during the t_2 through t_4 interval, producing fully sinusoidal voltage and current waveforms.

Simplified Converter Model

The converter model shown in fig. 5, which is valid for one half cycle simplifies analysis by reflecting all impedances to the primary and eliminating the transformer. The differential voltage developed across the push-pull stage primary (V1-V2) exhibits twice the voltage excursion as the center-tap (V3). This reflects C7 to V3 through the turns ratio squared, resulting in 4(C7) at V3. The secondary winding capacitance is also reflected by the square of the turns ratio (n). Reflected winding capacitance is usually significant due to the high turns ratios typically employed. The buck stage operates in continuous current mode and is synchronized to the push-pull stage.

Lamp current is proportional to lamp intensity, and is used as the feedback variable. Buck current (I_B) is the response variable, which in turn regulates the average push-pull primary voltage. The coupling capacitor's high impedance transforms the secondary voltage to lamp current.

Control Equations

Variable Summary:

C_R = Effective resonant tank capacitance
C_W = Secondary interwinding capacitance
F_L = Average lamp voltage
I_B = Average Buck output current
L_R = Primary Winding Inductance
n = Transformer turns ratio
Z_{sec} = Secondary impedance

Fig. 6 shows the buck output stage and forced output voltage waveform. The output voltage is a rectified sine wave, corresponding to the synchronous, resonant push-pull stage input

voltage. The inductor output configuration exhibits high impedance at the resonant frequency and averages the output voltage throughout the cycle. The buck output voltage as a function of time is:

$$V_{out}(t) = V_P \sin(\omega t)$$

Where the angular frequency is:

$$\omega = 2\pi f = \frac{2\pi}{2t_1} = \frac{\pi}{t_1}$$

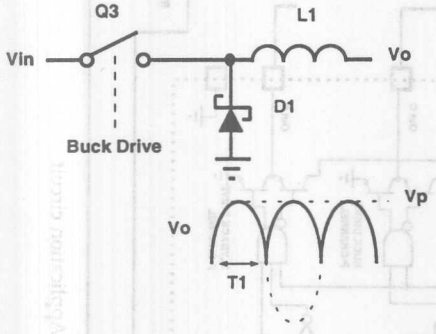


Fig. 6 Buck converter stage

The volts-second product across the inductor must be zero during steady state. Setting the on and off volt-second products equal and integrating gives the buck's transfer function:

$$V_{LR}(t_{on}) = -V_{LR}(t_{off})$$

$$\int_0^{t_{on}} V_{LR}\,dt = -\int_{t_{on}}^{t_1} V_{LR}\,dt$$

$$V_P = \frac{\pi}{2} Vi\ D \qquad (1)$$

This transfer function is identical to the familiar DC output buck transfer function, with the $\pi/2$ term accounting for peak versus average output voltage. As with the DC buck, primary voltage varies linearly with duty-cycle.

The peak primary voltage is also related to peak lamp current by:

$$V_P = \frac{(I_{FL(peak)})(Z_{sec}) + V_{FL}}{n} \qquad (2)$$

Setting (1) and (2) equal and solving for $I_{FL\,(avg)}$ expresses lamp current as a function of duty-cycle:

$$I_{FL(avg)} = \frac{DV_i\ n - \frac{2\ V_{FL}}{\pi}}{Z_{sec}} \qquad (3)$$

As expected from fig. 5, the lamp sustaining voltage, V_{FL} introduces a nonlinearity.

Buck output current is related to lamp current be equating input and output powers. The input power is:

$$P_{input} = \frac{1}{t}\int P\,dt$$

$$= \frac{1}{\pi/2}\int_0^{\pi/2} I\ V_P \sin(t)\,dt$$

$$P_{input} = \frac{2\ I_B\ V_P}{\pi}$$

The power to the load is:

$$P_{out} = V_{FL}\ I_{FL}\ (avg)$$

For analytical purpose, 100% power transfer is assumed:

$$P_{out} = P_{input}$$

$$V_{FL}\ I_{FL(avg)} = \frac{2 I_B V_P}{\pi}$$

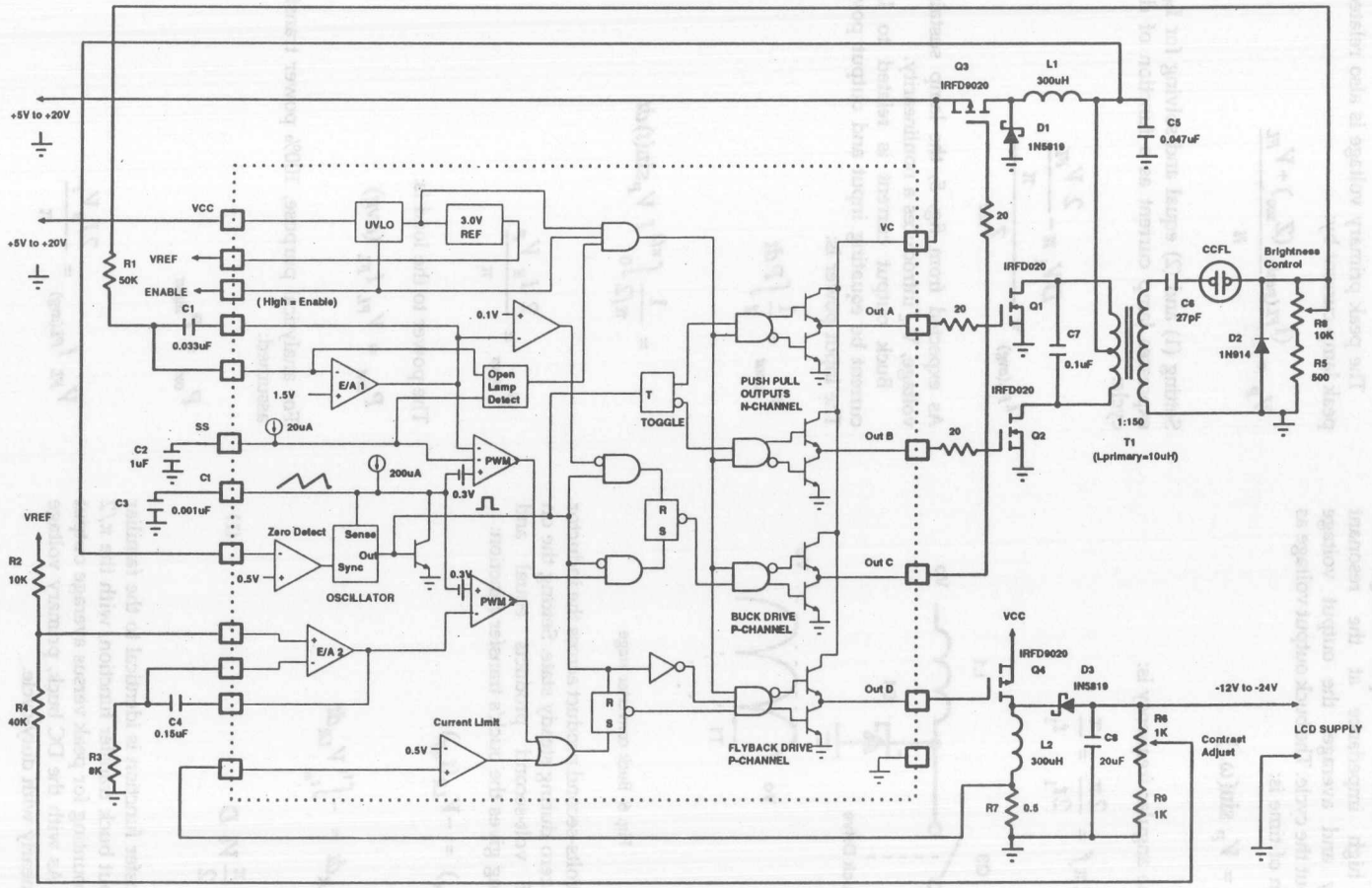


Fig. 7 UC3871 Application circuit

$$I_B = \frac{\pi I_{FL(avg)} V_{FL}}{2 V_P} \quad (4)$$

Substituting (2) for V_P in (4) gives the buck output current as a function of lamp current:

$$I_B = \frac{n V_{FL}}{Z_{sec} + \frac{V_{FL}}{\pi I_{FL(avg)}}} \quad (5)$$

The resonant frequency is approximately:

$$f_R \approx \frac{1}{2\pi\sqrt{L_R C_R}} \quad (6)$$

The nonlinearity introduced by V_{FL} causes the resonant frequency to vary with load. At very low lamp intensity the secondary voltage barely crests above V_{FL}. The effective resonant capacitance, C_R, is primarily the sum of C7 and C_W reflected to the primary. As the secondary voltage increase above V_{FL}, the reflected C6 value adds to the resonant capacitance, decreasing the frequency. The frequency range is approximated by assuming C6 has negligible effect at minimum lamp intensity, and fully adds to C_R at maximum intensity.

The peak resonant inductor current is the sum of the reflected load current from (5) and the resonant current:

$$I_{LR(peak)} = \frac{V_P}{Z_{tank}} + I_b \quad (7)$$

The tank impedance is determined by setting the resonant energy storage terms equal:

$$\frac{1}{2} L_R I^2 = \frac{1}{2} C_R V^2$$

Solving for V_R/I_R gives the tank impedance:

$$Z_{tank} = \sqrt{\frac{L_R}{C_R}} \quad (8)$$

Although relatively large currents are circulated through the resonant tank, the switches operate at low current levels. This is a direct result of the continuous resonant topology; the switches only must handle the energy that is removed by the load and lost in parasitics. The peak switch current is:

$$I_{SW(peak)} = I_b \quad (9)$$

The UC3871
A Completely integrated Solution

Fig. 7 shows a complete application circuit using the UC3871 Synchronous Resonant Fluorescent lamp and LCD driver. The IC provides all drive, control and housekeeping functions to implement CCFL and LCD converters. The buck output voltage (transformer center-tap) provides the zero crossing and synchronization signal. The LCD supply modulator is also synchronized to the resonant tank.

The buck modulator drives a P-channel MOSFET directly, and operates over a 0-100% duty-cycle range. The modulation range includes 100%, allowing operation with minimal headroom. The LCD supply modulator also directly drives a P-channel MOSFET, but it's duty-cycle is limited to 95% to prevent flyback supply foldback.

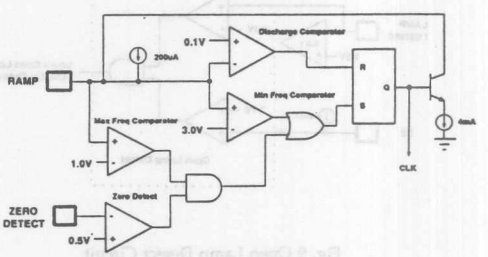


Fig. 8 UC3871 Oscillator Block Diagram

The Oscillator and synchronization circuitry are shown in fig. 8. The oscillator is designed to synchronize over a 3:1 frequency range. In an actual application however, the frequency range is only about 1.5:1. A zero detect comparator senses the primary center-tap voltage, generating

a synchronization pulse when the resonant waveform falls to zero. The actual threshold is 0.5 volts, providing a small amount of anticipation to offset propagation delay.

The synchronization pulse width is the time that the 4mA current sink takes to discharge the timing capacitor to 0.1 volts. This pulse width sets the LCD supply modulator minimum off time, and also limits the minimum linear control range of the buck modulator. The 200µA current source charges the capacitor to a maximum of 3 volts. A comparator blanks the zero detect signal until the capacitor voltage exceeds 1 volt, preventing multiple synchronization pulse generation and setting the maximum frequency. If the capacitor voltage reaches 3 volts (a zero detection has not occurred) an internal clock pulse is generated to limit the minimum frequency.

A unique protection feature incorporated in the UC3871 is the Open Lamp Detect circuit. An open lamp interrupts the current feedback loop and causes very high secondary voltage. Operation in this mode will usually breakdown the transformer's insulation, causing permanent damage to the converter. The open lamp detect circuit, shown in fig. 9 senses the lamp current feedback signal at the error amplifiers input, and shuts down the outputs if insufficient signal is present. Soft-start circuitry limits initial turn-on currents and blanks the open lamp detect signal.

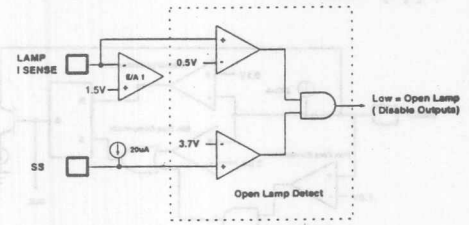


Fig. 9 Open Lamp Detect Circuit

Other features are included to minimize external circuitry requirements. A logic level enable pin shuts down the IC, allowing direct connection to the battery. During shut-down, the IC typically draws less than 100nA. The UC3871, operating from 4.5V to 20V, is compatible with almost all battery voltages used in portable computers. Under-voltage lockout circuitry disables operation until sufficient supply voltage is available, and a 1% voltage reference insures accurate operation. Both inputs to the LCD supply error amplifier are uncommitted, allowing positive or negative supply loop closure without additional circuitry. The LCD supply modulator also incorporates cycle-by-cycle current limiting for added protection.

Application Circuit Example

The application circuit shown in fig.7 resonates at approximately 50khz. This frequency allow a reasonable compromise between size and efficiency. This relatively low frequency by today's standards results from high voltage insulation and spacing requirements, and practical limitations in reducing stray and interwinding capacitance. The half wave current sense signal is sensed by Error Amp 1 and averaged by integral compensation. The range of current control is 500µA to 10mA.

A flyback converter generates the LCD supply, outputting -12V to -24V to bias monochrome LCDs. Color displays normally require a positive bias voltage. Since this voltage typically must also be stepped up, a coupled inductor flyback is normally used.

Actual circuit waveforms agree with the spice simulated waveforms in fig. 4. Distortion caused by lamp nonlinearity is clearly visible at the operating extremes. At more nominal levels, the waveforms are more ideal, with only a small amount of observable distortion.

All of the following waveforms were taken at minimum and maximum lamp intensity to indicate worst case conditions. Nominal measured efficiency was 80%. Further improvement is possible with lower resistance magnetics and lower on resistance MOSFETs. Fig. 10 shows secondary output voltage, fig 11 shows lamp voltage, and fig. 12 shows lamp current. Notice that the lamp voltage is fairly constant with widely varying current. A frequency shift from about 48kHz to 57kHz is also observed over the lamp intensity range. The lamp current exhibits additional harmonics induced by it's nonlinearity. Push-pull MOSFET drain to source voltage is shown in fig. 13, and drain current is shown in fig. 14. The transformer center-tap voltage (buck output) is shown in fig. 15. All waveforms are sinusoidal, exhibiting minimal harmonic content.

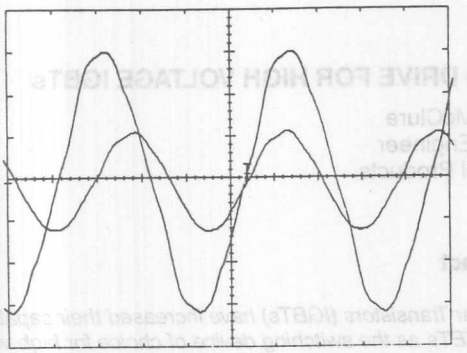


Fig. 10 Secondary output voltage
Vertical: 500V/div. Horizontal: 5µs/div.

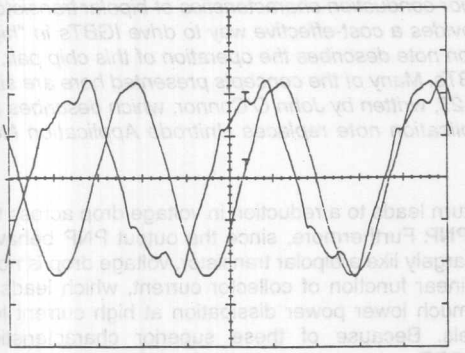


Fig. 11 lamp voltage
Vertical: 200V/div. Horizontal: 5µs/div.

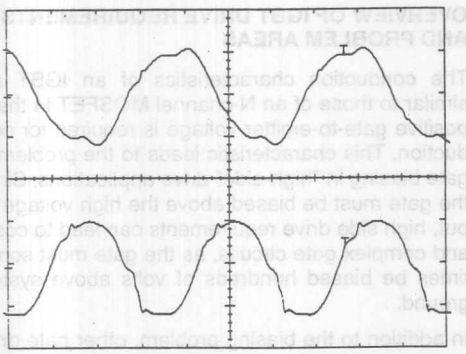


Fig. 12 Lamp current
Vertical: 10mA/div. Horizontal: 5µs/div.
500µA/div.

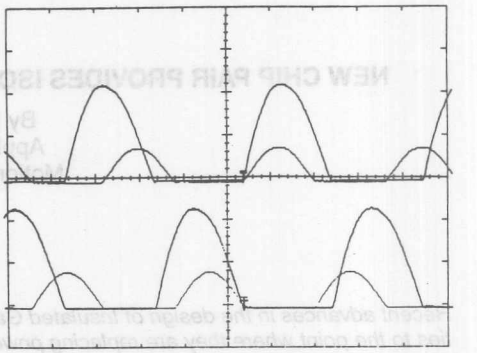


Fig. 13 Push-Pull MOSFET drain to source voltage
Vertical: 10V/div. Horizontal: 5µs/div.

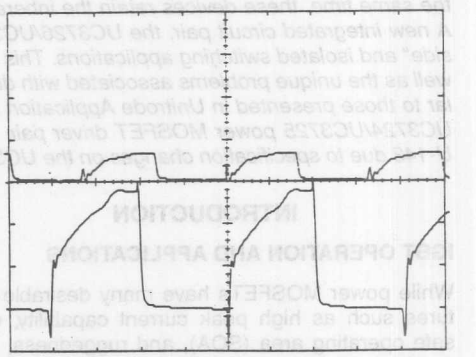


Fig. 14 Push-pull MOSFET drain current
Vertical: 200mA/div. Horizontal: 5µs/div.

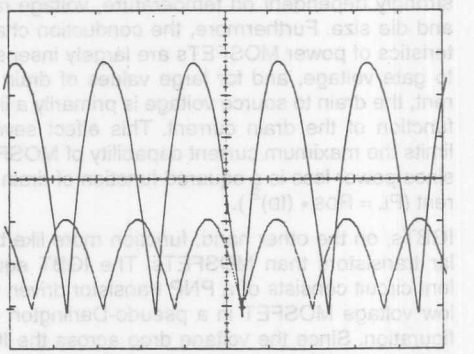


Fig. 15 Buck output voltage
Vertical: 200mA/div. Horizontal: 5µs/div.

Summary

The current fed push-pull ZVS converter efficiently develops high voltage, sinusoidal power for driving cold cathode fluorescent lamps. Design equations have been derived, and verified experimentally, simplifying application circuit design and analysis. The UC3871 provides a complete solution for high performance back-light and LCD power supplies.

NEW CHIP PAIR PROVIDES ISOLATED DRIVE FOR HIGH VOLTAGE IGBTs

By Mickey McClure
Application Engineer
Motion Control Products

Abstract

Recent advances in the design of Insulated Gate Bipolar Transistors (IGBTs) have increased their capabilities to the point where they are replacing power MOSFETs as the switching device of choice for high voltage/high current power supply and motor drive systems. Although switching speeds of IGBTs are generally slower than those of power MOSFETs, devices are now available with similar gate drive requirements. At the same time, these devices retain the inherent superior conduction characteristics of bipolar transistors. A new integrated circuit pair, the UC3726/UC3727, provides a cost-effective way to drive IGBTs in "high-side" and isolated switching applications. This application note describes the operation of this chip pair, as well as the unique problems associated with driving IGBTs. Many of the concepts presented here are similar to those presented in Unitrode Application Note U-127, written by John O'Connor, which describes the UC3724/UC3725 power MOSFET driver pair. This application note replaces Unitrode Application Note U-143 due to specification changes on the UC3727.

INTRODUCTION

IGBT OPERATION AND APPLICATIONS

While power MOSFETs have many desirable features such as high peak current capability, wide safe operating area (SOA), and ruggedness, they do have some inherent disadvantages. Among these are conduction characteristics that are strongly dependent on temperature, voltage rating and die size. Furthermore, the conduction characteristics of power MOSFETs are largely insensitive to gate voltage, and for large values of drain current, the drain to source voltage is primarily a linear function of the drain current. This effect severely limits the maximum current capability of MOSFETs since power loss is a squared function of drain current ($P_L = R_{DS} \bullet (I_D)^2$).

IGBTs, on the other hand, function more like bipolar transistors than MOSFETs. The IGBT equivalent circuit consists of a PNP transistor driven by a low voltage MOSFET in a pseudo-Darlington configuration. Since the voltage drop across the IGBT is the sum of the voltage drop across the P-N junction and the voltage drop across the driving MOSFET, the total voltage drop across the IGBT can never go below a diode drop. This leads to greater power dissipation at low current levels than for a MOSFET. However, this disadvantage is greatly offset by the fact that the conduction characteristics of IGBTs increase with increasing gate voltage. An increase in gate voltage leads to an increase in channel current for the driving MOSFET. This in turn leads to a reduction in voltage drop across the PNP. Furthermore, since the output PNP behaves largely like a bipolar transistor, voltage drop is not a linear function of collector current, which leads to much lower power dissipation at high current levels. Because of these superior characteristics, IGBTs can operate at much higher current levels than power MOSFETs of the same die size.

OVERVIEW OF IGBT DRIVE REQUIREMENTS AND PROBLEM AREAS

The conduction characteristics of an IGBT are similar to those of an N-channel MOSFET in that a positive gate-to-emitter voltage is required for conduction. This characteristic leads to the problem of gate biasing in "high-side" drive applications. Since the gate must be biased above the high voltage input, high side drive requirements can lead to costly and complex gate circuits, as the gate must sometimes be biased hundreds of volts above system ground.

In addition to the biasing problem, other gate drive requirements include low drive impedance to reduce switching losses, as well as sufficient current to charge the gate fast enough to achieve the desired switching time. The charge current requirement is derived from the total gate charge (Q_G) as specified on the IGBT data sheet. Additionally, since the combination of high voltage and relatively fast switching speed results in both high dv/dt and di/dt, the gate is usually biased with a negative voltage during turn off to prevent transient turn on.

faults.

Unitrode Application Note U-127 mentions several common approaches to solving the high side driver problem. Among the common techniques used are floating power supplies for the driver circuitry, charge pump circuits, high voltage driver ICs, and optocoupler isolated driver circuits. Each of these techniques have limitations, and those limitations are discussed in detail in U-127.

UC3726/UC3727 DRIVER PAIR

The UC3726/UC3727 IC pair provides an elegant, yet compact and cost-effective solution to the problem of driving IGBTs in high side and isolated applications. The chip pair is similar to the UC3724/UC3725 chip pair, except optimized for the unique problems associated with driving IGBTs. Figure 1 shows the basic circuit configuration for the UC3726/UC3727 circuit pair. In addition to the IC pair, a few passive components and a pulse transformer are required to complete the circuit. Also, an optocoupler can be used to provide fault information to the UC3726 if it is desired. The optocoupler can be eliminated and fault protection still provided by the UC3727 if it is not required to pass fault information back to the system. This feature is explained in detail in the fault section of this application note.

The UC3726 transmitter generates a carrier signal that utilizes a unique duty cycle modulation technique to transmit both command signal and power stead of silicon, two low voltage ICs can be used. This leads to a very cost effective and simple solution to the high voltage gate drive problem.

The UC3727 comparator circuitry senses the transmitted duty cycle and decodes the ON/OFF gate drive command. A diode bridge rectifies the carrier input to provide power to the IC. The output gate drive signal is in phase with the command, and is guaranteed to be 16V. Intermediate high drive or clamp levels can be programmed for various periods of time to limit surge current at turn on, and during short term fault conditions. A bipolar voltage supply is also provided to supply negative gate drive to insure that the IGBT remains off in the presence of high common mode slew rates.

UC3726 DRIVE TRANSMITTER

Figure 2 shows the block diagram for the UC3726 drive transmitter IC. The major components of the circuit include two tri-level output drivers with zero current sense detectors and control logic, a bias voltage generator with undervoltage lockout, a retriggerable one shot, a TTL compatible input with hysteresis, as well as fault sense circuitry and control logic.

The circuit operates by using a unique duty cycle modulation technique to simultaneously pass ON/OFF command information and power to the UC3727 isolated IGBT high side driver. This technique was originally developed for the UC3724/UC3725 high side MOSFET driver pair. Application

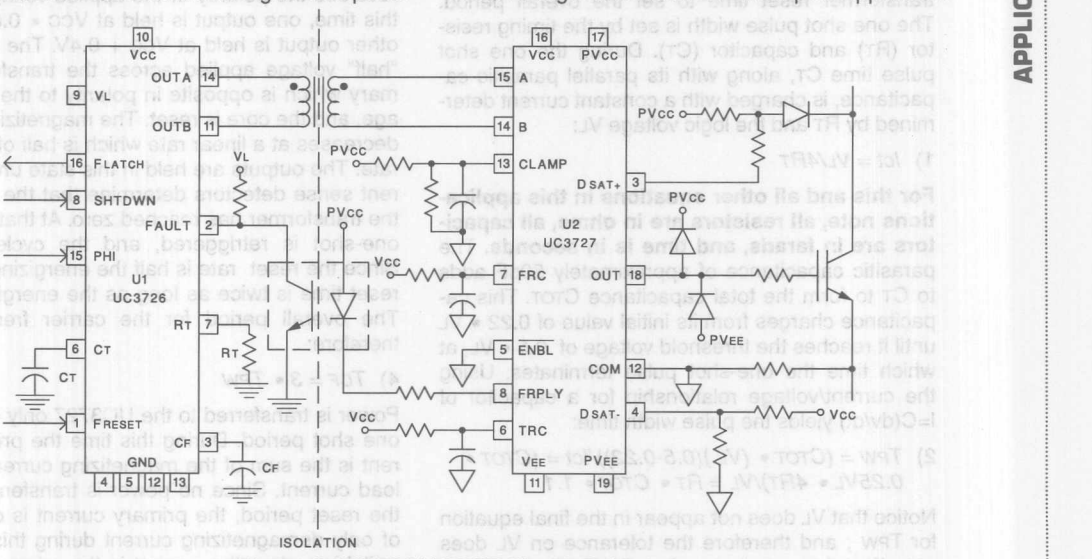


Figure 1. UC3726/UC3727 Circuit Pair

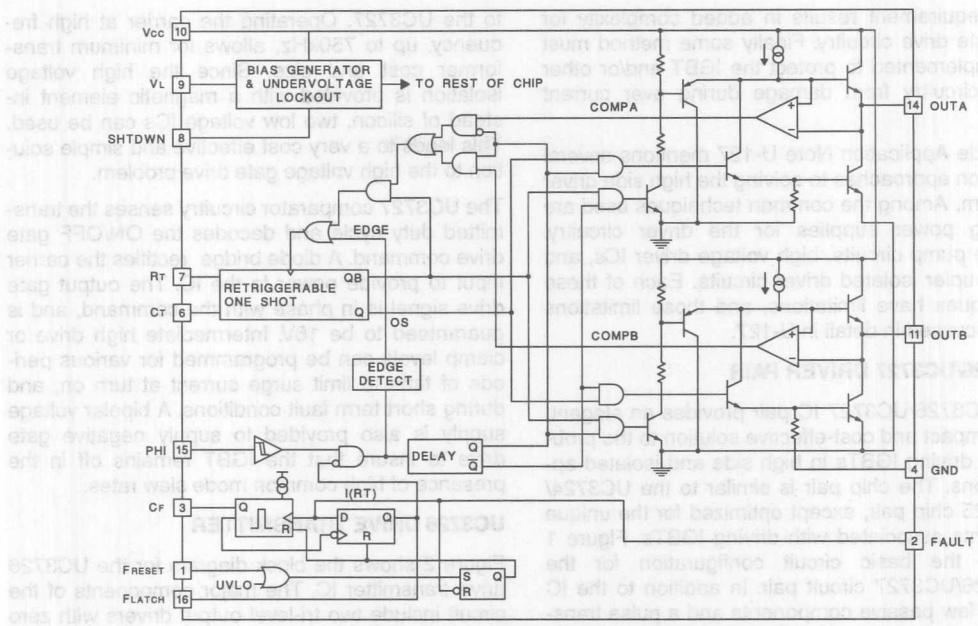


Figure 2. Drive Transmitter IC

Note U-127 describes the operation of that chip pair, and many of the concepts are similar. Specific differences primarily relate to waveform timing.

CARRIER FREQUENCY/TIMING/OUTPUT DRIVES/INPUT COMMAND

By choosing a high frequency carrier, cost efficiency can be maximized. The carrier frequency uses both a one shot pulse width and the pulse transformer reset time to set the overall period. The one shot pulse width is set by the timing resistor (R_T) and capacitor (C_T). During the one shot pulse time C_T, along with its parallel parasitic capacitance, is charged with a constant current determined by R_T and the logic voltage V_L:

1) $Ict = V_L/4R_T$

For this and all other equations in this applications note, all resistors are in ohms, all capacitors are in farads, and time is in seconds. The parasitic capacitance of approximately 50pF adds to C_T to form the total capacitance C_{TOT}. This capacitance charges from its initial value of 0.22 • V_L until it reaches the threshold voltage of 0.5 • V_L, at which time the one-shot pulse terminates. Using the current/voltage relationship for a capacitor of I=C(dv/dt) yields the pulse width time:

2) $T_{PW} = (C_{TOT} • (V_L)(0.5\text{-}0.22))/Ict = (C_{TOT} • 0.25V_L • 4R_T)/V_L = R_T • C_{TOT} • 1.1$

Notice that V_L does not appear in the final equation for T_{PW} , and therefore the tolerance on V_L does not affect the one shot period. During the one shot period "full" output voltage is applied across the primary of the pulse transformer, with one output held at V_{CC}-2.0V, and the other output held at 0.3V. During this time, transformer magnetizing current rises linearly at a rate determined by the transformer inductance and applied voltage:

3) $di/dt = (V_A\text{-}V_B)/L_{pri}$

At the end of the one shot period, the control logic reverses the polarity of the applied voltage. During this time, one output is held at V_{CC} • 0.6, and the other output is held at V_{CC} + 0.4V. The result is a "half" voltage applied across the transformer primary which is opposite in polarity to the "full" voltage, and the core is reset. The magnetizing current decreases at a linear rate which is half of the rising rate. The outputs are held in this state until the current sense detectors determine that the current in the transformer has reached zero. At that point, the one-shot is retriggered, and the cycle repeats. Since the reset rate is half the energizing rate, the reset time is twice as long as the energizing time. The overall period for the carrier frequency is therefore:

4) $T_{CF} = 3 • T_{PW}$

Power is transferred to the UC3727 only during the one shot period. During this time the primary current is the sum of the magnetizing current and the load current. Since no power is transferred during the reset period, the primary current is composed of only demagnetizing current during this time. By switching when the current in the primary reaches

zero, the UC3726 assures that the core is reset, and there is no danger of saturation.

Figure 3 shows steady state waveforms for a continuous logic low input command. At time to the one shot pulse begins, and the voltage across C_T charges until it reaches the threshold at time t_1. The magnetizing current in the primary builds up linearly during this time. At t_1 the one shot period ends, and the primary current begins decreasing. At time t_2 zero current is reached and detectors retrigger the one shot, initiating the next one shot cycle. The waveforms for V_A and V_B reflect the half and full voltage concepts described previously.

The downward slope on V_{CT} is the result of an internal timing circuit which provides a blanking interval which will not allow the output drivers to switch states while the inductor current is decreasing until a time period equal to the energizing period has expired. This protection feature is provided to prevent switching transients from triggering a state change on the output drivers prematurely.

If a continuous high input is commanded, the waveforms for V_A and V_B are interchanged, and the magnetizing current is inverted. The UC3727 determines command information by sensing the polarity of the full voltage at the transformer secondary.

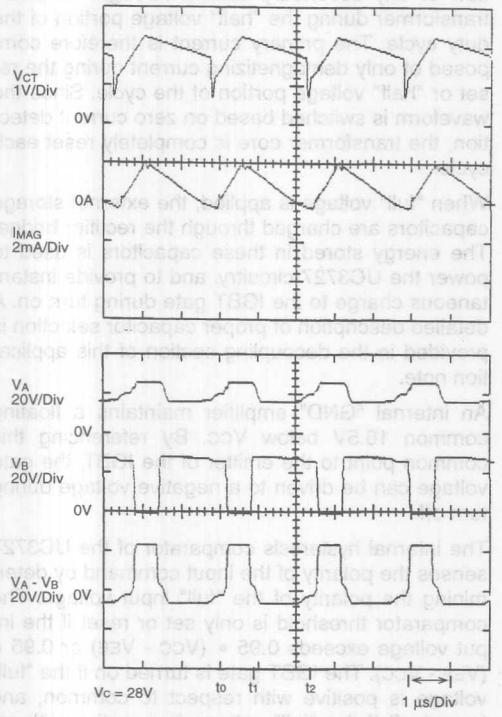


Figure 3. Steady State Waveforms Continuous Logic Low Input

This is described in detail later in this application note.

When a command transition occurs, the existing oscillator cycle is terminated, and a new cycle is started by applying full voltage in the opposite polarity. There is no danger of saturating the core, because the current must fall to zero before a new one shot trigger can occur. Newly incorporated circuitry prevents output jitter during a command transition by assuring equal propagation delay to the output regardless of the point in the cycle that the transition occurs.

FAULT/FAULT TIMING/FAULT RESET

The UC3726 contains special circuitry to prevent drive information from being transmitted during fault conditions. The FAULT input to the chip is designed to interface with the UC3727 through an optocoupler. At power up the UC3726 FAULT pin is pulled high through an external resistor, and the fault logic is reset by the UVLO circuitry.

Once its UVLO level is exceeded, the UC3727 drives the FAULT pin low, and the fault logic is enabled. After this point, the UC3727 will keep the FAULT pin low unless a fault is indicated. Special fault detection circuitry in the UC3727 detects overcurrent conditions (faults) and informs the UC3726 through the FAULT signal. To be recognized as a valid fault, the FAULT signal must remain high during the entire fault window. The timing for this window is set by C_F and R_T and is determined by the following equation:

5) $t_F = (C_F \bullet R_T) \bullet 2.1$

If a valid fault is recognized, the fault latch is set, and the outputs will remain in the logic low states until the FRESET signal (input to the UC3726) is toggled high. This signal should be powered up low, and remain low until a valid fault is recognized. Once the fault is cleared, the FRESET signal should be brought low again. The minimum pulse width on FRESET to guarantee a reset is 1µsec.

Figure 4 shows the waveforms for the FAULT circuitry signals for a valid fault. It should be noted that use of this function requires a "smart" system.

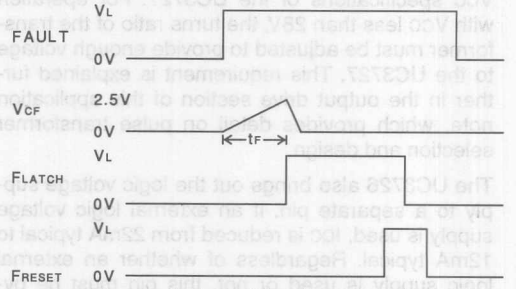


Figure 4. Fault Circuitry Signals

The fault latch must be reset in order for operation to continue once a valid fault is recognized. If the optocoupler used has a high level of output capacitance, it may be necessary to provide a reset pulse to the FRESET pin of the UC3726 after it has completed its power up sequence. Since a low to high transition on the FAULT pin indicates a valid fault, a slow rising waveform on this pin will result in a fault indication at power up. If this occurs, the output drive of the UC3726 will be latched off until the reset pulse is provided.

If this level of complexity is not desired or required, the FAULT input to the UC3726 can be permanently enabled by tying it low, allowing the UVLO circuitry to reset the fault latch. The UC3727 has additional fault protection circuitry that will protect the output IGBT independently, but the UC3726 will not be informed that a fault has occurred. Since the FAULT input to the UC3726 is tied low through a low impedance, the reset pulse after power up is not required for this case.

SHUTDOWN/UVLO/LOGIC VOLTAGE OPERATION

The UC3726 provides a shutdown pin (SHTDWN) which can be used to place the IC in a low power shutdown mode. By bringing this point high, the internal reference is disabled, and supply current is reduced to 2.5mA typical. Since the typical supply current when the chip is active is 20mA, the power savings are substantial. While in shutdown mode, both the A and B output drives are held low (ground). If an external logic supply is used, it must also be disabled for the shutdown feature to work.

The UC3726 also provides internal under voltage lockout (UVLO) circuitry. This feature will disable the internal reference, and disable the output drivers (hold at ground), if VCC is below 6.5V. It should be noted, however, that VCC must be held high enough to satisfy the UVLO feature of the UC3727. If the pulse transformer has a turns ratio of 1:1, VCC must be held at 28V to guarantee proper operation of the UC3727. This requirement is derived from the maximum saturation drops of the UC3726, as well as the UVLO, rectifier drops, and VCC specifications of the UC3727. For operation with VCC less than 28V, the turns ratio of the transformer must be adjusted to provide enough voltage to the UC3727. This requirement is explained further in the output drive section of this application note, which provides detail on pulse transformer selection and design.

The UC3726 also brings out the logic voltage supply to a separate pin. If an external logic voltage supply is used, ICC is reduced from 22mA typical to 12mA typical. Regardless of whether an external logic supply is used or not, this pin must be bypassed to ground with a high quality ceramic capacitor of at least 0.1μF.

UC3727 ISOLATED HIGH SIDE IGBT DRIVER

Figure 5 shows the block diagram of the UC3727 high side IGBT driver IC. The major circuit components include a Schottky diode rectifier bridge, a differential sense comparator with hysteresis, a bias and reference generator including undervoltage lockout circuitry and thermal shutdown, a high current gate driver stage with a programmable clamp drive level, a negative gate drive voltage supply, and fault detection and shutdown circuitry. An enable input is also provided to allow for stand alone operation with external bipolar voltage supplies.

SIGNAL AND POWER INPUT/NEGATIVE POWER SUPPLY

As shown on Figure 5, the input stage to the UC3727 both rectifies the input signal to supply power to the IC, and demodulates the input signal to determine the polarity of the gate drive command. Because the rectifier bridge peak detects the input signal, power is only transferred to the storage capacitors during the "full" voltage portion of the duty cycle. This operating mode prevents the flow of any secondary current through the pulse transformer during the "half" voltage portion of the duty cycle. The primary current is therefore composed of only demagnetizing current during the reset or "half" voltage portion of the cycle. Since the waveform is switched based on zero current detection, the transformer core is completely reset each cycle.

When "full" voltage is applied, the external storage capacitors are charged through the rectifier bridge. The energy stored in these capacitors is used to power the UC3727 circuitry, and to provide instantaneous charge to the IGBT gate during turn on. A detailed description of proper capacitor selection is provided in the decoupling section of this application note.

An internal "GND" amplifier maintains a floating common 16.5V below VCC. By referencing this common point to the emitter of the IGBT, the gate voltage can be driven to a negative voltage during turn off.

The internal hysteresis comparator of the UC3727 senses the polarity of the input command by determining the polarity of the "full" input voltage. The comparator threshold is only set or reset if the input voltage exceeds 0.95 • (VCC - VEE) or 0.95 • (VEE - VCC). The IGBT gate is turned on if the "full" voltage is positive with respect to common, and turned off if the "full" voltage is negative with respect to common. Note that this represents a logic

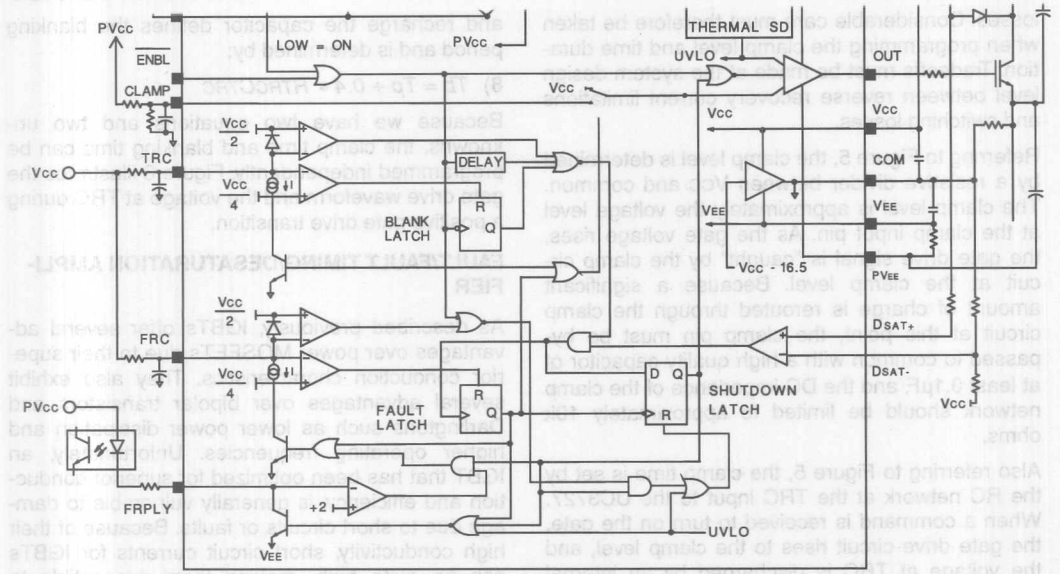


Figure 5. UC3727 High Side IGBT Driver IC

inversion to account for the logic inversion in the UC3726.

The UC3727 provides separate inputs for Vcc, PVcc, VEE, and PVEE. By separating the output driver supplies (PVcc and PVEE) from the power supplies for the rest of the circuitry, better noise immunity can be achieved. The PVcc and PVEE inputs should be isolated from their respective low current supplies by 3.3Ω and bypassed to the IGBT emitter with 1.0µF capacitors as shown on Figure 5.

OUTPUT DRIVER STAGE

The output stage of the UC3727 consists of a high current, bipolar power amplifier. The peak output current of 4A provides the ability to drive IGBT gates requiring large amounts of gate charge. In order to provide a controlled or "soft" gate drive signal, the gate drive can be programmed for a two step turn on waveform. At turn on, the drive amplifier waveform will rise to a user defined clamp level for a user defined time duration. The benefits and uses of this clamp level are explained in further detail in the following section of this application note. After the time duration expires, the drive waveform will then rise to its maximum level (approximately 15V).

The common output of the UC3727 is designed to be referenced to the emitter of the IGBT to allow the gate to be driven negative during turn off. By regulating this common point to a fixed level below Vcc, the remaining differential supply voltage (Vcc - VEE) - (Vcc - Vcom) can be used to generate the negative bias.

Under voltage lockout is also featured in the UC3727. Because Vcom is a regulated point below Vcc, the differential input voltage VA - VB must exceed the maximum potential difference between Vcc and Vcom, plus the UVLO level between Vcom and VEE, plus the diode drops of the rectifier bridge. In equation form this can be stated as:

6) $V_A - V_B \geq V_{CC} + V_{EEUVLO} + 2V_D$

The differential input voltage is supplied by the UC3726 through the pulse transformer (in most cases). Consideration must be given to Equation 6 when selecting a supply voltage for the UC3726, and during pulse transformer selection. If worst case specifications are considered, the differential input voltage must be greater than 25.3V to guarantee proper operation of the UC3727.

OUTPUT CLAMP/SOFT TURN ON

A common application of IGBTs involves driving clamped inductive loads. In this case, the maximum allowable reverse recovery current of the clamp diode can be a limiting factor. One way to limit the reverse recovery current is to provide a soft turn on to the IGBT gate. Since the conduction

of the IGBT channel is sensitive to gate voltage, the peak current through the channel can be limited by providing a clamp level during turn on. Unfortunately, this will result in greater switching losses. Considerable care must therefore be taken when programming the clamp level and time duration. Tradeoffs must be made at the system design level between reverse recovery current limitations and switching losses.

Referring to Figure 5, the clamp level is determined by a resistive divider between Vcc and common. The clamp level is approximately the voltage level at the clamp input pin. As the gate voltage rises, the gate drive signal is "caught" by the clamp circuit at the clamp level. Because a significant amount of charge is rerouted through the clamp circuit at this point, the clamp pin must be bypassed to common with a high quality capacitor of at least 0.1µF, and the DC impedance of the clamp network should be limited to approximately 10k ohms.

Also referring to Figure 5, the clamp time is set by the RC network at the TRC input to the UC3727. When a command is received to turn on the gate, the gate drive circuit rises to the clamp level, and the voltage at TRC is discharged by an internal current source. Once the threshold of Vcc/4 is reached, an internal comparator trips, and full gate voltage is applied. The clamp period is determined by:

$$7)\ Tp = R_{TRC} \bullet C_{TRC} \bullet ln\left(\frac{R_{TRC} - 7600}{R_{TRC} - 12400}\right)$$

This RC network also determines the blanking time for the desaturation comparator. The desaturation comparator is used to detect fault conditions which result in the IGBT coming out of saturation while the gate drive is high. Due to the turn on delay of the IGBT, this comparator must be ignored after a command transition to the on state until the IGBT transitions into saturation. The blanking time requirement is derived from the turn on and saturation characteristics of the IGBT.

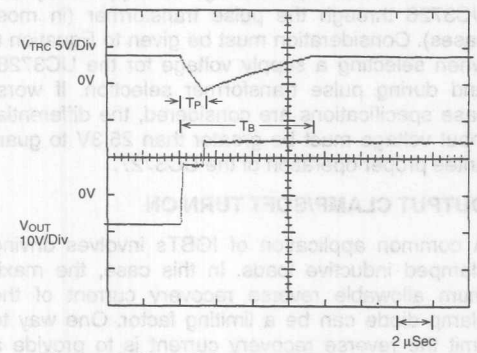


Figure 6. Gate Drive and TRC Waveforms Positive Gate Transition

Once the clamp time period has expired, the output driver increases the gate voltage to the fully on level. The voltage at TRC is then allowed to charge back to Vcc/2. The total time it takes to discharge and recharge the capacitor defines the blanking period and is determined by:

$$8)\ Tb = Tp + 0.4 \bullet R_{TRC}C_{TRC}$$

Because we have two equations and two unknowns, the clamp time and blanking time can be programmed independently. Figure 6 illustrates the gate drive waveform and the voltage at TRC during a positive gate drive transition.

FAULT/FAULT TIMING/DESATURATION AMPLIFIER

As described previously, IGBTs offer several advantages over power MOSFETs due to their superior conduction characteristics. They also exhibit several advantages over bipolar transistors and Darlingtons such as lower power dissipation and higher operating frequencies. Unfortunately, an IGBT that has been optimized for superior conduction and efficiency, is generally vulnerable to damage due to short circuits or faults. Because of their high conductivity, short circuit currents for IGBTs can be quite high, making them susceptible to damage due to excess power dissipation.

When building short circuit protection into an IGBT driver circuit, the response of the protection circuit must be fast enough to insure that the device is shut off before damage to the IGBT or any other part of the circuit occurs. At the same time, care must be taken to avoid nuisance triggering from short duration faults that do not result in any circuit damage. If the gate drive to the IGBT is shut off completely as soon as a fault is detected, the result may be an intolerable amount of nuisance shut downs. Therefore, it would be advantageous to program the allowable short circuit time as long as possible.

If the gate drive voltage is reduced when a fault is detected, the short circuit current can be reduced, and therefore the short circuit time can be stretched. However, reducing the gate voltage also increases the saturation voltage of the IGBT, which is undesirable for normal conduction. Therefore, the ideal short circuit protection technique will reduce the gate voltage only when a fault condition is detected, and keep the gate voltage at the reduced level for as long as possible, before shutting down the IGBT completely. In order for this technique to work effectively, the maximum short circuit time as a function of gate voltage must be known.

Referring again to Figure 5, the UC3727 provides a desaturation comparator designed to detect short circuit or fault conditions, and provide both short term and long term protection for the IGBT. The

DSAT+ input to the comparator is biased off to a DC level which is higher than the maximum saturation level of the IGBT plus one diode drop. During normal operation, the DSAT- input will be pulled down to the saturation voltage of the IGBT plus one diode drop. The blanking period discussed previously protects against false trips of the desaturation comparator while the IGBT is turning on.

If a fault occurs outside of the blanking interval, the gate drive will be reduced to the clamp level for a time period determined by the RC network at the FRC pin of the UC3727. The time period can be calculated by the following equation:

9) $T_f = R_{FRC} \bullet C_{FRC} \bullet \ln((R - 7600)/(R - 12400))$

As soon as the fault is detected the FRPLY output of the UC3727 will go high. If the UC3726 is configured to accept this signal as an input, through an optocoupler or level shift network, its own fault timing circuitry will be activated.

If the desaturation event ends before the fault time has expired, the gate drive will be driven back to its maximum level, and FRPLY will go back low. In order to insure that the desaturation amplifier can accurately determine that a fault condition no longer exists, the DSAT- input level must be biased higher than the desaturation level of the IGBT with the reduced gate drive, plus a diode drop.

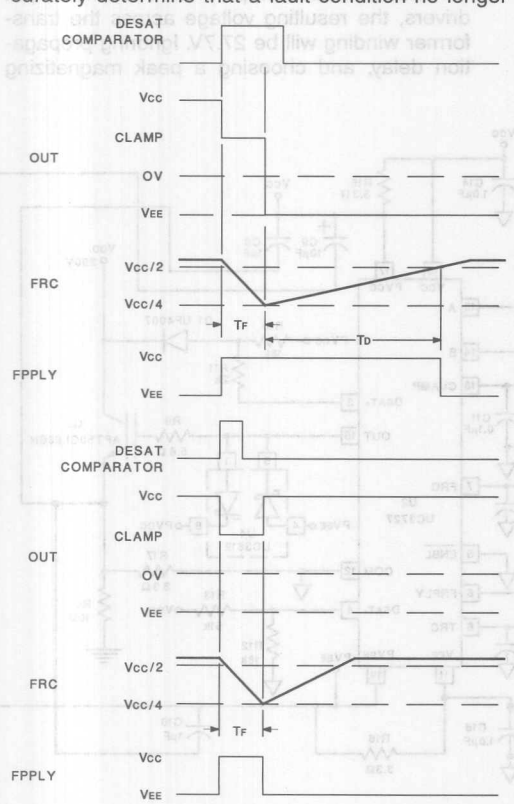


Figure 7. Fault Signal Waveforms

If the desaturation event does not end within the fault time, the output gate drive will be driven completely off, and the chip will not accept a command to drive the gate high until a delay period has expired. The equation for the delay period is determined by the same RC network as the fault time:

10) $T_d = 0.4 \bullet R_{FRC} \bullet C_{FRC}$

Again, since there are two equations and two unknowns, the fault time and delay time can be programmed independently. FRPLY will remain high for the entire delay period. If the UC3726 is configured to accept FRPLY as an input, it will have the ability to prevent any command to turn on the gate from being transmitted until its fault latch has been reset. Figure 7 shows the waveforms for fault signals for both transient and long term faults.

ENABLE INPUT/STAND ALONE OPERATION

The UC3727 provides an active low enable input for stand alone operation. This input is useful for operating the chip as a high side driver with isolated power supplies. The enable input can also be used to control the chip for low side driver applications if external power supplies are available. If the UC3727 is not used in stand alone mode, i.e. it is driven by the UC3726, the enable input should be tied to common.

If $\overline{\text{ENBL}}$ is used as a command input, the B input should be tied to VCC, and the A input should be tied to VEE. Note the polarity change described previously. The output gate drive will be driven high when $\overline{\text{ENBL}}$ is held at the same potential as common, and the gate drive will held low when $\overline{\text{ENBL}}$ is tied to VCC. For low side driver applications $\overline{\text{ENBL}}$ can be controlled by a discrete transistor operating off of conventional logic. For high side driver applications, $\overline{\text{ENBL}}$ must be controlled by an optocoupler, or a discrete transistor operating off as a level shift network. Because the optocoupler or discrete transistor will function as an inverter in this case, the result will be positive logic to the output. Therefore, turning on the optocoupler or transistor will turn on the IGBT. Figure 8 shows a circuit diagram for using the $\overline{\text{ENBL}}$ input as a command input.

If external power supplies as used for grounded emitter low side operation, common should never be connected to system ground. This point is not designed to sink the large amounts of current flowing out of the emitter of the IGBT. Both the positive and negative supplies should by bypassed to common with capacitors, and the common output should be DC isolated from ground.

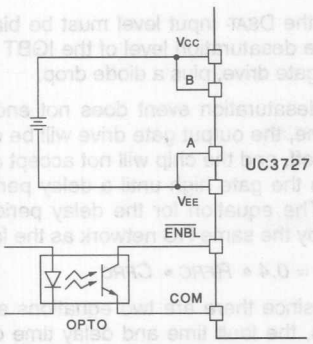


Figure 8. ENBL Used as Command Input

PRACTICAL DESIGN CONSIDERATIONS/EXAMPLE CIRCUIT

Figure 9 depicts a typical high side IGBT driver circuit. All of the features of the IC driver pair are utilized to provide maximum circuit protection and flexibility. This configuration might be used as a high side switch for a power supply, or it might form part of an H-bridge configuration for a motor driver. A resistive load is assumed in order to illustrate the high switching speeds of the driver pair. Real systems would likely require driving clamped inductive loads, and switching speed would be purposely slowed to protect external components such as clamp diodes. Component values for the support circuitry are chosen based on the specific requirements of the system. What follows is a step by step design procedure for a typical circuit.

PULSE TRANSFORMER DESIGN CONSIDERATIONS

Application note U-127 provides a detailed explanation of recommended transformer design criteria for the UC3724/UC3725 chip pair. Since the transformer design procedure is similar for the UC3726/UC3727 chip pair, the theory is not repeated in this application note. However, a transformer has been designed by Coilcraft (Q3868-A) specifically for use with the UC3726/UC3727 pair. This transformer has been optimized for operation at 400kHz, resulting in small size and low cost. Since the maximum switching frequency for the IGBT is 1/4 of the transformer frequency, the resulting 100kHz maximum IGBT frequency is near the typical maximum operating range of power IGBTs. The following calculations provide a brief overview of the design of the Q3868-A transformer:

Assuming a Vc of 30V for the UC3726 and typical total saturation drops of 2.3V for the output drivers, the resulting voltage across the transformer winding will be 27.7V. Ignoring propagation delay, and choosing a peak magnetizing

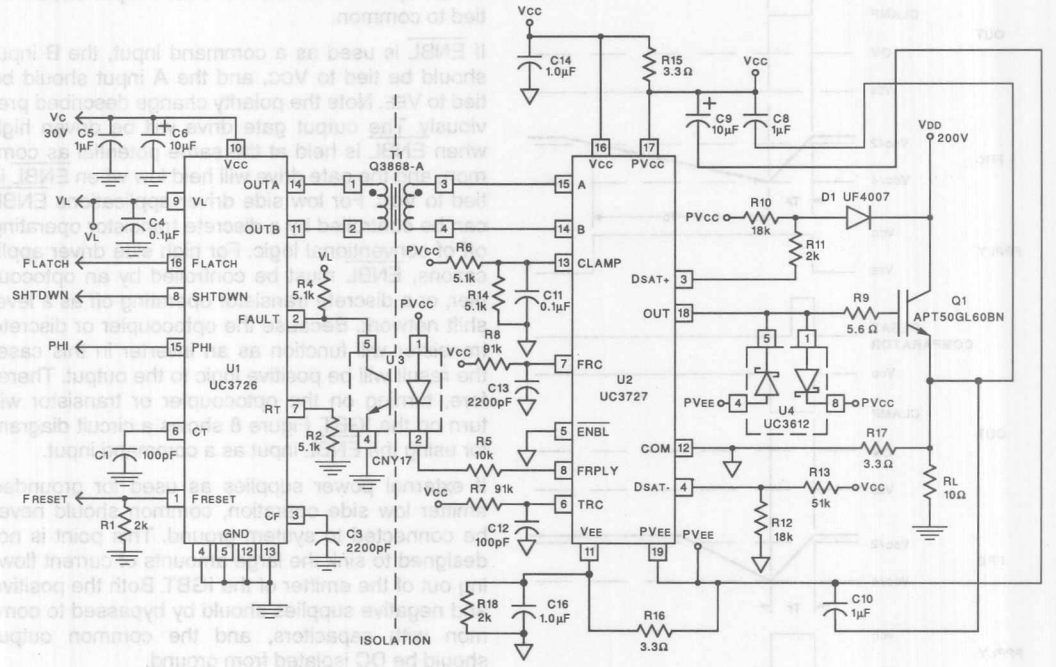


Figure 9. Typical High Side Driver Circuit

The 833ns represents 1/3 of the period of the 400kHz carrier, which is the pulse width time as defined by Equation 4 of this document:

12) $T_{PW} = 1/(3 \bullet 400kHz) = 833ns$

Using Equation 8 of U-127, and an initial value of A_L = 2000mH/1000 turns, an estimated number of turns is calculated:

13) $N_{TURNS} = ((659\mu H \bullet 10^9)/2000)^{1/2} = 18$ turns

From Equation 8 of U-127:

14) $A_e = ((27.7V)(833ns)(10^4)/((18\ turns)(0.05T)) = 0.256\ cm^2$

A Magnetics core, P-41206-TC was chosen with the following specifications:

A_L = 2820mH/1000 turns

A_e = 0.221 cm^2

V_e = 0.554 cm^3

Recalculating the number of turns yields:

15) $N_{TURNS} = ((659\mu H)(10^9)/2820)^{1/2} = 15.3$ turns, use 15 turns

The flux density of the transformer design is then checked using Equation 8 of U-127:

16) $delta\ B = ((27.7V)(833ns)(10^4)/((15\ turns)(0.221\ cm^3) = 0.069T$

To determine the core loss due to the magnetizing current, the core loss vs. flux density curve for the core is consulted:

At 400kHz and 0.069T, P_L = 400mW/cm^3

Therefore, the core loss can be calculated as:

17) $P_{CL} = (400mW/cm^3)(0.554\ cm^3) = 222mW$

The transformer is wound with AWG #30 KYNAR wire. In order to minimize leakage inductance, the primary and secondary windings are wound bifilar. The maximum DC resistance of the primary winding is 0.130 ohms, and therefore resistive losses due to magnetizing current are minimal. There will be additional resistive losses due to bias current for the UC3727 and gate drive current for the IGBT. For IGBTs with large gate charge requirements, these losses may become significant, and the transformer design must be adjusted accordingly.

In some cases it may be necessary to add a damping resistor across the transformer secondary to minimize ringing and eliminate false triggering of the hysteresis comparator.

available than capacitors, we choose C_T = 100pf. We then use Equation 2 and a one shot pulse width of 833ns to determine R_T :

18) $R_T = (833ns)/((100pF + 50pF) \bullet 1.1) = 5.1k$

Referring to Figure 9, this results in R2 = 5.1k and C1= 100pF.

OUTPUT DRIVE CONSIDERATIONS/CLAMP LEVEL AND BLANKING TIME

In order to design the gate drive portion of the IGBT driver circuit, several criteria must be considered to balance what sometimes are conflicting requirements. The ideal situation would involve switching the IGBT as fast as possible to minimize switching losses. However, there will be cases when it is desirable to reduce the switching speed of the IGBT. An example case would be slowing down the turn on time to limit the reverse recovery current into the free wheel diode when driving a clamped inductive load. Another example might be reducing the turn on time in a half bridge configuration to prevent cross conduction.

In order to evaluate the drive requirements of the IGBT, the gate charge characteristics of the device are used. However, evaluating the gate charge does not lead to a good prediction of switching times as it does with power MOSFETs. The reason for this is the fact that IGBTs are minority carrier devices. This characteristics leads to slower switching times than power MOSFETs due to base charge storage. The turn off time is much slower than the turn on time, and is characterized by a "tail" in the current waveform. To predict switching times of IGBTs, the manufacturers data sheets must be consulted for turn on delay (t_{d} on), rise time (t_r), turn off delay (t_{d} off), and fall time t_f.

The drive circuitry should be designed so that additional delay is not introduced due to gate charge requirements. In the example shown in Figure 9, an APT50GL60BN IGBT is used (500V, 60A). The key timing specifications of this device are as follows:

Total Gate Charge (Q_g) = 110nC

Turn On Delay (t_{d} on) = 15ns

Rise Time (t_r) = 50ns

Turn Off Delay (t_d) = 55ns

Fall Time (t_f) = 350ns

The UC3727 output stage is a 4A peak driver. The time required to charge the gate is therefore:

19) $T_{CH} = 110nC/4A = 27.5ns$

Since this time is about half of the sum of the turn on delay time and the rise time, significantly reducing the drive current will slow down the turn on time of the device. However the fall time of the IGBT is much longer (350ns), and therefore gate drive current does not significantly affect the turn off time.

For the example circuit it is assumed that the fastest switching speed possible is desired. However, since the UC3727 is rated for 4A peak drive current, a gate resistor is used to limit the peak current. Taking into account rectifier and saturation drops, the maximum swing of the gate voltage is 20.5 volts. The gate resistor is therefore chosen by:

20) $R9 = 21.5V/4A = 5.1ohm$, use 5.6ohm

For circuits like half bridge amplifiers where cross conduction is a concern, a diode can be used with dual gate resistors to provide a higher gate impedance for turn on than for turn off, to provide cross conduction protection. An example of this technique is shown in the design example section of this application note.

For circuits where the collector of the IGBT is subjected to high dv/dt, the gate resistor must be sufficiently small to prevent unwanted gate turn on due to voltage drop across the gate resistor when current flows through the Miller capacitance in the presence of the high dv/dt. For high current IGBTs, emitter inductance can also cause transient turn on in the presence of high di/dt, by pulling the emitter node negative. These problems are partially mitigated by the negative gate bias of the gate drive in the off state, but the designer must be aware of the additional limitations in gate resistor selection if large values of gate resistors are desired.

For large IGBTs the power rating of the gate resistor must also be considered. In order to determine the average power dissipated by the gate resistor, energy supplied to the capacitor is determined by:

21) $E = (2)(1/2) \bullet C_{GATE} \bullet V^2 = (Q_{GATE}/V) \bullet V^2 = Q_{GATE} \bullet V$

The factor of 2 comes from the fact that the gate must be both charged and discharged by the gate drive circuit. Each time the gate is charged or discharged, the gate drive circuit will dissipate an amount of energy which is equal to the amount of energy supplied to the gate. If we assume that the gate drive signal is running at 15kHz, the average power dissipated in the gate drive circuit is:

22) $P_{AVG} = E/T = (Q_{GATE} \bullet V)/T = Q_{GATE} \bullet V \bullet F = (110nC)(20.5V)(15kHz) = 34mW$

Obviously for this example power dissipation in the gate drive circuit is not a problem. However, for IGBTs with higher gate charge requirements, and higher operating frequencies, the power dissipation can become significant, and must be taken into consideration. To select the power rating of the gate resistor, assuming that all of the power in the gate drive circuit is dissipated in the gate drive resistor will lead to a conservative gate resistor rating. If a power resistor is required, it should have low inductance. A wirewound resistor is not recommended for this application, but if one is used, it must be noninductively wound.

The output of the UC3727 should be protected against adverse affects due to voltage overshoot on the gate drive signal by clamping the output circuit to both V_{CC} and V_{EE} with Schottky diodes. This is done in the circuit shown in Figure 9 with a UC3612 dual Schottky diode. For a detailed explanation of this problem see Unitrode Application Note U-111.

Once the gate drive resistor has been selected, the clamp level, clamp time, and desaturation amplifier blanking time must be selected. Choosing the clamp level involves a trade off between the soft turn on requirements and the short circuit characteristics of the IGBT. Basically the soft turn on requirements are derived from the reverse recovery characteristics of the free wheel diode if the IGBT is driving a clamped inductive load. Since the conductivity of the IGBT is reduced for lower gate voltage, the maximum current that the free wheel diode sees during reverse recovery can be controlled.

Since this example assumes a resistive load, the short circuit characteristics of the IGBT will determine the clamp requirements. Unfortunately, the short circuit characteristics are not always well known. Considerable effort must expended to test the device and determine a safe clamp level and clamp time. Test data has suggested that for the IGBT used in this example, a reduction in gate voltage to 10V will allow for a maximum short circuit time of about 40µs with a V_{DD} of 200V. With full 15V gate drive, the short circuit time would be 5µs worst case. However, a secondary requirement of the clamp circuitry is that the protection circuitry must be able to recognize that the device is back in saturation if the fault goes away during the allowable fault period. For a gate drive voltage of 8V, the APT50GL60BN will remain in saturation at the peak normal current load of 20A. Therefore 8V is chosen as a conservative number for the clamp level.

Once the clamp level is known, the only other constraint is that the DC impedance must be limited to approximately 10k ohms. With that in mind, referring to Figure 9 we have:

23) $(16.5V)(R14/(R6 + R14)) = 8V$

24) $R6 + R14 = 10k$

A solution of R6 = R14 = 5.1k will satisfy the design requirements. The clamp input is also bypassed to common with 0.1µF as discussed in the output clamp section of this application note.

As previously detailed, the clamp time on the rising edge of the gate drive waveform is only important when driving clamped inductive loads. For purposes of this example, this time is arbitrarily chosen as 0.5µs. The blanking time for the desaturation amplifier is limited by the maximum allowable short circuit time under full gate drive voltage. This requirement stems from the fact that if a fault is present before the IGBT is commanded on, the UC3727 has no way of determining that the fault is present. Therefore, the IGBT will drive into the short circuit at full gate voltage for the duration of the blanking time. Since the maximum allowable short circuit time under these conditions is 5µs, the blanking time should be less, and 4µs was selected. Equations 7 and 8 can be solved simultaneously to obtain C12 = 100pF, and R7 = 91k.

DESIGN CONSIDERATIONS FOR THE FAULT CIRCUITRY

To program the fault circuitry, the short circuit characteristics of the IGBT are again used. The first consideration is the threshold of the desaturation comparator, which is programmed at the inverting input. For fast response, this trigger amplitude should be as low as possible. However, it must also be high enough to allow the comparator to recognize if a fault has gone away during the fault window. As detailed in the previous section, the IGBT will be operating under reduced gate voltage at that time.

The data sheets for the APT50GL60BN indicate that for a gate voltage of 8V, and collector current of 20A, the collector to emitter saturation voltage is 2V. Allowing for 1V of margin, plus a maximum diode drop of 1V, the DSAT- input is selected as 4V. The level is programmed by the voltage divider formed by R12 and R13, assuming the minimum level for V_{CC} of 15.5V. This leads to R12 = 18k and R13 = 51k.

The diode used in the fault circuit must be chosen for fast reverse recovery, low capacitance, and high breakdown voltage rating. **The reverse recovery time should be at least an order of magnitude faster than the short circuit time rating of the IGBT.** The capacitance should be low enough to prevent high currents from flowing into the DSAT- input in the presence of high dv/dt. Finally, the breakdown voltage rating must obviously be greater than the maximum IGBT collector voltage.

If the IGBT collector voltage is relatively low, the diode can be replaced with a high value resistor. This solution has the advantages of low capacitance and no reverse recovery problems. However, extreme care must be exercised to insure that the resistor is large enough to prevent the DSAT+ from overvoltage conditions formed by the resistive divider when the IGBT is off.

Another alternative for low power applications is to use a more conventional current sense resistor at the emitter of the IGBT. The DSAT+ input can be tied to the high side of the sense resistor, and the DSAT- input can be biased to some trip point proportional to emitter current. This allows for more precise control of the maximum current through the IGBT. Usually the voltage drop and power dissipation of the sense resistor are two high to make this a practical solution though. An example of this technique is shown in the examples section of this application note.

R10 is chosen to provide adequate bias current to the diode to insure that it is in the on state when the IGBT is in saturation. R11 provides isolation between the diode and the DSAT+ input. Its selection is fairly arbitrary, but the reverse recovery and capacitance characteristics of the diode must be considered to insure that excess current is not injected into the DSAT+ input during switching transitions.

The next consideration is the selection of the time the gate will be held at the clamp level in the presence of a fault, referred to as the fault window. Since the allowable short circuit time with a gate drive of 10V is 40µs, the fault window is selected as 10µs to allow for plenty of margin. The selection of the delay period should take into account the relative slow speed of optocouplers, and the timing requirements on the FRESET signal that must be provided to the UC3726. The blanking period is chosen as 100µs for this example. Using equations 9 and 10 this leads to:

25) $10\mu s = (R8)(C13) \bullet ln((R8 - 7600)/(R8 - 12400)$

26) $100\mu s = 0.4 \bullet (R8)(C13)$

These equations do not yield standard values when solved simultaneously. A close solution is C13 = 2200pF and R8 = 91k. This results in a fault window of 11.8µs and a blanking period of 80µs.

The only remaining programmable option selection is the fault window timing for the UC3726. This time duration must be long enough to allow for the slow speed of the optocoupler. For this example, the optocoupler (CNY17) has a typical switching time of 10µs. Choosing C3 = 2200pF and solving Equation 5 results in a fault window of 23µsec.

FILTER/DECOUPLING CAPACITOR CONSIDERATIONS

Proper bypass capacitor selection is essential to insure proper operation of the UC3726/UC3727 chip pair. The UC3726 does not have the high peak current requirements that the UC3727 does and therefore a high quality ceramic capacitor of about 1µF is usually sufficient. This capacitor must be located as close to the VCC and GND pins of the chip as possible.

The UC3727 on the other hand must supply high peak currents during the charging and discharging of the IGBT gate. While all of the average current for the gate drive is ultimately supplied by the UC3726 through the pulse transformer, circuit inductances force most of the instantaneous peak current to come from the bypass capacitors. If insufficient bypassing is used, the ripple voltage at the UC3727 can be large enough to trip the under voltage lockout circuitry.

In order to determine the maximum allowable ripple voltage, Equation 6 is used. The margin allowed in Equation 6 becomes the maximum ripple voltage. Since the ripple voltage results from charging the IGBT gate, the equation leads to the bypass requirements for PVCC and PVEE:

27) $V_{ripple} = (V_A - V_B) - (V_{CC} + V_{EEUVLO} + 2V_D)$

The ripple voltage will be composed of a gate charge component and an ESR component. The gate charge component results from the voltage drop of the bypass capacitor due to gate charge requirements. The resulting voltage drop of the decoupling capacitor due to gate charge requirements is expressed as follows:

28) $dV_{CHARGE} = Q_G/C_{BYPASS}$

The ripple component due to ESR loss is directly proportional to the peak gate current. It is expressed as:

29) $dV_{ESR} = I_{PEAK} \bullet ESR$

In Equation 29, ESR represents the equivalent series resistance of the bypass capacitor. The sum of the voltage drops represented by Equations 28 and 29 must not exceed the maximum ripple voltage.

For the example shown in Figure 9, Equation 27 yields a maximum ripple voltage of 1.6V. The peak gate current is limited to 4A, and therefore we can calculate the maximum allowable ESR from Equation 9. If we use a maximum allowable ESR loss of 0.5V we have:

30) $ESR = 0.5V/4A = 0.125$ ohm (max)

Allowing 0.5V for the charge component of the ripple voltage sets the minimum value of bypass capacitance:

31) $C_{BYPASS} = 110nC/0.5V = 0.22\mu F$ (min)

For this circuit a single 1µF capacitor on both the PVCC and PVEE pins of the UC3727 is sufficient. For larger values of gate charge the solution would involve a small ceramic capacitor for low ESR and a larger electrolytic capacitor in parallel to supply gate charge. To be conservative, a 10µF electrolytic capacitor is added between PVCC and PVEE. The VCC and VEE pins are also bypassed as described earlier in this application note and resistive isolation is provided between the high power and low power voltage supplies. R18 is added to balance the supply currents to ensure active start up in the presence of slowly rising supply voltages. These equations only describe the minimum bypass requirements. If the system is particularly noisy, significantly more bypass capacitance may be required.

TEST CIRCUIT RESULTS

The example circuit was built and tested to verify operation, with the results shown in Figure 10. The waveforms for VE and IE are shown. Notice the characteristic "tail" in the turn off waveforms for both current and voltage. The tail results from the fact that IGBTs are minority carrier devices, and therefore have stored charge. At the beginning of turn off, the collector to emitter current decreases rapidly to the level of the hole recombination current for the device. At this point di/dt decreases, and the voltage and current waveforms tail off at a much slower rate. The reason for the bump in the voltage waveform is that as di/dt decreases, inductive voltage drops also decrease, and therefore

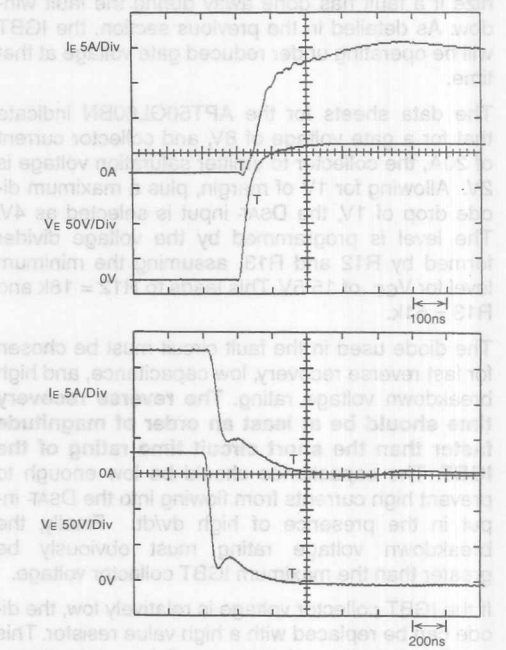


Figure 10. Test Circuit Waveforms (V_{PD} = 375V)

more voltage is dropped across the IGBT at the start of the tail.

Figure 11 shows waveforms for the same circuit when tested with V_{DD} = 375V. Notice the slower switching times due to the higher output voltage and current.

DESIGN EXAMPLES/APPLICATIONS

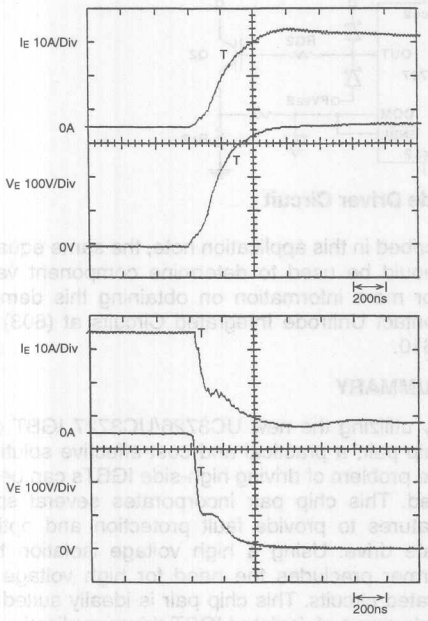


Figure 11. Test Circuit Waveforms (V_{PD} = 375V)

The example circuit described earlier in this application note provides a good baseline for calculating component values for the required support circuitry for the IGBT driver pair. Many other circuit topologies can be used with this chip set, and the same general rules apply as for the example circuit. The individual system designer must evaluate the particular requirements, and make component selections accordingly. This section illustrates some general circuit topologies which may be encountered by a typical system designer.

SENSING FAULTS WITH A CURRENT SENSE RESISTOR

Figure 12 shows a way of detecting faults with a current sense resistor. The desaturation comparator is used to detect over current conditions. Using a resistor divider network from Vcc allows the trip level to be set at the D_{SAT-} input to the comparator. Current is sensed at the emitter of the IGBT, with the filtered voltage across the current sense resistor fed into the D_{SAT+} input. This approach has an advantage for low power applications because there is no diode in the protection circuit and therefore no reverse recovery problems to worry about. Also with this technique, more precise control of the current limit is possible. A drawback to this approach is that the filter time constant required may be too long for IGBTs that can not tolerate fault conditions for very long. Also, for high power applications the power requirement for the sense resistor may be impractical.

HALF BRIDGE OUTPUT CIRCUIT

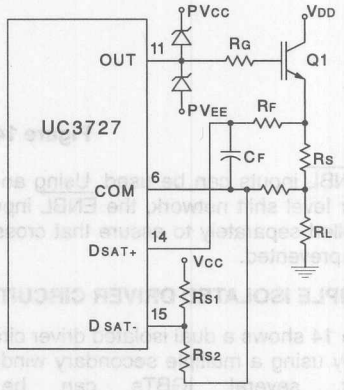


Figure 12. Detecting Faults with Current Sense Resistor

Figure 13 shows a half bridge output circuit with a dual secondary transformer. The low side of the bridge is driven by a UC3727 with its polarity reversed from the upper side driver. Cross conduction is controlled by providing dual gate resistors for both upper and lower IGBTs. Carefully selecting RG1 and RG2 can provide fast turn-off and slow turn-on. If more accurate dead time between on commands for upper and lower IGBTs is required,

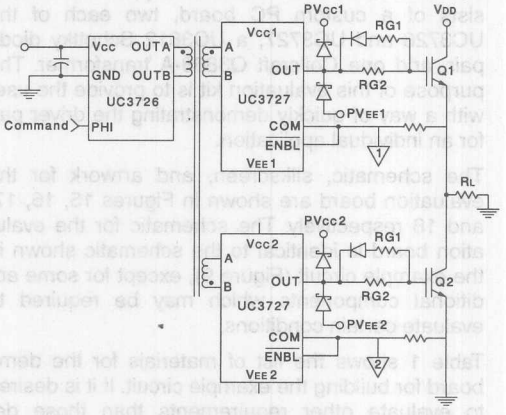


Figure 13. Half Bridge Output Circuit

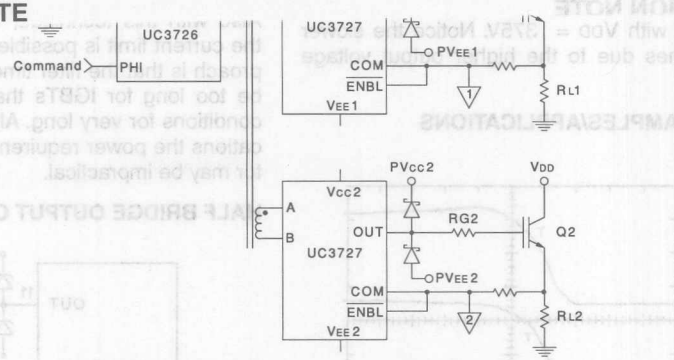


Figure 14. Dual High Side Driver Circuit

the $\overline{\text{ENBL}}$ inputs can be used. Using an optocoupler or level shift network, the $\overline{\text{ENBL}}$ input can be controlled separately to assure that cross conduction is prevented.

MULTIPLE ISOLATED DRIVER CIRCUIT

Figure 14 shows a dual isolated driver circuit topology. By using a multiple secondary winding transformer, several IGBTs can be driven simultaneously. Isolation, command signal, and power are provided to each IGBT by the single transformer. Obviously power dissipation in the UC3726 is a consideration, and ultimately will be a limiting factor in determining the maximum number of IGBTs that can be driven. The $\overline{\text{ENBL}}$ inputs can also be used to provide dead time between IGBTs if it is required.

UC3726/UC3727 IGBT EVALUATION KIT

Unitrode Integrated Circuits has designed an evaluation kit which can be used to demonstrate the UC3726/UC3727 IGBT driver pair. The kit consists of a custom PC board, two each of the UC3726 and UC3727, a UC3612 Schottky diode pair, and one Coilcraft Q3868-A transformer. The purpose of this evaluation kit is to provide the user with a way of quickly demonstrating the driver pair for an individual application.

The schematic, silkscreen, and artwork for the evaluation board are shown in Figures 15, 16, 17, and 18 respectively. The schematic for the evaluation board is identical to the schematic shown in the example circuit (Figure 9), except for some additional components which may be required to evaluate certain conditions.

Table 1 shows the list of materials for the demo board for building the example circuit. If it is desired to evaluate other requirements than those described in this application note, the same equations should be used to determine component values. For more information on obtaining this demo kit, contact Unitrode Integrated Circuits at (603) 429-8610.

SUMMARY

By utilizing the new UC3726/UC3727 IGBT driver chip pair, a practical and cost-effective solution to the problem of driving high-side IGBTs can be realized. This chip pair incorporates several special features to provide fault protection and optimum gate drive. Using a high voltage isolation transformer precludes the need for high voltage integrated circuits. This chip pair is ideally suited for a wide range of isolated IGBT driver applications.

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Coilcraft telephone number : 1-800-322-COIL

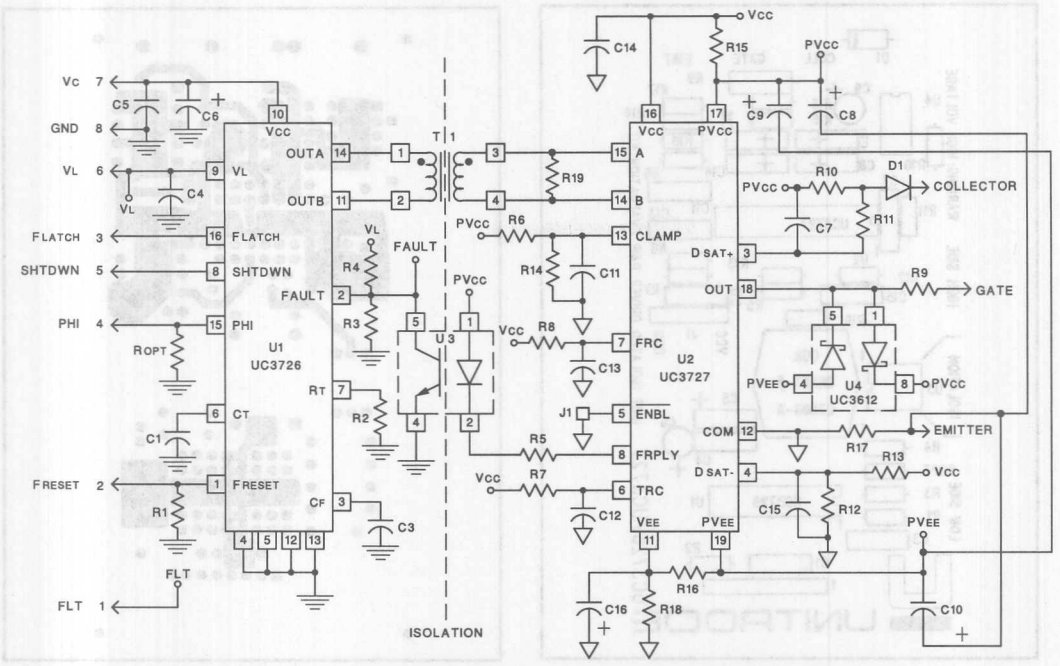


Figure 15. IGBT Driver Pair Evaluation Board Schematic

TABLE 1
UC3726/UC3727 IGBT ISOLATED DRIVER PAIR DEMO KIT
LIST OF MATERIALS

CAPACITORS

C1, C12	100pF, 35V
C3, C13	2200pF, 35V
C4, C11	0.1µF, 35V
C5, C8, C10	1µF, 35V
C14, C16	1µF, 35V
C6, C9	10µF, 35V

DIODES

D1	UF4007, BV= 1000V (General Instrument)

INTEGRATED CIRCUITS

U1*	UC3726Isolated Drive Transmitter
U2*	UC3727Isolated High Side IGBT Driver
U3	CNY17 Optocoupler, 10µs
U4*	UC3612 Schottky Diode Pair

R1, R8, R11, Ropt	2k, 1/4W
R2, R4, R6, R14	5.1k, 1/4W
R5	10k, 1/4W
R7, R8	91k, 1/4W
R9	5.6Ω, 1W
R10, R12	18k, 1/4W
R13	51k, 1/4W
R15, R16, R17	3.3Ω, 1/4W

MAGNETICS

T1*	Coilcraft Q3868-A

*Included with demo kit.

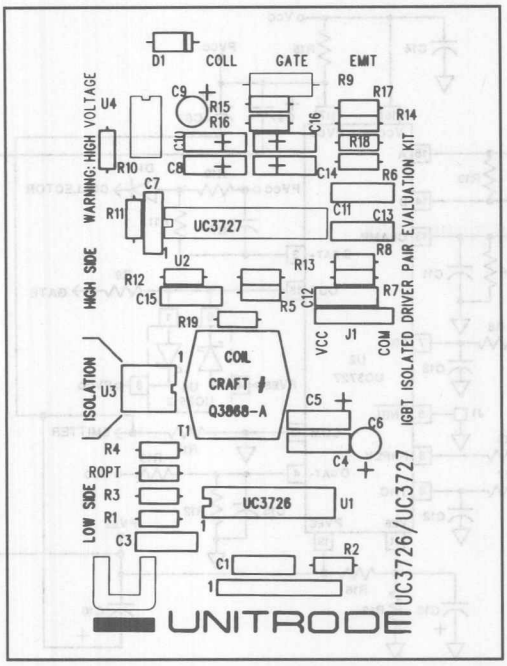


Figure 16. Silkscreen

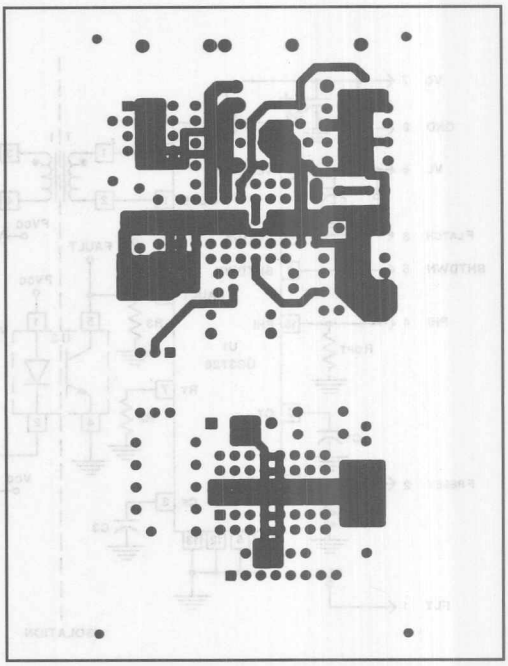


Figure 17. Component Side

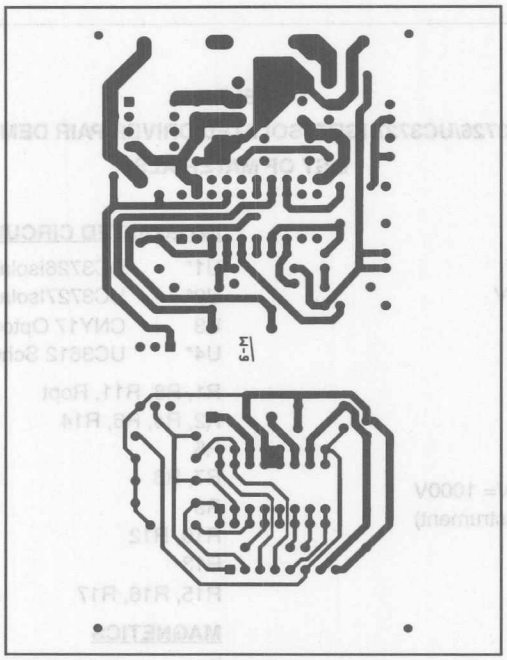


Figure 18. Solder Side

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UCC3806 BiCMOS CURRENT MODE CONTROL IC

By Jack Palczynski
Application Engineer
Power Supply Products

Abstract

Space and cost constraints have forced power supply designs into smaller spaces and demanded more efficient designs with higher switching frequencies. With the introduction of the UCC3806 BiCMOS current mode controller, a designer has the advantages of reduced current consumption, power loss and propagation delays within the IC. The UCC3806 is pin-for-pin compatible with the popular UC3846 and UC3856 controllers. With minimal part changes, this device may be suitable for retrofit into many existing designs where higher power consumption and propagation delays posed problems in the past. An ideal application for the UCC3806 is in battery operated equipment where low power consumption is critical to extended operation.

INTRODUCTION

As power supply requirements are demanding higher switching frequencies and lower power consumption, bipolar PWM IC's may limit design flexibility. The versatile UC3846 consumes relatively low power but is slow by today's standards. The UC3856 fulfills the high speed requirements but uses significantly more power to accomplish the task. Unitrode's BiCMOS process produces fast, low power BiCMOS control ICs with the high power capabilities of bipolar devices, a prime example being the UCC3806.

The UCC3806 features slew rate limiting of the current sense amplifier input voltage. This allows direct injection of the primary current sense signal without the need to filter the inductive leading edge spike. The propagation delay from current sense to output is reduced to 125ns and rise and fall times of the gate drive outputs are only 65ns. Gate drive current remains high at ±500mA from the dual totem pole MOSFET drivers. The low undervoltage lockout thresholds make this IC ideal for many battery and automotive applications. Most features will be familiar to the designer acquainted with the UC3846. The one volt pulse by pulse current limiting remains, along with programmable latched or non-latched shutdown modes triggered via the Shutdown pin.

This Application Note highlights retrofit applications of the UCC3806 and provides a step by step process to accomplish this. Several new applications will be introduced with a review of some popular applications. Unitrode Application Note U-93 describing the UC3846 should be reviewed for background and additional information.

UCC3806 BiCMOS Current Mode PWM Control IC Features

- 100µA startup current
- 1.4mA operating current
- Pin-for-pin compatible with UC3846 and UC3856
- Operating frequency to 1MHz
- ±500mA MOSFET output stage
- 65ns output rise and fall times
- 125ns current amp to output delay
- Current Sense Slew Rate Limiting
- Undervoltage Lockout

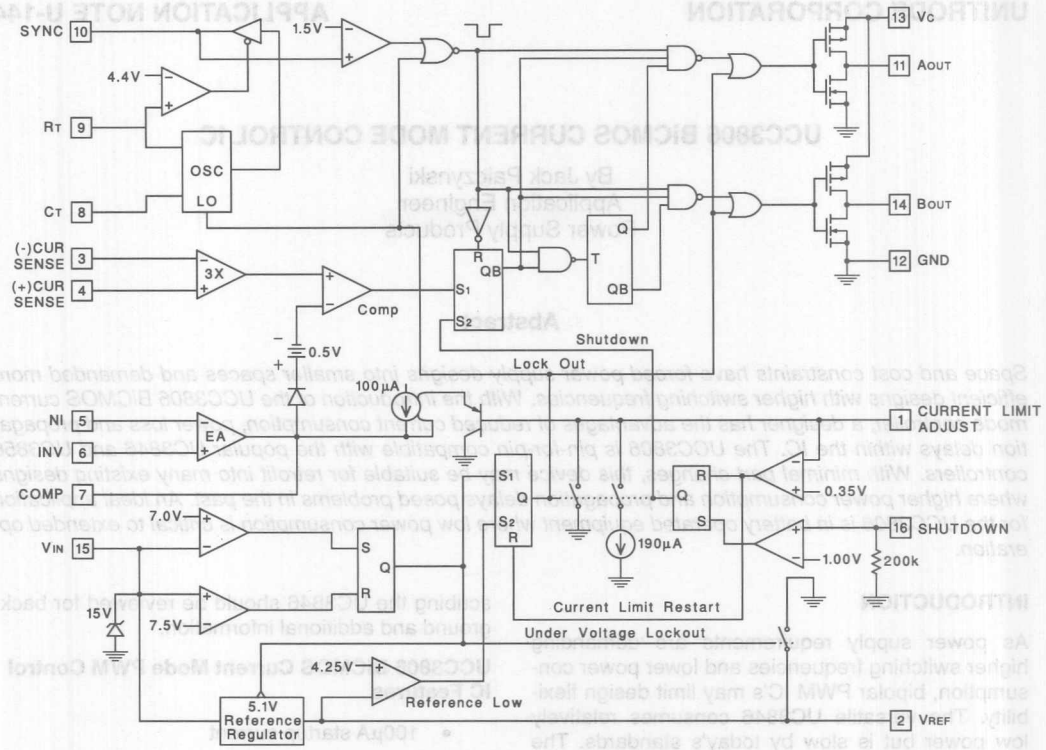
DEVICE DIFFERENCES

For designers familiar with the UC3846 or UC3856 devices, this section will provide a quick overview of necessary design changes to incorporate the UCC3806.

1) **UVLO**: Three parameters should be observed here. The start up voltage threshold is 8.0V with an operating hysteresis of 0.75V. The absolute maximum voltage for V_{IN} (pin 15, IC power) is 15V and for V_C (pin 13, gate drive voltage), 18V.

2) **DEAD TIME** (t_d) is determined by the timing capacitor (C_T).

$t_d = 961C_T$ (approximately)



UCC1806 Block Diagram

3) **SWITCHING FREQUENCY** (f_S) may be found by using the equation

$$f_S = \frac{1}{2R_TC_T + t_d}$$

4) **SHUTDOWN** threshold voltage on pin 16 has been raised to 1.0V.

5) **GATE DRIVES**: The maximum gate drive current is ±500mA.

6) **CURRENT LIMIT**: As in the UC3846 and UC3856, R1 and R2 (see Figure 5) program the threshold for primary current limit and determine whether the IC will latch off or retry. When a shutdown signal is generated, a 190µA current source to ground pulls down on pin 1. If the voltage on the current limit adjust pin (pin 1) remains above 350mV the IC will remain latched and power must be cycled to restart. If the voltage on the current limit adjust pin falls below 350mV, then the IC will attempt a re-start.

DESCRIPTION

SUPPLYING POWER

Power can be applied to the UCC3806 by a single source or by two separate sources, one for the IC supply and another for the FET drive outputs. In either case, adequate local capacitive bypassing is required. The IC supply voltage is internally limited by a 15 volt shunt regulator circuit. This is advantageous in off-line applications where the IC is powered-up by a resistor to the high voltage input. Shunted supply current in the IC must be limited to 10mA maximum. The IC's ground should be separated from any high current or noisy ground paths, but at the same electrical potential. This is best done by routing a local ground for the UCC3806 circuitry and then connecting this to a single point system ground.

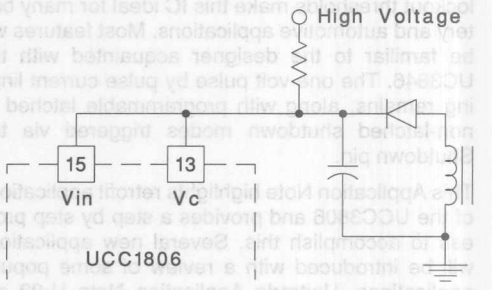


Figure 1. Supplying Power

UNDER VOLTAGE LOCKOUT (UVLO)

A minimum of 8V is needed to start the UCC3806, and once operational, the IC operates down to 7.25V. Below this level the UCC3806 will turn off and again require at least 8V to re-start. Care must be taken to be sure that the voltage source can supply adequate current to maintain operation or the IC will cross its turn-off undervoltage lockout threshold and shut down. The most obvious symptom where this problem occurs is when the entire power supply pulses on and off. Depending on the storage capacitor size and bias supply circuitry, the supply may eventually continue to run or may simply hiccup. A good design will include a large capacitor across the IC power inputs to store energy long enough to avoid UVLO. Note that the gate drive requirements of most power MOSFETs will usually use more current than the IC draws by itself, and must not be overlooked. Please refer to application note U-93 and U-137 for more details.

SELF-BIASING, ACTIVE LOW OUTPUTS DURING UNDER VOLTAGE LOCKOUT.

During any undervoltage lockout the UCC3806 outputs are actively held low to eliminate problems caused by a power MOSFET switch device inadvertently turning on. As with other Unitrode PWM IC's, gate drive outputs cannot pull high until the IC has been properly turned on. This self-biasing circuitry derives its power from the MOSFET gate voltage which is attempting to rise. Note that this protection feature is also activated when the supply voltage falls below the UVLO point, causing the IC to turn off.

REFERENCE VOLTAGE

The UCC3806 provides a 5.1V ± 1% reference output. Bypass capacitors with low impedance (ESL and ESR) and good high frequency response should be used. Generally, a ceramic monolithic or MLC capacitor with short leads to the IC ground pin is required even if the reference is not externally used. Note that the maximum current available from the reference pin is 10mA. Erratic operation can be caused by exceeding the maximum current or from connecting very noisy loads to the V_{REF} pin without adequate bypassing and filtering.

OSCILLATOR

The oscillator timing section of the UCC3806 is similar to it's predecessors yet uses different voltage thresholds throughout. Frequency is programmed by selecting the values of two timing components; C_T, the timing capacitor and R_T, the timing resistor. Current flowing from the internal 1.25V reference at the R_T pin divided by the value of R_T is mirrored to the timing capacitor pin (C_T). This causes a linear charging of C_T from 0V to 2.5V, the lower and upper oscillator thresholds. Note that the current mirror is limited to a maximum of 100µA so R_T must be greater than 12.5k.

Oscillator discharge is facilitated by switching on a 2.6mA current sink from C_T to ground. This causes a linear discharge of C_T to zero and then initiates the next switching cycle. Dead time occurs during the discharge time of the capacitor during which time both outputs are active low. Subjecting other IC pins to excessive noise or pulling some points below ground may reset the oscillator or cause periodic termination. f_s and t_d may be approximated by:

$$f_s = \frac{1}{2R_TC_T + t_d} \qquad t_d = 961\ C_T$$

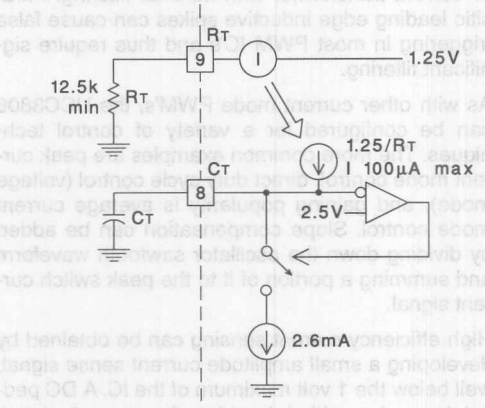


Figure 2. Frequency and Deadtime Programming

SYNCHRONIZATION

The SYNC pin allows external synchronization of the UCC3806 to an outside control signal with TTL compatible thresholds. The oscillator C_T pin must be grounded in order to use the SYNC input feature. The internal clock is reset and a deadtime generated by applying a voltage greater than 2V (high) to the SYNC pin. Returning this input to a voltage less than 0.8V toggles the output flip-flop and initiates a new switching cycle.

External synchronization may be sourced from the SYNC pin. The oscillator output goes to the SYNC pin and affects the outputs as described above. Another UCC3806 may be connected to the SYNC pin in order to match the frequency of the master device. Other circuits or devices may use the characteristics of the SYNC pin. A high output state is at least 2.4V with 5mA current sourced and low output state 0.4V maximum with a 1mA sink.

OUTPUT DRIVER SECTION

The two UCC3806 alternating outputs consist of totem-pole MOSFET pairs. Duty cycle may be varied from 0 to 98% where minimum dead time is determined by the timing capacitor value. Both outputs use MOS transistor switches with inherent anti parallel body diodes to clamp voltage swings to the supply rails. This may allow operation without the use of clamp Schottky diodes on each gate drive as recommended with all bipolar ICs. Drive currents of ±500mA peak with rise and fall times of 65ns are typical performance specifications.

CURRENT AMPLIFIER SECTION

Slew rate limiting on the current sense amplifier output is featured in the UCC3806 device. This allows direct connection to the current sense resistor or current transformer with minimal filtering. Parasitic leading edge inductive spikes can cause false triggering in most PWM IC's and thus require significant filtering.

As with other current mode PWM's, the UCC3806 can be configured for a variety of control techniques. The more common examples are peak current mode control, direct duty cycle control (voltage mode), and gaining popularity is average current mode control. Slope compensation can be added by dividing down the oscillator sawtooth waveform and summing a portion of it to the peak switch current signal.

High efficiency current sensing can be obtained by developing a small amplitude current sense signal, well below the 1 volt maximum of the IC. A DC pedestal can be added to raise the current signal, gaining noise immunity. One easy method of achieving this is to add resistors from output A and output B to the positive current sense input in a system where the negative current sense pin is grounded. Note that this pedestal will vary with changes in the IC collector supply voltage, Vc. Another method to add a DC level to the current sense input or the current limit input is to use a resistive divider from VREF.

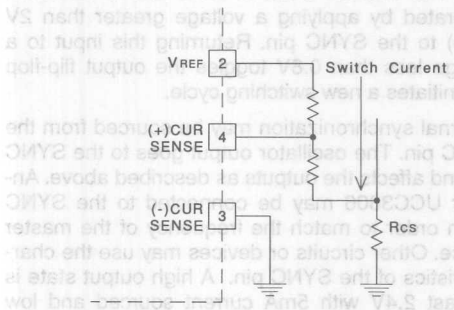


Figure 3A. Level Shifted Current Sense

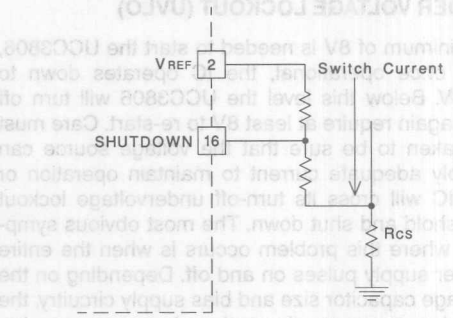


Figure 3B. Level Shifted Shutdown

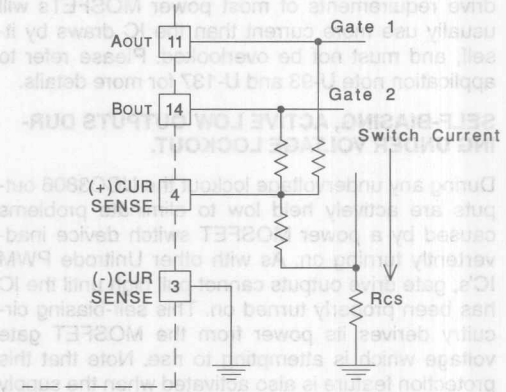


Figure 3C. Adding a Pedestal from Gate Drives

PROTECTION CIRCUITRY

By adjusting the pulse-by-pulse current limiting, a converter can be protected against short circuit conditions. The UCC3806 terminates the PWM output protecting the switching device and other power components when sensed switch current reaches the 1 volt current limit threshold. The ratio of this signal to actual switch current is determined by the current sense resistor value. Additionally, the

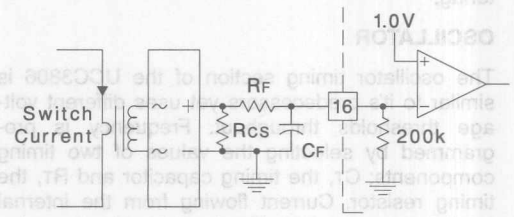


Figure 4. Overcurrent Shutdown

SHUTDOWN feature can be incorporated for further protection as shown in Figure 4.

The pulse-by-pulse current sense amplifier allows differential voltage sensing for ungrounded sense resistors. The current amplifier will terminate the ON-time when it's differential voltage reaches that set at the current limit input. Pulse by pulse current limiting is programmed by two resistors at the current limit. These resistors also set the shutdown mode to either latching or non-latching shutdown. To choose Values of R1 and R2:

$$V_{CS} = (V_{pin1} - 0.5)/3$$

$$I_{CL} = \left(\left(\frac{R_2 \bullet V_{REF}}{R_1 + R_2}\right) - 0.5\right) / 3R_S$$

During Shutdown:

$$V_{pin1} = \frac{V_{REF} - 190(10^{-6})R_1}{1 + \frac{R_1}{R_2}}$$

Latch Mode: $V_{pin1} > 350mV$
Non-Latch Mode: $V_{pin1} < 350mV$

A SHUTDOWN pin is provided for enhanced protection. Pin 16 can be programmed to force a shutdown when it's voltage exceeds 1V, and latching or non-latching modes are programmable options. When a shutdown is triggered, a 190µA current sink is connected to the current limit pin. If the voltage on pin 1 remains above 350mV, then the IC remains latched and outputs are held actively low. If the voltage is allowed to fall below 350mV, then the IC will reset and initiate a re-start. Of course, a wider margin is recommended to guarantee that resistor tolerances and external noise do not affect

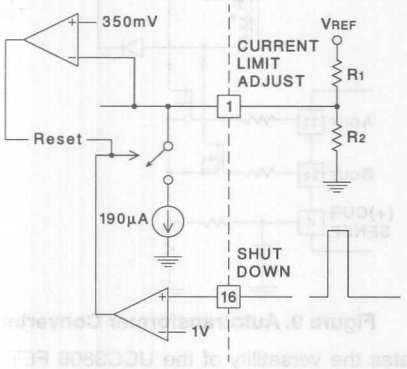


Figure 5. Shutdown Mode Programming

this mode selection. Again, a bypass capacitor from pin 1 to ground can also help eliminate problems from external noise.

SOFT START

Several methods of soft starting of a converter are possible with the UCC3806, and two common examples are shown. In the first example, an R/C network isolated by a PNP transistor sinks current from the output of the error amplifier. In the second, an R/C network alone is used on the error amplifier non-inverting (E/A+) input. This ramps up the non-inverting input of the op-amp to reduce the slew of output voltages and delivers true closed loop controlled start-up. In both cases, the diode provides

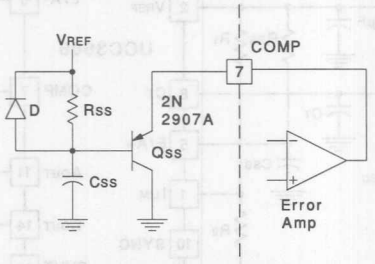


Figure 6. Buffered Soft Start

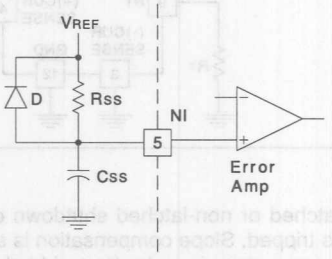


Figure 7. Closed Loop Soft Start

automatic capacitor discharge when the VREF turns off, typical of a power-up or shutdown condition.

APPLICATIONS

Push-Pull Converter

One of the most common uses for the UCC3806 is in an isolated Push-Pull configuration utilizing current mode control. A summation of the components and their functions follows.

Resistors Rg1 and Rg2 limit the output current to 0.5A. Rv limits current to the IC to 10mA. RT and CT set frequency and dead time. Note that oscillator waveforms may become non-linear at higher frequencies and so RT and CT should be selected to obtain the desired frequency. Rss and Css are used to ramp up the reference on the error amp so the output voltage comes up in an orderly manner. R1 and R2 program the pulse by pulse current limit for primary peak current. R3 and R4 set a shutdown triggered by excessive primary current. These levels should be set to assure that a shutdown will be triggered before the pulse by pulse current limit threshold is reached. R1 and R2 deter-

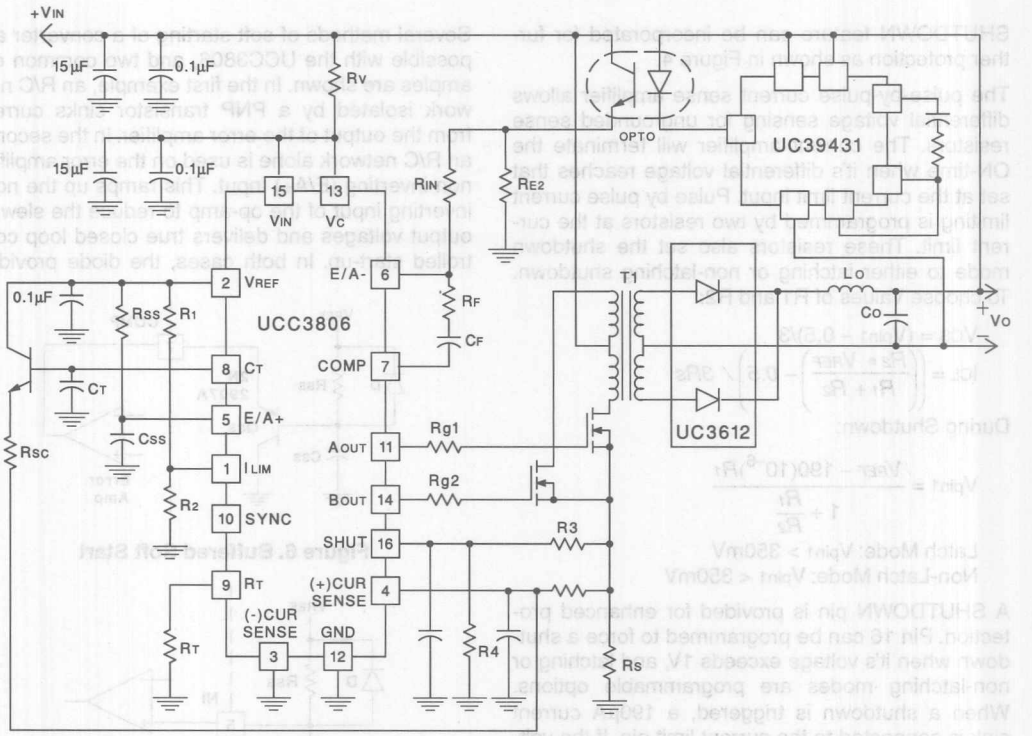


Figure 8

mine latched or non-latched shutdown once shutdown is tripped. Slope compensation is shown and may be necessary in order to avoid sub-harmonic oscillations when duty cycles greater than 50% occur. Note that bypass capacitors are used in several locations to filter noise around the UCC3806 circuitry. The value of these capacitors will vary depending on input and output variables, layout, and power level.

Non-Isolated Autotransformer Converter

When isolation is not needed but a voltage step up desired, a simple push-pull configuration may be used with a non-isolated transformer to step up the input to output voltage. Figure 9 shows how a UCC3806 may be used to achieve a very efficient converter ideal for battery applications. Because of the voltage step up, output regulation is maintained even when input voltage falls below output voltage. Notice that the UCC3806 is otherwise used in a very conventional application here. Circuit set up follows the same simple rules as a conventional transformer isolated converter. Efficiencies over 90% can be realized for low power converters similar to this example.

Self Contained Low Power Converter

A non-isolated converter of Figure 10 demonstrates the versatility of the UCC3806 FET output stage. In this application, the lower drive FET of each output totem pole is used as a synchronous rectifier along with the parasitic body diode, and no external diodes or switches are used. Interleaved inductors are incorporated and operated in the continuous current mode. Inductor current must not become discontinuous, or current will reverse direction and circulate into the IC. When this occurs,

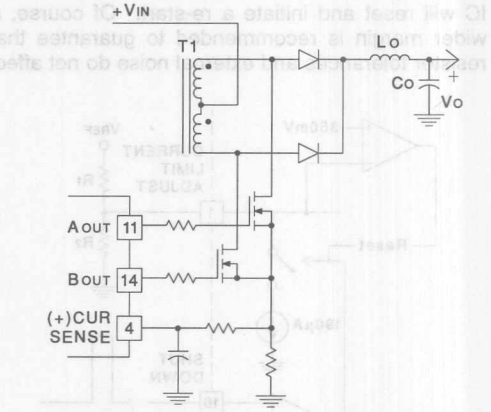


Figure 9. Autotransformer Converter

the other inductor circulates current into the lower output FET creating excessive heating and forcing the IC to overcome backwards current when turning on again.

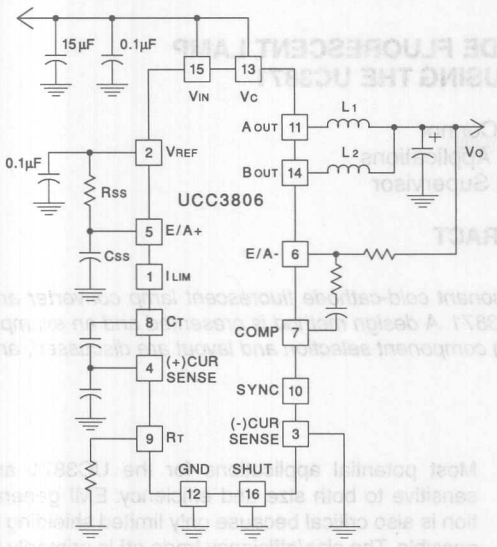


Figure 10

Summary

BiCMOS technology in the UCC3806 has added a new dimension to PWM IC's available today. This IC enables the designer to optimize circuits by allowing higher switch frequencies and decreasing IC delays. This breakthrough in technology brings a dramatic reduction in IC operating current and the ability to use larger resistor values in support circuitry which further cuts power loss. Less parts can be used by eliminating Schottky diodes which protect Bipolar IC's as well as the possible elimination of current sense filtering. The UCC3806 remains pin for pin compatible with the familiar UC3846 and possesses all of the desirable functions found in that popular PWM control IC. These features include a 500mA output drive capability, current mode control, fully differential current sense amplifier, pulse by pulse current limiting under voltage lock out and built in shutdown circuitry.

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DIMMABLE COLD-CATHODE FLUORESCENT LAMP BALLAST DESIGN USING THE UC3871

by J. O'Connor
New Product Applications
Engineering Supervisor

ABSTRACT

This application note describes how to design a resonant cold-cathode fluorescent lamp converter and liquid crystal display (LCD) bias supply using the UC3871. A design method is presented and an example circuit is designed. Practical considerations regarding component selection and layout are discussed, and performance results are shown.

DESIGN CONSIDERATIONS

The UC3871 provides a complete power supply control solution for backlit LCDs that are typically used in laptop and notebook computers, and portable instrumentation. These applications require an adjustable high voltage AC current source to drive a cold cathode fluorescent lamp (CCFL) and an adjustable low voltage DC supply to bias the LCD. The UC3871 provides all control functions for these two supplies and also incorporates protection and synchronization circuitry. A low power shut-down input places the entire circuit into a very low current standby mode to reduce battery drain in portable systems and eliminate the need for a low-drop series switch.

The power circuitry illustrated in figure 1 consists of three sections:

1. A pulse width modulated (PWM) buck regulator to provide a variable, regulated voltage
2. A zero voltage switched (ZVS) resonant push-pull converter to transform the variable, regulated voltage to a high voltage AC output
3. A PWM flyback regulator to generate a variable DC voltage to bias an LCD

The buck and flyback regulators are synchronized to the ZVS push-pull converter, which free runs at its resonant frequency. Unitrode application note U-141 also covers the UC3871, along with further description and analysis of this topology and the application's requirements.

Most potential applications for the UC3871 are sensitive to both size and efficiency. EMI generation is also critical because only limited shielding is possible. The size/efficiency trade off is primarily in the magnetics, with the high voltage transformer by far the single most critical component. The design therefore must begin with an assessment of the performance and size goals, and their impact on the transformer design. In general, higher frequencies are preferred to minimize the size of the buck and flyback regulator magnetics, but excessively high frequencies will cause significant efficiency degradation.

DESIGN PROCEDURE

The ZVS resonant push-pull converter is designed first, and then the buck regulator and LCD bias flyback converter since both of these circuits are dependent on the push-pull converter. Resonant push-pull converter design requires an iterative approach because almost all of the variables are interdependent. A few initial variables come from the lamp and application specifications. These are normally the lamp starting voltage, operating voltage, and operating current, and the input supply voltage range. The desired resonant frequency is then chosen in order to calculate the remaining variables.

To help illustrate the design procedure, the following design example is presented which is typical of what a small computer would use for LCD power and back lighting. The application requirements are as follows:

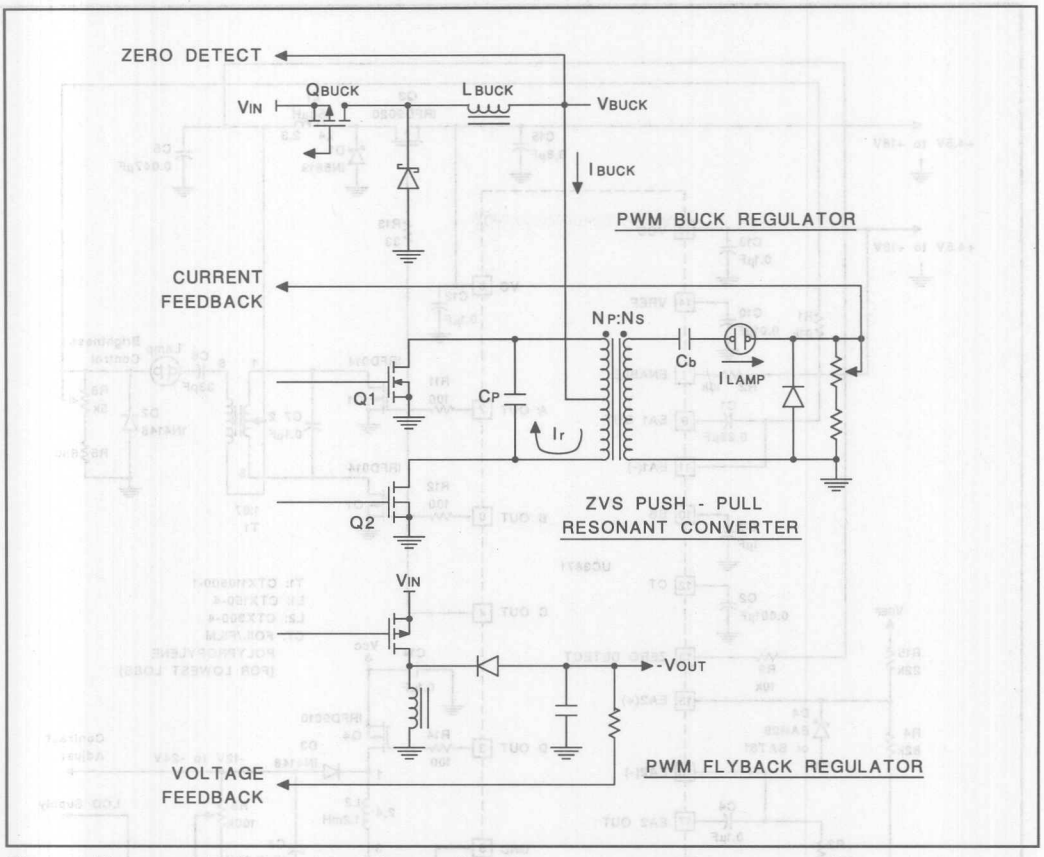


Figure 1. The power circuitry consists of three sections.

Input Voltage Range (Vin) 4.5V to 18V

LCD Bias Supply:

Output Voltage (Vlcd) -12V to -24V

Output Current (Ilcd) 25mA

Fluorescent Lamp Ballast:

Starting Voltage (Vlamp) 900V (peak)

Operating Voltage (Vlamp) 350V (peak)

Operating Current (Ilamp) 0.5mA to 5mA (avg.)

The desired minimum resonant frequency is 50kHz so that the buck and flyback operating frequency will be at least 100kHz. At this frequency, switching losses will be low. Increasing the frequency will allow smaller magnetics, but efficiency will most likely suffer. The complete schematic of the design example circuit is shown in figure 2.

ZVS RESONANT PUSH-PULL CONVERTER

The minimum input voltage and maximum lamp starting voltage determine the minimum transformer turns ratio. After calculating the initial transformer parameters, the turns ratio should be checked to make sure that full load current can be developed at the minimum input voltage. The minimum turns ratio is then:

$$\frac{N_S}{N_P} \geq \frac{V_{START(PEAK)}}{\pi V_{INmin}} \quad (1)$$

$$\geq \frac{900}{4.5\pi}$$

$$\geq 64$$

Note that this ratio relates the entire primary winding to the secondary. Sometimes the turns ratio is specified to relate one-half of the primary winding (end to center-tap) to the secondary.

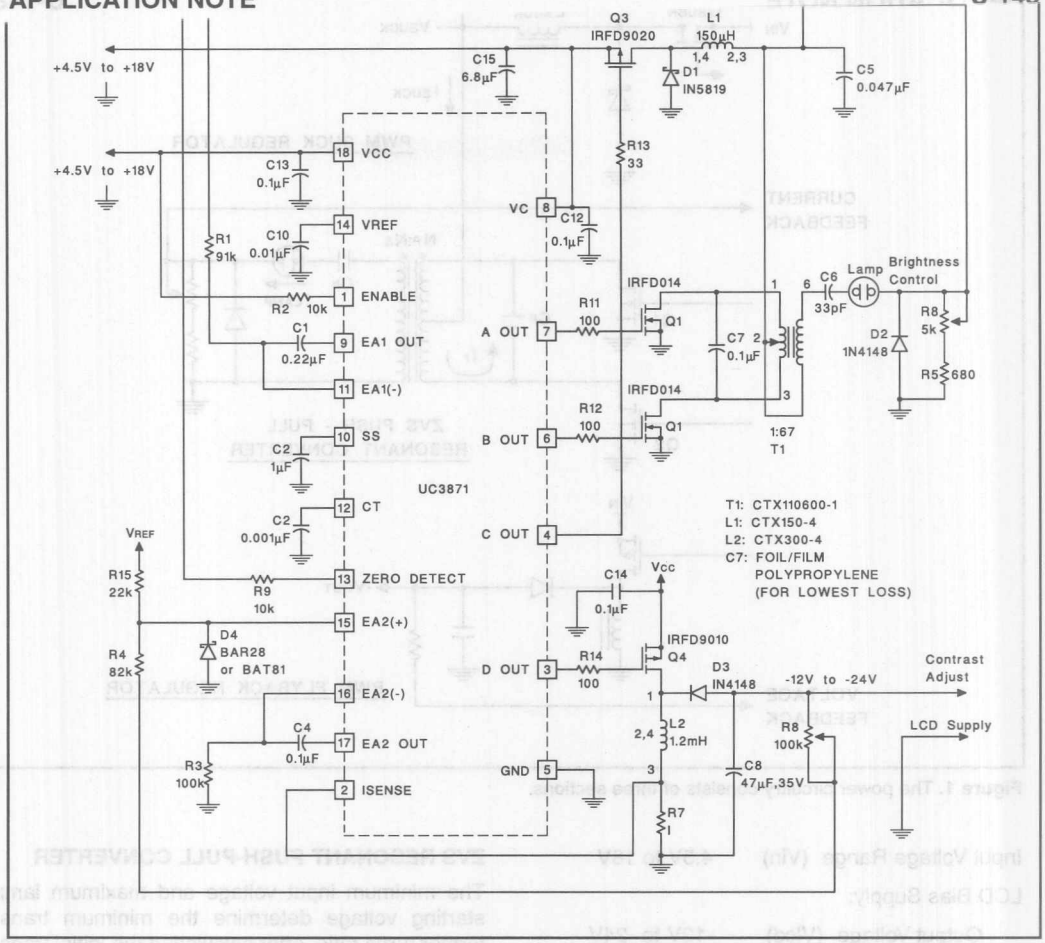


Figure 2. Complete circuit schematic.

A nominal ballast capacitor (Cb) value is calculated by setting the voltage across the ballast capacitor approximately twice the lamp sustaining voltage. This is an arbitrary relationship which serves as a starting point. Dropping a large voltage across the ballast capacitor voltage gives the converter a high output impedance and makes the converter relatively insensitive to the lamp's highly nonlinear impedance. Unfortunately, it also increases the circuit's losses. Tradeoffs between circuit size, distortion, and efficiency are governed by this component, so further iterations will usually result in a different final value. Setting the ballast capacitor's voltage equal to twice the lamp voltage at maximum current and minimum resonant frequency gives the value for Cb:

$$V_{CB} = \frac{I_{LAMP}}{2\pi F C_B} = 2V_{LAMP} \quad (2)$$

$$C_B = \frac{I_{LAMP}}{4\pi F V_{LAMP}}$$

$$= \frac{0.005}{4\pi(50 \bullet 10^3)(222)}$$

$$= 36pF$$

High secondary voltage and turns ratio result in poor coupling between the transformer's primary and secondary windings resulting in high leakage inductance. Capacitors across both the primary and secondary windings form two loosely coupled

parallel resonant circuits. To minimize output distortion, the independent primary and secondary resonant frequencies should be approximately the same. This requirement establishes a desired relationship between the primary (Cp) and secondary (Cs) capacitance:

$$C_P = \left(\frac{N_S}{N_P}\right)^2 C_S \quad (3)$$

$$= (64)^2 (36 \cdot 10^{-12})$$

$$= 0.15\mu F$$

The majority of the secondary capacitance comes from the series connected lamp and ballast capacitor. The lamp appears as an AC short circuit for much of the cycle, making the equivalent capacitance a little less than the ballast capacitor value. Distributed winding capacitance, stray PC board and lamp wiring capacitance contribute to the small secondary capacitance. Setting the load capacitance equal to the ballast capacitor value is therefore a reasonable initial estimate. Distributed transformer winding and stray capacitance are ignored for initial calculations. Parasitic capacitances have negligible effect on the primary capacitance since its value is several orders of magnitude larger than on the secondary.

With the independent primary and secondary resonant tank frequencies approximately equal, the secondary circuitry is reflected to the primary, allowing treatment as a single resonant tank. With both the primary and secondary resonant tanks set to the same frequency, the equivalent resonant capacitor (Cr) is simply twice Cp. The primary inductance is then calculated to give the desired resonant frequency:

$$L_P = \frac{1}{(2\pi F)^2 C_R} \quad (4)$$

$$= \frac{1}{(2\pi 50 \cdot 10^3)^2 (0.3 \cdot 10^{-6})}$$

$$= 34\mu H$$

Primary and secondary RMS currents are then calculated to determine maximum acceptable transformer winding resistances. The secondary current is mostly lamp current, although the currents to drive distributed winding and stray wiring capacitances are also factors. For now we will ignore these parasitic effects, since in most cases the additional loss they cause will not be enough to significantly alter the transformer design.

Each half of the primary winding sees an asymmetrical sinusoidal current which is the sum of the primary resonant current and the input current source from the buck regulator during one-half of the cycle. The primary voltage must be calculated first in order to determine the primary resonant current:

$$V_P = \frac{N_S}{N_P} V_S \quad (5)$$

$$= \frac{N_P}{N_S} \sqrt{V_{CB}^2 + V_{LAMP}^2}$$

$$= \frac{1}{64} \sqrt{(700)^2 + (350)^2}$$

$$= 12.2V(peak)$$

The primary resonant current is then:

$$I_R = \frac{V_P}{Z_P} \quad (6)$$

$$= \frac{V_P}{\sqrt{\frac{L_P}{C_P}}}$$

$$= \frac{12.2}{\sqrt{\frac{34}{0.15}}}$$

$$= 0.810A(peak)$$

The buck regulator current is calculated by equating input and output power while assuming 90% efficiency for the push-pull stage:

$$P_{IN} = \frac{P_{OUT}}{0.9} \quad (7)$$

$$= \frac{V_{LAMP(RMS)}\ I_{LAMP(RMS)}}{0.9}$$

$$= \frac{(248)(5.55 \cdot 10^{-3})}{0.9}$$

$$= 1.53W$$

The buck regulator sources current to the push-pull stage through the primary winding's centertap. The average voltage at this point is one-half of the total primary voltage. The average buck regulator output voltage is therefore one-half the average primary voltage calculated in (5):

$$V_{BUCK} = \frac{V_P}{\pi} \quad (8)$$

$$= \frac{12.2}{\pi}$$

$$= 3.88V\ (avg)$$

The buck output current is then:

$$I_{BUCK} = \frac{P_{IN}}{V_{BUCK}} \quad (11)$$

$$= \frac{1.53}{3.88}$$

$$= 0.394A$$

During the first half of the resonant cycle, one-half of the primary winding conducts the resonant current, while the other half of the primary winding conducts the sum of the resonant current and the buck regulator current. During the second half of the cycle the conditions reverse such that both halves of the primary conduct the same asymmetrical current 180 degrees out of phase from each other. A close approximation of the primary current is made by simply adding the average value of the buck output current to the peak resonant current for one-half of the cycle, and calculating the rms value as an asymmetrical sinewave:

$$I_{PRI} = \sqrt{\left(\frac{I_R}{2}\right)^2 + \left(\frac{I_R + I_{BUCK}}{2}\right)^2} \quad (12)$$

$$= \sqrt{\left(\frac{0.810}{2}\right)^2 + \left(\frac{0.810 + 0.394}{2}\right)^2}$$

$$= 0.725A(rms)$$

PUSH-PULL TRANSFORMER

All parameters necessary to design the transformer are now known and an initial design can be started. Optimal transformer design for this application is beyond the scope of this paper. The additional complexity of the resonant circuitry, along with the high output voltage and small required size present a significant mechanical design challenge. Any variable can be iterated since the ballast capacitor value was arbitrarily selected. Optimal design normally requires many design iterations.

Often the preceding analysis is done by a transformer manufacturer that specializes in resonant ballast design. A standard transformer from Coiltronics, Inc. [5], which is intended specifically for portable computer LCD back lighting was selected for the design example. Its specifications closely match the application's requirements. Selecting a standard transformer eliminated numerous iterations and reduced the design cycle considerably. The Coiltronics transformer has the following specifications:

CTX110600-1 specifications:

Primary Inductance	44mH
Ns/Np	67
Primary Resistance	0.160 ohms
Secondary Resistance	176 ohms

The CTX110600-1 employs a unique method of secondary winding termination. The secondary return lead terminates at the primary centertap, making it unnecessary to insulate it from the rest of the winding. Distributing the secondary across several sections of a multi-section bobbin also eliminates insulation between winding layers. The secondary current has negligible effect on the primary since its value is roughly two orders of magnitude smaller than the primary current. This connection scheme does add a small amount of asymmetry to the secondary voltage waveform, but again, this effect is negligible.

To design with an existing transformer, the equations are rearranged to calculate the nominal capacitor values, or the capacitor values are recommended by the transformer manufacturer. Some experimentation is usually necessary, regardless of how the initial paper design is done, to achieve the optimum circuit for a particular application.

BUCK REGULATOR

The ZVS push-pull converter's resonant frequency establishes the buck and flyback regulators' conversion frequency. Each time the push-pull converter's primary voltage crosses through zero, the UC3871's oscillator is reset. The design frequency for both the buck and flyback circuits is therefore twice the minimum push-pull resonant frequency.

The buck regulator provides a regulated, variable output voltage for the push-pull converter to reject input voltage variations and allow lamp brightness adjustment. Due to the absence of a large output capacitor, the buck regulator presents a high impedance to the push-pull converter at its resonant frequency. Neglecting the sawtooth ripple, the output inductor's current is nearly constant.

Inductor ripple current is greatest when the duty cycle and frequency are minimum. This occurs at maximum input voltage and lamp current, where the buck OFF time is maximum:

$$T_{OFF(MAX)} = \frac{1-D}{F_{MIN}} \quad (13)$$

$$= \frac{1-D}{F_{MIN}} \left(1 - \frac{V_{BUCK}}{V_{IN(MAX)}}\right)$$

$$= \frac{1}{10^5} \left(1 - \frac{3.88}{18}\right)$$

$$= 7.84\mu s$$

To minimize inductor value, ripple current is normally 30% to 50% of the average value.

$$L > \frac{T_{OFF}\ V_{BUCK}}{I_{RIPPLE}} \quad (14)$$

$$> \frac{(7.84 \bullet 10^{-6})(3.88)}{(0.5)(0.394}$$

$$> 154\mu H$$

A Coiltronics part number CTX150-4 was selected for the buck inductor that has the following specifications:

Inductance	150μH
Resistance	0.175 ohms
Rated Current	0.72ADC

CONFIGURING THE CONTROL CIRCUITRY OSCILLATOR

The UC3871 contains a synchronizable oscillator internally configured to operate over a 3:1 frequency range. A 200μA current source is used to charge an external capacitor (Ct) from 0.1V to 3.0V. At the 3.0V threshold, a 4.0mA current sink discharges the capacitor back down to 0.1V. The zero detect input senses the transformer primary centertap voltage and indicates when the resonant tank voltage is crossing through zero. Under normal circumstances, the zero detect input will trigger the discharge circuit before the capacitor voltage reaches the 3.0V threshold, synchronizing the oscillator to twice the resonant tank frequency.

To improve noise immunity and prevent false triggering from comparator chatter, another comparator is used to lock out the zero detect input until Ct's voltage reaches 1.0V. The 3V maximum, 1V minimum peak oscillator amplitudes establish a 3:1 synchronization range. Ideally, the synchronization range should be centered around the resonant frequency range. A good starting point is to set the oscillator amplitude (Vct) to 2.2V at the minimum synchronization frequency, which is twice the minimum resonant frequency. The timing capacitor value is then:

$$C_T = \frac{10^{-4}}{F} \quad (15)$$

$$= \frac{10^{-4}}{10^5}$$

$$= 1.0nF$$

The resonant tank frequency must always be within the oscillator synchronization range to prevent severe output distortion and non-ZVS operation.

A 10k resistor in series with the zero detect input is recommended to protect against high voltages that occur during turn-off. The zero detect input is specified to withstand a maximum input current when driven from a high impedance source. A capacitor connected to the transformer center-tap limits the maximum voltage at turn-off by absorbing all of the inductive energy in the buck inductor when both of the push-pull MOSFETs turn off. This capacitor also attenuates noise and ringing which would otherwise be present at this node.

SOFT-START AND OPEN LAMP DETECT

The primary function of soft-start is to allow time for the lamp to strike and conduct the programmed level of current before enabling the open lamp detection circuitry. A 20μA current source charges an external capacitor (Css) when either the supply voltage exceeds the nominal 4.2V under-voltage lockout, or the IC is enabled. Once the external capacitor voltage exceeds 3.4V, the open lamp detect circuit is enabled. The soft-start time is normally determined empirically, since many factors such as minimum supply voltage and temperature influence the time it takes the lamp to strike. A 150ms soft-start was required to insure that the lamp started in the application example circuit. Once the soft-start time is determined, the capacitor value is calculated by:

$$C_{SS} = 5.9 \bullet 10^{-6}\ T_{SS} \quad (16)$$

$$= (5.9 \bullet 10^{-6})(0.15)$$

$$= 0.88\mu F\ (use = 1\mu F)$$

An open lamp is detected by sensing that the current feedback loop has opened. During normal operation the current loop is closed, and the error amplifier inverting input is at 1.5V. If the lamp circuit either opens or shorts to ground, insufficient feedback voltage develops, and the inverting input voltage drops to a level determined by input offset current and radiated signal pickup. Input bias current limits the maximum feedback resistor value to 100k, with lower values providing greater margin at

plex problem, and is addressed later in the PC board layout considerations section.

LAMP CURRENT CONTROL LOOP

The UC3871 controls lamp intensity by closing an average current feedback loop around the buck regulator and push-pull resonant converter. Optimal compensation of this system is extremely difficult because of the complex output stage and load characteristics. High frequency response is

the buck inductor and primary resonant and load capacitances reflected to the transformer center-tap. Typically, this double pole has a Q between 1 and 5, and occurs less than a decade below the resonant tank frequency unless an excessively large value is used for the buck inductor. Furthermore, the current feedback signal must be filtered sufficiently for correct PWM operation, requiring significant signal attenuation at the resonant tank frequency. These factors make it nearly impossible to cross the loop over above the output stage's double pole.

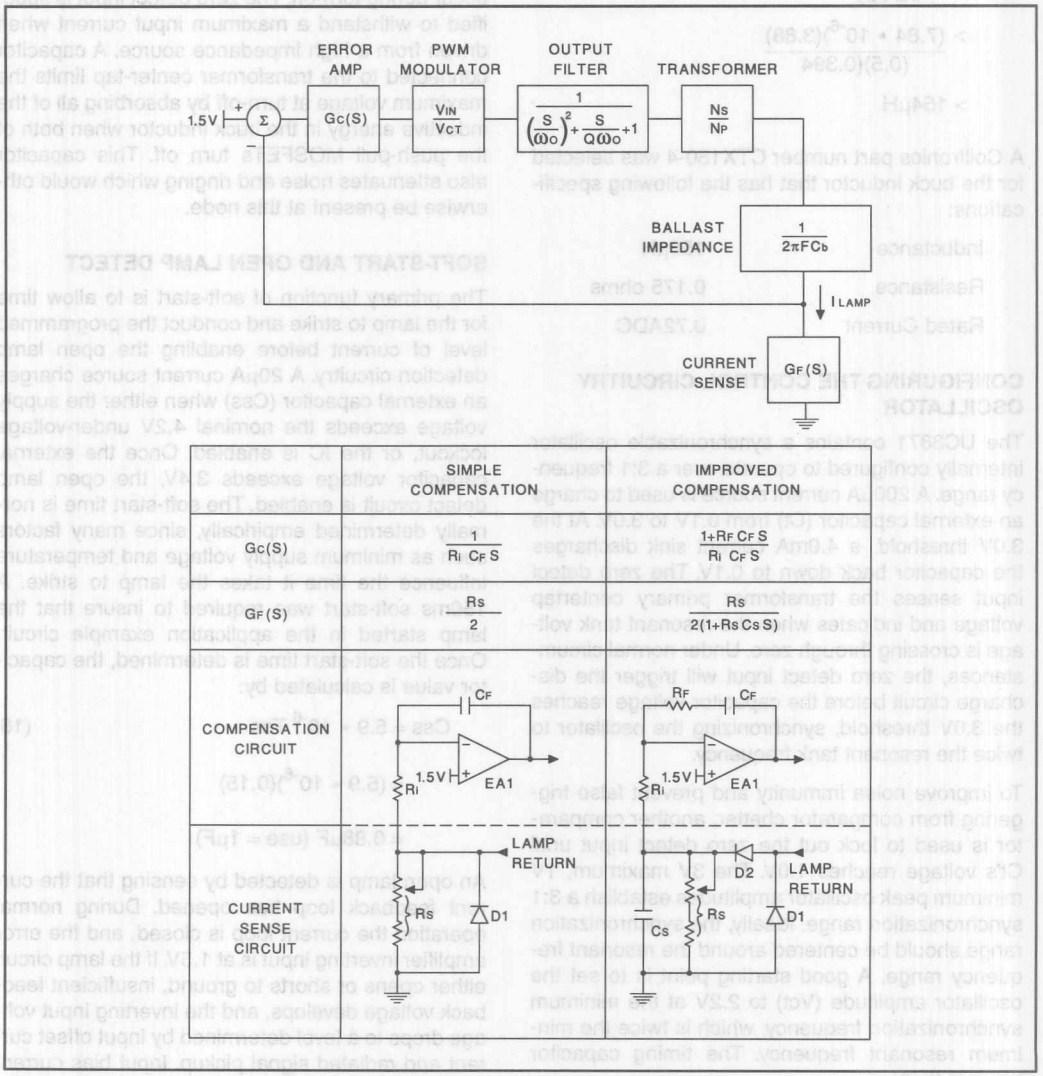


Figure 3. Control loop block diagram.

Below the double pole the power stage gain is flat. The simplest way to compensate the loop is to introduce a low frequency dominant pole that sets the unity gain crossover frequency well before the output filter double pole. This pole also sufficiently filters the half-wave rectified current feedback signal for proper PWM operation. The design example circuit shown in figure 2 employs this compensation technique, which requires a minimal number of components. Figure 3 shows the circuit's control loop block diagram. With the unity gain frequency set well below the resonant double pole, higher frequency effects caused by capacitor ESR and transformer leakage inductance can be ignored.

Three of the blocks exhibit gain variation with input or load changes. Most notable is the current sensing resistor, which in a typical application will cause a 25dB to 30dB gain change over the lamp current adjustment range. The ballast capacitor (Cb) is treated as a fixed impedance determined by the converter's resonant frequency, but since the resonant frequency varies about 20% in an actual application, the ballast impedance varies inversely by the same amount. The modulator gain is directly proportional to frequency since the PWM ramp amplitude (Vct) varies inversely with frequency, and to a first order, cancels the ballast impedance variation. The more dominant modulator gain variation however, is from the input supply voltage (Vin), which may vary more than 3:1.

The output filter resonant frequency is determined by the buck inductor value and the equivalent value of the primary resonant, output ballast, and output stray capacitances reflected to the buck regulator output:

$$\omega_O = \sqrt{L_{BUCK}\, C_{EQ}} \qquad (17)$$

$$C_{EQ} \approx 4C_P + \left(\frac{N_S}{N_P}\right)^2 C_B$$

$$\approx 8C_P$$

Output filter Q is the ratio of the resonant tank impedance to the effective series damping resistance:

$$Q = \frac{\omega_O L}{R_{SERIES}} \qquad (18)$$

The effective series resistance is the sum of all power circuit resistances reflected to the buck regulator output, plus the reflected load resistance transformed to its effective series value (Rseries). With every effort made to minimize series resistance for maximum efficiency, the reflected load term dominates.

$$R_{SERIES} \approx \frac{V_{BUCK}^2}{1.1\, P_{OUT}} \text{ (ohms)} \qquad (19)$$

Output filter Q is greatest at minimum lamp current. Gain peaking at the filter resonant frequency is then:

$$G_{PEAK} = 20 \log Q_{MAX} \text{ (dB)} \qquad (20)$$

The maximum unity gain crossover frequency is typically set nearly a decade below the output filter resonant frequency to insure adequate gain margin. Loop gain (and crossover frequency) is greatest at maximum input voltage and minimum current. At minimum input voltage and maximum lamp current, the unity gain crossover frequency may decrease two decades or more. Fortunately, wide bandwidth and good transient response are not required in most applications.

The example circuit's output filter has a maximum Q of 3, and a resonant frequency of 13kHz. The maximum unity gain crossover frequency is 1.5kHz, giving a worst case gain margin of about 9dB.

IMPROVED LOOP COMPENSATION CIRCUIT

Some applications require quick transient response to prevent lamp flicker from input voltage disturbances. Systems which have poor input supply regulation, particularly those with transient loads or a pulsed current battery charger are examples of such applications. With the typical UC3871 circuit, lamp current is adjusted by varying the closed loop gain. This causes the unity gain crossover frequency to decrease one decade for each 20dB increase in lamp current.

The control loop block diagram in figure 3 shows an improved current sense and loop compensation scheme that makes the unity gain crossover frequency insensitive to lamp current adjustment. A capacitor (Cs) connected in parallel with the current sense resistor forms a pole that varies directly with the current sense gain. This configuration provides variable low frequency gain for lamp current adjustment with fixed high frequency gain for constant loop crossover frequency.

This pole can theoretically provide acceptable loop compensation with a fixed error amplifier gain, but the required value for Cs would be much to large for a practical circuit. Adding a pole-zero pair to the error amplifier allows for an acceptable Cs value and provides high DC gain by maintaining a pole at the origin. The current sense pole (1/(RsCs)) and

the error amplifier zero (1/(RfCf)) are placed at the control loop's unity gain crossover frequency with Rs set to its minimum value.

LCD BIAS SUPPLY FLYBACK REGULATOR

The design procedure for the flyback converter is not given here since it differs little from a conventional power supply application. The only unique condition is that the conversion frequency varies with the push-pull converter's frequency. As with the buck converter, the initial design frequency is twice the minimum resonant frequency (the design example's buck and flyback regulator's minimum frequency is 100kHz). At the lowest lamp brightness, the frequency will typically increase 15% to 25%, minimally influencing the flyback converter's operation.

For the design example, the flyback converter is operated in the continuous inductor current mode. For most power supply applications, this mode of operation is avoided because of the poor closed loop bandwidth dictated by the right-half plane zero in the transfer function. Continuous mode operation does result in lower power stage loss however, and since for this application power loss is usually more critical than dynamic response, it is normally the preferred mode of operation.

The minimum component compensation circuit shown in the design example schematic employs a dominant pole to cross over the loop before the output stage's resonant double pole. Output voltage overshoot at power-up can be significant with this configuration if the error amplifier's integration capacitor is allowed to fully charge as the output voltage slews to its nominal value. This large signal problem is exacerbated by the ground referenced error amplifier configuration, which only allows a small discharge current to be developed.

For the design example, a 0.1μF integration capacitor is used although a value nearly ten times smaller will provide maximum loop bandwidth. The 0.1μF capacitor charges slowly during power-up, and eliminates overshoot by soft-starting the supply. A shottky diode (BAT81) is used to clamp the non-inverting error amplifier input to prevent it from phase inverting and latching up the control loop. This diode should have a forward drop less than 0.5V at room temperature.

IMPROVED FLYBACK COMPENSATION

As with the lamp driver circuit, there are applications that require better transient response than is achievable with dominant pole compensation. A simple alternative technique, shown in figure 4, is to cancel one of the output stage's resonant poles by a zero in the compensation circuitry, and cross the loop over at about 1/4 the minimum right-half plane zero frequency. This technique does result in lower DC gain than the dominant pole circuit used in the design example, but offers much better large signal behavior and a decade or more increase in loop bandwidth. Another pole-zero pair can be added to improve DC load regulation and input line rejection, although this additional complexity appears unnecessary.

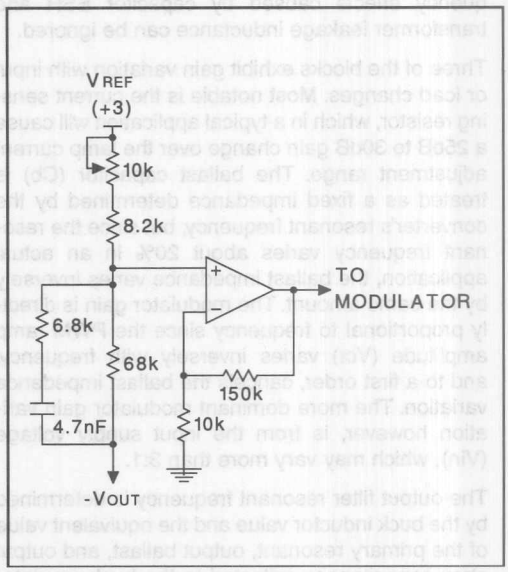


Figure 4. Improved flyback regulator compensation.

Discontinuous inductor current operation is also an option to significantly improve transient response if a small decrease in efficiency is tolerable. Discontinuous mode compensation is illustrated in the following positive output, coupled inductor flyback circuit.

POSITIVE OUTPUT VOLTAGE FLYBACK REGULATOR

A positive output LCD bias supply circuit is more complicated than the negative output, because the output voltage can be greater or less than the input voltage. This eliminates both buck and boost circuits, and makes the coupled inductor flyback converter a good choice for this application. Discontinuous inductor current operation is employed in the circuit shown in figure 5, allowing simple compensation and excellent transient response.

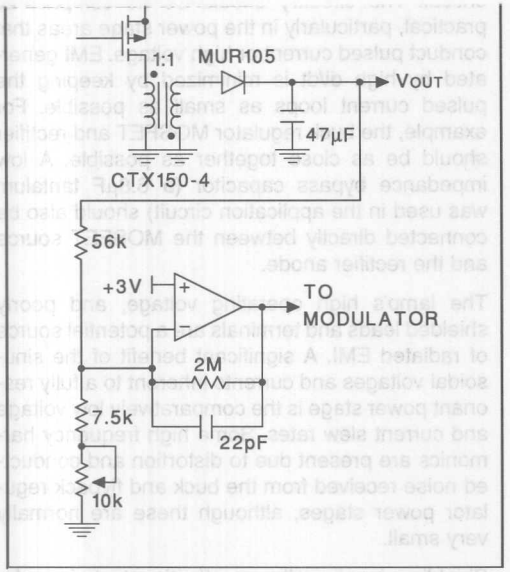


Figure 5. Positive output coupled inductor flyback regulator.

Since the output MOSFET is relatively large, and has significant output capacitance and avalanche energy capability compared to the current it must switch, a clamp or snubber network is not required to insure reliable operation. Snubbing may be necessary to reduce EMI however. This circuit can, of course be operated with continuous inductor current for a small improvement in efficiency. The compensation circuitry would then be similar to the previous flyback regulator examples. Flyback regulator and control loop design is covered in the references.

PRACTICAL CONSIDERATIONS

MEASUREMENT TECHNIQUES

The combination of low power, high voltage, and high frequency AC present a unique challenge in determining circuit efficiency. An absolute efficiency measurement is important because it allows meaningful comparison with work done by others. Since an electrical efficiency measurement removes lamp performance from the equation, it is the most universal performance index.

For an actual application however, high output light intensity for a given input power is the actual design goal. Once reasonable electrical efficiency is achieved, further circuit refinement should be

To measure electrical efficiency, extreme attention to measurement technique and equipment is required. Output current is relatively easy to measure with a current sense resistor in series with the lamp return to ground. For the design example circuit shown in figure 2, a small resistor can be added in series with R5 and D2 to measure both half cycles of the lamp current.

To measure lamp voltage, a 100X or 1000x oscilloscope probe with low input capacitance and good high frequency accuracy is required. Accurate AC probe calibration is critical in achieving a meaningful measurement. At low lamp current, both the lamp current and voltage exhibit clean sinusoidal waveforms with minimal harmonic distortion. The product of the RMS lamp current and voltage then give an accurate measurement of the output power. As current is increased, the lamp's nonlinearity becomes apparent, as significant distortion is observable in the lamp voltage waveform. The product of the RMS lamp current and voltage will no longer yield an accurate output power measurement.

A true RMS measurement that is insensitive to waveform shape is made by taking the average product of the instantaneous lamp voltage and current. Many digital oscilloscopes provide this function with reasonable accuracy. The accuracy of this technique can be further improved by calibrating to a known sinusoidal source.

EFFICIENCY OPTIMIZATION

Most of power lost in the lamp driver circuit is dissipated in the transformer, inductor, MOSFETs, primary resonant capacitor, buck regulator diode, and the UC3871. Although the output ballast capacitor (Cb) dissipates little power, its value greatly influences the performance of the circuit. Consider the effect of increasing Cb such that the secondary voltage drops 10%. The transformer's flux density and primary resonant current decrease 10%, reducing both transformer core and winding losses. Both of these losses are exponential, so the power savings can be significant. Smaller transformer losses decrease the input power required, reducing the current through, and the power lost in the other power handling components.

Of course the ballast capacitor cannot be continually increased, as waveform distortion will quickly become unacceptable, but there is an optimal value for a particular application that is best deter-

mined experimentally. The same is true for the primary resonant capacitor, where a decrease in value will increase the resonant frequency, and decrease the resonant current and associated losses. Again, there is an optimal value that yields the best distortion/efficiency tradeoff for a particular application.

The losses contributed by the other power components are more easily determined, as circuit operation is affected minimally by their variation. For lowest loss, MOSFETs are selected for minimal combined conduction and gate drive loss. Bigger is not necessarily better! Logic-level threshold devices are required for high efficiency at low input supply voltages, although standard threshold devices will usually function with reduced efficiency down to about 6V.

The primary resonant capacitor, Cp conducts the primary resonant current and must have low losses for good circuit efficiency. A monolithic ceramic capacitor, and several film capacitors from Electronic Components, Inc. [6], were evaluated to determine the relative performance differences among various dielectric and construction techniques. Polypropylene film/foil capacitors exhibit the lowest losses. Metalized polypropylene capacitors are usually smaller than foil/film construction, but will result in about a 1 percent decrease in efficiency.

Further size reduction is possible with polycarbonate or polyester capacitors, but efficiency will be about 1 percent to 3 percent lower than the foil/film polypropylene units. Since the capacitor value is too high for an NPO dielectric, ceramic capacitors must be avoided. The dissipation factor of Z5U and X7R ceramics is much too high for reasonable efficiency. A Z5U monolithic ceramic reduced efficiency more than 12% in the test circuit!

Separate bias (Vcc) and collector (Vc) supply inputs are provided by the UC3871 to take advantage of its ability to operate down to 4.5V. Supplying Vcc from a switching regulated supply while operating the rest of the circuit directly from the battery typically saves from 30mW to more than 100mW.

The buck inductor's winding resistance will dissipate significant power if its winding resistance is excessive. Minimum inductor values are therefore usually preferred to maintain reasonable size. This results in high ripple current that can lead to high core loss. Like all the other power components, every source of dissipation must be investigated and analyzed to squeeze maximum efficiency from the converter.

PC BOARD LAYOUT CONSIDERATIONS

As with all switching regulators, PC board layout is critical. The circuitry should be as compact as practical, particularly in the power stage areas that conduct pulsed current or high voltage. EMI generated by high di/dt is minimized by keeping the pulsed current loops as small as possible. For example, the buck regulator MOSFET and rectifier should be as close together as possible. A low impedance bypass capacitor (a 6.8μF tantalum was used in the application circuit) should also be connected directly between the MOSFET source and the rectifier anode.

The lamp's high operating voltage, and poorly shielded leads and terminals are a potential source of radiated EMI. A significant benefit of the sinusoidal voltages and currents inherent to a fully resonant power stage is the comparatively low voltage and current slew rates. Some high frequency harmonics are present due to distortion and conducted noise received from the buck and flyback regulator power stages, although these are normally very small.

Shielding is normally an effective technique for attenuating EMI generated by high dv/dt nodes, but the performance tradeoffs with the high voltage ballast circuity can be misleading. Shields (or ground planes) increase the capacitive loading on the circuit, but the shield itself dissipates negligible power. When a shield is added however, circuit efficiency will drop because the additional load capacitance will increase the resonant current, just as if the primary resonant capacitance were increased. This effect is minimized by making high voltage traces as short as possible.

Loss due to leakage current in the high voltage section is also possible, particularly as the assembly ages and the PC board surface becomes contaminated. Milling slots in the PC board is a good way to get sufficient creapage distance between the high voltage traces and the rest of the circuitry while maintaining a compact layout.

Another important consideration in the high voltage area is the length and routing of the return lead and PCB trace connecting to the current sense circuitry. If a fault opens the lamp circuit, the error amplifier will command maximum secondary voltage in an attempt to keep the current loop closed. The stray capacitance between the high voltage circuitry and the return lead may conduct sufficient current to keep the loop closed, particularly at low command current and maximum input voltage. This condition will prevent open lamp detection and severely over stress the circuitry.

This problem is avoided by keeping the lamp return path as short as possible, with the current sense resistor placed as close to the lamp as practical. Traces between the current sense resistor and the UC3871 are insensitive to noise and switching harmonics since the signal is DC at this point. Ideally, the majority of the return path length is placed between the current sense resistor and the feedback resistor.

Keeping the high voltage path as short as possible helps by reducing the radiated signal. Shielding around the high voltage area also reduces the radiated signal, but may not be practical in many application. The dimming range should be set no wider than necessary since high current sense resistor values increase sensitivity to this problem. The circuit described in the following section for wide dimming range applications is significantly more robust in this regard, and should be considered when packaging constraints force non-ideal layout.

WIDE DIMMING RANGE APPLICATIONS

Most cold cathode fluorescent lamps function acceptably down to about 1/20 of their rated current. Below this level, they begin to illuminate unevenly across the tube. This "thermometer" effect is caused by parasitic capacitive current, and is heavily influenced by shielding and grounding. Wide dimming ranges are accommodated without uneven lamp brightness by driving the lamp at maximum current, and pulse width modulating the current on and off at low frequency.

Figure 6 shows modifications to the standard application circuit for low frequency PWM control. A fixed current sensing resistor sets the maximum lamp current. An external PWM signal drives the inverting error amplifier input through a series diode and resistor. The input resistor value is chosen to force the lamp current to zero when the PWM input is pulled high. These modifications

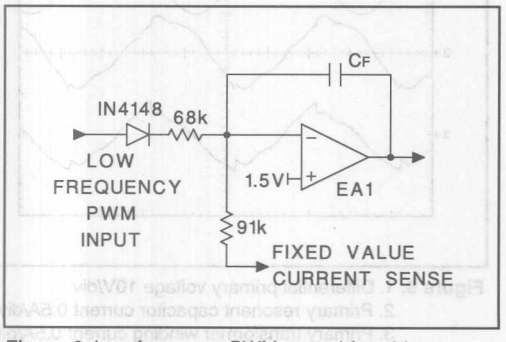


Figure 6. Low frequency PWM control for wide dimming range aplications.

where made to accept a 100Hz PWM signal from 5V CMOS logic through a 1N4148 and a 68k resistor. A 680 ohm current sense resistor set the continuous lamp current at approximately its rated value. Fixed current gain allowed the compensation capacitor (Cf) to be reduced to 4.7nF for more optimum loop performance.

With no further modifications, the circuit maintained uniform lamp intensity over a current range of more than a 500:1. Operation was linear with negligible effect from input voltage variation, down to about 1% of rated current. Below 1%, the current rise and fall time became significant, limiting the practical open loop dimming range to about 100:1. An accurate, stable dimming range greater than

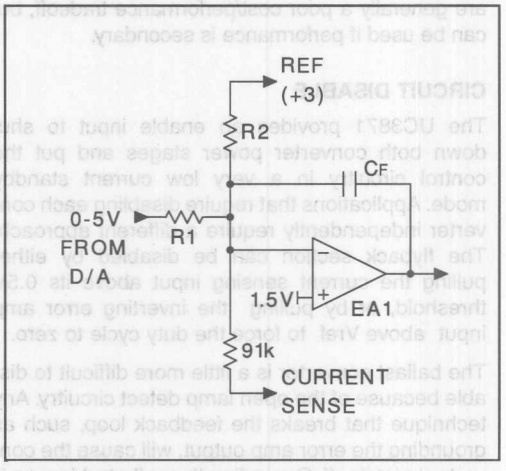


Figure 7. External voltage command interface.

500:1 can be achieved with the addition of a low bandwidth outer current or lamp intensity feedback loop.

DIGITAL LAMP CURRENT CONTROL

The preceding technique for wide dimming range applications is also the best method for digital lamp intensity control. A 100Hz PWM signal generated by a microprocessor combines excellent dimming range with single line digital control. An alternative approach is to use the circuit shown in figure 7, where a D/A injects a command signal into the control loop. This technique provides excellent performance for less than 20:1 dimming ranges, but unfortunately it also defeats the open lamp detect circuit. A third approach is to replace the current sense potentiometer with a digital pot or a multiplying D/A converter, but these devices can usually only handle low current.

BIPOLAR TRANSISTOR OUTPUT STAGES

When cost is more critical than performance, PNP bipolar transistors can be substituted for the P-channel MOSFETs. High gain, low saturation devices such as the Zetex [7] ZTX788B (3A, 20V PNP) perform quite well for the buck regulator when the input voltage is low. A PNP can also be used for the flyback converter, but at a greater efficiency reduction than the buck regulator because it requires a higher voltage device and has greater switching losses.

Simple high speed base drive is implemented by choosing a base resistor for sufficient drive at the minimum input voltage. A small capacitor in parallel with the base resistor improves switching speed. Bipolar NPNs in place of the N-channel MOSFETs are generally a poor cost/performance tradeoff, but can be used if performance is secondary.

CIRCUIT DISABLE

The UC3871 provides an enable input to shut down both converter power stages and put the control circuitry in a very low current standby mode. Applications that require disabling each converter independently require a different approach. The flyback section can be disabled by either pulling the current sensing input above its 0.5V threshold, or by pulling the inverting error amp input above Vref to force the duty cycle to zero.

The ballast converter is a little more difficult to disable because of the open lamp detect circuitry. Any technique that breaks the feedback loop, such as grounding the error amp output, will cause the converter to latch off. Grounding the soft-start input will not bring the duty cycle zero, and therefore will not completely disable the converter. The best shut down method is to source enough current into the inverting error amp input to force its output to ground. This saturates the loop, causing the duty cycle to go to zero without falsely indicating an open lamp condition.

MULTIPLE LAMP CIRCUITS

The ballast circuit is easily modified to drive two or more parallel lamps by splitting the ballast capacitance into two or more capacitors of equivalent value. Because of lamp mismatch, the dimming range must normally be less than single lamp circuits. Additionally, a higher ballast capacitor voltage than is optimum for a single lamp may be required to insure that both lamps start.

DESIGN EXAMPLE PERFORMANCE AND WAVEFORMS

Figures 8 through 10 show typical ballast waveforms from the design example (figure 2) delivering 1.0W into a lamp from a 10V input supply. Figure 8 shows the primary voltage waveforms. Note that the center-tap waveform is one-half the amplitude of the push-pull waveforms, and that no distortion or ringing is evident at the cusps of the waveform.

Figure 9 shows the primary current waveforms and the differentially sensed transformer primary voltage waveforms. The transient steps at the peaks of the primary current are from the push-pull switches turning on, which allow input (reflected load) current to conduct in addition to the resonant current.

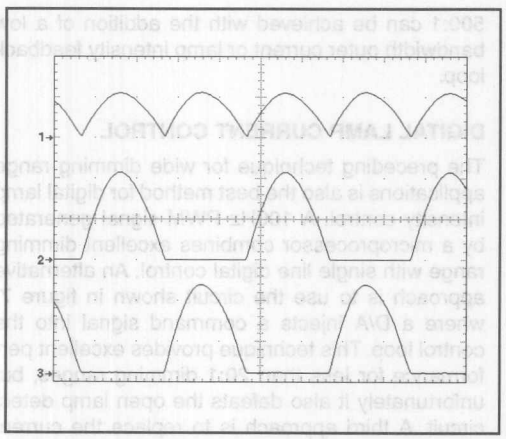


Figure 8. 1. Centertap voltage 5V/div
2. Q1 drain voltage 5V/div
3. Q2 drain voltage 5V/div
Horizontal: 5μs/div

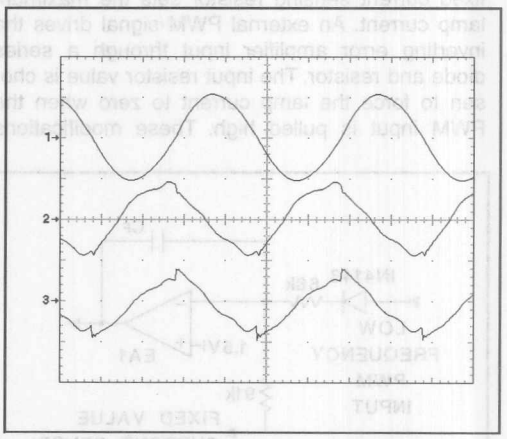


Figure 9. 1. Differential primary voltage 10V/div
2. Primary resonant capacitor current 0.5A/div
3. Primary transformer winding current 0.5A/div
Horizontal: 5μs/div

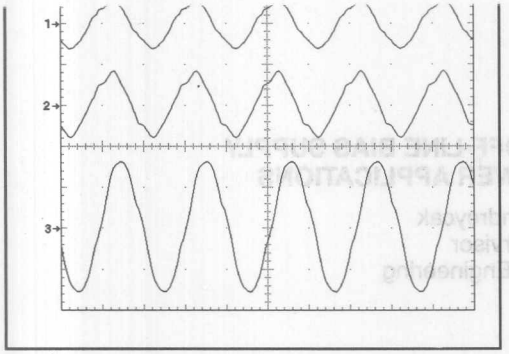


Figure 10. 1. Lamp current 10mA/div
2. Lamp voltage 500V/div
3. Transformer secondary voltage 500V/div
4. Horizontal: 10µs/div

Figure 10 shows the secondary voltage and current waveforms. Lamp current and voltage are in phase indicating that the lamp appears resistive. These waveforms lead the secondary voltage waveform because of the capacitive coupling. Distortion in the lamp voltage waveform is caused by lamp impedance nonlinearity, which also causes some distortion in the secondary voltage waveform.

Figures 11 and 12 illustrate circuit efficiency with varying input supply voltage and output power. In both cases a separate 5V supply powered Vcc, since this is available in most applications. Figure 11 shows the efficiency of the complete converter over an input supply range of 5.5V to 18V. For this plot, the lamp power was 1.0W, and the LCD bias power was 0.324W (18V across 1k). The sudden decrease in efficiency at low input voltage is from insufficient gate drive voltage. This efficiency drop can be eliminated by using logic level MOSFETs.

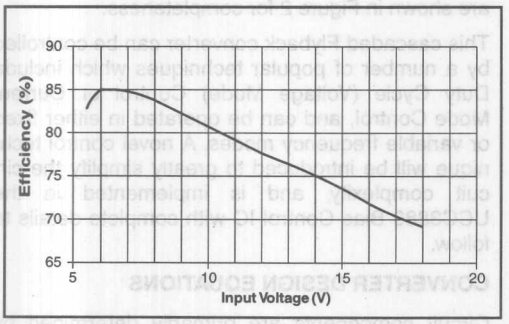


Figure 11. Efficiency vs. input voltage for 1.324W output.

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control circuitry was still active. The lamp power was then varied from 0.2W to 1.9W while keeping the supply voltage at 10V. Above about 3/4W, efficiency was greater than 80%. At light load, the control circuit and gate drive losses became significant, and efficiency was greatly reduced.

SUMMARY

The UC3871 provides a complete power supply control solution for backlit LCDs. A design method illustrated with a circuit example has been presented, along with alternate configurations and loop compensation techniques. Example circuit waveforms and efficiency graphs show that the UC3871 provides a simple, yet high performance solution.

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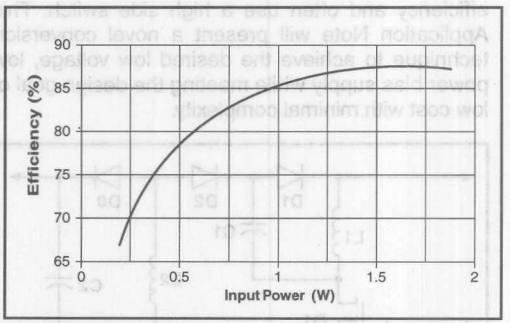
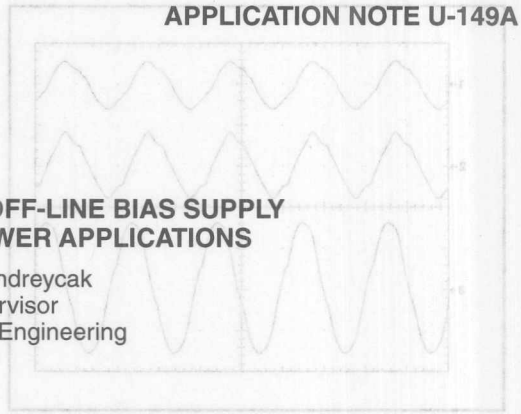


Figure 12. Efficiency vs. output power for 10V input.



ELEGANTLY SIMPLE OFF-LINE BIAS SUPPLY FOR VERY LOW POWER APPLICATIONS

by Bill Andreycak
Supervisor
Application Engineering

INTRODUCTION

Generating a low power, low voltage bias supply in an off-line application may not seem like a major design challenge – at first glance. However, obtaining an efficient, cost effective and compact 1 Watt supply can be a frustrating ordeal as the various approaches are evaluated. A simple transformerless technique, like the Buck regulator, requires a rather complex high side switch which can be difficult to drive. Narrow duty cycles are another inescapable problem with a significant step down in input to output voltage.

The Flyback converter can provide a relatively simple solution for this low power application, but it requires more costly coupled windings instead of a single inductor to perform the voltage conversion. Other topologies too, have their own unique sets of problems. For example, the SEPIC Converter is a viable option, but needs a high voltage blocking capacitor and two inductors, in addition to the high voltage switch. It will also require current mode control for stability as opposed to simpler control techniques. Charge pump circuits are another possibility, but are generally much noisier, deliver poor efficiency and often use a high side switch. This Application Note will present a novel conversion technique to achieve the desired low voltage, low power bias supply while meeting the design goal of low cost with minimal complexity.

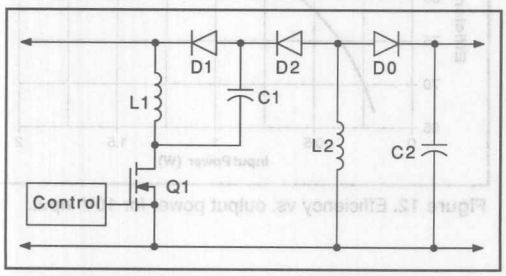


Figure 1. Cascaded Flybacks

Approach : The basic converter shown in Figure 1 is a cascaded Flyback Converter operated in the discontinuous current mode. Two flyback stages are placed in a series configuration to complete the voltage transformation. Inductor L1 of the first stage is switched across the input voltage when MOSFET (Q1) turns on. Energy is stored in L1 as its current rises linearly until the switch is turned off. When this occurs, inductor L1 discharges its energy into capacitor C1, and diode D1 is conducting. In steady state operation the switching action develops a net DC voltage across C1, the "output" capacitor of the first Flyback converter, C1.

The inductor of the second stage (L2) is also switched across capacitor C1 while the MOSFET is on. Although the voltage across inductor L2 is negative with respect to ground, energy is stored in L2 as the current linearly rises. When the switch is turned off, inductor L2 discharges to the output capacitor of this second Flyback stage, C2. A regulated DC output voltage is obtained across C2 and controlled by varying the ON-time of switch Q1. Voltage and current waveforms for this converter are shown in Figure 2 for completeness.

This cascaded Flyback converter can be controlled by a number of popular techniques which include Duty Cycle (Voltage Mode) Control or Current Mode Control, and can be operated in either fixed or variable frequency modes. A novel control technique will be introduced to greatly simplify the circuit complexity, and is implemented in the UCC3889 Bias Control IC with complete details to follow.

CONVERTER DESIGN EQUATIONS

Circuit components are primarily determined by several key factors; switching frequency, output power, efficiency and duty cycle. First, the voltage conversion relationship for the Flyback topology is reviewed.

Duty Cycle :

Duty cycle (d) = $\frac{t_{ON}}{t_{PERIOD}}$

where $t_{PERIOD} = t_{ON} + t_{OFF}$, or $\frac{1}{f_{SWITCHING}}$

For the Flyback topology, the duty cycle can be approximated by the following relationship:

$$V_{OUT} = V_{IN} \bullet \frac{d}{1-d}$$

The cascaded Flyback conversion technique utilizes the output of the first Flyback converter as the input to the second stage. The voltage transformation of the two Flyback converters in series can be approximated by :

$$V_{OUT} = V_{IN} \left(\frac{d}{1-d} \right)^2$$

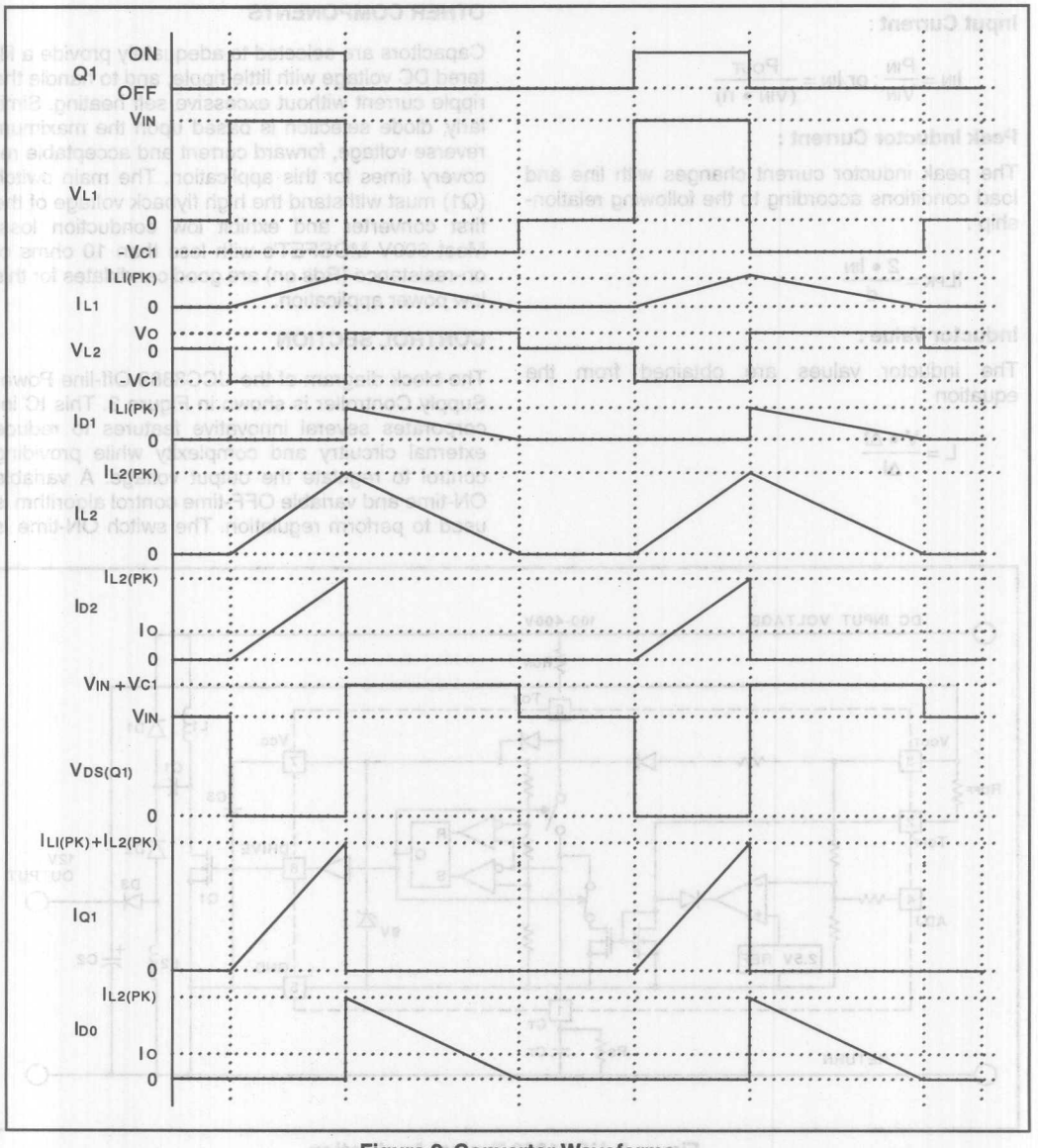


Figure 2. Converter Waveforms

This equation can be rearranged to solve for the duty cycle with respect to **VIN** and **VOUT** as:

$$\text{duty cycle} = \frac{1}{1 + \sqrt{\frac{V_{IN}}{V_{OUT}}}}$$

Input Power :

$$P_{IN} = \frac{P_{IN}}{n} \text{ ; where } n = \text{efficiency}$$

Input Current :

$$I_{IN} = \frac{P_{IN}}{V_{IN}} \text{ ; or } I_{IN} = \frac{P_{OUT}}{(V_{IN} \bullet n)}$$

Peak Inductor Current :

The peak inductor current changes with line and load conditions according to the following relationship :

$$I_{LPK} = \frac{2 \bullet I_{IN}}{d}$$

Inductor Value :

The inductor values are obtained from the equation :

$$L = \frac{V \bullet \Delta t}{\Delta I}$$

Any set of operating conditions can be used to solve this, and other equations. It is often easiest to standardize on using low line, full load conditions when the inductor (L1) is charging during the switch ON-time.

$$L = V_{INmin} \bullet \frac{t_{ON}}{I_{LPK}}$$

The second Flyback inductor value (L2) is obtained using this equation but by substituting the output voltage of the first converter (**VOUT1**) for **VIN**.

OTHER COMPONENTS

Capacitors are selected to adequately provide a filtered DC voltage with little ripple, and to handle the ripple current without excessive self heating. Similarly, diode selection is based upon the maximum reverse voltage, forward current and acceptable recovery times for this application. The main switch (Q1) must withstand the high flyback voltage of the first converter and exhibit low conduction loss. Most 600V MOSFET's with less than 10 ohms of on-resistance (Rds on) are good candidates for this low power application.

CONTROL SECTION

The block diagram of the UCC3889 Off-line Power Supply Controller is shown in Figure 3. This IC incorporates several innovative features to reduce external circuitry and complexity while providing control to regulate the output voltage. A variable ON-time and variable OFF-time control algorithm is used to perform regulation. The switch ON-time is

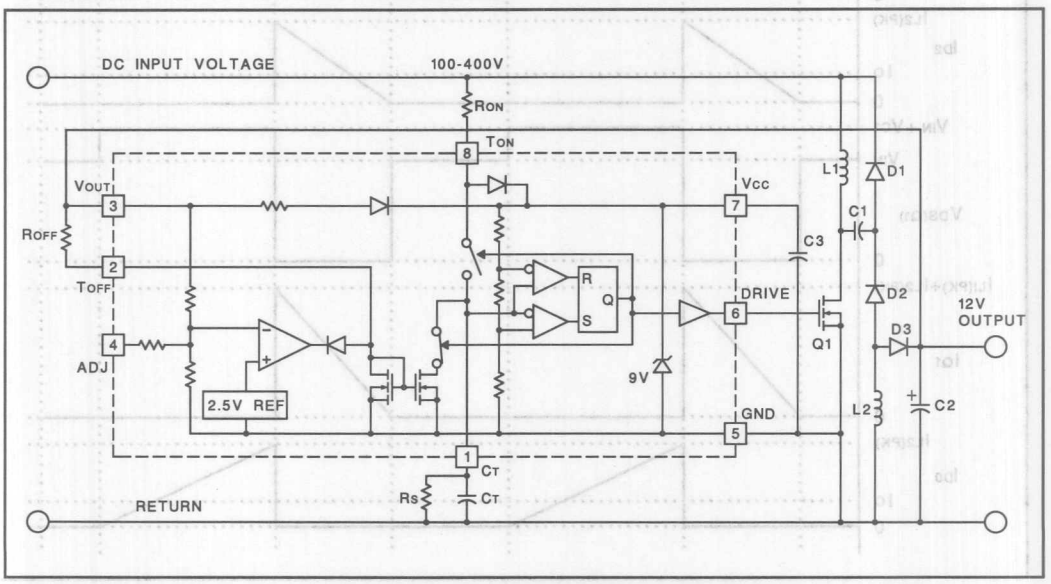


Figure 3. UCC1889 Typical Application

varied inversely with the supply input voltage, whereas the OFF-time is varied inversely with the supply's output voltage. This results in inherent short circuit protection, input voltage feedforward and a greatly simplified control technique. Operation and programming of these key features will be explored in more thorough detail.

POWERING THE UCC3889 CONTROLLER

Note that the UCC3889 is powered by connecting a resistor from the IC's **TON** pin to the high voltage supply, and not from the **VCC** connection. An internal switch directs the current from **TON** to either **VCC** or to a current mirror used for a timing function, and further details are presented in the TIMING section. Prior to turn-on, this switch is positioned to connect **TON** to **VCC**, steering the current into the **VCC** supply capacitor.

This BiCMOS Control IC consumes less than 250 microamps from the input supply while **VCC** is below it's 8.5 volt undervoltage lockout (UVLO) turn-on threshold. Once on, the IC typically draws only 1.5 milliamps from **VOUT**, and has a UVLO turn-off threshold of 6.3 volts. The **VCC** supply capacitor, **CVcc**, must maintain the IC supply voltage within it's 2.2 volt UVLO hysteresis region during the start-up of the converter.

Additionally, the minimum line voltage to begin operation of the converter can be programmed. **RON**, the timing circuit programming resistor also functions to program a current indicative of the AC input line voltage. Turn on occurs when this current reaches 220µA typically, so select the value of **RON** accordingly. This protection feature therefore will require a minimum current drawn by the IC from the line at all times, so the worst case power dissipation for **RON** will be at high line.

Two other noteworthy features are the IC's internal 9V zener clamp diode between **VCC** and ground, and the switched current source and diode from **VOUT** to **VCC**. The zener eliminates the need for external overvoltage protection when powered from a current source (resistor) to a high voltage supply, typical of an off-line converter. It also clamps the supply voltage when normally powered from the converter's output voltage. When **VOUT** rises above **VCC**, a switched internal current source is enabled thus limiting the current shunted to ground by the zener clamp diode. This helps minimize wasted power which would otherwise reduce overall efficiency and raise the IC's junction temperature. The series diode also prevents **VCC** from powering **VOUT** during start-up and short circuited output conditions.

GATE DRIVE OUTPUT

A CMOS totempole output stage is incorporated in this IC which provides a rail-to-rail voltage swing of the DRIVE output. A 200mA peak sink current and a 150mA peak source current will adequately drive MOSFETs gates for this low power application. Typical rise and fall times into a 1 nanoFarad load are 35 and 25 nanoseconds respectively.

Schottky clamp diodes to protect the IC's gate drive output from swings below ground and above **VCC** are NOT needed. The internal body diodes of the CMOS output stage transistors provide sufficient clamping.

OSCILLATOR AND TIMING FUNCTIONS

Programming begins with a selection of the highest operating frequency which will typically occur at low line and full load. As either the load is decreased, or input line increased, the switching frequency will adjust to regulate the output voltage. Therefore, the first parameter to determine is the switching frequency, **FS**. A good first approximation is 100kHz which will be used for this example.

Fs = 100kHz at low line, full load

The switching frequency selection will determine the exact values of the converter inductors (L1 and L2) in addition to the exact ON-time and OFF-time. Once the inductor values are calculated, the IC can be programmed to deliver the specific control timing functions, **TON** and **TOFF**. Likewise, the selected ON and OFF times can be used to determine the exact inductor values needed to facilitate the power conversion.

Switch ON-time is developed by charging a timing capacitor from a constant current source. The exact charging current is varied directly with the converter input voltage to deliver a constant volt-second charging of the timing capacitor. This characteristic will exhibit input voltage feedforward and immunize the output from changes in line voltage.

During the charging period of the timing capacitor, the voltage at **TON** is approximately 4.5 volts. Note that only eighty percent (80%) of the current into the **TON** pin is used to charge the timing capacitor. The other twenty percent is diverted to the minimum line voltage detection circuitry which is described in the Protection Circuits portion of this Application Note. The exact timing capacitor charging current is therefore :

$$I(C_{T+}) = 0.8 \bullet \frac{(V_{IN} - 4.5)}{R_{TON}}$$

The timing capacitor has a peak to peak amplitude of approximately 3.7 volts for high noise immunity. It begins charging from a lower threshold of 1.3 volts to it's upper threshold of 5.0 volts. While the timing capacitor is charging, the IC's output is high and the converter switch is on. The control circuit ON-time is programmed according to the following formula:

$$t_{ON} = \frac{C_T \bullet 3.7}{I(C_{T+})}$$

This can also be expressed as :

$$t_{ON} = \frac{4.6 \bullet C_T \bullet R_{TON}}{V_{IN} - 4.5}$$

The ON-time must correspond to the time required to charge the inductors to a peak current value necessary to maintain regulation of the output voltage for any given set of line and load conditions. Note that the exact voltage at **TON** will rise from about 2.5 to 6.5 volts while the timing capacitor is charging, so these equations are approximations.

Once the timing capacitor crosses the upper oscillator threshold, the IC output goes low and the main switch is turned off. The timing capacitor is then discharged by a current programmed at the **TOFF** pin. This discharge current is varied as a function of the converter's output voltage to perform regulation, facilitate startup and provide protection against overload and short circuit conditions. Discharge current is programmed by a resistor (**ROFF**) from the **TOFF** pin to ground according to the following equation:

$$I(C_{T-}) = \frac{V_{OUT} - 0.7}{R_{OFF}}$$

The OFF-time is expressed as :

$$t_{OFF} = \frac{3.7 \bullet C_T \bullet R_{OFF}}{V_{OUT} - 0.7}$$

The total conversion period is a sum of the ON-time and OFF-time for a given set of operating conditions. Combining equations, this can be stated as:

$$t_{PERIOD} = 3.7 \bullet C_T \bullet \left(\frac{R_{TON}}{0.8 \bullet (V_{IN} - 4.5)} + \frac{R_{TOFF}}{V_{OUT} - 0.7} \right)$$

Since one percent resistors are more readily available than capacitors with such a tight tolerance, it is advisable to first select the timing capacitor. Also, resistor values should be kept as high as possible to minimize oscillator currents to attain high overall efficiency, especially in a low power application. A good first approximation is to use 150pF for the timing capacitor value which will "home-in" on timing resistor values between 200k and 2meg ohms for approximately 100kHz operation.

C_T = 150pF (first approximation)

REGULATING THE OUTPUT VOLTAGE

The converter output voltage can be regulated in two different modes, depending on the application. In it's simplest configuration, the output voltage is connected to the IC's V_{OUT} pin and the ADJ pin is unused. An internal 116k/30k ohm resistor network is used to divide the output voltage down for comparison to a precision 2.5 volt reference at the transconductance (gm) amplifier. It's output alters the timing capacitor discharge current to adjust the Off-time in response to any changes in the converter output voltage. In this configuration with the ADJ pin "floating", the output voltage is regulated at 12 volts. This level was selected for general purposes and is compatible with many applications.

Another simple configuration of this control circuit is to ground the ADJ pin. An additional 50kΩ is then placed in parallel with the 30kΩ internal divider resistor thus lowering the impedance to about 18.75kΩ. Grounding the ADJ pin will regulate the converter output voltage at approximately 18 volts instead of 12 volts, as with the ADJ pin floating. This amplitude was selected for use with many popular off-line PWMs as this converters principal load which utilize a 16 volt turn-on threshold. After accommodating their UVLO tolerances, eighteen volts was selected to fulfill nearly all PWM undervoltage lockout requirements.

The converter output voltage can be programmed for any level above 2.5 volts with two parts. An external resistive divider network between V_{OUT}, ADJ and GND is all that's needed. This should be a lower impedance than the IC's internal divider network to null out any inaccuracies due to initial tolerance. By proper IC layout design and procedures, resistor ratios within the device will be maintained quite accurately although their exact values can vary significantly. For this reason, best results are obtained by using lower impedances externally than the 116k, 30k and 50k used within the UCC3889.

CLOSING THE FEEDBACK LOOP

An internal transconductance amplifier (gm type) is used to maintain regulation of the output voltage. The converter's output voltage is divided down by the 116k and 30k ohm resistor network and fed to the inverting input of the error amplifier. This statement applies for the simple configuration where the ADJ pin is unused and left floating. For all other applications which utilize the ADJ pin for programming the output voltage, then the 50k ohm series resistance must be accommodated in the design

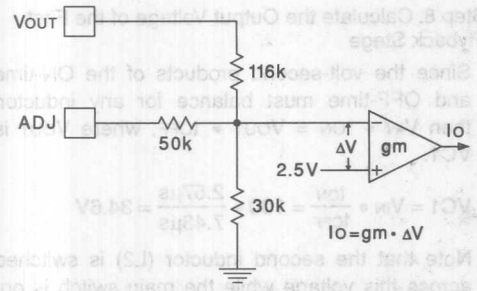


Figure 4. Adjust Pin Details

equations, as shown in Figure 4. For either case, the noninverting error amplifier input is internally tied to a precise 2.5 volt reference. The corresponding amplifier output current is the transconductance of the amplifier (gm) multiplied by the difference in amplifier input voltages (ΔV) and is expressed as:

$$I(E/A)_{OUT} = gm \bullet \Delta V, \text{ where } gm = 1mA/V$$

The error amplifier output current is used to modulate the discharge current of the timing capacitor and perform regulation. This current is subtracted from the capacitor's maximum discharge current which is programmed by ROFF, as shown in Figure 5. Note that the maximum discharge current is limited to 225 microamps within the IC, so a value below this should be used.

When the converter output voltage is low, the timing capacitor discharge current is also low. This is typical of start-up and short circuit conditions. Low discharge current indicates a long discharge time, or OFF-time for CT, corresponding to a low duty cycle. This feature delivers excellent protection under either of these conditions. As the output voltage increases, so does the discharge current. This has the effect of widening the duty cycle in response to the output voltage being lower than it's ideal setpoint. More energy is transferred as the duty cycle widens which continues to raise the output voltage.

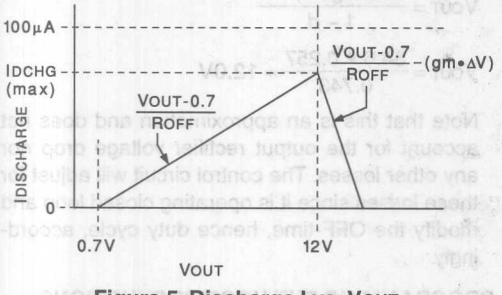


Figure 5. Discharge I vs. VOUT

As the exact point of regulation is reached, the timing capacitor discharge current will decrease as shown in Figure 5. This has the effect of reducing the effective duty cycle in response to the output voltage getting above the ideal threshold. If the output voltage continues to climb, then the discharge current is reduced even further. This will result in a longer OFF-time, or further reduced duty cycle, thus bringing the output voltage back to it's set point. Note that this operational mode also provides overvoltage protection.

PROTECTION CIRCUITRY

For an eight pin device, this UCC3889 features a number of internal protection features. As highlighted in previous sections, the IC has a 9V zener clamp on its supply rail. There is also a diode isolating VCC from the normal power source (VOUT) to keep the IC alive in case of a shorted output or overload condition. A switched current source also protects the zener from the low impedance present at VOUT.

Undervoltage lockout guarantees that the IC does not turn on until all internal circuits are properly biased for normal operation. It also insures an adequate gate drive amplitude is present to the main switch. This is performed by the "VCC OK" comparator as indicated in the UCC3889 block diagram, Figure 3.

Low line lockout protection is also contained within the IC to prevent operation during brown-out conditions and at power down. This eliminates the potential for excessively low frequency operation which can cause saturation of the inductors and abnormally high currents within the power stage. One-fifth of the current flowing into TON is used in conjunction with the "V LINE OK" comparator to detect this situation. Note that this conditional test is performed at every oscillator clock cycle during the charging of the timing capacitor. To further reduce power consumption, the current used for detection of low line, in addition to CT's charging current are switched off while the oscillator discharges each cycle.

Once a low line fault triggers the "V LINE OK" comparator, a 0.5 millisecond fault delay period begins. During this time the IC output is held off regardless of the oscillator operation. This delay limits the converter's retry rate during a brownout to around 2 kilohertz which is a significant reduction in comparison to the switching frequency. In addition, the ON-time of the converter is reduced to 600ns independent of the input line voltage.

Further details and specifications can be obtained on the device's datasheet.

DESIGN EXAMPLE

V_{IN} = 80 to 132VAC, or 100 to 180VDC

V_{OUT} = 12VDC

P_{OUT} = 1 Watt maximum

$F_{SWITCHING}$ = 100kHz

Efficiency = 50% (estimate)

Low line, full load condition will be used to begin the design procedure.

Step 1. Calculate Maximum Duty Cycle

$$\text{DutyCycle (d)} = \frac{1}{1+\sqrt{\frac{V_{IN}}{V_{OUT}}}}$$

$$d(max) = \frac{1}{1+\sqrt{\frac{100}{12}}} = \frac{1}{3.887} =$$

d(max) = 0.257 (roughly 26%)

Step 2. Calculate $t_{ON}(max)$

$$F_{SWITCHING} = \frac{1}{t_{PERIOD}} = \frac{1}{10\mu s} = 100kHz$$

$$t_{ON}(max) = \frac{d(max)}{F_{SWITCHING}}$$

$$t_{ON}(max) = \frac{0.257}{100kHz} = 2.57\mu s$$

Step 3. Calculate $t_{OFF}(min)$

$t_{OFF}(min) = t_{PERIOD} - t_{ON}(max)$

$t_{OFF}(min) = 10\mu s - 2.57\mu s = 7.43\mu s$

Step 4. Calculate the Maximum Input Power

$$P_{IN}(max) = \frac{P_{OUT}}{n(efficiency)} = \frac{1W}{0.5} = 2W$$

Step 5. Calculate the Input Current at Low Line

$$I_{IN} = \frac{P_{IN}}{V_{IN}(min)}$$

$$I_{IN} = \frac{2W}{100V} = 0.020A$$

Step 6. Calculate the Peak Inductor Current, $I_{L1}(pk)$

$$I_{L1}(pk) = 2 \bullet \frac{I_{IN}}{d} = 2 \bullet \frac{0.020}{0.257} = 0.156A$$

Step 7. Calculate the First Inductor Value (L1)

$$L1 = \frac{V_{IN} \bullet t_{ON}(max)}{I_{L1}(pk)} = 100 \bullet 2.57 \bullet \frac{10^{-6}}{0.156} = 1.67mH$$

Step 8. Calculate the Output Voltage of the First Flyback Stage

Since the volt-second products of the ON-time and OFF-time must balance for any inductor, then $V_{IN} \bullet t_{ON} = V_{OUT} \bullet t_{OFF}$, where V_{OUT} is VC1.

$$VC1 = V_{IN} \bullet \frac{t_{ON}}{t_{OFF}} = 100 \bullet \frac{2.57\mu s}{7.43\mu s} = 34.6V$$

Note that the second inductor (L2) is switched across this voltage while the main switch is on, so VC1 is the applied voltage to the second Flyback stage. Although this capacitor is switched between the lower and upper supply rails, the voltage rating of C1 is much lower than the input. The worst case can be easily calculated using the previous equation for VC1, but note that the IC will adjust the duty cycle to minimize this voltage change over line and load ranges. Specifically, the switching frequency will adjust, so a high voltage capacitor is not needed for normal operation.

Step 9. Calculate the Peak Current in the Second Inductor (L2)

$$I_{L2}(pk) = 2 \bullet \frac{I_{OUT}}{1-d}$$

$$\text{where } I_{OUT} = \frac{P_{OUT}}{V_{OUT}} = \frac{1W}{12V} = 0.083A$$

$$I_{L2}(pk) = \frac{2 \bullet I_{OUT}}{d} = \frac{2 \bullet 0.083}{1-0.257} = 0.223A$$

Step 10. Calculate the Second Inductor Value (L2) using the Output Voltage of the First Stage, ON-time and Required Peak Current of L2.

$$L2 = VC1 \bullet \frac{t_{ON}}{I_{L2}(pk)} = \frac{34.6 \bullet 2.57 \bullet 10^{-6}}{0.223} = 398\mu H$$

Step 11. Verify the Estimated Output Voltage, V_{OUT}

$$V_{OUT} = \frac{V_{IN}(stage\ 2) \bullet d}{1-d}$$

$$V_{OUT} = \frac{34.6 \bullet 0.257}{0.743} \approx 12.0V$$

Note that this is an approximation and does not account for the output rectifier voltage drop nor any other losses. The control circuit will adjust for these losses since it is operating closed loop and modify the OFF-time, hence duty cycle, accordingly.

PROGRAMMING THE UCC3889 FUNCTIONS

The timing functions of the IC will be programmed according to the timing intervals which

have been calculated for 100kHz operation. A 150pF timing capacitor has been selected as a starting point to simplify the design process. The specific ON-time and OFF-time programming resistors are obtained from the previous equations by inserting the appropriate times and capacitor value.

Step 12. Calculate R_{TON}

$$R_{TON} = \frac{t_{ON} \bullet (V_{IN} - 4.5)}{4.6 \bullet C_T}$$

$$R_{TON} = \frac{2.57 \bullet 10^{-6} \bullet (100 - 4.5)}{4.6 \bullet 150 \bullet 10^{-12}}$$

R_{TON} = 348.9k (use 330kΩ)

Step 13. Calculate R_{OFF}

$$R_{OFF} = \frac{t_{OFF} \bullet (V_{OUT} - 0.7)}{3.7 \bullet C_T}$$

$$R_{OFF} = \frac{7.43 \bullet 10^{-6} \bullet (12 - 0.7)}{3.7 \bullet 150 \bullet 10^{-12}}$$

R_{OFF} = 149.3k (use 150k)

Step 14. Calculate R_{DCHG}

A resistor placed in parallel with the timing capacitor is used to discharge C_T when the converter output voltage goes to zero. This also sets the maximum OFF-time of the switch and is used to program the minimum frequency for startup and short circuit protection. A one millisecond (1ms) duration will be used for this example.

$$R_{DCHG} \approx \frac{t_{OFFmax}}{3.7 \bullet C_T}$$

R_{DCHG} = 1.78 meg (use 1.8 or 2 meg)

PROGRAMMING THE OTHER PINS

An output voltage of 12VDC has been selected which does not require a resistor divider for feedback. The IC's ADJ pin is open for this application. Also, the MOSFET gate will be directly connected to the IC's output and no gate drive resistor is needed. Typical 0.1µF bypassing will be used at the IC's supply voltage, V_{CC}. A tight prototype layout is also recommended as good design practice.

PROTOTYPE ASSEMBLY

The entire 1 Watt off-line power supply can be built with as few as 16 parts for a 110VAC only input as shown in Figure 6. Using surface mount assembly techniques and a tight PC board layout, the completed assembly requires about one square inch (1" sq.of area). A performance evaluation for this example is summarized below.

UNIVERSAL INPUT VOLTAGE (80 to 265VAC)

Due to the higher voltage input (373Vpk), L1 and R_{TON} will be broken-up into series components which can conservatively handle the applied voltage. For example, three identical 1/4W resistors will be used as R_{TON} due to the maximum voltage rating of 200 volts each. Inductor L1 is divided into two very inexpensive axial type inductors also placed in series to withstand the high voltage. All other lower voltage components are similar to the 110VAC only application, and are readily available, standard types used in the industry.

The bulk input capacitor should be conservatively rated for 450VDC, and the input diodes are 800V types. Since the circuit operates in the discontinuous inductor current mode, diode switching speed is not very critical. However, diodes should have recovery times below a quarter of a microsecond (trr < 250ns) for efficient high frequency operation, and rated for the proper reverse voltage. Standard

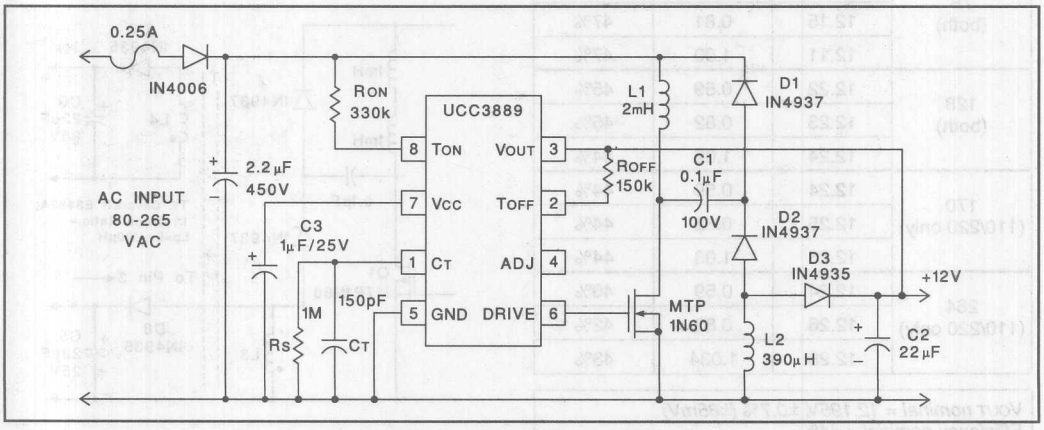


Figure 6. Design Example

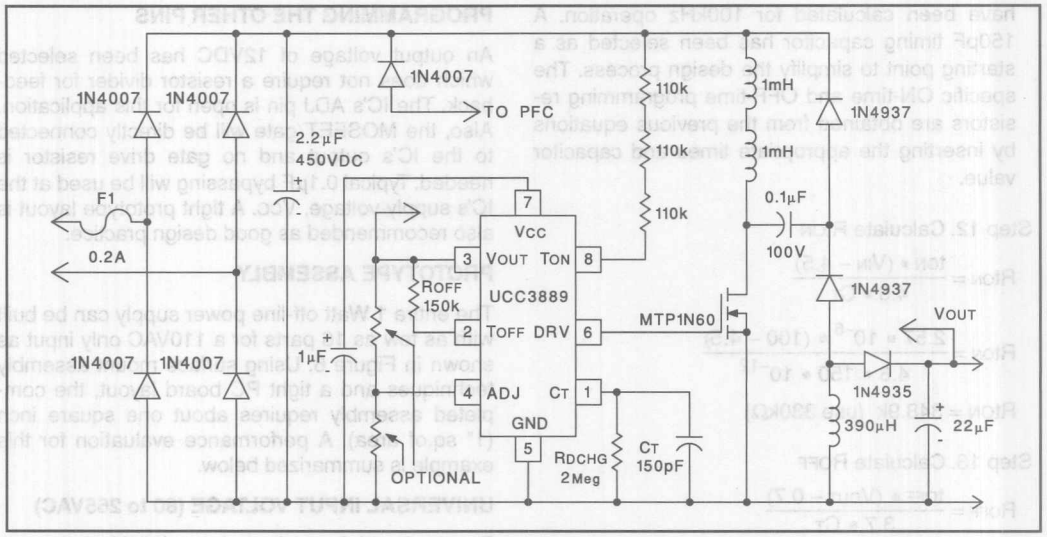


Figure 7. Typical 110/220VAC Application

1N4937 type 600V diodes can be used in the high voltage switching sections, and a lower voltage 1N4935 is a good selection for the output diode. To simplify manufacturing, 1N4937s can be used for all three rectifier applications. The complete schematic and list of components is shown in figure 7. Measured performance is indicated above.

UCC3889 Application Circuit Performance Measurements

110VAC (only) and 110/220 Universal AC input Nonisolated models

VIN (VAC)	VOUT (VDC)	POUT (W)	EFFCY (approx)
78 (both)	12.16	0.58	45%
	12.15	0.81	47%
	12.11	1.00	47%
128 (both)	12.22	0.59	45%
	12.23	0.82	45%
	12.24	1.02	44%
170 (110/220 only)	12.24	0.59	44%
	12.25	0.82	44%
	12.26	1.03	44%
264 (110/220 only)	12.24	0.59	40%
	12.26	0.82	42%
	12.28	1.034	43%

VOUT nominal = 12.195V, ±0.7% (±85mV)
Efficiency nominal = 44%

ISOLATING THE OUTPUT VOLTAGE

An isolated output voltage is obtainable with this UCC3889 controlled cascaded Flyback conversion technique. While several possibilities exist, one of the easiest places to attain isolation is at the inductor used in the second power conversion stage, as shown in Figure 8. Due to its lower inductance than the first stage, fewer turns are required and generally a smaller core can be utilized. Note, however, that the core size could be predominantly determined by the isolation requirements and not the stored energy requirements of the system. Designers are encouraged to pursue various core geometry options depending on the specific isolation voltage, safety agency and creepage/clearance distance requirements.

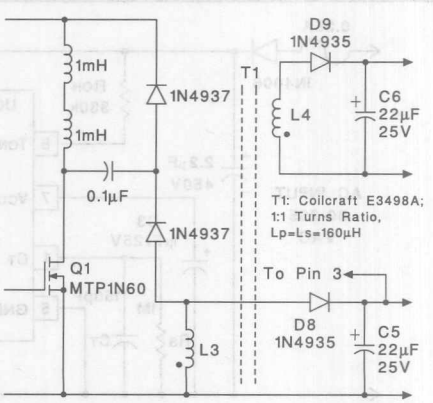


Figure 8. Isolated Output

One rather quick, inexpensive and effective way to provide an isolated output is to use an "off-the-shelf" isolation transformer which meets the design specifications. Many standard "Common Mode Line Chokes" used for EMI filters and suppression meet the appropriate voltage isolation requirements. One example of this is the Coilcraft "EE Style" series of line chokes. Specifically, their E3496A through E3498A coupled chokes have inductances between 168µH and 468µH, and can handle currents from 2.5 to 4 amps. As stated previously, there are a variety of other manufacturers, core styles and ratings to choose from, in addition to designing one's own.

REGULATING THE ISOLATED OUTPUT

Maintaining adequate regulation of the isolated output voltage over all line and load conditions without any feedback path to the IC via optocoupler (etc.) is possible. If both windings of the isolating inductor were perfectly coupled then the voltages of each would look identical regardless of which one was being loaded. As is always the case, truly perfect magnetic coupling cannot be obtained, resulting in detrimental series, leakage inductance. This detracts from the ability for one winding to perfectly track the other which will degrade output voltage regulation. These effects are minimized by a low leakage inductance design, but some finite leakage is to be expected, especially with high voltage isolation between windings.

Preloading of the "feedback" winding which powers the UCC3889 IC and provides the voltage feedback information will improve regulation of the isolated output over all load conditions. While this does reduce overall efficiency, the small penalty may be an acceptable compromise for the improvement in regulation.

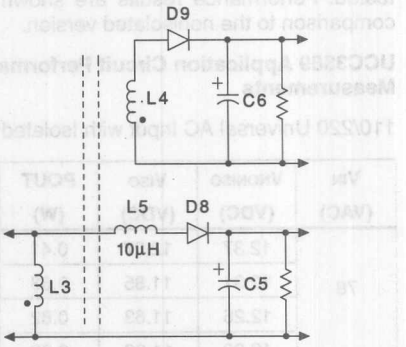


Figure 9. Adding Series Inductance to Improve Cross Regulation

The best option to improve regulation is to add some series inductance to the "feedback" winding as shown in Figure 9. Note that when placed as shown, the inductance is not part of the circuit while the coupled inductor is charging, but only during the discharge. This additional inductance has the effect of steering all ripple current (hence stored energy) to the isolated output which is more heavily loaded. Energy is transferred to where it is needed most, at the load, and not to the control circuit. By varying the series inductance and preloading of each output, excellent regulation of the isolated output voltage can be achieved without requiring a separate feedback path.

An isolated version of the universal input range application circuit of Figure 10 was constructed and

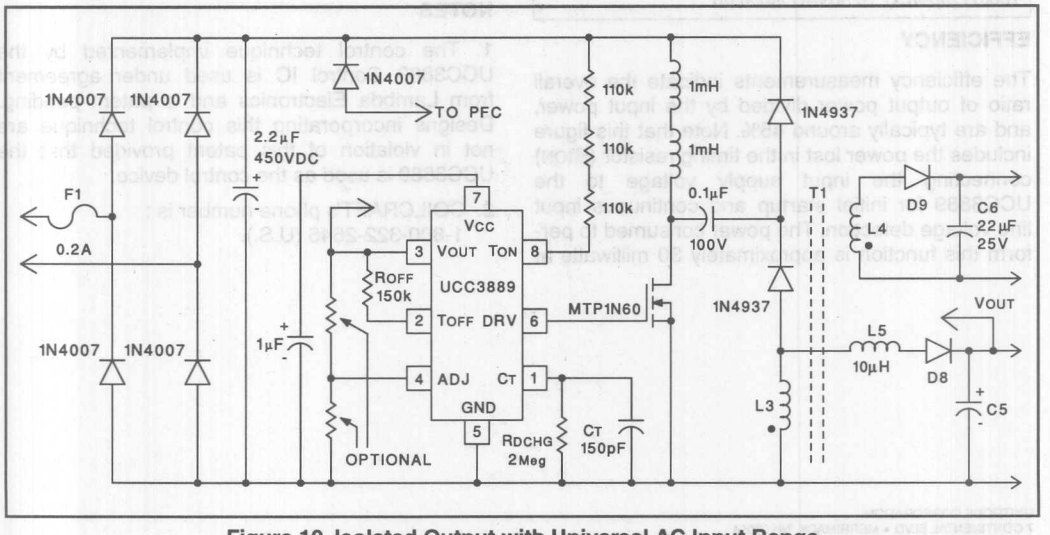


Figure 10. Isolated Output with Universal AC Input Range

tested. Performance results are shown below for comparison to the nonisolated version.

UCC3889 Application Circuit Performance Measurements

110/220 Universal AC Input with Isolated Output

VIN (VAC)	VNONISO (VDC)	VISO (VDC)	POUT (W)	EFFCY (approx)
78	12.37	12.07	0.41	45%
	12.31	11.85	0.63	46%
	12.26	11.63	0.82	47%
	12.26	11.33	0.99	51%
156	12.39	12.14	0.42	44%
	12.36	12.00	0.64	45%
	12.37	11.80	0.85	46%
	12.37	11.72	1.06	44%
195	12.42	11.77	0.39	43%
	12.39	11.59	0.60	44%
	12.36	11.33	0.78	44%
	12.33	11.42	1.00	45%
240	12.43	11.819	0.39	39%
	12.41	11.697	0.61	42%
	12.39	11.605	0.81	43%
	12.38	11.626	1.04	43%

Nonisolated VOUT nominal = 12.349V, ±0.7% (±85mV)
Isolated VOUT nominal = 11.74V, ±3.4% (±400mV)
Efficiency nominal = 45%
Main Transformer = COILCRAFT E3498A "Common Mode EMI Filter Choke", Turns Ratio = 1:1, Lp = Ls = 160µH (approx), 3750VAC Isolation

EFFICIENCY

The efficiency measurements indicate the overall ratio of output power divided by the input power, and are typically around 45%. Note that this figure includes the power lost in the timing resistor (RtON) connecting the input supply voltage to the UCC3889 for initial startup and continuous input line voltage detection. The power consumed to perform this function is approximately 30 milliwatts at low line, but nearly 400 milliwatts at high line. Once this loss is accounted for, the remaining losses demonstrate that this converter runs between 51% and 63% efficiency at high line, depending on load. It is clear that this cascaded flyback conversion technique is a highly efficient solution to low power applications, especially with a high voltage input.

OTHER APPLICATIONS

Although primarily designed for off-line applications, the UCC3889 Bias Supply Controller and the cascaded Flyback Conversion technique are equally applicable for low power DC/DC converters. Typical usages are to generate a bias supply for the main PWM controller, or to deliver a regulated, low power output supply. The simple implementation of this control technique is further applicable to numerous other topologies including conventional Flyback, Forward and other single switch converters.

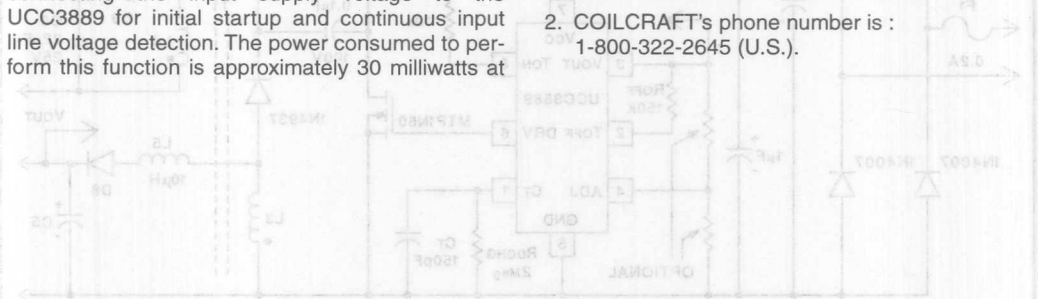
SUMMARY

The task of generating a low power, low voltage bias supply can be greatly simplified using this novel cascaded Flyback converter technique. Inexpensive, readily available standard components can be used in cost sensitive applications, while miniature surface mount devices are best suited where size is a premium. Furthermore, this approach can be utilized to generate an isolated low power supply without the complexity of voltage feedback circuitry. Finally, a sophisticated 8 pin IC, the UCC3889 Bias Supply Controller has been introduced to minimize external components while providing complete protection of the converter and regulation of the output voltage.

NOTES

1. The control technique implemented by the UCC3889 Control IC is used under agreement from Lambda Electronics and is patent pending. Designs incorporating this control technique are not in violation of this patent provided that the UCC3889 is used as the control device.

2. COILCRAFT's phone number is : 1-800-322-2645 (U.S.).



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APPLYING THE UCC3570 VOLTAGE-MODE PWM CONTROLLER TO BOTH OFF-LINE AND DC/DC CONVERTER DESIGNS

By Robert A. Mammano
Vice President
Advanced Technology

Abstract

BiCMOS processing provides the key to a new integrated PWM controller which offers higher switching frequencies at lower quiescent current drain while including new innovations in both performance and protection features. Its versatility is demonstrated with the description of a 50W, wide input voltage range, off-line inverter and a 48-to-5V isolated DC/DC converter, both of which feature efficiencies in the range of 80 percent.

INTRODUCTION

Over the years, our industry continues to see a steady evolution in power control technologies as new circuit topologies offer performance improvements over those achievable with older designs. For instance, current-mode control has become today's dominant control algorithm as its introduction brought such benefits as:

- Instant response to line variation
- Inherent pulse-by-pulse current limiting
- Faster loop response

These characteristics were quite significant when compared to the voltage-mode circuits built with the technology of the early 1980's when current-mode IC's were first introduced. However, both circuit design and IC process developments during the intervening years have shown that these capabilities are not necessarily limited to current-mode control. And along with the benefits of current-mode control have come several difficulties which have notably complicated the power supply designer's tasks. Among these are:

- Dealing with the current waveform's leading-edge spike
- Eliminating the effects of ringing or other noise sources
- Adding the appropriate amount of slope compensation
- Analyzing circuit performance with two feedback loops
- Providing good regulation with multiple outputs
- Stabilizing PWM operation with low amplitude ramp waveforms

Although solutions can and have been found for all the above issues, these difficulties have inspired a re-evaluation of voltage-mode control in the light of today's technology. In particular, it seemed desirable to incorporate some newer circuit concepts - such as voltage feed-forward, programmable duty-cycle limiting, and sophisticated fault protection - into a design which could also benefit from low-current BiCMOS processing. These circuit and process innovations have resulted in a new IC controller equally at home in wide voltage range off-line inverters and highly efficient isolated DC/DC converters.

INTRODUCING THE UCC3570

The overall block diagram for the UCC3570 is shown in Figure 1. While this architecture may look relatively complex, it is not because of the pulse-width modulation circuitry. Although this may be the heart of the controller, it is implemented with only the comparator, OR-gate, latch, and output driver shown across the center of the diagram. Since the UCC3570 is intended for isolated applications, there is no error amplifier, anticipating that this function will be on the opposite side of the isolation boundary.

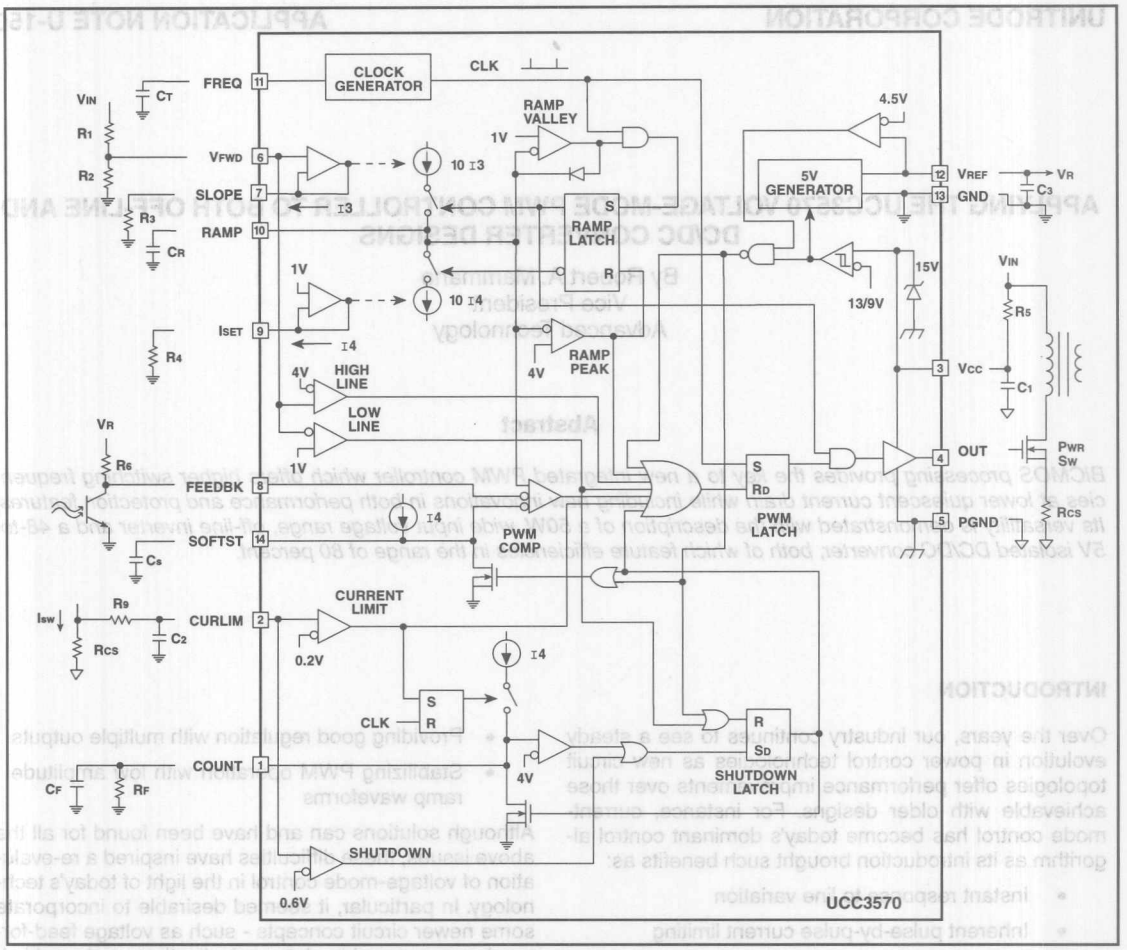


Figure 1. The overall block diagram of the UCC3570 showing connections to typical external components.

The emphasis given to programming and protection is indicated by the multiple-input OR-gate in the PWM path. This gate will terminate or prevent an output pulse if any of its inputs are high. The input signals to this gate are derived from the remainder of the circuitry. These other circuits can be divided into three sections which are described below: Ramp generation, Power sequencing, and Fault protection.

RAMP GENERATION CIRCUITRY

An important circuit feature incorporated into the design of the UCC3570 is a unique PWM ramp generator which combines voltage feed-forward, duty-cycle clamping, and fixed frequency operation. While all of these characteristics have individually been used before, combining them into a control which will automatically and linearly provide an open-loop PWM correction for large input voltage variations, and allow a maximum duty-cycle clamp to be user-set over a 20%-to-80% range, while maintaining constant switching frequency, was a challenge met with the circuitry shown separately in Figure 2.

The ramp voltage waveform is formed by charging an external capacitor with a current source made proportional to the input line voltage, and discharging it with a programmable current sink which determines the minimum deadtime. Switching between the charging and discharging currents is commanded by a flip-flop which is set with a constant-frequency clock signal, and reset when the ramp reaches four volts. To insure constant ramp amplitude, the bottom of the ramp is held at one volt while awaiting the clock command to start the next charge cycle. If the ramp discharge has not returned to one volt at the end of the period, the clock is blocked, forcing the circuit to wait through the next period before charging again by accepting the following clock signal.

These relationships are shown in Figure 3 which compares the ramp waveform with three different levels of input voltage.

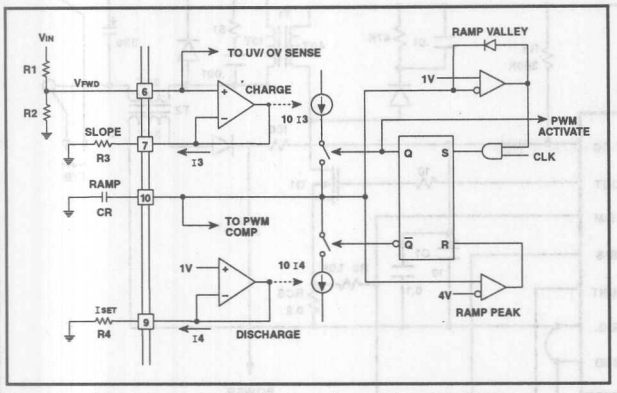


Figure 2. The ramp generation portion of the UCC3570 with independent rise-time, fall-time, and frequency control.

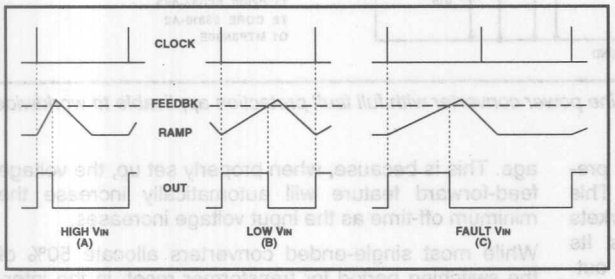


Figure 3. Effects of line voltage on the ramp waveform showing a variable slope rise, constant fall, and guaranteed minimum off-time.

PROGRAMMING AND PROTECTION

The power sequencing features of the UCC3570 are highly optimized for off-line operation beginning with the fact that the BiCMOS process yields very low operating currents for this device - one milliamp to run and less than 100 microamps prior to starting. In addition, there are two pins which sense the line voltage and provide turn-on/turn-off functions. Vcc provides chip power and has a UVLO circuit which sets turn-on at 13 volts with a 4-volt hysteresis. VFWD is primarily intended to provide voltage feed-forward by adjusting the ramp slope, but this pin is also monitored by over and under-voltage sensing comparators which terminate output pulses if the line voltage is outside its defined operating range. Because Vcc will normally require an energy storage capacitor, it will respond more slowly than VFWD and since both must be above a minimum for operation, turn-on will typically be initiated by Vcc while a collapsing voltage on VFWD will provide a faster turn-off. Turn-on is further controlled by a Soft-Start circuit which minimizes both starting currents and output voltage overshoot.

Another valuable circuit feature is an over-current fault protection technique which provides fast pulse-by-pulse current limiting with the ability to accept a definable period of over-current operation and then shut the system down if the fault is continuous. Referring again to Figure 1, the Current Limit pin is shown monitored by two comparators with thresholds of 0.2 and 0.6 volts. (It might be noted that noise filtering here has no impact on the feedback control loop as it would with current-mode control.) When the 0.2V threshold is exceeded, the output is commanded off within 100nsec. In addition, each time this occurs, an increment of charge is added to the capacitor on the COUNT pin and should the voltage on this pin rise to 4V, a Shutdown Latch is activated. This latch is also triggered immediately if the current limit signal crosses the 0.6V threshold. Reset of the Shutdown Latch occurs when either Vcc or VFWD falls below its lower threshold which allow a variety of options for either manual or automatic restart but, in either case, reset initiates a normal soft-start.

AN OFF-LINE APPLICATION

WARNING

Off-line AC power supplies are intrinsically hazardous!!!

The power supply described herein contains dangerous voltages!

Never allow human contact with any part of the input circuitry of any power supply, including the input ground connections, if it is not connected through an isolation transformer, whether the supply is turned on or off.

The supply described herein uses and can produce voltages which are potentially lethal! It should be serviced or tested only by experienced, qualified personnel, with proper techniques and equipment!

WARNING

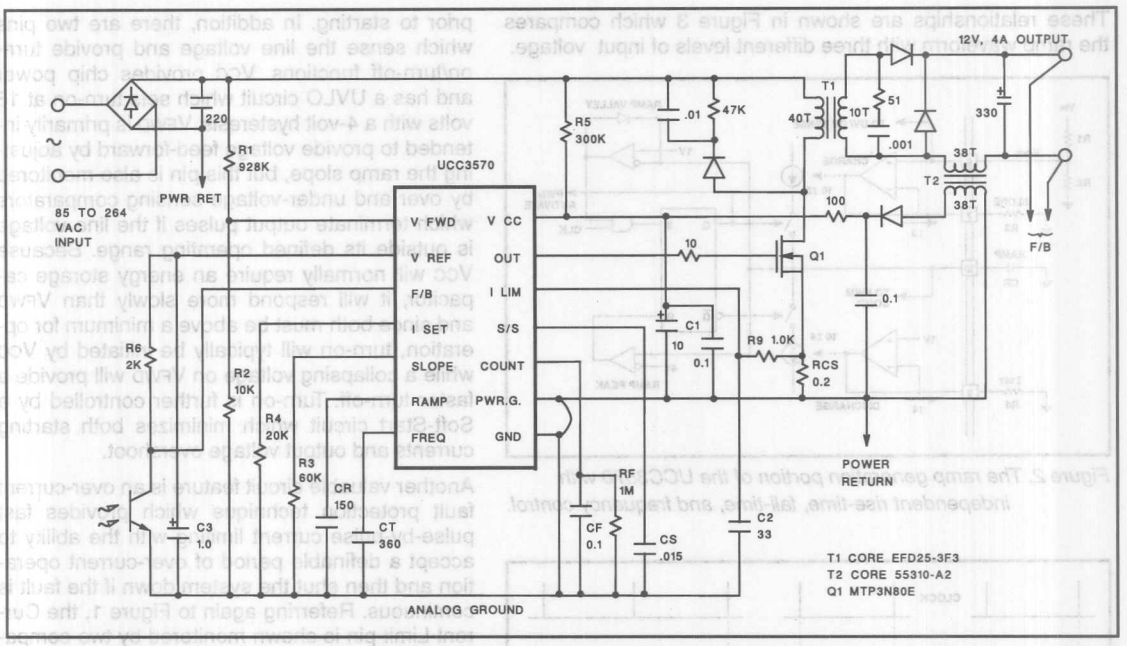


Figure 4. A simplified schematic for a 50 Watt, off-line power converter with full fault protection applicable to worldwide line voltages.

The 50 Watt off-line supply shown in Figure 4 is presented to illustrate a typical use for this controller. This application is intended for highly cost-sensitive markets requiring operation over world-wide line voltages. Its forward topology provides good regulation with low output ripple and it takes advantage of the low current requirement of the UCC3570 to allow simple interfacing to the high voltage line with minimal power loss. The switching frequency is 225kHz with the allowable duty-cycle range set to a maximum of 67% - a value which keeps the peak switch current low while still insuring a finite reset time for the transformer. The design steps which follow, while perhaps less rigorous than some might wish, should still provide a check list of items for the designer to consider when applying the UCC3570, regardless of the specific application.

TRANSFORMER RESET

In any single-ended power stage design, the plan for transformer reset is one of the first design decisions needed. In providing a power pulse to the output, the transformer is driven in one polarity for a finite number of volt-seconds. To prevent saturation, the same number of volt-seconds must be provided in the opposite polarity between the termination of one power pulse and the beginning of the next one. Since it is the volt-second product which must be met, many compromises can be made between the amount of reset voltage allowed and the time allocated. The UCC3570 simplifies this analysis to the extent that the worst case situation will always be at the lowest operating voltage. This is because, when properly set up, the voltage feed-forward feature will automatically increase the minimum off-time as the input voltage increases.

While most single-ended converters allocate 50% of the switching period for transformer reset, in the interests of allowing a lower peak input current, the maximum duty-cycle for this application was extended to 67%, allowing only one-third of the period for reset. This precluded using a reset winding on the power transformer with a 1-to-1 turns ratio. While a higher turns ratio could have been used, that would have offered the choice of either recycling the reset energy to the source and thereby requiring a much higher voltage power switch, or wasting all the reset energy in a lower voltage clamping circuit.

Since neither choice was particularly attractive - and to save the cost of a separate reset winding on the transformer - the solution for this design was to use an R-C-D snubber for reset. This passive resistor-capacitor-diode network will generate a variable clamp voltage - high at minimum V_{IN} since the capacitor has less time when it is not charging, and lower at high V_{IN} since the shorter on-time provides more discharge time for the capacitor. An obvious benefit of this solution is simplicity - only three passive components and no reset winding on the transformer. The disadvantage is that there is some reset energy lost in the resistor but in this case it was only approximately 0.5W. Using this R-C-D clamp allowed setting the maximum duty cycle at 67% at low line, while still clamping the maximum drain voltage of

the switch to 500 volts under high line conditions. These drain voltage waveforms are shown in Figure 5.

TRANSFORMER DESIGN

Since this power supply is intended for world-wide op-

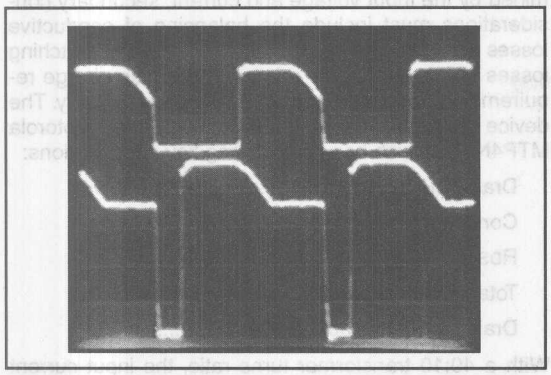


Figure 5. FET drain voltage at full load with VIN = 85 VAC (top trace) and VIN = 264 VAC (lower trace) V = 100V/div, H = 1.0µs/div.

eration, the line voltage range was established as 85-264 VAC. This means the peak rectified DC input voltage could be assumed to range from 120 to 373 VDC, but allowing 25 volts of ripple at low line brings the lower limit down to 95 volts. With a switching frequency of 225kHz, the maximum on-time would be 67% of 4.44µsec, or 2.9µsec at the lowest input voltage.

For reasons of cost and size, a Philips EFD-25 ferrite core (3F3 material) was selected through an iterative process of determining a flux swing from the high-frequency core loss characteristics of an assumed core size, using Faraday's law to calculate the number of turns, and then verifying that these turns would fit onto that core size. The EFD-25 core structure is shown in Figure 6 and its size yields a core area of 0.58cm^2 and a volume of 3.3cm^3. If the flux swing is less than

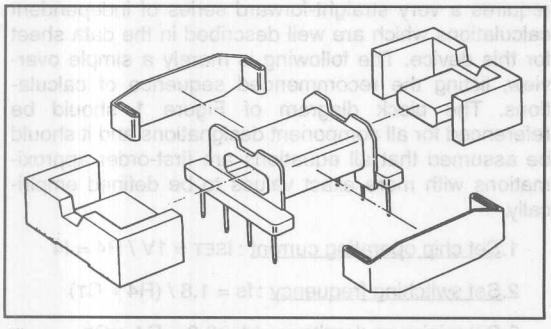


Figure 6. The Philips EFD core assembly optimized for low board profile.

1.25kG at 225kHz, the core loss should be less than 0.25 Watt. The number of turns are calculated from

$$V_{IN} = \frac{N \Delta B Ae}{T_{ON}\, 10^8} \quad \text{or}$$

$$N = \frac{95V \bullet 2.9\mu s \bullet 10^8}{1250G \bullet 0.58cm^2} = 38t$$

which was rounded up to 40 turns.

The number of secondary turns is calculated from

$$Vo = [V_{IN} \bullet \frac{Nsec}{Npri} - Rect\ drop] \bullet Duty\ Cycle, \text{ or}$$

$$12 = [95 \bullet \frac{Nsec}{40} - 1.0V]\ 0.67, \text{ which yields}$$

Nsec = 8 turns. (10 turns was used in this example to provide added operating margin.)

The final transformer design, which is illustrated in Figure 7, incorporated 40 turns of #24 wire wound in two sections to sandwich the secondary, which consisted of 10 turns of four strands of #26 wire. The DC resistance of the primary calculated 0.16 Ohm while the secondary amounted to 0.016 Ohm. Using these values and the core loss curves, the total power loss was calculated as:

Primary loss	=	153mW
Secondary loss	=	243mW
Core loss	=	165mW
Total loss	=	561mW

which, in consideration of the transformer's volume of approximately four cm^3, should experience a maximum temperature rise of less than 20°C.

OUTPUT INDUCTOR DESIGN

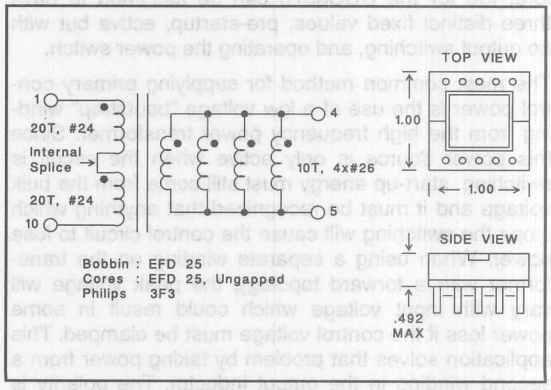


Figure 7. Power transformer schematic and physical dimensions.

The output inductor must be designed to handle the maximum DC load current without saturating while maintaining continuous conduction at the minimum load. This minimum load was arbitrarily set at 5% of the full 4 Amp load. The worst-case light-load condition occurs at high line where the duty-cycle is calculated to be 0.13 which gives an off-time of 3.9µsec. The minimum value of inductance can then be calculated as

$$L = V\ dt/di,\ or\ \frac{13V \bullet 3.9\mu s}{0.4A} = 127\mu H$$

The number of turns is calculated from the core characteristics, picking a core large enough to retain adequate inductance at maximum load. In this case, these goals were met with a Mag Inc toroidal 55310-A2 core and 38 turns of #20 wire. Since the control bootstrap voltage and the output can be equal in this case, a second 38 turns of #34 wire powers the control circuit. Power lost in the inductor is calculated as 92mW in the core and 630mW in the wire resistance for a total of approximately 0.75 Watt.

CONTROL CIRCUIT POWER

Another early question to be answered in the design of an off-line power supply is the method used to power the control circuit. Two obvious possibilities are often ruled out: using a separate 60Hz step-down transformer is costly overhead in a low power application; and powering the primary circuitry directly from the high bulk voltage will require a series dropping resistor whose power dissipation is usually unacceptable. While BiCMOS control circuits require very little quiescent current, the determining factor is now usually the power MOSFET gate drive energy. The average gate current for a power MOSFET can be approximated by

$$Ig(ave) = Qt \bullet f$$

where Qt is the total gate charge and f is the switching frequency. Note that this current is relatively unaffected by input voltage, duty-cycle, or output loading. Therefore, Icc for the UCC3570 can be assumed to have three distinct fixed values: pre-startup, active but with no output switching, and operating the power switch.

The most common method for supplying primary control power is the use of a low voltage "bootstrap" winding from the high frequency power transformer. Since this power source is only active when the circuit is switching, start-up energy must still come from the bulk voltage and it must be recognized that anything which stops the switching will cause the control circuit to lose power. When using a separate winding on the transformer with a forward topology, the peak voltage will vary with input voltage which could result in some power loss if the control voltage must be clamped. This application solves that problem by taking power from a second winding in the output inductor. The polarity is such that this winding conducts during flyback when it has the output voltage (times the turns ratio) across it.

POWER MOSFET SELECTION

While the choice of power switch is primarily determined by the input voltage and current, secondary considerations must include the balancing of conductive losses - determined by $R_{DS(on)}$ - against the switching losses which are largely related to the gate charge requirements and the capability of the drive circuitry. The device selected for this supply is the Motorola MTP4N80E which has the following key specifications:

Drain-source voltage.....800 Volts

Continuous drain current .....3 Amps

$R_{DS(on)}$ at 25°C.....1.95 Typ, 3.0 Max Ohms

Total gate charge .....36 Typ, 80 Max nC

Drain-source capacitance 200pF

With a 40:10 transformer turns ratio, the input current will be approximately one Amp. The conductive loss is calculated from the input current (adding a factor to account for less than 100% efficiency), the drain-source resistance (accounting for its positive temperature coefficient), and the maximum duty cycle.

The switching losses are best determined empirically but they can be estimated with a knowledge of the switching times, calculated from the total gate charge divided by the peak gate current. These times are typically less than 50nsec since the UCC3570 can deliver up to one Amp of gate current.

In this design, the total power loss estimates for the MOSFET are

Conductive loss..... 2.0 Watts

Switching losses ..... 4.7 Watts

With a total of 6.7W, this device will have the highest dissipation within the supply and heatsinking the TO-220 package will be required.

UCC3570 PROGRAMMING

Establishing the operating parameters for the UCC3570 requires a very straight-forward series of independent calculations which are well described in the data sheet for this device. The following is merely a simple overview, listing the recommended sequence of calculations. The block diagram of Figure 1 should be referenced for all component designations and it should be assumed that all equations are first-order approximations with more exact values to be defined empirically.

1. Set chip operating current : $I_{SET} = 1V / R4 = I4$

2. Set switching frequency : $fs = 1.8 / (R4 \bullet C_T)$

3. Set minimum deadtime : $td = 0.3 \bullet R4 \bullet C_R$

4.Set feed-forward range : The UCC3570 establishes this range as 4:1 by the 4V and 1V limits set for V_{FWD}. Therefore,

$V_{IN}(Max) = 4 \bullet (R1 + R2) / R2$, and

$V_{IN}(Min) = 1 \bullet (R1 + R2) / R2$.

Note that if a greater range is required, or a voltage range different from that of the duty cycle, it can be accommodated by raising R2 and R3 off ground by a small bias voltage, $0 < Vb < 1V$, or by using the equivalent circuit shown in Figure 8.

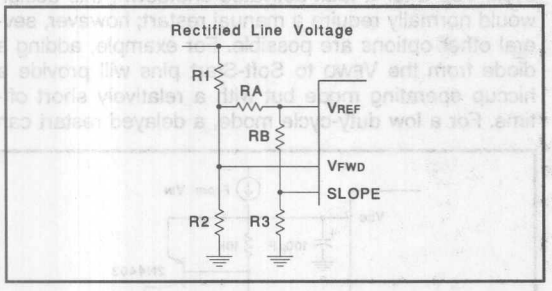


Figure 8. Modifying the 4:1 the input voltage ratio. RA works with R2 to increase the voltage range and RB works with R3 to change the feed-forward gain.

5.Set feed-forward slope : The up-slope of the ramp waveform is

$$dV / dt = 10 \bullet V_{FWD} / (R3 \bullet C_R).$$

This can be used to define

$t_{ON}(Max) = 0.3 \bullet R3 \bullet C_R / 1V$, and

$t_{ON}(Min) = 0.3 \bullet R3 \bullet C_R / 4V$.

6.Set current fault parameters : The value for the current sensing resistor is established by the 200mV threshold for the CURLIM pin. Shutdown will occur when the circuit is operating in current limit mode for a time determined by

$$\text{Time to S/D} = 4V \bullet C_F \bullet R4 \bullet (T / t_{OFF})$$

Note that this time will be extended by the current which is drained away from C_F by the action of R_F.

The total schematic and parts list for this application are given in Appendix A (see page 10) and some representative waveform photographs of its performance are shown in Figures 9 through 12. While this converter design could find many practical applications as shown, many additional options are possible. For example, reducing the value of the start-up resistor (R5 in Figure 1) such that V_{CC} will not fall below 9 volts after shutdown interrupts the bootstrap voltage, will provide a positive latch-off from a fault. Output over-voltage shutdown can easily be added by a sensing circuit on the secondary driving the COUNT pin through a second optocoupler. And, of course, it should be easy to reconfigure this design to further optimize efficiency, size, cost, or power level to meet a different set of priorities.

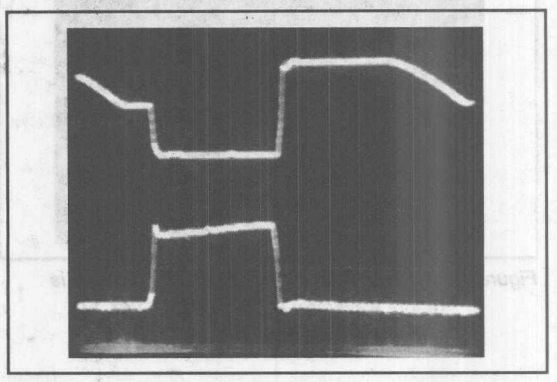


Figure 9. Drain voltage and current at 115VAC and full load. V1 = 100V/div, V2 = 0.5A/div, H = 0.5µsec/div.

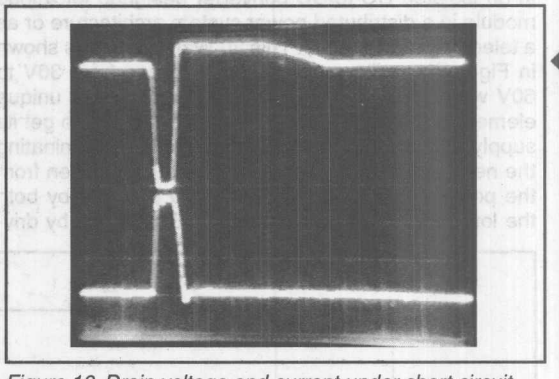


Figure 10. Drain voltage and current under short circuit conditions at 264VAC input. V1 = 100V/div, V2 = 0.5A/div, H= 0.5µsec/div.

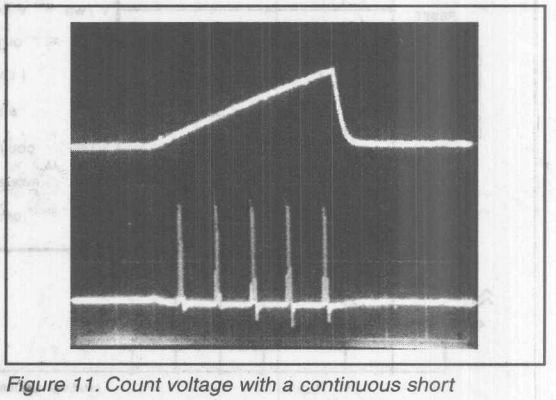


Figure 11. Count voltage with a continuous short circuit (current waveform is aliased) V = 2V/div, H = 2msec/div.

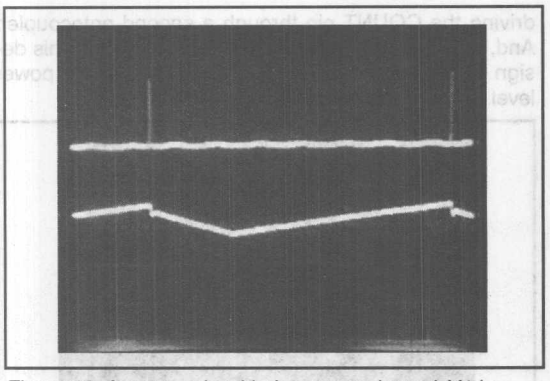


Figure 12. Auto recycle with the output shorted. V1 is count waveform at 2V/div, V2 is VCC at 5V/div, H = 0.2 seconds/div.

A SIMPLE DC/DC CONVERTER

A second application for the UCC3570 illustrates its use in an isolated DC-to-DC converter designed for a load module in a distributed power system architecture or as a telecom power source. This 20 Watt design, as shown in Figure 13, will accept an input voltage from 30V to 60V while maintaining a constant 5V output. A unique element of this design is the controller's ability to get its supply current from only the input voltage, eliminating the need for a low-voltage bootstrap supply driven from the power transformer. This is made practical by both the low operating current of the UCC3570 and by driving a low-gate charge FET at less than maximum frequency. The IRF630 has a total gate charge requirement of only 30nC maximum which, at 100kHz, means only 3mA of average gate current. Add 1mA for the IC, another for miscellaneous programming resistors, and 5mA is all that is needed for the total primary circuitry. This can readily be taken directly from the input voltage but, for improved efficiency, a simple current source has been added to keep this current constant with changing input voltage levels.

Without a bootstrap voltage source to collapse and recycle Vcc after a fault-activated shutdown, this design would normally require a manual restart; however, several other options are possible. For example, adding a diode from the VFWD to Soft-Start pins will provide a hiccup operating mode but with a relatively short off-time. For a low duty-cycle mode, a delayed restart can

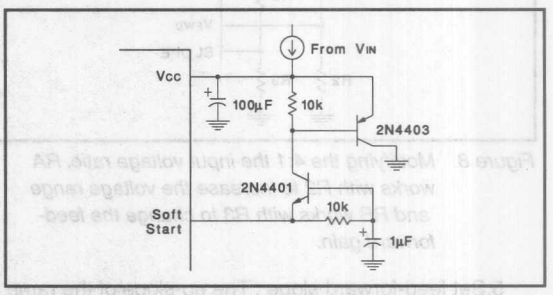


Figure 14. Two transistors will provide an external auto-restart by recycling VCC when Soft-Start is reset.

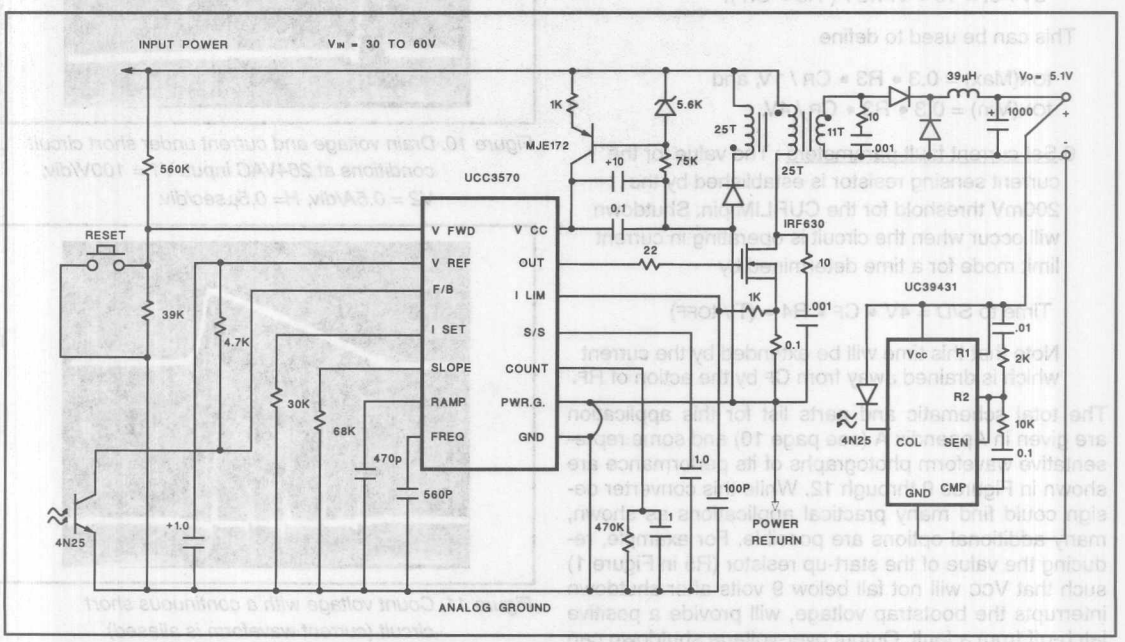


Figure 13. An isolated 25W, 48V to 5V converter including the UC39431 as an optocoupled feedback generator.

be accomplished with the two-transistor circuit shown in Figure 14. This circuit uses the energy in the soft-start capacitor to discharge the Vcc capacitor which gives a turn-on delay equivalent to normal start up. The operation of this circuit is illustrated in Figure 15.

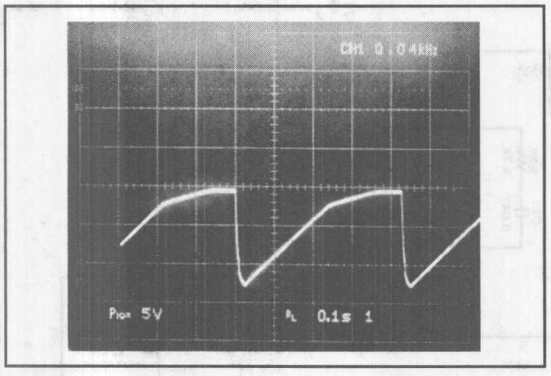


Figure 15. With auto re-start, a shorted output recycles VCC with a 0.4 second delay.

Another option for eliminating a latched shutdown is to simply short the COUNT pin to ground which will prevent activation of the Shutdown Latch unless the Current Limit threshold of 600mV is exceeded - an unlikely event considering the 80nsec response of the pulse-by-pulse current protection. Figure 16 shows operation in this mode with a continuous shorted output.

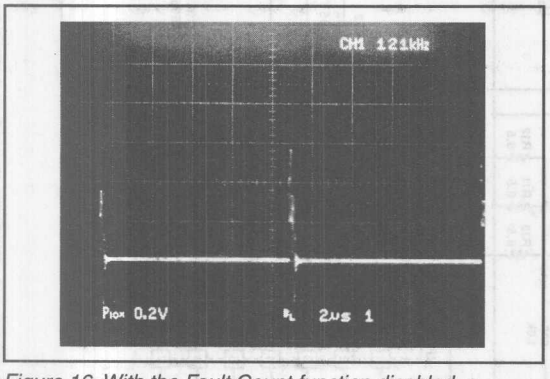


Figure 16. With the Fault Count function disabled, a shorted output reduces the current pulse width such that the peak across RCS remains below shutdown threshold.

This converter design illustrates another characteristic of the UCC3570 which provides both added safety and better utilization of the transformer magnetics. With an input voltage range specified as 30 to 60 Volts, If the OV clamp is set for 60V, the controller will continue to operate down to 15V (1/4 of 60V). However, if the maximum duty-cycle clamp is set for 50% at 30V, the ramp waveform will cause the output to skip pulses at voltages less than 30V insuring against saturation of the power transformer.

The rest of the circuit details for this application can be deduced from the information presented above and the complete schematic and parts list given in Appendix B (see page 12).

SUMMARY

With the minimal need for additional external components and support functions which these two quite different applications have shown, the versatility of the UCC3570 has been demonstrated. Not shown, but equally important is this device's ability to provide the same protection and programmability with power stages scaled up to several hundred Watts, and to efficiently operate at switching frequencies above 500kHz. Thus, once again it has been demonstrated that one can never close the door to "older" technologies and, in this case, revisiting voltage-mode control has yielded a new controller combining efficient operation, stable performance, and ease of application highly attuned to meeting today's stringent requirements for cost-effective power systems.

REFERENCES

Leu, Hua, Lee, and Zhou, "Analysis and Design of R-C-D Clamp Forward Converter" VPEC, Virginia Tech and Delta Power Electronics Lab, Blacksburg, VA.

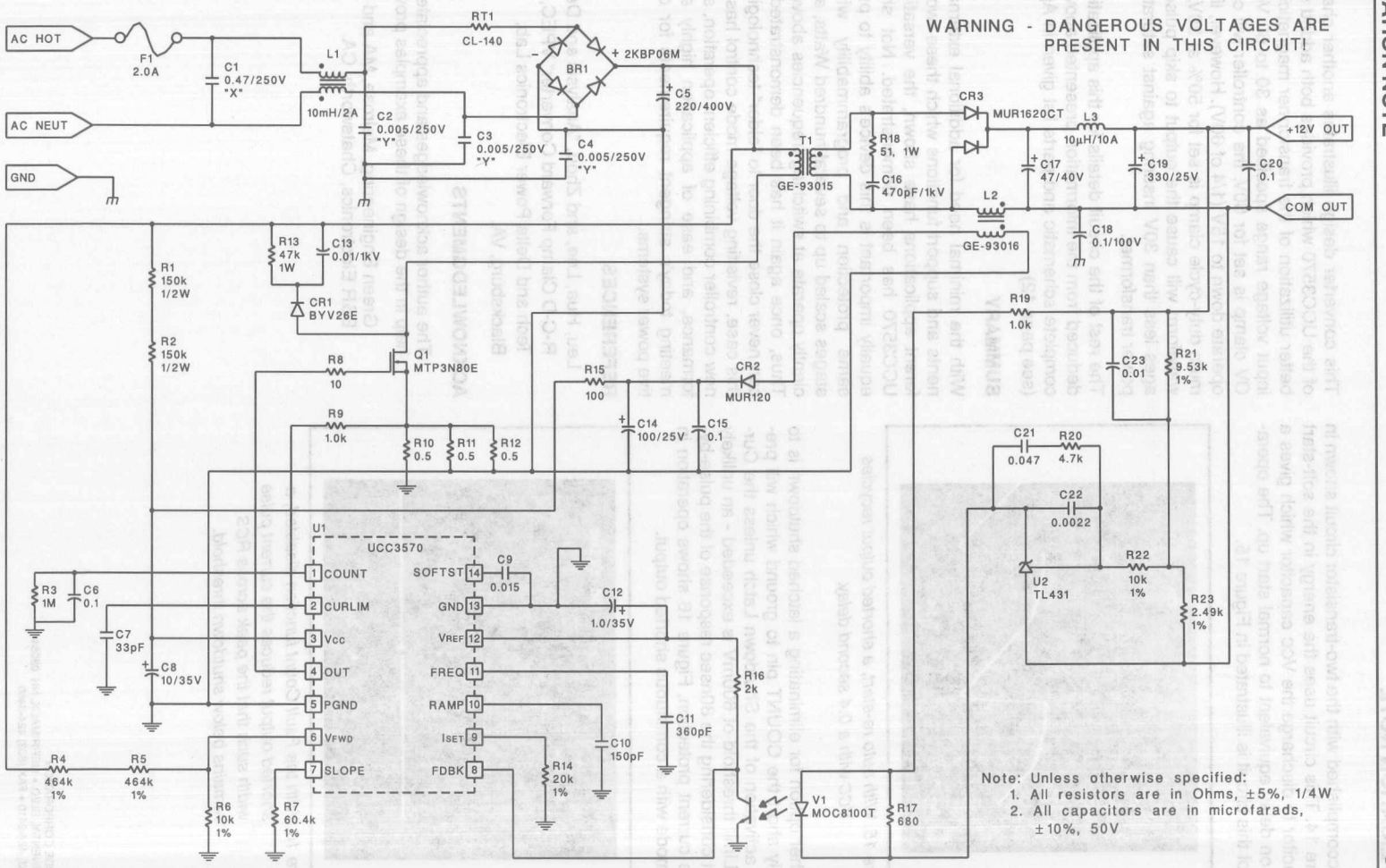
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APPENDIX - A
12 VOLT, 50 WATT POWER SUPPLY

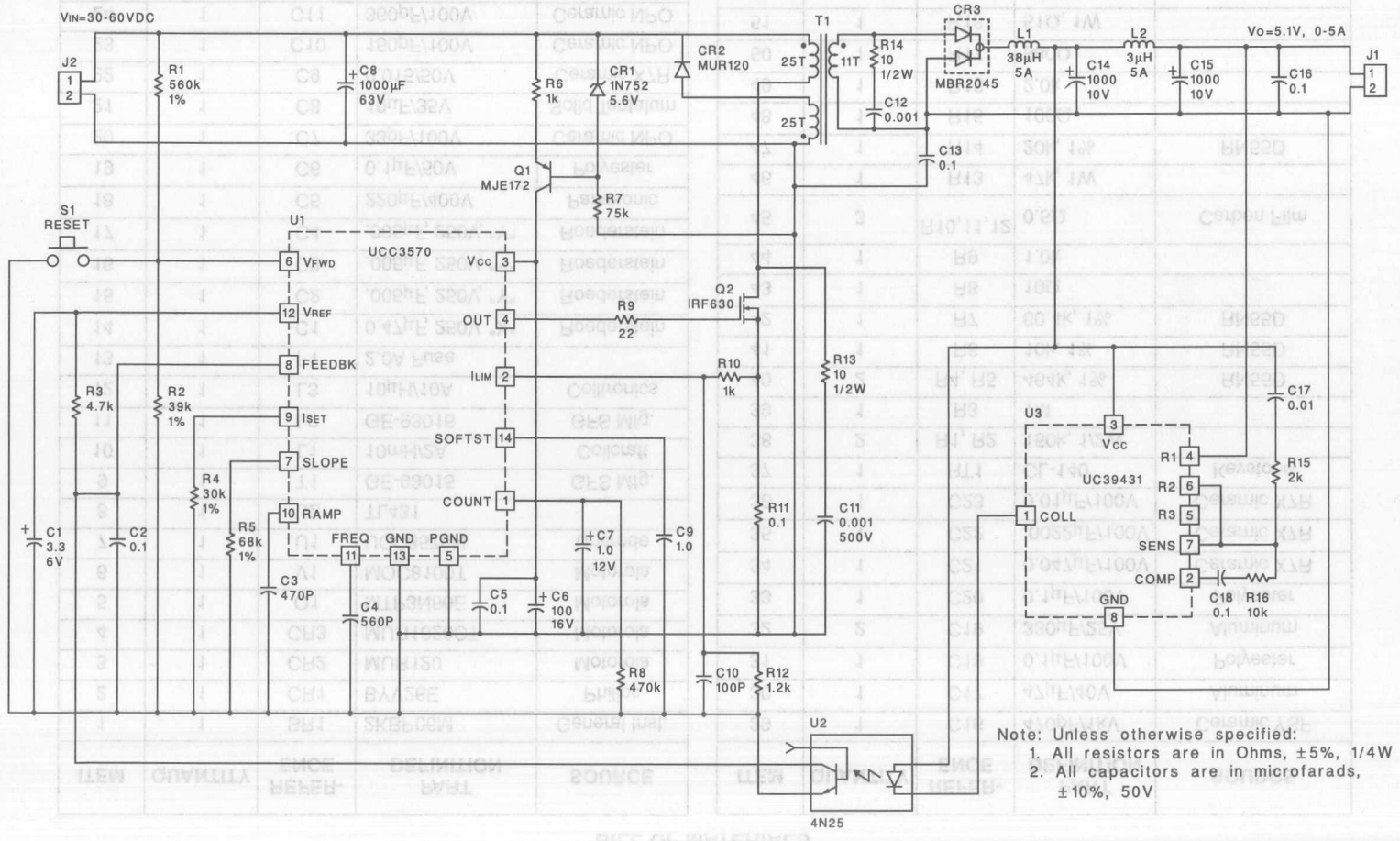


12 VOLT, 50 WATT POWER SUPPLY
BILL OF MATERIALS

ITEM	QUANTITY	REFER-ENCE	PART DEFINITION	SOURCE
1	1	BR1	2KBP06M	General Inst.
2	1	CR1	BYV26E	Philips
3	1	CR2	MUR120	Motorola
4	1	CR3	MUR1620CT	Motorola
5	1	Q1	MTP3N80E	Motorola
6	1	V1	MOC8100T	Motorola
7	1	U1	UCC3570N	Unitrode
8	1	U2	TL431	
9	1	T1	GE-93015	GFS Mfg.
10	1	L1	10mH/2A	Coilcraft
11	1	L2	GE-93016	GFS Mfg.
12	1	L3	10µH/10A	Coiltronics
13	1	F1	2.0A Fuse	
14	1	C1	0.47µF, 250V, "X"	Roederstein
15	1	C2	.005µF, 250V, "Y"	Roederstein
16	1	C3	.005µF, 250V, "Y"	Roederstein
17	1	C4	.005µF, 250V, "Y"	Roederstein
18	1	C5	220µF/400V	Panasonic
19	1	C6	0.1µF/50V	Polyester
20	1	C7	33pF/100V	Ceramic NPO
21	1	C8	10µF/35V	Solid Tantalum
22	1	C9	0.015/50V	Ceramic X7R
23	1	C10	150pF/100V	Ceramic NPO
24	1	C11	360pF/100V	Ceramic NPO
25	1	C12	1.0µF/35V	Solid Tantalum
26	1	C13	0.01µF/1kV	Ceramic X5F
27	1	C14	100µF/25V	Aluminum
28	1	C15	0.1µF/100V	Polyester

ITEM	QUANTITY	REFER-ENCE	PART DEFINITION	SOURCE
29	1	C16	470pF/1kV	Ceramic YSF
30	1	C17	47µF/40V	Aluminum
31	1	C18	0.1µF/100V	Polyester
32	2	C19	330µF/25V	Aluminum
33	1	C20	0.1µF/100V	Polyester
34	1	C21	0.047µF/100V	Ceramic X7R
35	1	C22	.0022µF/100V	Ceramic X7R
36	1	C23	0.01µF/100V	Ceramic X7R
37	1	RT1	CL-140	Keystone
38	2	R1, R2	150k, 1/2W	
39	1	R3	1M	
40	2	R4, R5	464k, 1%	RN55D
41	1	R6	10k, 1%	RN55D
42	1	R7	60.4k, 1%	RN55D
43	1	R8	10Ω	
44	1	R9	1.0k	
45	3	R10,11,12	0.5Ω	Carbon Film
46	1	R13	47k, 1W	
47	1	R14	20k, 1%	RN55D
48	1	R15	100Ω	
49	1	R16	2.0k	
50	1	R17	680Ω	
51	1	R18	51Ω, 1W	
52	1	R19	1.0k	
53	1	R20	4.7k	
54	1	R21	9.53k, 1%	RN55D
55	1	R22	10k, 1%	RN55D

APPENDIX - B
48V - 5V, 20W DC/DC CONVERTER



Note: Unless otherwise specified:
1. All resistors are in Ohms, ±5%, 1/4W
2. All capacitors are in microfarads, ±10%, 50V

48V - 5V, 20W DC/DC CONVERTER
BILL OF MATERIALS

ITEM	QUANTITY	REFERENCE	PART DEFINITION	SOURCE
1	1	CR1	1N752, 5.6V	
2	1	CR2	MUR120	Motorola
3	1	CR3	MBR2045	Motorola
4	1	Q1	MJE172	Motorola
5	1	Q2	IRF630	Int. Rect.
6	1	U1	UCC3570	Unitrode
7	1	U2	4N25	
8	1	U3	UC39431	Unitrode
9	1	T1	Transformer	Custom
10	1	L1	38µH, 5A	Custom
11	1	L2	3µH, 5A	Toko
12	1	C1	3.3µF, 6V	Solid Tantalum
13	4	C2, 5, 16, 18	0.1	
14	1	C3	470pF	
15	1	C4	560pF	
16	1	C6	100µF, 16V	Solid Tantalum
17	1	C7	1.0µF, 12V	Solid Tantalum
18	1	C8	1000µF, 63V	
19	1	C9	1.0µF	
20	1	C10	100pF	

ITEM	QUANTITY	REFERENCE	PART DEFINITION	SOURCE
21	1	C11	.001µF, 500V	
22	1	C12	.001µF	
23	1	C13	0.1µF, 100V	
24	2	C14, 15	1000µF, 10V	
25	1	C17	.01µF	
26	1	R1	560k, 1%	
27	1	R2	39k, 1%	
28	1	R3	4.7k	
29	1	R4	30k,1%	
30	1	R5	68k, 1%	
31	1	R6	1.0k	
32	1	R7	75k	
33	1	R8	470k	
34	1	R9	22Ω	
35	1	R10	1.0k	
36	1	R11	0.1Ω	
37	1	R12	1.2k	
38	2	R13, 14	10Ω, 1/2W	
39	1	R15	2k	
40	1	R16	10k	

Magnetics Winding Information

T1:
Core: EI187-3C80 (Philips)
Primary: 25 Turns Bifilar = 26AWG
Reset: 25 Turns = 31AWG (Wound with Primary)
Secondary: 11 Turns Quadfilar = 25AWG

L1:
Core: T68-52D (Micrometals)
Winding: 21 Turns = 20AWG

L2:
Toko 262LYF-0077M

UCC3912 INTEGRATED ELECTRONIC CIRCUIT BREAKER IC FOR HOT-SWAP AND POWER MANAGEMENT APPLICATIONS

by Dave Zendzian
Applications Engineer

ABSTRACT

This application note describes the design and performance characteristics of the UCC3912 Electronic Circuit Breaker. The practical aspects of applying the circuit breaker are discussed as well as its performance compared to existing technologies. The UCC3912 integrates a power MOSFET with all of the necessary control and housekeeping functions including current limiting, short circuit protection, and auto recovery capabilities. The performance of the circuit breaker is compared to PolySwitches® and conventional fuses in both hot swap and short circuit applications.

INTRODUCTION

Today's design engineers are faced with a variety of choices when selecting protection devices to meet their circuit or system's design requirements. Fuses, positive temperature coefficient (PTC) resistors, and electromechanical circuit breakers represent only a sampling of the technologies available to meet their needs. Each of these devices provides a different degree of security, ranging from simple short circuit protection to devices which offer active current limiting and remotely resettable operation.

Fuses, while providing an inexpensive solution, fall short of many of the protection requirements imposed on modern electronic equipment. Figure 1 illustrates the protection capability of two general fuse categories; fast-acting and slow-blow. Although both devices provide gross short circuit protection, even the fastest devices react on the order of milliseconds, passing currents up to 500% of their rated value. In addition, fuses, by their very nature, have to be physically replaced following an overload condition. This increases the equipment's down time along with the chance of an incorrect device being installed, thereby reducing overall system reliability.

PTC resistors, on the other hand, eliminate the need for human intervention by providing resettable overcurrent protection. However, because they are actuated by the heating effect of an overcurrent load, their reaction time is limited to several milliseconds. This results in output currents several times their steady state rating. Figure 2 illustrates typical "time to trip" data for polymeric PTC resistors.

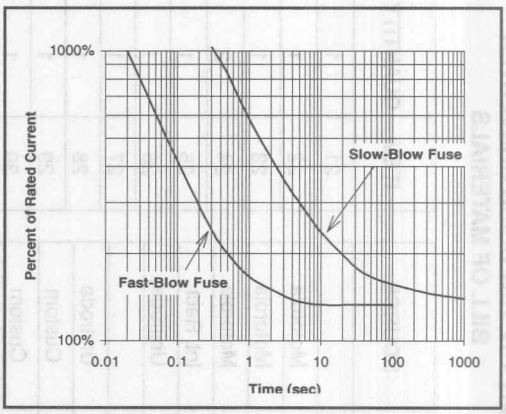


Figure 1. Relation of Percent of Rated Current to Fuse Blowing Time.

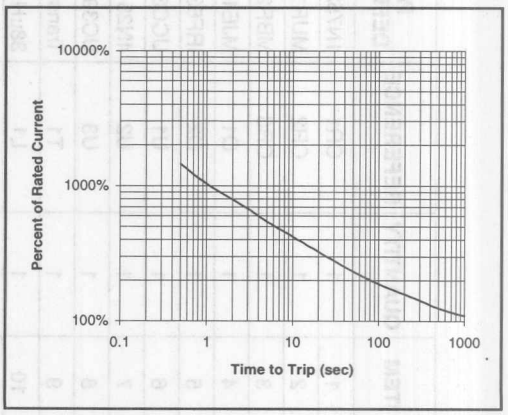


Figure 2. Relation of Percent of Rated Current to Blowing Time.

The UCC3912 Electronic Circuit Breaker offers a new, integrated solution to the problem of circuit protection and power management. Each of the drawbacks associated with existing technologies are addressed in the UCC3912 design. In addition, the UCC3912 provides logic level load control for power management applications. This note describes the features and performance of the UCC3912 as compared to other available protection techniques. In particular, hot swap, power management, and short circuit protection applications are addressed in detail.

HOT SWAPPING

The term hot swap refers to the system requirement that submodules be swapped out upon failure or system modification without removing power to the hardware. Design of modern computer systems, disk arrays, network hubs and communication switches require modules to be hot swapped while maintaining the integrity of the powered and operating system. This requirement allows the hardware to maintain operation, increasing the system's performance and reliability.

Implementing the hot swap requirement imposes several design constraints upon the equipment's power system. In order for the hardware to maintain error free operation during the installation or removal of a submodule, the 5 volt power bus must not drop below a minimum voltage of 4.5V. Voltages below 4.5V can disrupt logic levels, causing an indeterminate number of failures including data corruption and logic lockups. This ultimately reduces system reliability and data integrity.

The potential for glitching the power bus exists whenever an unpowered module is inserted into an operational system. Virtually all modules possess some amount of onboard bus capacitance which serves to filter and maintain power quality once the board becomes operational. However, these very same capacitors require an initial charging current in order to bring their voltage up to the same level as the system's power supply. The only factors limiting the magnitude of this current is the equivalent series resistance (ESR) of the capacitors themselves and the impedance of the interconnect between the module and the rest of the system. Unfortunately, the better the capacitors are at serving their purpose of filtering the bus, the lower their ESR. As a result, the initial inrush current during the hot swap can become excessively high.

Figure 3 illustrates the inrush current and corresponding voltage glitch when a load of 2A and 120µF is switched onto a 5V power bus. The 120µF of load capacitance consisted of a solid tantalum, surface mount style capacitor (Sprague #595D127X9020R2T) with a typical ESR of 0.25Ω at 100kHz. The power bus was bypassed with 240µF of the same style capacitor. As the figure illustrates, the inrush current reaches a maximum value of approximately 27A, resulting in a 1V glitch on the power bus. This exceeds the 4.5V limit by 500mV causing the supply to drop to 4.0V! In addition to causing the voltage glitch, the excessive inrush current can also result in arcing between connector pins and excessive heating of the load capacitance. Each of these effects shortens the life of the component, ultimately reducing system reliability.

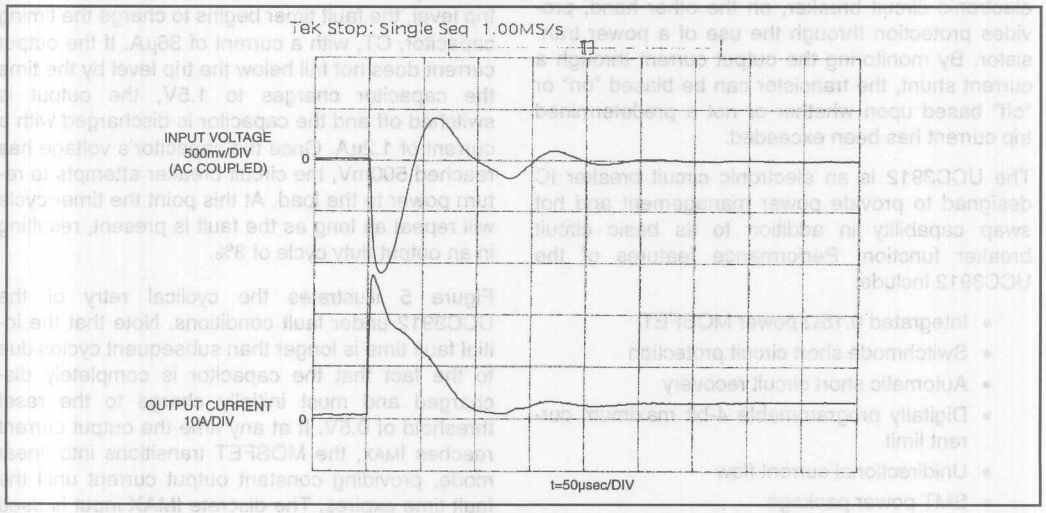


Figure 3. Inrush Current and Corresponding Voltage Glitch for a 2A, 120µF Load.

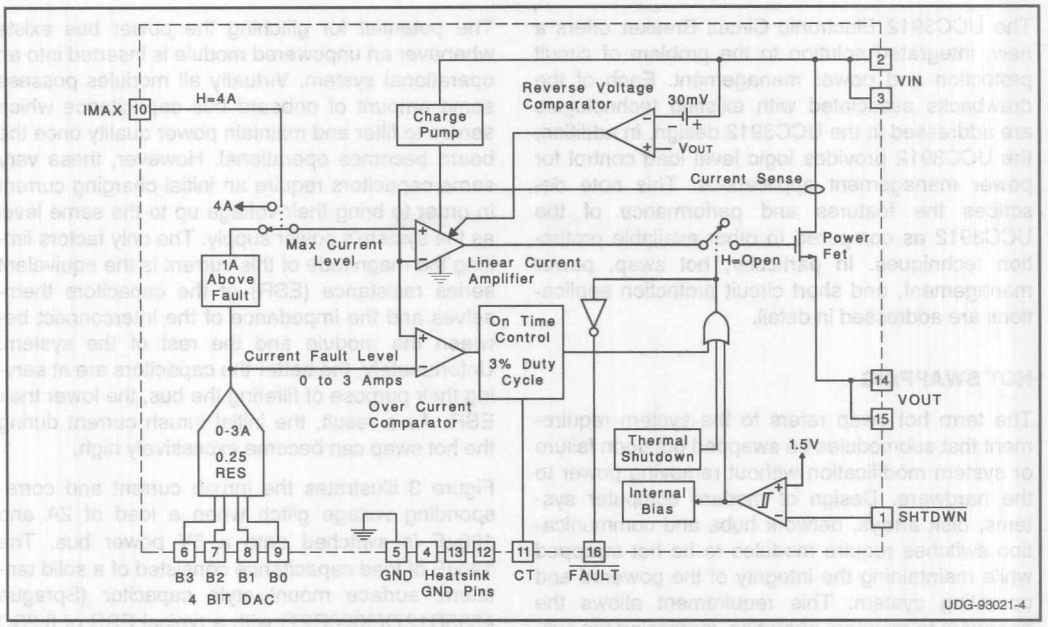


Figure 4. UCC3912 Electronic Circuit Breaker Block Diagram

THE UCC3912 ELECTRONIC CIRCUIT BREAKER

In its most rudimentary form, a circuit breaker, whether electromechanical or electronic, protects a circuit from excessive current flow. Electromechanical devices accomplish this by opening a set of contacts when the current exceeds a specified level. These types of breakers usually latch off during a fault and therefore need to be manually reset once the current falls below a reasonable value. An electronic circuit breaker, on the other hand, provides protection through the use of a power transistor. By monitoring the output current through a current shunt, the transistor can be biased "on" or "off" based upon whether or not a predetermined trip current has been exceeded.

The UCC3912 is an electronic circuit breaker IC designed to provide power management and hot swap capability in addition to its basic circuit breaker function. Performance features of the UCC3912 include:

- Integrated 0.15Ω power MOSFET
- Switchmode short circuit protection
- Automatic short circuit recovery
- Digitally programmable 4-bit maximum current limit
- Unidirectional current flow
- SMT power package
- Fault indicator output
- Low power "sleep" mode
- Thermal shutdown
- Low part count implementation

The block diagram of the UCC3912 is shown in Figure 4. Under normal operating conditions the integrated N-channel MOSFET is biased "on" using the internal charge pump to drive the gate. Output current is sensed using a mirrored MOSFET and is compared to an adjustable trip level set by the 4-bit DAC input. When the output current exceeds the trip level, the fault timer begins to charge the timing capacitor, CT, with a current of 36μA. If the output current does not fall below the trip level by the time the capacitor charges to 1.5V, the output is switched off and the capacitor is discharged with a current of 1.2μA. Once the capacitor's voltage has reached 500mV, the circuit breaker attempts to return power to the load. At this point the timer cycle will repeat as long as the fault is present, resulting in an output duty cycle of 3%.

Figure 5 illustrates the cyclical retry of the UCC3912 under fault conditions. Note that the initial fault time is longer than subsequent cycles due to the fact that the capacitor is completely discharged and must initially charge to the reset threshold of 0.5V. If at any time the output current reaches IMAX, the MOSFET transitions into linear mode, providing constant output current until the fault time expires. The discrete IMAX input is used to set the maximum output current to either a fixed

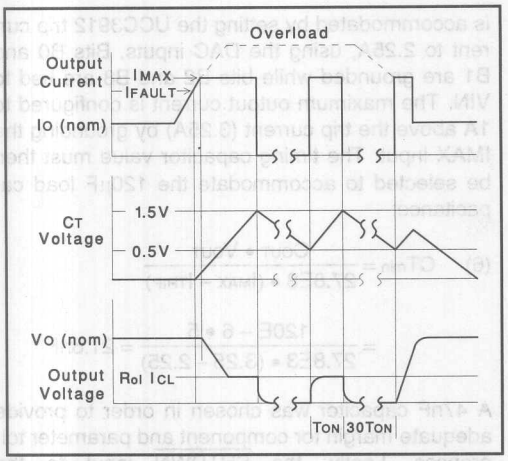


Figure 5. Load Current, Timing Capacitor Voltage and Output Voltage of the UCC3912 under Fault Conditions.

value of 4A, (logic level high), or to a value 1A above the trip current as set by the DAC inputs, (logic level low). The 4 bit DAC allows the fault current level to be programmed from 0 to 3A in 250mA increments.

Fault time duration is controlled by the value of the timing capacitor, CT, according to the following equation:

$$(1)\quad t_{FAULT} = CT \bullet \frac{\delta v}{I} = CT \bullet \frac{1.5 - 0.5}{36E - 6} = 27.8E3 \bullet CT$$

Figure 6 provides a plot of fault time vs timing capacitance. The fault time duration is set based upon the load capacitance, load current, and the maximum output current. *The "on" or fault time must be of sufficient duration to charge the load capacitance during a normal startup sequence or when recovering from a fault.* If not, the charge accumulated on the output capacitance will be depleted by the load during the "off" time. The cycle will then repeat, preventing the output from turning on.

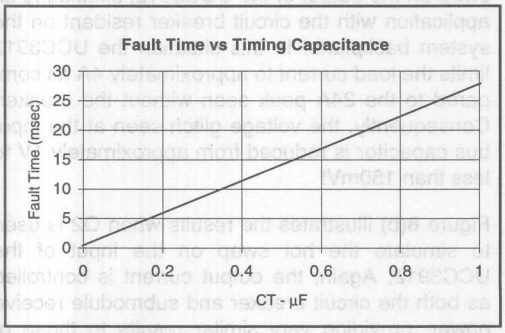


Figure 6. Fault Time vs Timing Capacitance

To determine the minimum fault time, assume a maximum load current just less than the trip limit. This leaves the difference between the IMAX and ITRIP values as the current available to charge the output capacitance. The minimum required fault time can then be calculated as follows:

$$(2)\quad t_{FAULTmin} = \frac{C_{OUT} \bullet V_{OUT}}{I_{MAX} - I_{TRIP}}$$

The minimum timing capacitor can be calculated by substituting equation (1) for tFAULT in equation (2) and solving for CT.

$$(3)\quad CT_{min} = \frac{C_{OUT} \bullet V_{OUT}}{27.8E3 \bullet (I_{MAX} - I_{TRIP})}$$

In addition to the IMAX and DAC inputs, the UCC3912 provides a fault indicator output and shutdown command. The $\overline{\text{FAULT}}$ signal is an open drain output which is active low under any condition which turns the output MOSFET "off". These conditions include under voltage lockout (UVLO), over current faults, thermal shutdown, and active shutdown as commanded by the $\overline{\text{SHTDWN}}$ input. Note that $\overline{\text{FAULT}}$ is asserted (low) during power up while the UCC3912 is in a UVLO state.

The $\overline{\text{SHTDWN}}$ command is an active low input which turns the MOSFET "off" and puts the IC into sleep mode, reducing the quiescent current to less than 5µA. The shutdown command can be used to extend the life of battery powered systems by powering down subsystems when not in use.

Unidirectional current flow is another attractive feature of UCC3912. The reverse voltage comparator senses the output voltage and turns the MOSFET "off" whenever the output voltage is less than 30mV below the input. Under light loads, the UCC3912 regulates the voltage drop until

$$(4)\quad (I_{OUT}) \bullet (R_{DSon}) \geq 30mV,$$

thus preventing false shutdowns. This effectively prevents current flow from output to input, eliminating the need for series diode protection and the associated voltage drop and power losses incurred with its use.

PRACTICAL CONSIDERATIONS

The UCC3912 is supplied in 16-pin power surface mount packages. Four ground leads are provided in order to effectively transfer heat out of the package. These pins should always be terminated to as large an area of copper as possible. Although the 3% duty cycle switchmode protection drastically minimizes power dissipation, thermal analysis

should still be performed in order to insure reliable circuit operation.

When interfacing with larger values of load capacitance, the UCC3912 fault time must be increased accordingly. While the average power remains low due to the 3% duty cycle, the power dissipation during the fault time will result in a junction temperature rise based on the thermal time constant of the system. A simplified thermal model of the system is comprised of the die, leadframe and PC board. However, for fault times less than 30msec, the effect of the leadframe and PC board can be considered negligible as their thermal time constants are on the order of 2 and 300sec respectively. A rough estimate of the transient junction temperature can then be calculated based on the following equation:

$$(5)\quad T_j(t) = P_{DISS}\left[\Theta_{DIE}\left(1 - e^{-t/\tau}\right)\right] + T_L$$

Where P_{DISS} = transient power dissipation
Θ_{DIE} = thermal resistivity between die and leadframe ≈ 4°/W
t = fault time
τ = thermal time constant of the die ≈ 30msec
T_L = steady state lead temperature

As the fault time is increased beyond 30msec, a more thorough transient thermal analysis is required. For additional information regarding thermal analysis and transient response, the reader is directed to reference (1).

In applications requiring minimum voltage losses, it is important to take the effects of PCB trace resistance into account. When passing two to three amps of current, minimum trace widths can result in enough I • R voltage drop to effect system performance. By increasing either the trace width or copper weight, these effects can be made negligible. Table I provides resistance/inch values for various trace widths of 1, 1.5, and 2 oz. copper.

Table I
PCB Trace Resistance (mΩ/inch)

Copper Wt.	Trace Width (inches)					
	0.01	0.02	0.03	0.05	0.07	0.1
1.0 oz.	48.5	24.23	16.2	9.7	6.9	4.9
1.5 oz.	38.8	19.4	12.9	7.8	5.5	3.9
2.0 oz.	24	12	8	4.8	3.4	2.4

A TYPICAL APPLICATION

In order to evaluate the performance of the UCC3912, consider a typical application consisting of a 2A maximum load current in parallel with 120µF of load capacitance. The 2A output current is accommodated by setting the UCC3912 trip current to 2.25A, using the DAC inputs. Bits B0 and B1 are grounded while bits B2 and B3 are tied to VIN. The maximum output current is configured to 1A above the trip current (3.25A) by grounding the IMAX input. The timing capacitor value must then be selected to accommodate the 120µF load capacitance:

$$(6)\quad CT_{min} = \frac{C_{OUT} \bullet V_{OUT}}{27.8E3 \bullet (I_{MAX} - I_{TRIP})}$$

$$= \frac{120E-6 \bullet 5}{27.8E3 \bullet (3.25 - 2.25)} = 21.6nF$$

A 47nF capacitor was chosen in order to provide adequate margin for component and parameter tolerances. Lastly, the SHTDWN input to the UCC3912 is connected to VIN since it is not used in this example.

In actual hot swap applications, the circuit breaker function may reside on the system's backplane servicing one or more submodules, or be distributed throughout the individual submodules depending on system requirements. In order to test both of these application scenarios, a MOSFET was used to simulate a hot swap on the input and output of the UCC3912. A test load was constructed using a 120µF low ESR tantalum capacitor in parallel with a carbon power resistor, while 240µF was used to simulate the system's input bus capacitance. Output current was monitored using a noninductive 10mΩ current shunt in series with the load. Figure 7 illustrates the test setup including the UCC3912 circuit configuration.

HOT SWAP PERFORMANCE

Figure 8 illustrates the load current and input voltage waveforms, measured at points A and B in Figure 7, with and without the UCC3912. In Figure 8(a), transistor Q2 was used to perform the hot swap on the output of the UCC3912, simulating an application with the circuit breaker resident on the system backplane. In this situation the UCC3912 limits the load current to approximately 4A as compared to the 24A peak seen without the breaker! Consequently, the voltage glitch seen at the input bus capacitor is reduced from approximately 1V to less than 150mV!

Figure 8(b) illustrates the results when Q2 is used to simulate the hot swap on the input of the UCC3912. Again, the output current is controlled as both the circuit breaker and submodule receive power, providing very similar results to those of Figure 8(a).

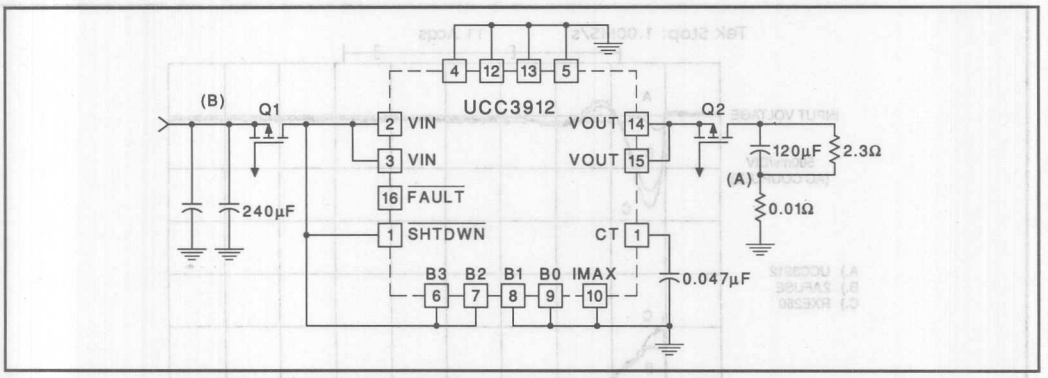


Figure 7. Typical UCC3912 Configuration and Hot Swap Test Circuit Setup.

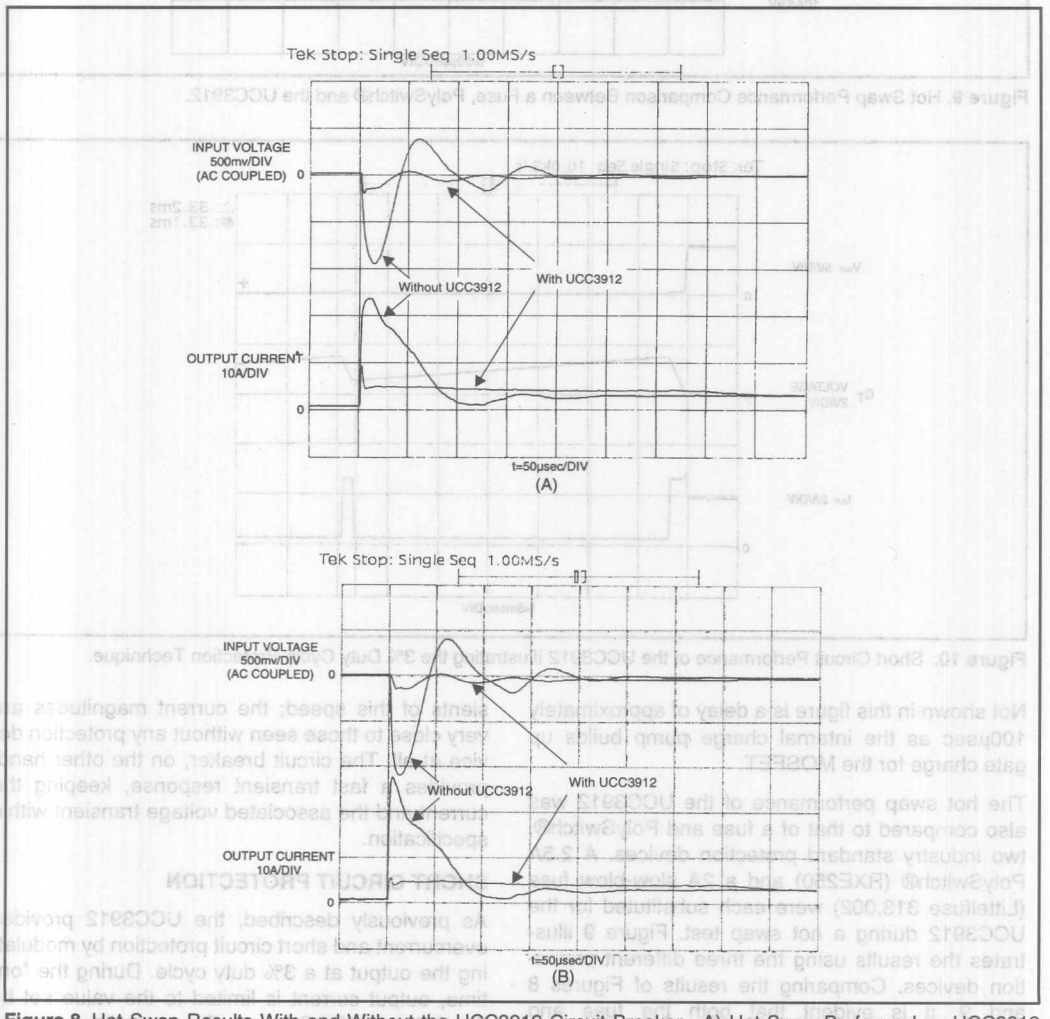


Figure 8. Hot Swap Results With and Without the UCC3912 Circuit Breaker. A) Hot Swap Performed on UCC3912 Output. B) Hot Swap Performed on UCC3912 Input.

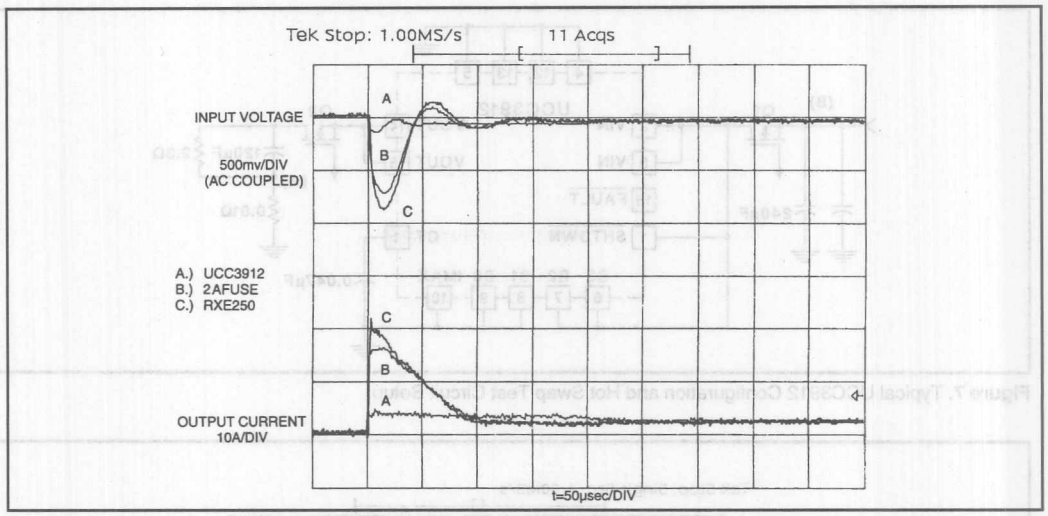


Figure 9. Hot Swap Performance Comparison Between a Fuse, PolySwitch® and the UCC3912.

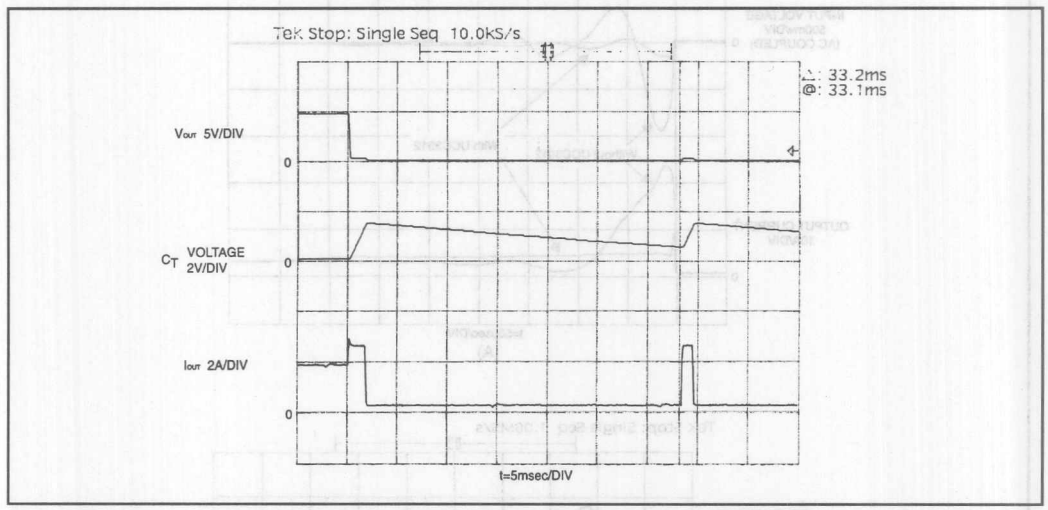


Figure 10. Short Circuit Performance of the UCC3912 Illustrating the 3% Duty Cycle Protection Technique.

Not shown in this figure is a delay of approximately 100µsec as the internal charge pump builds up gate charge for the MOSFET.

The hot swap performance of the UCC3912 was also compared to that of a fuse and PolySwitch®, two industry standard protection devices. A 2.5A PolySwitch® (RXE250) and a 2A slow-blow fuse (Littelfuse 313.002) were each substituted for the UCC3912 during a hot swap test. Figure 9 illustrates the results using the three different protection devices. Comparing the results of Figures 8 and 9, it is evident that both the fuse and PolySwitch® offer virtually no protection for transients of this speed; the current magnitudes are very close to those seen without any protection device at all. The circuit breaker, on the other hand, provides a fast transient response, keeping the current and the associated voltage transient within specification.

SHORT CIRCUIT PROTECTION

As previously described, the UCC3912 provides overcurrent and short circuit protection by modulating the output at a 3% duty cycle. During the "on" time, output current is limited to the value set by the IMAX and DAC inputs. Figure 10 illustrates the performance of the UCC3912 test circuit when a

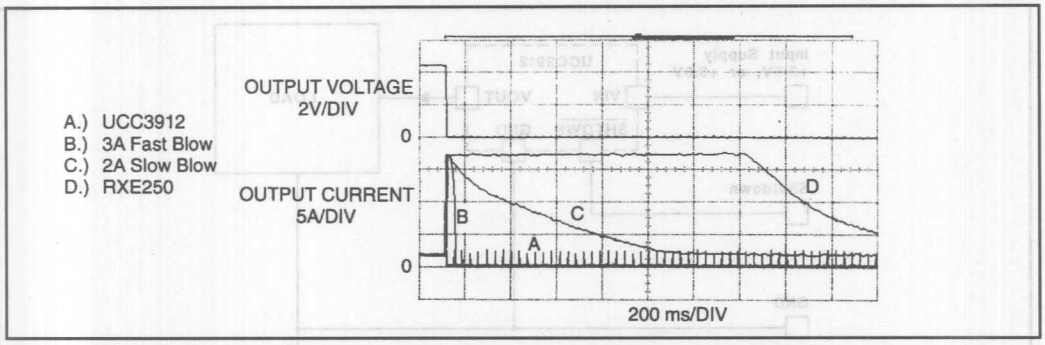


Figure 11. Short Circuit Performance Comparison of a Fuse, PolySwitch® and the UCC3912.

short-circuit is applied in place of the load. The bottom trace is the output current, modulated at a 3% duty cycle, while the center trace is the voltage across the timing capacitor. Note that the first current pulse is approximately 50% longer than subsequent pulses due to the timing capacitor initially charging from 0V.

The short circuit test was also conducted on the 2.5A PolySwitch®, 2A slow-blow fuse, and a 3A fast-acting fuse (Littelfuse 312.003). Figure 11 compares the performance of the 4 different protection techniques. The peak currents incurred with each of the fuses and the PolySwitch® reach approximately 17.5A and are limited only by the output capability of the 5V power supply. The PolySwitch® takes approximately 1.25sec before it begins to limit the current and eventually latches into high impedance mode. At this point it will remain in a high impedance state due to a sustained self heating current and will only reset after it has cooled and the fault condition has been corrected. As a result, the device requires that the input voltage be removed from the system in order to insure a circuit reset. The fuses on the other hand, respond faster than the PolySwitch®, but once blown require manual replacement before the hardware can resume operation. Table II compares the I • T and peak current characteristics of the four techniques.

Table II

Protection Device	Peak Current (Amps)	I • T (Amp-sec)
PolySwitch® RXE250	17.5	17.5
Fuse 312.003	17.5	9.75
Fuse 313.002	17.5	0.875
UCC3912	3.25	0.098

Note: 1) Peak currents are limited by power supply.
2) I • T estimated for first second of short circuit.

When compared to any of the other commonly used technologies, the performance of the UCC3912 is superior. The electronic circuit breaker responds almost immediately to a short circuit, limiting the current to 3.25A before turning off the output. The breaker then attempts to reapply power at a 3% duty cycle until the fault has been corrected. The low duty cycle, coupled with the current limiting feature keeps the power dissipation at a reasonable level, eliminating the need for extensive heating sinking. In this example the UCC3912 dissipates only 5V • 3.25A • 3% = 488mW of power during the short circuit.

POWER MANAGEMENT APPLICATIONS

In an effort to save energy, the federal government is working to impose regulations that will require electronic equipment and appliances to operate more efficiently. As an example, consider the personal computer (PC). PCs typically dissipate 100 to 200W, with an additional 150 to 350W consumed by the monitor. In order to limit the power dissipation to a recommended 30W during periods of nonusage, circuitry must be added to shutdown key components such as the monitor, high powered cache circuits and bus interfaces. The UCC3912 offers a simple solution to these types of power management applications.

The UCC3912 can be configured as a low current (<5µA) standby power switch, as shown in Figure 12. The shutdown input, SHTDWN, is utilized to turn off the internal MOSFET, removing power from the load and reducing the UCC3912 quiescent current to <5µA. When reactivated by the logic command, the current limiting features of the UCC3912 allow the load circuits to resume operation without disrupting the rest of the system.

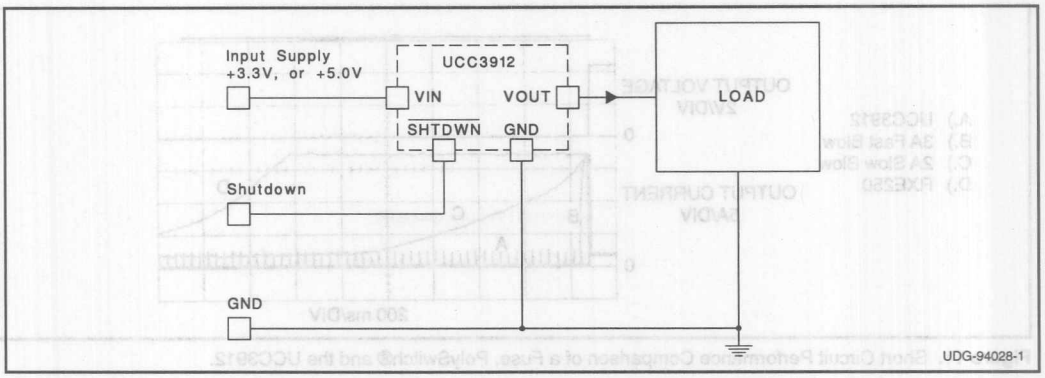


Figure 12. Low Current Standby Power Switch

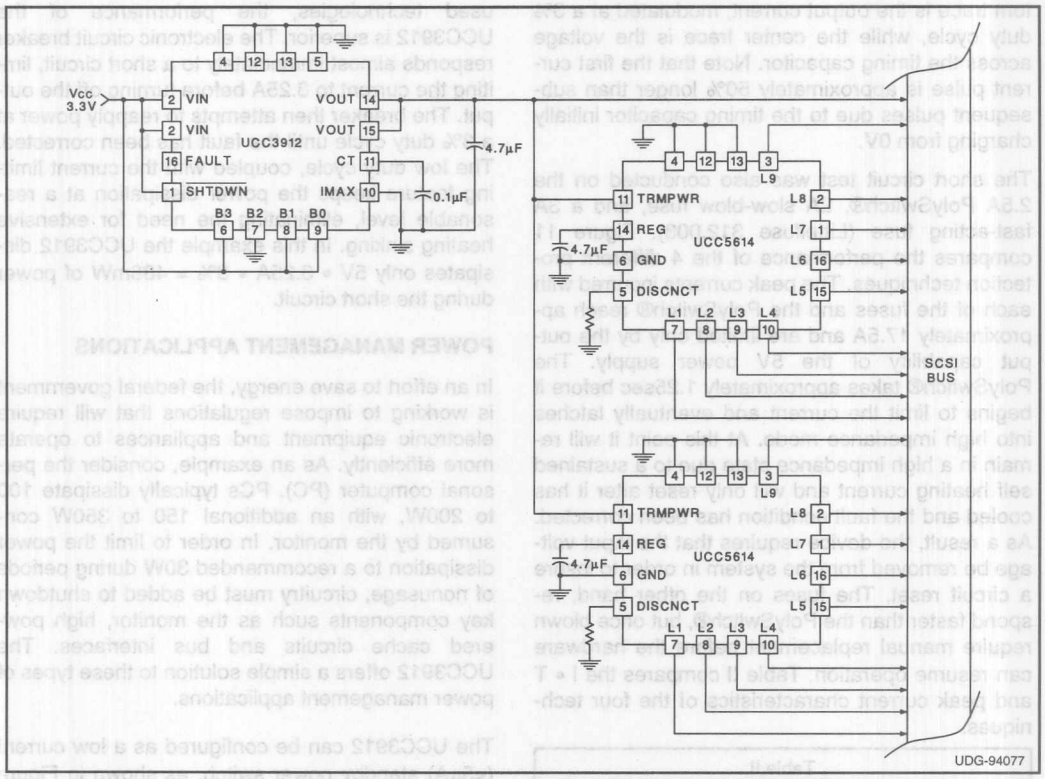


Figure 13. Typical 3.3V SCSI Application

APPLICATION CIRCUITS

The 3.3V power bus has quickly become the standard for laptop computers and other battery operated equipment. Unfortunately, SCSI standards specify an active termination voltage of 2.7V. In addition, standards require that the Termpwr source be fused and provide for unidirectional current flow. These requirements have typically forced designers to include a 5V supply in 3.3V systems - a 5%, 3.3V bus leaves only 130mV of headroom for a diode, fuse, and regulator overhead. Replacing the diode and fuse with the UCC3912 limits the voltage drop to less than 60mV while still meeting SCSI requirements. Combining the UCC3912 with a low dropout active terminator such as the UCC5614 results in a complete design. Figure 13 illustrates a typical 3.3V SCSI application.

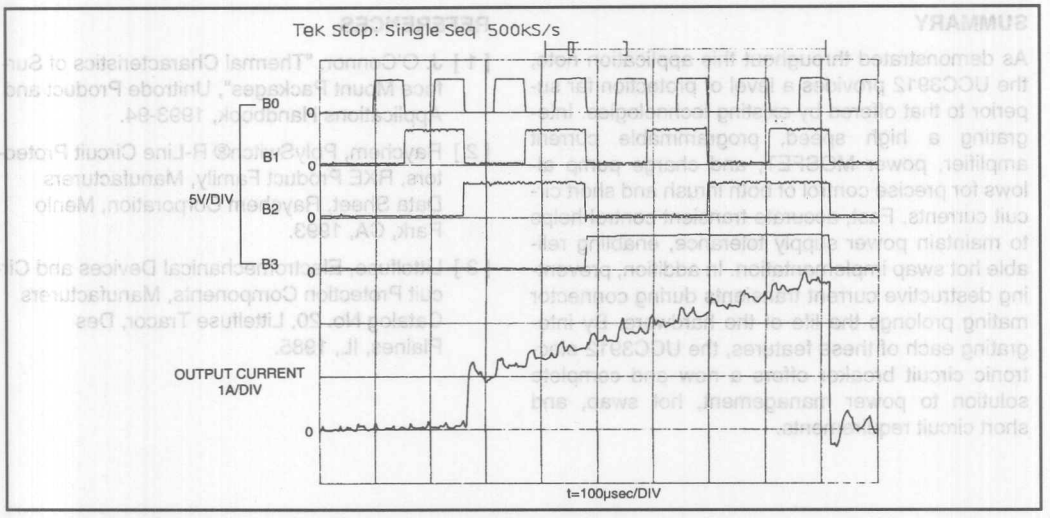


Figure 14. Controlled Current Slew Rate Using the UCC3912 4-Bit DAC.

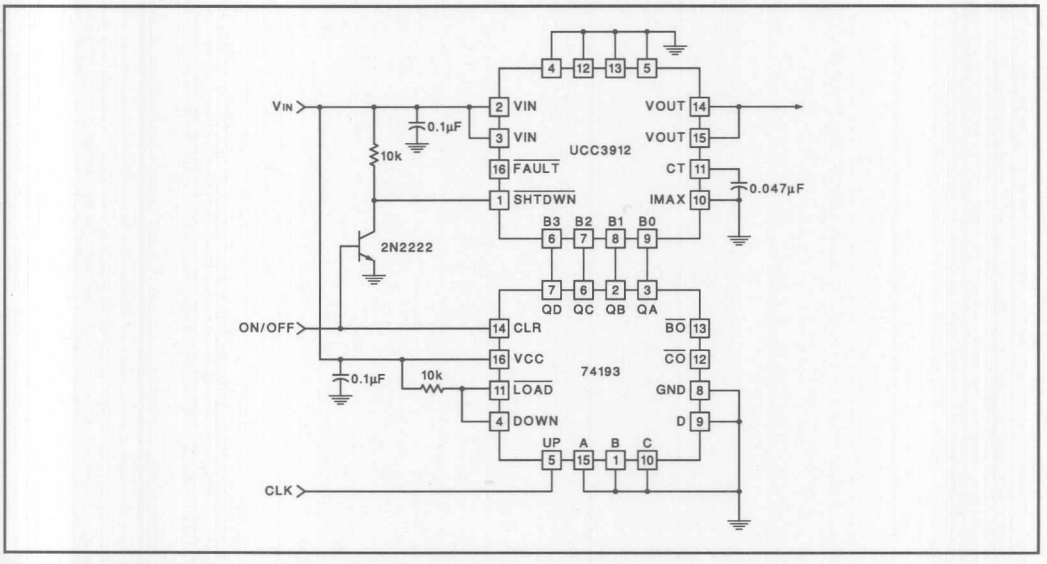


Figure 15. UCC3912 Current Control Circuit Implementation.

The UCC3912 lends itself well to more sophisticated current limiting schemes through the use of the DAC inputs. Greater control of output current slew rate can be obtained by stepping the DAC through a series of its input codes. Figure 14 illustrates the output current as the DAC inputs are controlled using the output of a 4-bit counter as shown in Figure 15. Similarly, loads such as motors often require inrush currents several times their normal running value. By using the counter in Figure 15 to count down rather than up, the motor can be quickly accelerated to speed using maximum current and then closely protected against overload.

The duty cycle protection capability of the UCC3912 can be disabled by grounding the timing capacitor input, CT. This causes the UCC3912 to remain in constant current mode during a fault condition. When operating in this manner the UCC3912 is in linear mode and will dissipate power as function of the maximum output current and differential input/output voltage. It is extremely important that adequate heatsinking is provided when operating in this configuration.

SUMMARY

As demonstrated throughout this application note, the UCC3912 provides a level of protection far superior to that offered by existing technologies. Integrating a high speed, programmable current amplifier, power MOSFET, and charge pump allows for precise control of both inrush and short circuit currents. Fast, accurate transient control helps to maintain power supply tolerance, enabling reliable hot swap implementation. In addition, preventing destructive current transients during connector mating prolongs the life of the hardware. By integrating each of these features, the UCC3912 electronic circuit breaker offers a new and complete solution to power management, hot swap, and short circuit requirements.

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[3] Littelfuse, Electromechanical Devices and Circuit Protection Components, Manufacturers Catalog No. 20, Littelfuse Tracor, Des Plaines, IL, 1985.

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A HIGH PERFORMANCE LINEAR REGULATOR FOR LOW DROPOUT APPLICATIONS

Dave Zendzian
Applications Engineer

INTRODUCTION

Today's microprocessors are placing ever greater demands upon power system design. Most state of the art devices now require a 3.3V bus and therefore necessitate some means of stepping down the existing 5V system supply. To complicate matters further, microprocessor performance is directly related to the quality of the supply voltage. This results in the need for tight regulation and excellent transient response if the maximum potential of the processor is to be realized. Recently, the trend has been to implement the function using a switching regulator, primarily due to the high efficiencies obtainable with this topology. However, when the difference between input and output voltage is low, the efficiency advantage of the switcher is no longer as great. A linear regulator design, on the other hand, offers several desirable features including low output noise and wide bandwidth, resulting in excellent transient load response. This application note presents a high performance linear regulator design capable of maximizing the performance of these digital systems.

LINEAR VS SWITCHER

Figure 1 illustrates the basic elements of both a linear and switching stepdown regulator. In the linear topology, the output is regulated by controlling the voltage drop across a power transistor biased in the linear region. The switching circuit, on the other hand, provides regulation by varying the duty cycle of a saturated power switch. Although switchers offer a substantial efficiency advantage in applications with large differences between input and output voltage, the savings become less significant as this difference is reduced. To illustrate this point, consider the differences in a 3A, 5V to 3.3V converter design using the two topologies.

The power dissipation in the linear regulator is a function of the difference between input and output voltage, output current, output driver power, and quiescent controller power:

Input/Output Voltage Drop (5.0-3.3V)(3A) = 5.1W

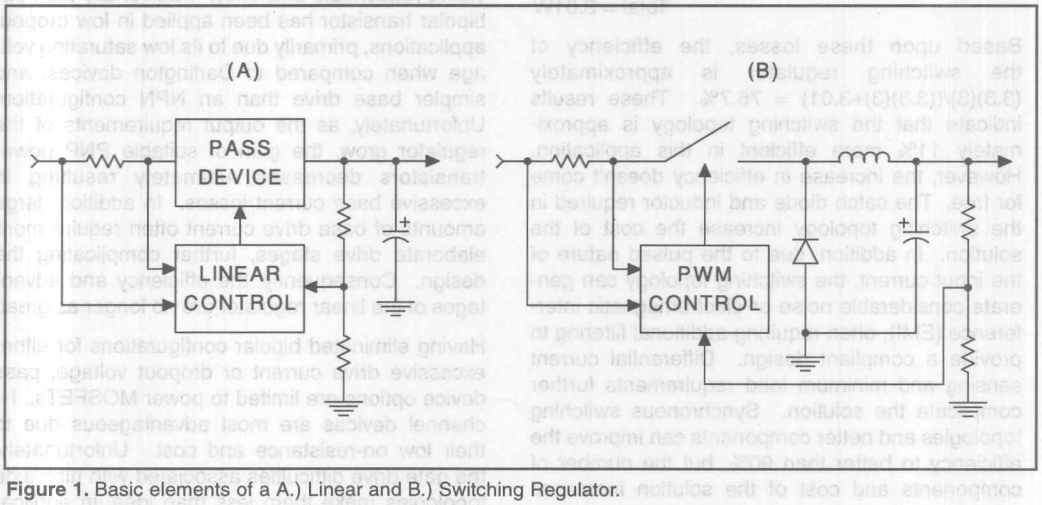


Figure 1. Basic elements of a A.) Linear and B.) Switching Regulator.

Pass Device Driver	(5.0V)(0.005A) = 0.03W
Controller Icc	(5.0V)(0.01A) = 0.05W
	Total = 5.18 W

The resulting efficiency is equivalent to the ratio of output power to input power or (3.3)(3)/((3.3)(3)+5.18) = 65.7%.

The efficiency of the switching regulator is not as simple to calculate. Power dissipated by the regulator is a combination of both conduction and switching losses in each of the circuit elements. Assuming an inexpensive, commercial power MOSFET with an Rds(on) of 0.28W, the duty cycle of the regulator is approximately:

$$\frac{t_{ON}}{t_{OFF}} = \frac{3.3}{(5 - 3(0.28))} \approx 88\%$$

Taking duty cycle into account, the itemized circuit losses are estimated as follows:

FET Conduction Losses	$(3A)^2(0.28\Omega)(80\%) = 2.02W$
FET Switching Losses	(8.4E-9C)(5V)(250kHz) = 0.01W
Diode Forward Voltage	(0.6V)(3A)(20%) = 0.36W
Inductor Voltage	$(3A)^2(0.017\Omega)(100\%) = 0.15W$
RSENSE Voltage	$(3A)^2(0.043\Omega)(80\%) = 0.31W$
AC Capacitor Losses	$(0.15)^2(2.2\Omega) = 0.05W$
Controller Icc	(5V)(1E-3A) = 0.01W
Switching Transients	≈ 0.10W
	Total = 3.01W

Based upon these losses, the efficiency of the switching regulator is approximately (3.3)(3)/((3.3)(3)+3.01) = 76.7%. These results indicate that the switching topology is approximately 11% more efficient in this application. However, the increase in efficiency doesn't come for free. The catch diode and inductor required in the switching topology increase the cost of the solution. In addition, due to the pulsed nature of the input current, the switching topology can generate considerable noise or electromagnetic interference (EMI), often requiring additional filtering to provide a compliant design. Differential current sensing and minimum load requirements further complicate the solution. Synchronous switching topologies and better components can improve the efficiency to better than 90%, but the number of components and cost of the solution increases even further.

The linear regulator, on the other hand, while slightly less efficient offers several attractive features. Low noise is inherent to the design due to the lack of fast switching circuits. Reduced component count coupled with a relatively simple design help to ensure system reliability and lower cost. Moreover, the linear solution does not have a minimum load restriction making it attractive in applications with widely varying load currents. The remainder of this application note provides the design details for a high performance linear regulator, taking advantage of each of these performance features.

TOPOLOGY OVERVIEW

Referring again to Figure 1, the linear design can be broken-down into several key elements including a pass device, driver, error amplifier, reference, output capacitance and over current protection block. The crux of the design arguably lies in the pass device. It's characteristics determine what the differential, input/output voltage limitations are in addition to how much quiescent power is required by the regulator. Error amplifier characteristics directly effect system bandwidth and the achievable DC regulation while the voltage reference primarily governs the steady state accuracy of the output voltage. Lastly, the overcurrent protection block protects the regulator during output fault conditions.

POWER PASS DEVICES

The power device selected to provide the pass function must be capable of operating under very low differential input/output voltages while still providing reasonable efficiency. Traditionally the PNP bipolar transistor has been applied in low dropout applications, primarily due to its low saturation voltage when compared to Darlington devices, and simpler base drive than an NPN configuration. Unfortunately, as the output requirements of the regulator grow, the gain of suitable PNP power transistors decreases, ultimately resulting in excessive base current losses. In addition, large amounts of base drive current often require more elaborate drive stages, further complicating the design. Consequently, the efficiency and advantages of the linear regulator are no longer as great.

Having eliminated bipolar configurations for either excessive drive current or dropout voltage, pass device options are limited to power MOSFETs. N-channel devices are most advantageous due to their low on-resistance and cost. Unfortunately, the gate drive difficulties associated with high side topologies make them less than ideal in applica-

tions
operating from a single supply. P-channel MOSFETs, while easier to drive in high side applications, have historically been plagued with higher on-resistance. However, recent advancements in high cell density technology have led to substantial reductions in $R_{DS(on)}$. For instance, Motorola's new HDTMOS devices boast 50% lower on-resistance than the previous generation of P-channel devices. The MTP50P03HDL, a 50A, 30V, P-channel MOSFET is one such example, specified with a maximum on-resistance of 30mΩ at drain currents of 25A and a maximum gate threshold voltage of 2.0V. The logic level gate characteristics are required in applications limited to a supply voltage of 5 volts. An additional advantage of the MOSFET power stage is the minimum amount of drive current required. Since the device is voltage controlled and operating in transconductance mode it can be biased with minimal drive current, further improving the efficiency and decreasing the complexity of the regulator.

OUTPUT CAPACITANCE

Bulk output capacitance is required in order for the design to meet the specified transient requirements. As with any control system, the voltage loop has a finite bandwidth and cannot instantaneously respond to a change in load conditions. In order to keep the output voltage within the specified tolerance, sufficient capacitance must be provided to source the increased load current throughout the initial portion of the transient period. During this time, charge is removed from the capacitor and its voltage correspondingly decreases until the control loop can catch the error and correct for the increased current demand. The amount of capacitance used must be enough to keep the voltage drop within specification according to the charge relationship I=CdV/dt. Unfortunately, the equivalent series resistance (ESR) and inductance (ESL) of the capacitor generate an additional voltage transient, the total of which must be kept within specification. In order to limit this transient, the ESR and ESL of the selected devices will usually dictate a much larger value of capacitance than might normally be expected to satisfy the charge relationship.

OVERCURRENT PROTECTION

Traditional over current protection schemes usually involve either "constant current" or "current foldback" techniques. Unfortunately, each of these solutions offers a compromise between the needs of the
user and the optimization of the power supply. Constant current techniques, while easy to interface with, result in massive overkill in terms of thermal management and heatsink implementation. Current foldback implementations, on the other hand, ease the design of the regulator while complicating startup scenarios for the user. Newer, switchmode protection techniques offer a solution to this compromise. By modulating the output at a fixed duty-cycle during an over current condition, thermal management of the regulator is greatly simplified. Adjusting the pulse width of the duty-cycle allows start-up load characteristics to be easily accommodated.

CONTROL CIRCUIT

In the design example that follows, the regulator is implemented using a UC3833, precision linear controller. This IC incorporates all of the functions required to design a very low dropout, precision regulator, including a 1% reference, error amplifier, and an uncommitted output stage. Providing an output driver with both source and sink capabilities allows the use of a variety of power devices including NPN or PNP bipolar devices and N or P-channel MOSFETs. Switchmode current limiting is also implemented by the UC3833, significantly reducing power dissipation during fault conditions. Further information regarding this device can be found in Unitrode application note U-116.

DESIGN DETAILS

The regulator was designed to meet the following performance requirements, typical of today's microprocessor systems. The schematic is shown in Figure 2.

V_{IN} = 5V, ±10%

V_{OUT} = 3.3V, ±5%

I_{OUT} = 3.5A typical, 4A maximum

Transient Response: 5% to 75% I_{OUTmax} in 100nsec, Vreg = ±5%

In order to select a pass device for the design, the dropout voltage requirements must first be established. Input voltage tolerance, along with the voltage drop across the current sense resistor, must be taken into account. The sense resistor value is calculated based on the maximum output current specification of the regulator and the current limit threshold of the UC3633. In order to ensure the regulator can deliver 4A under worst case conditions, the maximum resistor value, including tolerance, is given by:

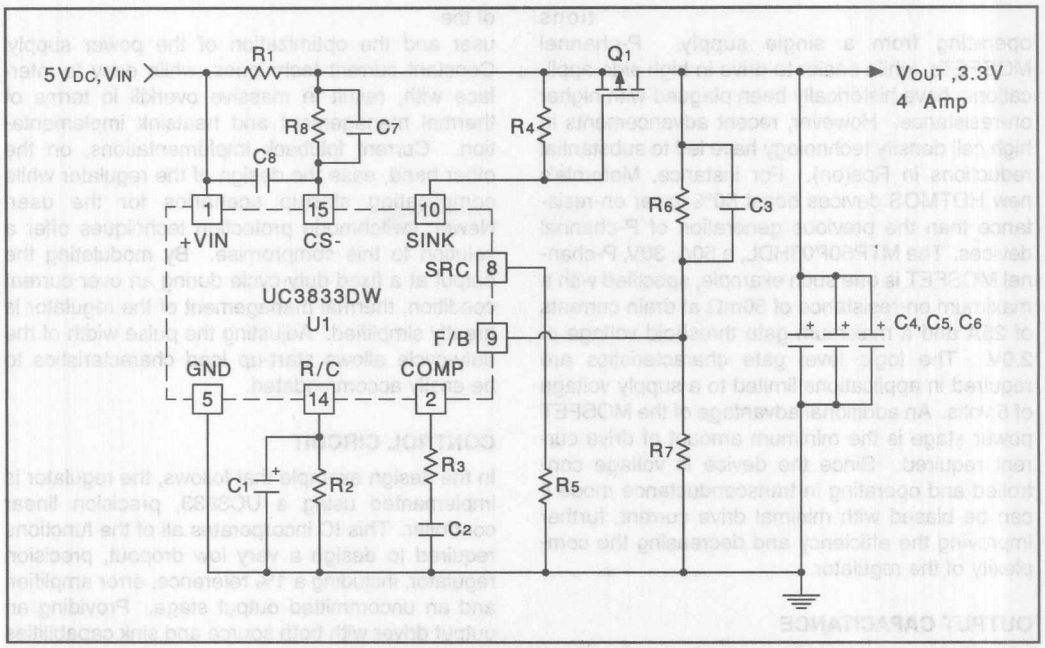


Figure 2: A 3.3V, 4A regulator featuring low dropout voltage, switchmode overcurrent protection and excellent transient response.

$$R_{MAX} = \frac{V_{CLmin}}{I_{OUT}} \quad (1)$$

$$R_{MAX} = \frac{0.093}{4} = 23.25m\Omega$$

Using a 5%, 22mΩ sense resistor and low line conditions, the dropout requirement for the pass device is calculated as follows:

$$V_{DO} = V_{INmin} - I_{OUTmax}(R_{SENSEmax}) - V_{OUT} \quad (2)$$

$$V_{DO} = 4.5 - 4(1.05)(0.022) - 3.3 = 1.29V$$

This dropout voltage results in a maximum MOSFET $R_{DS(on)}$ of 0.323Ω. In addition, logic level gate characteristics are required in order to ensure adequate gate enhancement with a 5 volt input. These requirements are easily met with the MTP50P03HDL's 30mΩ (T_C=25°C) on-resistance and 2.0V maximum gate threshold voltage.

Having selected the pass device, the UC3833 output driver can now be configured. While the simplest approach would be to configure the driver as a common emitter, including a small amount of emitter resistance eliminates the drive transistor's β from the loop gain expression, thereby simplifying the frequency compensation. Resistors R6 and R7 attenuate and feedback the output voltage to the inverting input of the error amplifier.

Sprague 595D surface mount tantalum capacitors were chosen for the output based upon their ESR/ESL specifications and package style. By paralleling three 270µF, 10V capacitors, the equivalent ESR/ESL is reduced by 1/3, providing an equivalent impedance of approximately 13mΩ typical and 60mΩ maximum at 100kHz. Surface mount packaging helps to further reduce the parasitic effects induced by component leads. The equivalent 810µF provides more than sufficient capacitance to keep the transient voltage drop within specification.

SMALL SIGNAL AC RESPONSE

With the driver and power stage configured, the voltage and current control loops can now be analyzed and properly compensated. Figure 3 illustrates the basic configuration of the two loops. The frequency response of the MOSFET driver includes a gain factor of R4/R5 with a pole introduced from the combination of the MOSFET's gate to source capacitance and R4. The transconductance of the MOSFET is represented by g_{FS}. Modeling the load as a resistance in parallel with

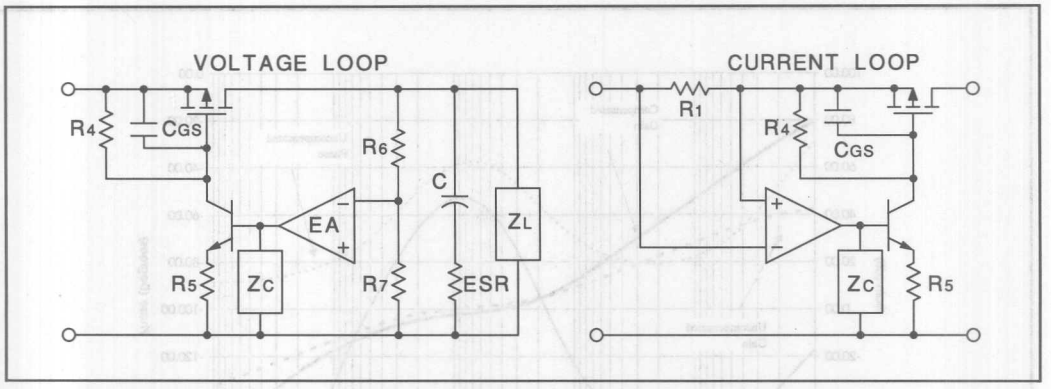


Figure 3. Basic configuration of the voltage and current control loops.

the output capacitor and it's associated ESR results in a loop gain expression, excluding the error amplifier, of:

$$A_V = \left(\frac{R_4}{R_5(1 + sR_4C_{GS})}\right) \cdot \left(g_{FS}\left(\frac{R_L\,(1 + s(ESR)C)}{(1 + s(R_L + ESR)C)}\right)\right)\left(\frac{R_7}{R_6 + R_7}\right) \quad (3)$$

The dashed curves of Figure 4a represent the resulting voltage loop response. Although the response is stable, the low frequency gain and closed loop accuracy are limited. This is easily improved by compensating the UC3633's error amplifier using a series RC network. Doing so introduces a pole at 0Hz, thereby improving the DC regulation, in addition to a zero at $1/(2\pi RC)$Hz. The zero is located between the poles resulting from the load and the MOSFET gate to source capacitance. Together with the ESR zero, they provide enough phase boost to maintain adequate phase margin. Adding a capacitor across R6 helps to squeeze additional bandwidth from the loop by introducing another pole/zero pair. The gain and phase of the compensated voltage loop (solid lines) are also shown in Figure 4a.

Having stabilized the voltage loop, the current loop can now be examined. The established compensation impedance must be taken into account as both the current and error amplifier share a common output node. The complete current loop expression, including the transconductance (g_M) of the current amplifier, is given below:

$$A_I = \left(\frac{R_4}{R_5(1 + sR_4C_{GS})}\right) \cdot \left(g_{FS}R_1\right)\left(\frac{g_M\,(1 + sR_3C_2)}{sC_2}\right) \quad (4)$$

The corresponding response is shown in Figure 4b. From this plot, it is evident the loop lacks sufficient phase margin to be stable under all conditions. Filtering the current signal with the network composed of R8, C7 and C8, as shown in Figure 2, introduces a pole and zero according to the following transfer function, rolling off the current loop gain without effecting the voltage loop. The gain and phase of the compensated current loop (solid lines) are also shown in Figure 4b.

$$\frac{V_O(s)}{V_I(s)} = \frac{(1 + sR_8C_7)}{(1 + sR_8(C_7 + C_8))} \quad (5)$$

When performing small signal analysis such as this, the use of a spreadsheet program can prove invaluable. The software can be easily configured to provide Bode plots using pole and zero locations input by the user. The graphical output allows the user to quickly evaluate a variety of compensation techniques and relatively easily optimize the design.

OVERCURRENT PROTECTION AND THERMAL MANAGEMENT

Overcurrent protection is provided via the UC3833's internal amplifier and overcurrent comparator. When the voltage across R1 crosses the comparator threshold the UC3833 begins to modulate the output driver. During the on-time the current sense amplifier provides constant output current by maintaining a fixed voltage across R1. On and off times are controlled by timing components C1 and R2 according to the following expressions:

$$T_{ON} = 0.693(10k)(C_T) \quad (6)$$

$$T_{OFF} = 0.693(R_T)(C_T) \quad (7)$$

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{10k}{10k + R_T} \quad (8)$$

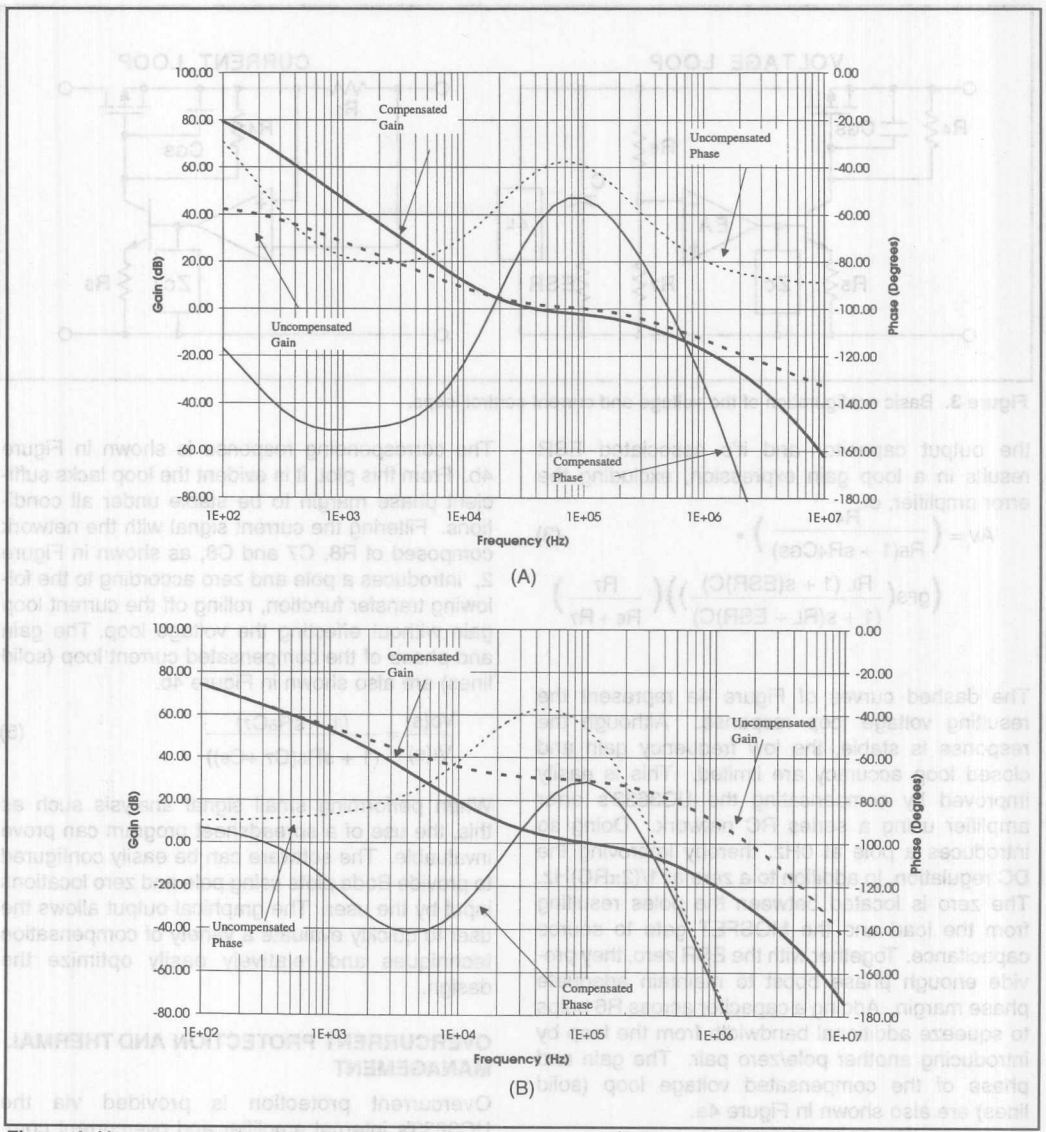


Figure 4: Uncompensated and compensated open loop responses for the circuit of Figure 2. (A) Voltage Loop, (B) Current Loop.

When implementing switchmode protection, the "on" time (T_{ON}) must be of sufficient duration to charge the output capacitance during a normal startup sequence or when recovering from a fault. If not, the charge accumulated on the output capacitor will be depleted by the load during the "off" time. The cycle will then repeat, preventing the output from turning on. A maximum load current of just less than the trip limit results in the difference between the I_{MAX} and I_{TRIP} values as the current available to charge the output capacitance. In this case the minimum "on" time can be calculated as follows:

$$T_{ONmin} = \frac{C_{OUTmax} \bullet V_{OUT}}{I_{MAX} - I_{TRIP}} \quad (9)$$

The duty cycle can then be adjusted to minimize power dissipation using equation (8).

Switchmode protection offers significant heat sinking advantages when compared to conventional, constant current solutions. Since the average power during a fault condition is reduced as a function of the duty cycle, the heat sink need only have adequate thermal mass to absorb the maximum steady state power dissipation and not the full short circuit power. With a 5.5 volt input and a maximum output of 4A, the power dissipated in Q1 is given by:

$$P = (V_{IN} - V_{RSENSE} - V_{OUT})(I_{OUT}) \quad (10)$$

$$P = (5.5 - 4(0.022)(0.95) - 3.3)4 = 8.47W$$

The thermal resistivity of the MOSFET is specified as 1.0°C/W for the TO-220 package style. Assuming an ambient temperature of 50°C and a case to heat sink resistivity of θcs=0.3°C/W, the heat sink required to maintain a 125°C junction temperature can be calculated as follows:

$$T_J = T_A + P(\theta_{JC} + \theta_{CS} + \theta_{SA}) \quad (11)$$

$$25 = 50 + 8.47(1.0 + 0.3 + \theta_{SA})$$

$$\theta_{SA} \leq 7.55°C/W$$

Based on this analysis, any heatsink with a thermal resistivity of 7.55°C/W or less should suffice. Under short circuit conditions the output current will be limited to 6.14A at a 5% duty cycle, resulting in a MOSFET power dissipation of only:

$$P = \left(\left(V_{INmax} - (I_{OUT})(R_{SENSE})\right)I_{OUT}\right)(d.c.) \quad (12)$$

$$P = \left(\left(5.5 - 6.14(0.022)\right)6.14\right)0.05 = 1.65W$$

Without switchmode protection, the short circuit power dissipation would be 33W, almost four times the nominal dissipation!

PRACTICAL CONSIDERATIONS

In order to achieve the expected performance, careful attention must be paid to circuit layout. The printed circuit board should be designed using a single point ground, referenced to the return of the output capacitor. All traces carrying high current should be made as short and wide as possible in order to minimize parasitic resistance and inductance effects.

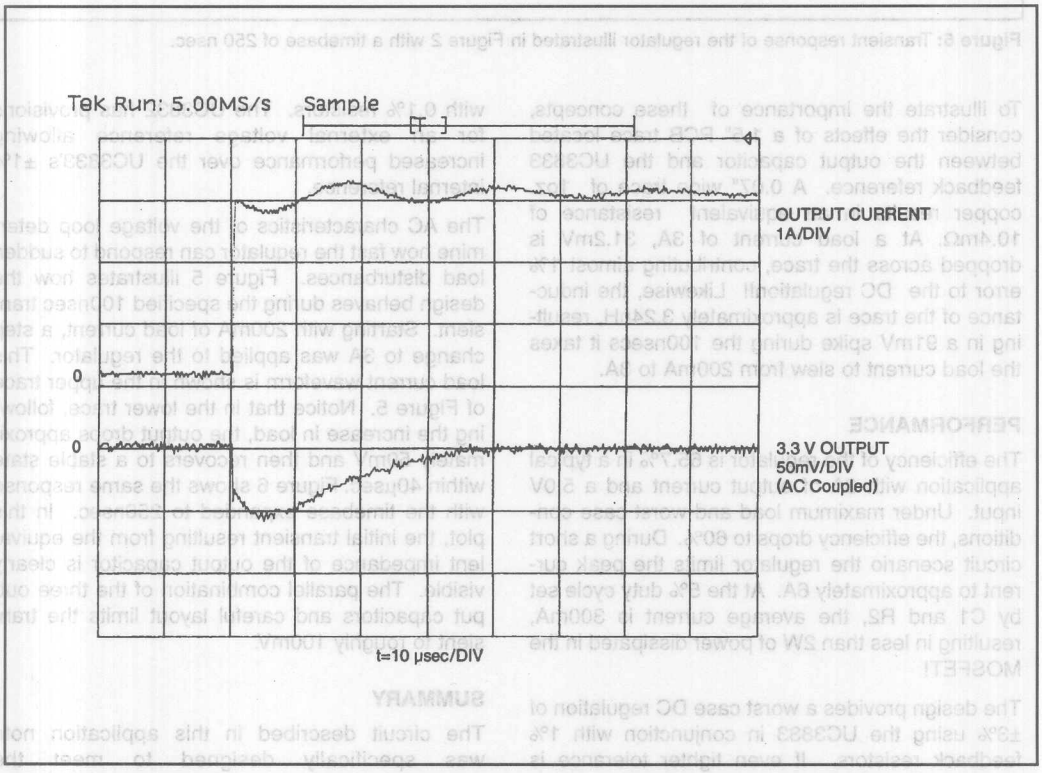


Figure 5: Transient response of the regulator illustrated in Figure 2 with a time base of 10 µsec.

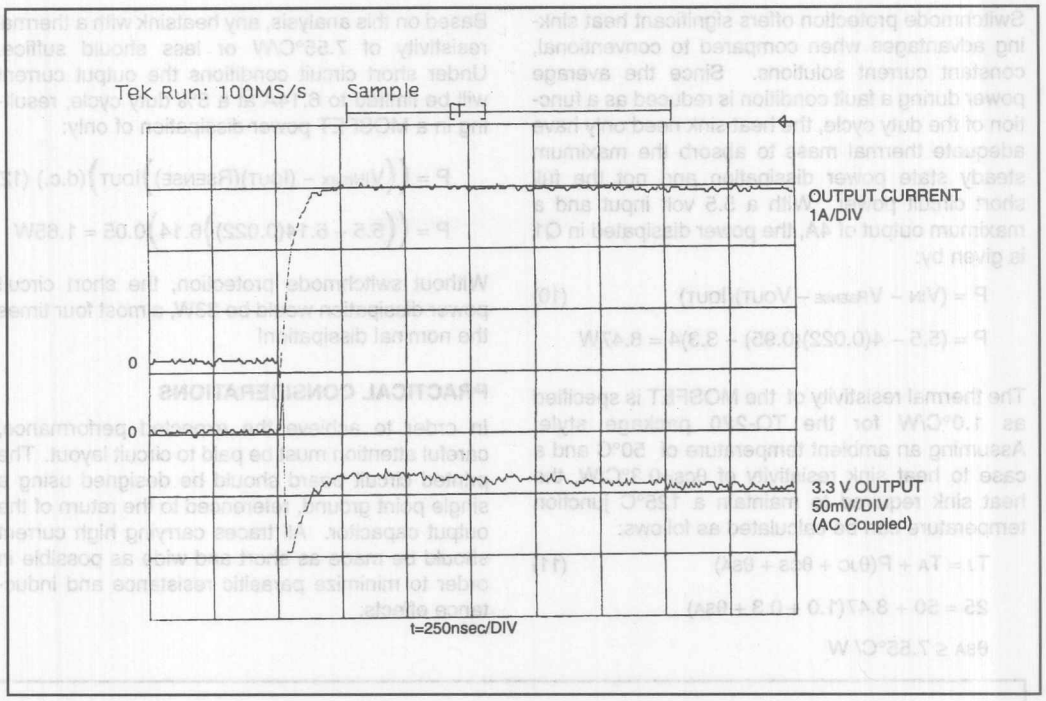


Figure 6: Transient response of the regulator illustrated in Figure 2 with a timebase of 250 nsec.

To illustrate the importance of these concepts, consider the effects of a 1.5" PCB trace located between the output capacitor and the UC3833 feedback reference. A 0.07" wide trace of 1oz. copper results in an equivalent resistance of 10.4mΩ. At a load current of 3A, 31.2mV is dropped across the trace, contributing almost 1% error to the DC regulation!! Likewise, the inductance of the trace is approximately 3.24nH, resulting in a 91mV spike during the 100nsecs it takes the load current to slew from 200mA to 3A.

PERFORMANCE

The efficiency of the regulator is 65.7% in a typical application with 3A of output current and a 5.0V input. Under maximum load and worst case conditions, the efficiency drops to 60%. During a short circuit scenario the regulator limits the peak current to approximately 6A. At the 5% duty cycle set by C1 and R2, the average current is 300mA, resulting in less than 2W of power dissipated in the MOSFET!

The design provides a worst case DC regulation of ±3% using the UC3833 in conjunction with 1% feedback resistors. If even tighter tolerance is required, the UC3832 can be substituted along with 0.1% resistors. The UC3832 has provisions for an external voltage reference allowing increased performance over the UC3833's ±1% internal reference.

The AC characteristics of the voltage loop determine how fast the regulator can respond to sudden load disturbances. Figure 5 illustrates how the design behaves during the specified 100nsec transient. Starting with 200mA of load current, a step change to 3A was applied to the regulator. This load current waveform is shown in the upper trace of Figure 5. Notice that in the lower trace, following the increase in load, the output drops approximately 50mV and then recovers to a stable state within 40μsec. Figure 6 shows the same response with the timebase expanded to 250nsec. In this plot, the initial transient resulting from the equivalent impedance of the output capacitor is clearly visible. The parallel combination of the three output capacitors and careful layout limits the transient to roughly 100mV.

SUMMARY

The circuit described in this application note was specifically designed to meet the demanding performance requirements of today's

TABLE I

VOUT	Io	R6	R1	COUT	θSAmax	Applications
3.0V	3A	1k	0.03	810µF	9.06°C/W	D/A converters, Gate Arrays
	5A	1k	0.0169	1320µF	4.91°C/W	
	7A	1k	0.012	1980µF	3.13°C/W	
2.7V	3A	698	0.03	810µF	7.9°C/W	MCUs
	5A	698	0.0169	1320µF	4.22°C/W	
	7A	698	0.012	1980µF	3.64°C/W	
2.5V	3A	499	0.03	810µF	7.28°C/W	Low voltage digital logic
	5A	499	0.0169	1320µF	3.84°C/W	

Notes: 1. Thermal resistivities assume 50°C ambient and max TJ of 125°C.
2. COUT is comprised of multiple Sprague 595 style tantalum capacitors.

microprocessors. It is capable of providing excellent transient response with reasonable efficiency for less cost and complexity than a switching regulator. The design is easily modified to accommodate other output voltage and current requirements. Table I provides the necessary component substitutions to achieve a variety of the more popular output voltages and their typical applications. The same MTP50P03HDL MOSFET is used for all designs.

Output voltages below 2.0V dictate the use of a UC3832. The UC3832 enables the user to set the error amplifier voltage reference below 2.0V. In the UC3833 the noninverting error amplifier input is internally committed to 2.0V. For additional information regarding the UC3832/3 linear controllers, consult Unitrode application note U-116.

Additional information on HDTMOS MOSFETs and low impedance capacitors is available from Motorola (602-244-3377) and Sprague (603-224-1961) respectfully.

REFERENCES

[1] "Versatile UC1834 Optimizes Linear Regulator Efficiency", Application Note U-95, Unitrode Integrated Circuits, Merrimack, NH,1993-94.

[2] Mammano, R., Radovsky, J. and Harlan, G. "A New Linear Regulator Features Switch Mode Overcurrent Protection", Application Note U-116, Unitrode Integrated Circuits, Merrimack, NH,1993-94.

PARTS LIST:

Resistors	Capacitors	Transistors	Integrated Circuits
R1 = 0.022Ω	C1, C8 = 1µF	Q1 = MTP50P03HDL	U1 = UC3833
R2 = 200k	C2, C3 = 0.1µF		
R3, R8 = 100Ω	C4, C5, C6 = 270µF		
R4 = 300Ω	C7 = 33000pF		
R5 = 20Ω			
R6 = 1.3k			
R7 = 2.0k			

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UC3855A/B HIGH PERFORMANCE POWER FACTOR PREREGULATOR

James P. Noon
New Product
Applications Engineer

INTRODUCTION

The trend in power converters is towards increasingly higher power densities. Usually, the method to achieve this is to increase the switching frequency, which allows a reduction in the filter component's size. Raising the switching frequency however, significantly increases the system switching losses which generally precludes operating at switching frequencies greater than 100kHz.

In order to increase the switching frequency while maintaining acceptable efficiency, several soft switching techniques have been developed [1,2,3]. Most of these resonant techniques increase the semiconductor current and/or voltage stress, leading to larger devices and increased conduction losses due to greater circulating current. A new class of converters has been developed [4], however, that allow an increase in switching frequency without the associated increase in switching losses, while overcoming most of the disadvantages of the resonant techniques. Zero voltage transition (ZVT) converters operate at a fixed frequency while achieving zero voltage turn-on of the main switch and zero current turn-off of the boost diode. This is accomplished by employing resonant operation only during switch transitions. During the rest of the cycle, the resonant network is essentially removed from the circuit and converter operation is identical to its nonresonant counterpart.

This technique allows a improvement in efficiency over the traditional boost converter, as well as operating the boost diode with reduced stress (due to controlled di/dt at turn-off). Soft-switching of the diode also reduces EMI, an important system consideration.

Active power factor correction programs the input current of the converter to follow the line voltage and power factors of 0.999 with THD of 3% are possible. The Unitrode UC3855A/B IC incorporates power factor correction control circuitry capable of providing high power factor with several enhancements relating to current sensing and ZVT operation of the power stage.

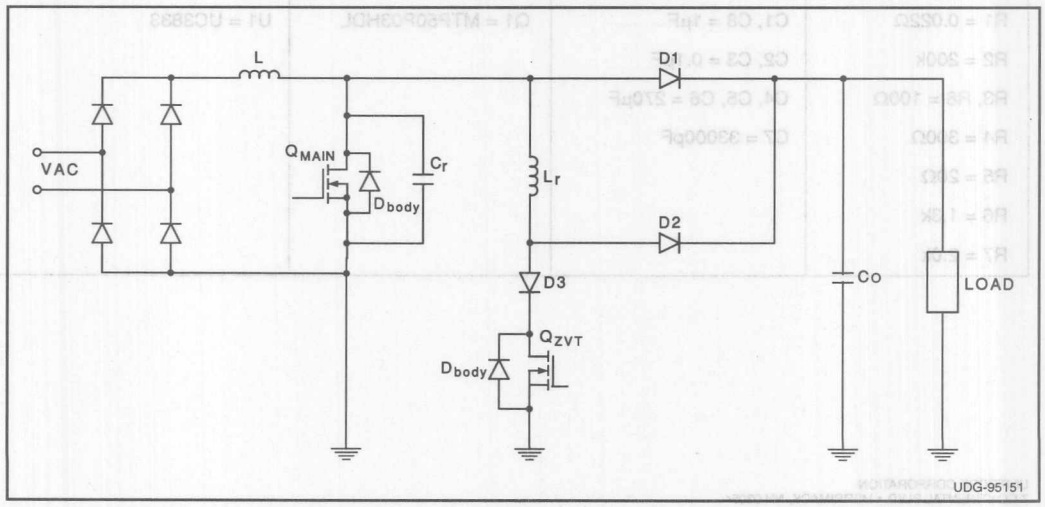


Figure 1. Boost Converter with ZVT Power Stage

The UC3855 incorporates all of the control functions required to design a ZVT power stage with average current mode control. Average current mode control has been chosen for its ability to accurately program the input current while avoiding the slope compensation and poor noise immunity of other methods [5,6].

ZVT TECHNIQUE

ZVT Boost Converter Power Stage

The ZVT boost converter operates the same as a conventional boost converter throughout its switching cycle except during the switch transitions. Figure 1 shows the ZVT boost power stage. The ZVT network, consisting of Q_{ZVT} , D2, L_r, and C_r, provides active snubbing of the boost diode and main switch. The ZVT circuit operation has been described in [4, 7, 8] and will be reviewed here for completeness. Referring to Figure 2, the following timing intervals can be defined:

ZVT Timing

$t_0 - t_1$ During the time prior to t_0, the main switch is off and diode D1 is conducting the full load current. At t_0, the auxiliary switch (Q_{ZVT}) is turned on. With the auxiliary switch on, the current in L_r ramps up linearly to I_{IN}. During this time the current in diode D1 is ramping down. When the diode current reaches zero the diode turns off (i.e. soft switching of D1). In the practical circuit some reverse recovery of the diode will occur since the diode needs time to remove the junction charge. The voltage across the ZVT inductor is V_O, and therefore the time required to ramp up to I_{in} is:

$$t_{01} = \frac{I_{IN}}{\left(\frac{V_O}{L_r}\right)}$$

$t_1 - t_2$ At t_1, the L_r current has reached I_{IN} and L_r and C_r will begin to resonate. This resonant cycle discharges C_r until its voltage equals zero. The dv/dt of the drain voltage is controlled by C_r (C_r is the combination of the external C_{DS} and C_{oss}). The current through L_r continues to increase while C_r discharges. The time required for the drain voltage to reach zero is 1/4 of the resonant period. At the end of this period the body diode of the main switch turns on.

$$t_{12} = \frac{\pi}{2} \bullet \sqrt{L_r C_r}$$

$t_2 - t_3$ At the beginning of this interval the switch drain voltage has reached 0V and the body diode is turned on. The current through the body diode is being driven by the ZVT inductor. The voltage

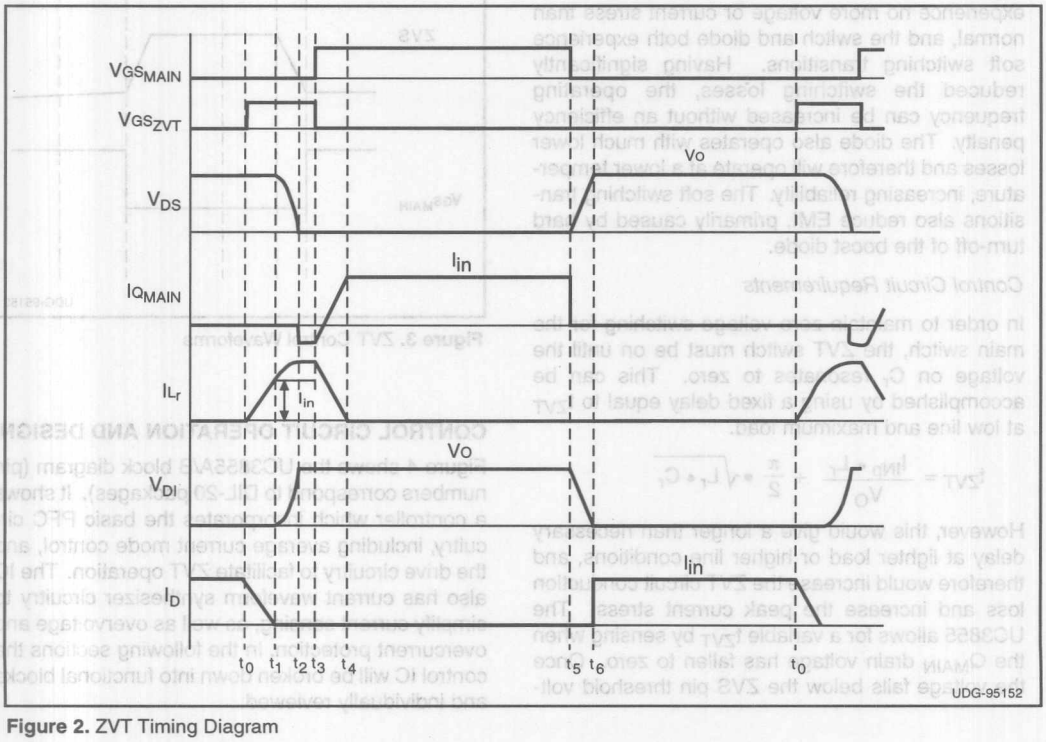


Figure 2. ZVT Timing Diagram

across the inductor is zero and therefore the current freewheels. At this time, the main switch can be turned on to achieve zero voltage switching.

t_3 - t_4 At t_3, the UC3855 senses that the drain voltage of Q_{MAIN} has fallen to zero and turns on the MAIN switch while turning off the ZVT switch. After the ZVT switch turns off, the energy in L_r is discharged linearly through D2 to the load.

t_4 - t_5 At t_4, the current in D2 goes to zero. When this occurs, the circuit is operating like a conventional boost converter. In a practical circuit however, L_r will resonate with C_{oss} of the ZVT switch driving the node at the anode of D1 negative (since the opposite end of L_r is clamped to zero). This effect will be discussed in the ZVT circuit design section.

t_5 - t_6 This stage is also exactly like a conventional boost converter. The main switch turns off. The Q_{MAIN} drain-to-source node capacitance charges to V_O and the main diode begins to supply current to the load. Since the node capacitance initially holds the drain voltage to zero, the turn off losses are significantly reduced.

It can be seen through the above description that the operation of the converter differs from the conventional boost only during the turn-on switch transitions. The main power stage components experience no more voltage or current stress than normal, and the switch and diode both experience soft switching transitions. Having significantly reduced the switching losses, the operating frequency can be increased without an efficiency penalty. The diode also operates with much lower losses and therefore will operate at a lower temperature, increasing reliability. The soft switching transitions also reduce EMI, primarily caused by hard turn-off of the boost diode.

Control Circuit Requirements

In order to maintain zero voltage switching for the main switch, the ZVT switch must be on until the voltage on C_r resonates to zero. This can be accomplished by using a fixed delay equal to t_{ZVT} at low line and maximum load.

$$t_{ZVT} = \frac{I_{INp} \bullet L_r}{V_O} + \frac{\pi}{2} \bullet \sqrt{L_r \bullet C_r}$$

However, this would give a longer than necessary delay at lighter load or higher line conditions, and therefore would increase the ZVT circuit conduction loss and increase the peak current stress. The UC3855 allows for a variable t_{ZVT} by sensing when the Q_{MAIN} drain voltage has fallen to zero. Once the voltage falls below the ZVS pin threshold voltage (2.5V), the ZVT gate drive signal is terminated and the main switch gate drive goes high. The control waveforms are shown in Figure 3. The switching period begins when the oscillator begins to discharge, and the ZVT gate drive goes high at the beginning of the discharge period. The ZVT signal will stay high until the ZVS pin senses the zero voltage condition or until the discharge period is over (the oscillator discharge time is the maximum ZVT pulse width). This allows the ZVT switch to be on only for as long as necessary.

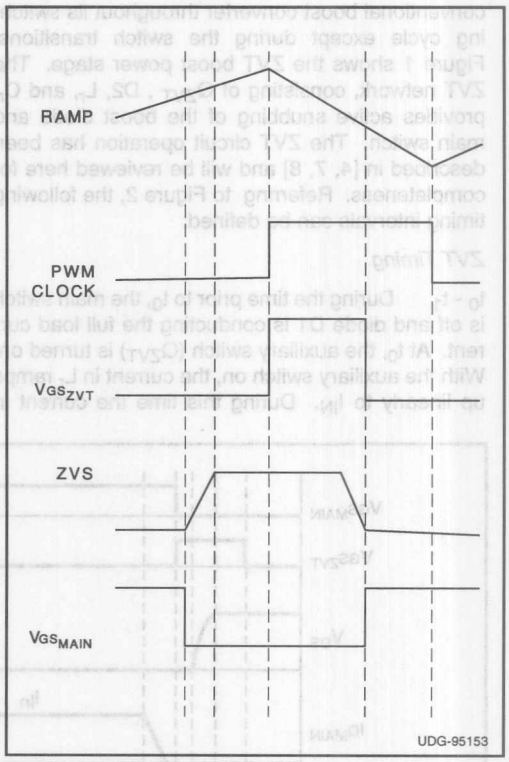


Figure 3. ZVT Control Waveforms

CONTROL CIRCUIT OPERATION AND DESIGN

Figure 4 shows the UC3855A/B block diagram (pin numbers correspond to DIL-20 packages). It shows a controller which incorporates the basic PFC circuitry, including average current mode control, and the drive circuitry to facilitate ZVT operation. The IC also has current waveform synthesizer circuitry to simplify current sensing, as well as overvoltage and overcurrent protection. In the following sections the control IC will be broken down into functional blocks and individually reviewed.

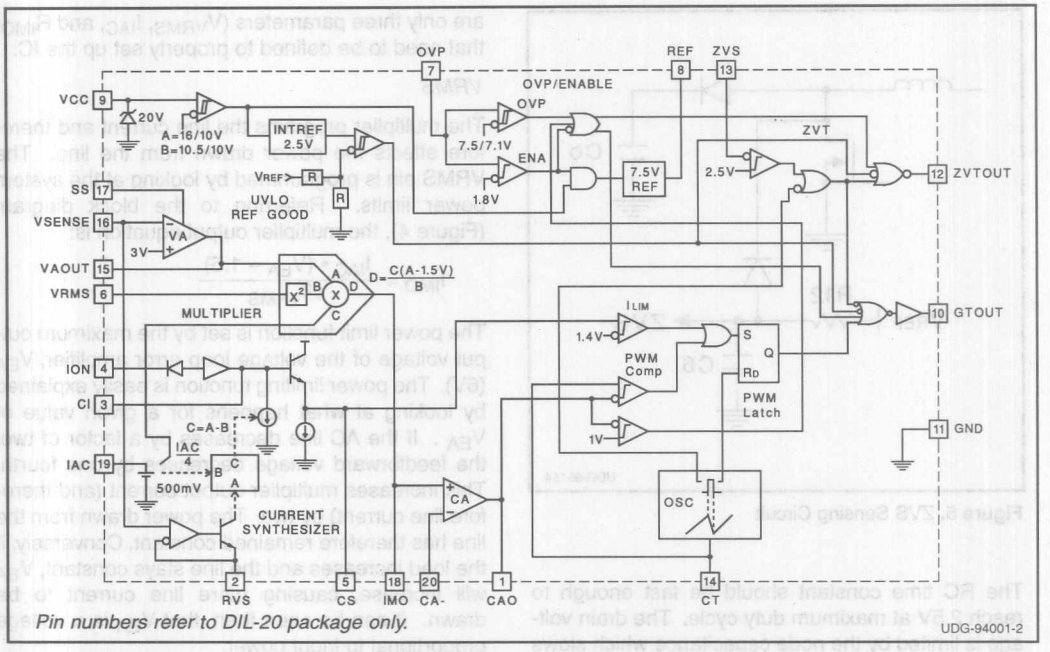


Figure 4. UC3855 Controller Block Diagram

Comparison with UC3854A/B

The PFC section of the UC3855A/B is identical to the UC3854A/B. Several common design parameters are highlighted below to illustrate the similarities.

FUNCTION	UC3854A/B	UC3855A/B
Enable	Dedicated pin	Incorporated into OVP
Design Range for V_{RMS}	1.5V - 4.7V	1.5V - 4.7V
V_{REF} for VA	3V	3V
Max. VA Output Voltage	6V	6V
Offset Voltage at IAC	0.5V	0.7V
Multiplier Gain	$\frac{IAC(VA - 1.5)}{V_{RMS}^2 \bullet IMO}$	$\frac{IAC(VA - 1.5)}{V_{RMS}^2 \bullet IMO}$

New features incorporated into the UC3855A/B include:

ZVT control circuitry
Overvoltage protection
Current Synthesizer

Oscillator

The oscillator contains an internal current source and sink and therefore only requires an external timing capacitor (CT) to set the frequency. The nominal charge current is set to 500µA and the discharge current is 8mA. The discharge time is approximately 6% of the total period, which defines the maximum ZVT time. CT is calculated by:

$$CT = \frac{1}{11200 \bullet F_S}$$

ZVT Control Circuit

As stated in the ZVT Technique section, the UC3855A/B provides the control logic to ensure ZVT operation over all line and load conditions without using a fixed delay. The ZVS pin senses the MOSFET drain voltage and is an input to the ZVT drive comparator. The other comparator input is internally biased to 2.5V. When the ZVS input is above 2.5V (and the PWM clock signal is present) the ZVT drive signal can go high. Pulling the ZVS pin low will terminate the ZVT drive signal and turn on the main switch output (recall that the maximum ZVT output signal is equal to the oscillator discharge time). The network used to sense the node voltage is shown in Figure 5. R12 pulls up the pin to a maximum of 7.5V, and C6 provides filtering.

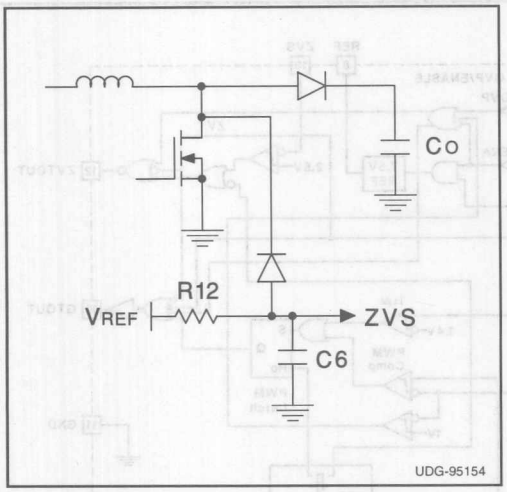


Figure 5. ZVS Sensing Circuit

The RC time constant should be fast enough to reach 2.5V at maximum duty cycle. The drain voltage is limited by the node capacitance which slows down the dv/dt across the main MOSFET, which reduces the high speed requirement on the ZVS circuit. The maximum ZVS pin voltage should be limited to V_{REF}, otherwise the ZVS circuitry can become latched and will not operate properly.

An alternative method for ZVS operation, is to sense the drain voltage through a simple voltage divider. This voltage will still have to be filtered (and clamped) however, so as not to inject noise into the ZVS pin.

Refer back to Figure 3 for the timing waveforms.

GATE DRIVES

The main drive can source $1.5A_{PK}$ and the ZVT drive is $0.75A_{PK}$. The main switch drive impedance requirements are reduced due to ZVT operation. At turn-on the drain voltage is at zero volts and therefore the Miller capacitance effect is not an issue, and during turn-off, the dv/dt is limited by the resonant capacitor. Since the ZVT MOSFET is generally at least two die sizes smaller than the main switch, its drive requirements are met with a lower peak current capability.

Multiplier / Divider Circuit

The multiplier section of the UC3855A/B is identical to the UC3854A/B. It incorporates input voltage feedforward (through the VRMS input) to eliminate loop gain dependence on the input voltage. There are only three parameters (V_{VRMS}, I_{IAC}, and R_{IMO}) that need to be defined to properly set up the IC.

VRMS

The multiplier programs the line current and therefore effects the power drawn from the line. The VRMS pin is programmed by looking at the system power limits. Referring to the block diagram (Figure 4), the multiplier output equation is:

$$I_{IMO} = \frac{I_{IAC} \bullet (V_{EA} - 1.5)}{V^2_{VRMS}}$$

The power limit function is set by the maximum output voltage of the voltage loop error amplifier, V_{EA} (6V). The power limiting function is easily explained by looking at what happens for a given value of V_{EA} . If the AC line decreases by a factor of two, the feedforward voltage decreases by one fourth. This increases multiplier output current (and therefore line current) by two. The power drawn from the line has therefore remained constant. Conversely, if the load increases and the line stays constant, V_{EA} will increase, causing more line current to be drawn. It can be seen then, that V_{EA} is a voltage proportional to input power.

Normally the multiplier is set to limit maximum power at low line, corresponding to maximum error amplifier output voltage. The multiplier equation can be solved for the feedforward voltage that corresponds to maximum error amplifier voltage and maximum multiplier current (internally limited to 2 times I_{IAC}).

$$V^2_{VRMS} = \frac{I_{IAC} \bullet (V_{EA} - 1.5)}{2 \bullet (I_{IAC})}$$

$$V_{VRMS} = 1.5V$$

Knowing the VRMS voltage at low line defines the voltage divider from the line to VRMS pin. This feedforward voltage must be relatively free of ripple in order to reduce the amount of second order harmonic that is present at the multiplier input (which in turn would cause 3rd order harmonics in the input current) [9]. The filtering will produce a dc voltage at the VRMS pin. Since the input voltage is defined in terms of its RMS value, the dc to RMS factor (0.9) must be taken into account [9]. For example, if the low line voltage is 85V, the attenuation required is:

$$\frac{85V_{RMS} \bullet (0.9)}{1.5 \bullet V_{DC}} = 51:1$$

At a high line of 270V, this will correspond to V_{VRMS} = 4.76V. The common mode range of the VRMS input is 0V to 5.5V. The calculated range is therefore within the accepted limits.

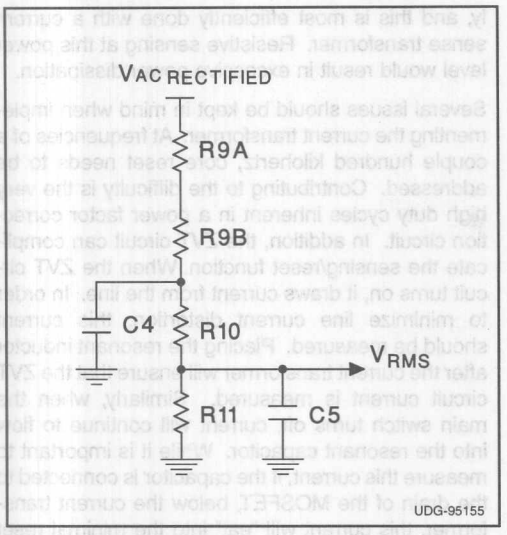


Figure 6. VRMS Circuit

A two pole filter is recommended to provide adequate attenuation without degrading the feedforward transient response. A single pole filter will require a pole at too low of a frequency to still allow VRMS to respond quickly enough to changes in line voltage.

The filter poles can be calculated once the distortion contribution from V_{RMS} is determined. If the feedforward circuit's contribution to the total distortion is limited to 1.5%, the required attenuation of the filter can be calculated. Recall that the percentage of 2nd harmonic in a full wave rectified sinewave is approximately 66.7% of the dc value. The percentage of second harmonic will translate to the same percent 3rd harmonic distortion in the input current waveform [9]. Therefore, the filter attenuation required is:

$$\frac{1.5\%}{66.7\%} = 0.0025$$

The individual stages should have an attenuation of $\sqrt{0.0225}$ or 0.15. For a single stage filter:

$$A_V = \frac{f_c}{f} \Rightarrow f_c = 120Hz\ (0.15) = 18Hz$$

Referring to Figure 6 the components correspond to R9A = R9B = 390kΩ, R10 = 120kΩ, and R11 = 18kΩ with C4 = 0.082µF and C5 = 0.47µF.

I_{IAC}

The value of I_{IAC} is chosen to be 500µA at high line. This value is somewhat arbitrary, however it should be kept below 1mA to stay within the linear region of the multiplier. This corresponds to a total resistance of approximately 766kΩ from the line to IAC pin.

R_{IMO}

The multiplier output resistor can be calculated by recognizing that at low line and maximum load current, the multiplier output voltage will equal 1V (in order to stay below the undercurrent trip point). This will also correspond to the maximum sense voltage of the current transformer. The multiplier current under this condition is equal to 1V / R_{IMO}, and can be equated with the multiplier equation which yields:

$$\frac{1V}{R_{IMO}} = \frac{I_{IAC} \bullet (V_{EA} - 1.5)}{V^2_{VRMS}}$$

At low line I_{IAC} will equal 156µA (if low line = 85V and I_{IAC} was set to 500µA at 270V), V_{EA} will be at its maximum of 6V, and V_{VRMS} will be 1.5V. Therefore R_{IMO} equals 3.2kΩ.

Current Synthesizer

Current sensing is simplified due to the current synthesis function built into the UC3855A/B. Switch current is the same as inductor current when the switch is on and can be sensed using a single current transformer. The current synthesizer charges a capacitor (CI) with a current proportional to the switch current when the switch is on. During the switch off-time, the inductor current waveform is reconstructed by the controller. To get an accurate measure of the inductor current then, all that is required is to reconstruct the down slope of the inductor current, which is given by:

$$\frac{\Delta i}{\Delta t} = \frac{V_{OUT} - V_{AC}}{L}$$

Discharging CI with a current proportional to $V_{OUT} - V_{AC}$ will allow reconstruction of the inductor current waveform. The capacitor down slope is :

$$\frac{\Delta v}{\Delta t} = \frac{I_{DIS}}{CI}$$

The UC3855A/B develops I_{DIS} by subtracting $I_{IAC}/4$, from a current proportional to V_{OUT}. The voltage at the RVS pin is regulated at 3V and therefore picking the RVS resistor will set the current proportional to V_{OUT}.

$$I_{DIS} = \frac{3V}{R_{RVS}} - \frac{I_{IAC}}{4}$$

The ratio of the current in R_{RVS} to $I_{IAC}/4$ should equal the ratio of V_{OUT} to V_{AC}. Therefore if

I_{IAC} / 4 is 125µA, the current through R_{RVS} should be set to 130µA.

$$R_{RVS} = \frac{3V}{130\mu A} = 23k\Omega, \text{ use } 22k\Omega$$

Equating inductor current slope with capacitor voltage slope, and recognizing that maximum slope occurs when V_{AC} equals zero, CI can be solved for:

$$CI = \frac{3 \bullet L \bullet N}{R_{RVS} \bullet V_{OUT} \bullet R_S}$$

where N is the current transformer (CT) turns ratio, (Ns / Np) and R_S is the current sense resistor.

The current synthesizer has approximately 20mV of offset. This offset can cause distortion at the zero crossing of the line current. To null out this offset, a resistor can be connected between VREF and the IMO pin. The resistor value is calculated based on R_{IMO} and the offset at the output of the synthesizer. For a 20mV offset and R_{IMO} = 3.3k a resistor from VREF to IMO of 1.2MΩ will cancel the offset.

Current Sensing

Current Transformer

As was seen in the previous section, synthesizing inductor current with the UC3855A/B is quite simple. Only switch current needs to be sensed directly, and this is most efficiently done with a current sense transformer. Resistive sensing at this power level would result in excessive power dissipation.

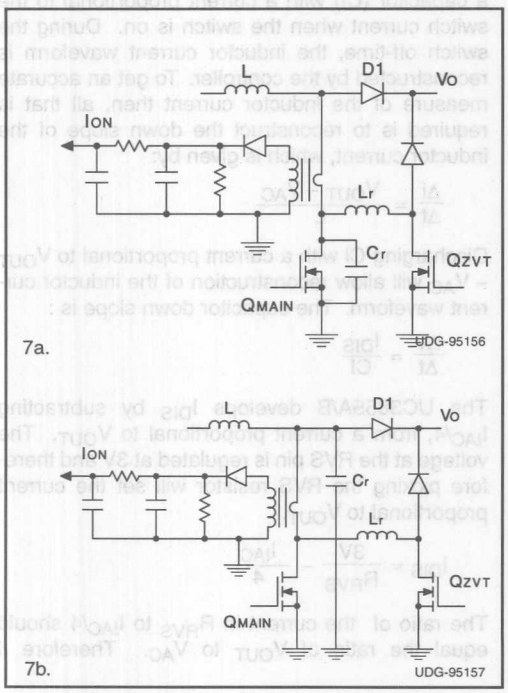


Figure 7. Current Transformer Sensing.

Several issues should be kept in mind when implementing the current transformer. At frequencies of a couple hundred kilohertz, core reset needs to be addressed. Contributing to the difficulty is the very high duty cycles inherent in a power factor correction circuit. In addition, the ZVT circuit can complicate the sensing/reset function. When the ZVT circuit turns on, it draws current from the line. In order to minimize line current distortion, this current should be measured. Placing the resonant inductor after the current transformer will ensure that the ZVT circuit current is measured. Similarly, when the main switch turns off, current will continue to flow into the resonant capacitor. While it is important to measure this current, if the capacitor is connected to the drain of the MOSFET, below the current transformer, this current will "eat" into the minimal reset time available at line zero crossings, where duty cycles are approaching 100%. This configuration is shown in Figure 7a. If the current transformer does not have enough time to reset, it can begin to saturate and lose accuracy, even if complete saturation is avoided, causing distortion at the zero crossings. A better configuration is shown in Figure 7b. In this circuit, the capacitor current will be measured when it discharges during the ZVT circuit on time. Since this occurs at the beginning of the switching cycle, the current transformer doesn't lose any of its reset time. Connecting C_r above the current transformer will not adversely affect the MOSFET dv/dt control. Since the IC is controlling average current, it doesn't matter whether the capacitor current is measured at the beginning or end of the switching cycle.

Figure 7 also shows that filtering is added to the transformer secondary in order to reduce noise filtering. The bandwidth of this filter should be low enough to reduce switching noise without degrading the switch current waveform.

In addition to position and reset considerations, actual current transformer construction must be considered. Using current transformers that have been designed and manufactured for operation at 20kHz will not give good performance at switching frequencies of 100kHz and greater. Low frequency designs generally have too much leakage inductance to be used for high frequency operation and can cause inaccurate sensing and/or noise problems.

Resistive Sensing

Resistive sensing is still possible with the UC3855A/B. Since both inputs to the current error amplifier are available to the user, resistive sensing

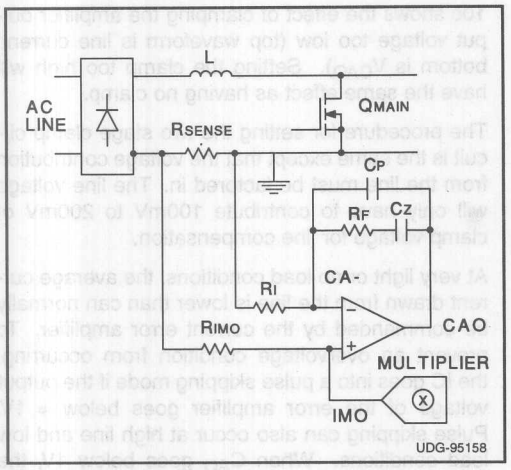


Figure 8. Resistive Sensing

is easy to implement. Figure 8 shows the typical configuration. The common mode range of the current error amplifier is –0.3V to 5.0V. The R_{IMO} value will remain the same as was calculated above if the maximum signal level remains at 1V. This will also allow the resistively sensed signal to be fed into ION and used for peak current limiting. It is recommended that the RVS resistor still be connected and a resistor connected from CS to ground in order to eliminate the possibility of noise being injected into these high impedance nodes.

Current Error Amplifier

The current error amplifier ensures that the input current drawn from the line follows the sinusoidal reference. The positive input to the amplifier is the multiplier output. The negative input is connected to the output of the current synthesizer (CS) through a resistor (usually the same value as R_{IMO}). The output of the current error amplifier is compared to the sawtooth waveform at the PWM comparator and terminates the duty cycle accordingly. At zero crossings of the line, the duty cycle will be at its maximum. Since the duty cycle is approaching 100%, proper reset of the current transformer will become increasingly difficult. Standard PWM controllers terminate the duty cycle during the oscillator discharge time, however, due to the ZVT operation, the UC3855A/B is capable of achieving 100% on-time. If the duty cycle is allowed to approach 100%, the current transformer will begin to saturate and cause the current error amplifier to "believe" that less current is being drawn from the line than is being commanded. This will cause the current amplifier to overcompensate, causing line current distortion at the zero crossings.

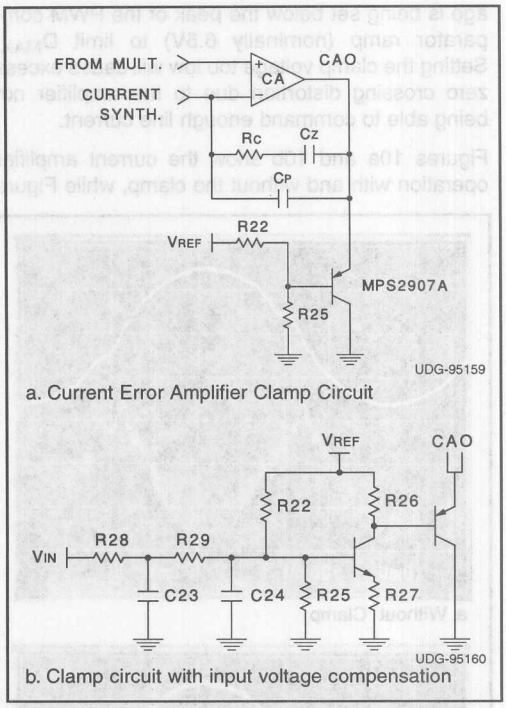


Figure 9. Clamp Circuit

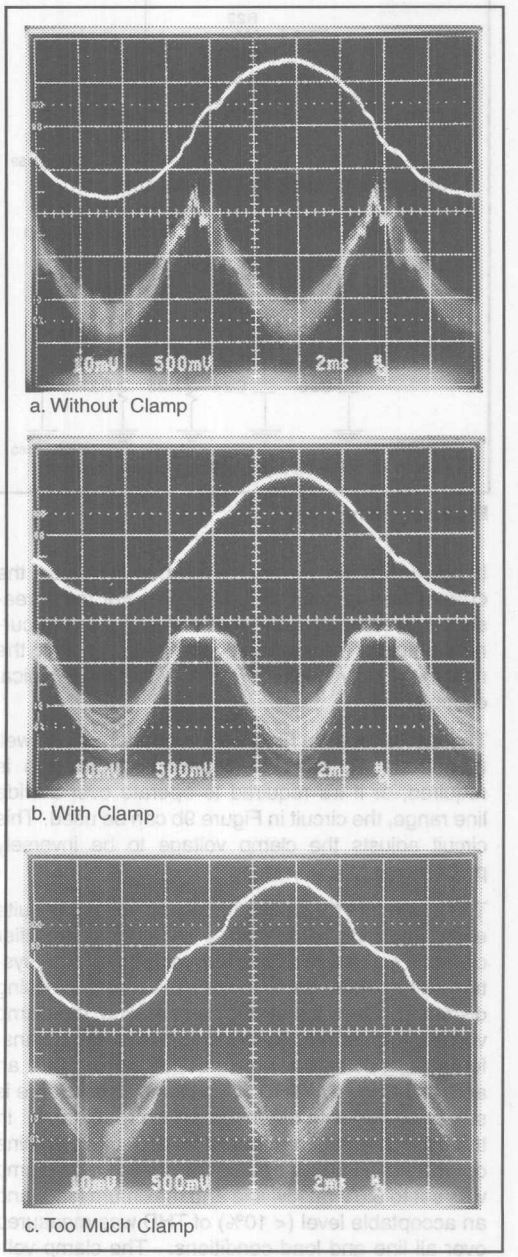
In addition, if the current transformer saturates, the current limiting function will be lost. For these reasons it is recommended that the output of the current amplifier be clamped externally, to limit the maximum duty cycle. Figure 9 shows a typical clamp circuit.

The clamp circuit in Figure 9a will perform quite well (see Table 1), however if better performance is required, or if it's required to operate over a wide line range, the circuit in Figure 9b can be used. This circuit adjusts the clamp voltage to be inversely proportional to line voltage.

The procedure for setting the clamp voltage is quite easy. If during initial startup the current amplifier clamp is set to a relatively low value (≈ 4V) the system will operate but with excessive zero crossing distortion. Once the system is operating, the clamp voltage can be increased until the current transformer is not saturating, and line current has an acceptable level of THD. Once the clamp voltage is set, operation with other ICs will be repeatable. In the experimental breadboard built for universal line operation and 500W output, the single stage clamp was set to 5.6V (at low line and maximum load) and an acceptable level (< 10%) of THD was measured over all line and load conditions. The clamp volt-

age is being set below the peak of the PWM comparator ramp (nominally 6.5V) to limit D_{MAX}. Setting the clamp voltage too low will cause excess zero crossing distortion due to the amplifier not being able to command enough line current.

Figures 10a and 10b show the current amplifier operation with and without the clamp, while Figure 10c shows the effect of clamping the amplifier output voltage too low (top waveform is line current, bottom is V_{CAO}). Setting the clamp too high will have the same effect as having no clamp.



a. Without Clamp

b. With Clamp

c. Too Much Clamp

Figure 10. C/A Clamp Circuit Effects on I Line

The procedure for setting the two stage clamp circuit is the same except that the voltage contribution from the line must be factored in. The line voltage will only have to contribute 100mV to 200mV of clamp voltage for line compensation.

At very light or no load conditions, the average current drawn from the line is lower than can normally be commanded by the current error amplifier. To prevent an overvoltage condition from occurring, the IC goes into a pulse skipping mode if the output voltage of the error amplifier goes below ≈ 1V. Pulse skipping can also occur at high line and low load conditions. When C_{AO} goes below 1V, the pulse skipping comparator is activated. The output of the comparator goes to an input of an OR gate in the OVP/ENABLE circuit, causing the output of that OR gate to go high. This signal prevents the ZVT and main gate drives from going high.

The procedure for compensating the current error amplifier will be covered in the Design Procedure section (IV).

Voltage Error Amplifier

The output voltage is sensed by the VSENSE input to the voltage error amplifier and compared to an internally generated reference of 3V. The output of the amplifier, V_{EA}, (at a given input voltage) will vary proportionally with output power. The output voltage range for the voltage error amplifier is approximately 0.1V to 6V. The output of the amplifier is one of the multiplier inputs, and an input voltage below 1.5V will inhibit the multiplier output. The design procedure for compensating the voltage loop will be outlined in the Design Procedure section.

Protection Circuitry

OVP/ENABLE

The UC3855A/B combines the enable and OVP function into one pin. It requires a minimum of 1.8V to enable the IC, and below this voltage, the reference is held low and the oscillator is disabled. A voltage above 7.5V will interrupt the gate drive. The resistor divider should be sized for 7.5V when an over voltage condition is reached, this will allow startup at a reasonable line voltage. For example, if an overvoltage condition is defined as an output voltage exceeding 450V, then the voltage divider from V_{OUT} to the OVP pin is 60:1. This divider will allow startup at a line voltage of $76V_{RMS}$ ($108V_{PK}$).

Current Limit

The UC3855A/B has pulse by pulse current limiting. The multiplier power limit determines the maximum average power drawn from the line. However, during transients or overload conditions, a peak current limiting function is necessary. This function is implemented by sensing the switch current and feeding this value into ION, to a current limiting comparator that terminates the gate drive signal if the switch current signal exceeds 1.5V (nominal).

Soft Start

In order to ensure a smooth, controlled startup, the UC3855A/B provides a soft-start (SS) function. The SS pin sources 1.5μA into an external capacitor. This capacitor limits the supply voltage to the voltage loop error amplifier, which effectively limits the output voltage of the amplifier and therefore the maximum commanded output voltage. This allows the output voltage to ramp up in a controlled fashion.

Undervoltage Lockout

The UC3855A has a 15.5V (nominal) turn-on threshold with 6V of hysteresis while the UC3855B turns on at 10.5V with 0.5V of hysteresis.

TYPICAL APPLICATION

A typical application will be designed in order to illustrate the design procedure and highlight the design parameters that need to be defined. The design specifications are:

- V_{IN} = 85 - 270 VAC
- V_O = 410 VDC
- P_{omax} = 500W
- F_S = 250kHz
- Eff > 95%
- Pf > 0.993
- THD < 12%

The above specifications represent a common universal input voltage, medium power application. The switching frequency of 250kHz is now possible due to the soft switching, zero voltage transitions. The Pf and THD numbers correspond to achievable line correction with the UC3855.

Design Procedure

This design procedure is a summary of what was presented in [8]. However, several values have been changed in order to consolidate component values and/or specify more readily available parts.

1. Power Stage Design

Inductor Design

The power stage inductor design in a ZVT converter is identical to the conventional boost converter. The inductance required is determined by the amount of switching ripple desired, and allowing more ripple will reduce the inductor value. The worst case for peak current occurs at low line, maximum load. Peak power is equal to twice the average power and V_{PK} is $\sqrt{2}\,V_{RMS}$. To calculate input current, assume an efficiency of 95%.

$$I_{PK} = \frac{2 \bullet P_{IN}}{\sqrt{2} \bullet V_{INmin}} = \frac{\sqrt{2} \bullet \left(\frac{500}{0.95}\right)}{85}$$

$$= 8.7A \text{ (60Hz component)}$$

A good compromise between current ripple and peak current is to allow a 20% ripple to average ratio. This will also keep the peak switch current less than 10A.

$$\Delta I_L = 0.2 \bullet (8.7A) = 1.7A_{pp}$$

Rearranging the conversion ratio for the boost converter to solve for D yields :

$$D = \frac{V_O - V_{IN}}{V_O} = \frac{410 - \sqrt{2} \bullet 85}{410} = 0.71$$

We can now calculate the required inductance.

$$L = \frac{V_{IN} \bullet D \bullet T_S}{\Delta I} = \frac{\sqrt{2} \bullet 85V \bullet (0.71 \bullet 4\mu s)}{1.7A}$$

$$= 200\mu H$$

Output Capacitor Selection

The value of output capacitor effects both hold-up time and output voltage ripple. If hold up time (t_H) is the main criteria, the following equation will give a value for C_O:

$$C_O = \frac{2 \bullet P_O \bullet t_H}{V_O^2 - V^2_{MIN}}$$

In this example a compromise between holdup time and capacitor size was made and a capacitor value of 440μF was selected. The capacitor bank consists of two 220μF, 450V DC capacitors in parallel.

Power MOSFET & Diode Selection

The main MOSFET selected is an Advanced Power Technology's APT5020BN (or equivalent). This is a

500V, 23A device, with $R_{DS(on)}$ = 0.20Ω (25°C) and C_{OSS} ≈ 500pF in a TO-247 package. A 5.1Ω resistor is placed in series with the gate to damp any parasitic oscillations at turn-on with a Schottky diode and 2.7Ω resistor in parallel with the resistor to speed up turn-off. A Schottky is also placed from GTOUT to ground to prevent the pin from being driven below ground, and should be placed as close to the IC as possible.

The boost diode selected is the International Rectifier HFA15TB60, a 15A, 600V ultrafast diode (or equivalent). Recall that a converter employing ZVT benefits from soft switching of the diode. With ZVT, the boost diode has a negligible impact on switching losses, and therefore a slower diode could potentially be used. However, there are still valid reasons for using an ultra fast diode in this application.

The ZVT inductor is sized according to the recovery time of the diode, and a slower diode will require a larger inductor. This will require a correspondingly longer Q_{ZVT} on-time, which increases conduction loss. A larger inductor will also require a longer time to discharge. To ensure complete discharge of the resonant inductor, the main switch minimum on-time should be approximately equal to the ZVT circuit on-time. This yields:

$$D_{MIN} = \frac{t_{01} + t_{12} + t_{rr}}{T}$$

D_{MIN} effects the minimum allowable output voltage for the boost converter to continue operating. The ZVT circuit on-time is a strong function of t_{rr}, and therefore choosing an ultra fast diode will keep the resonant circuit losses to a minimum and cause the least impact on the output voltage. The effective system duty cycle is primarily a function of the main switch on-time, since for a large portion of the resonant circuit's on-time, the voltage at the anode of the boost diode is held up by the resonant capacitor.

These considerations suggest a diode with a recovery time less than 75ns. Average output current in this design is less than 1.2A with a peak current of 9.2A. The conduction loss associated with the diode is approximately 2.2W.

While an ultra fast diode is being used, the diode is operating with significantly reduced switching losses. This will increase the overall system efficiency and reduce the peak stress of the diode.

2. ZVT Circuit Design

Resonant Inductor

The ZVT circuit design is straightforward. The circuit is performing an active snubber function and, as such, the inductor is designed to provide soft turn off of the diode. The ZVT capacitor is selected to provide soft switching of the MOSFET.

The resonant inductor controls the di/dt of the diode by providing an alternate current path for the boost inductor current. When the ZVT switch turns on, the input current is diverted from the boost diode to the ZVT inductor. The inductor value can be calculated by determining how fast the diode can be turned off. The diode's turn-off time is given by its reverse recovery time. Calculating an exact value for L_r is difficult due to the variation in reverse recovery characteristics within the actual circuit as well as variations in how reverse recovery is specified from manufacturer to manufacturer. An example of circuit conditions effecting the reverse recovery is the natural snubbing action of the resonant capacitor, which limits the dv/dt at the anode of the diode. A good initial estimate is to allow the inductor current to ramp up to the diode current within three times the diode's specified reverse recovery time. One constraint on the maximum inductance value is its affect on the minimum duty cycle. As was shown in the diode selection section, the L-C time constant effects D_{MIN} and therefore V_{Omin}. Making L_r too large will also increase the conduction time of the ZVT MOSFET, increasing the resonant circuit conduction losses. As the value of L_r is reduced, the diode will experience more reverse recovery current, and the peak current through the inductor and ZVT MOSFET will increase. As the peak current is increased, the amount of energy stored in the inductor will also increase ($E = 1/2 \bullet L \bullet I^2$). This energy should be kept to a minimum in order to reduce the amount of parasitic ringing in this node at turn-off.

The reverse recovery of the diode is partially a function of its turn-off di/dt. If a controlled di/dt is assumed, the reverse recovery time of this diode can be estimated to be approximately 60ns. If the inductor limits the rise time to 180ns ($3 \bullet t_{rr}$), the inductance can be calculated.

$$\frac{di}{dt} = \frac{I_{INp}}{3 \bullet t_{rr}} = 53A/\mu s$$

$$I_{INp} = I_{pk} + \frac{1}{2} \Delta I$$

$$L_r = \frac{V_O}{di/dt} = \frac{410V}{53A/\mu s} = 7.7\mu H$$

The inductor design is limited by core loss and resultant temperature rise, not saturating flux density. This is due to the high AC current component and the relatively high operating frequency. A good design procedure is outlined in [10] and is beyond

the scope of this review. Several points will be mentioned however. The core material should be a good high frequency, low loss material such as gapped ferrite or molypermalloy powder (MPP). Powder iron cores will generally not be acceptable in this application. The less expensive Magnetics Kool Mu material, although exhibiting higher losses than the MPP material, can also be used. The higher loss material will actually tend to damp the resonant ringing at the turn off of the ZVT switch. The inductor winding construction is also optimized by keeping interwinding capacitance to a minimum. This reduces the node capacitance at turn off and reduces the amount of damping required.

The inductor current can by found by analyzing the resonant circuit formed by L_r and C_r and recognizing that the resonant cycle begins when the current reaches I_{IN}.

$$I_{L_r} = I_{IN} + \frac{V_O}{Z_n} \bullet \sin\omega t$$

$$\text{where } Z_n = \sqrt{L_r / C_r}\ , \ \omega = \sqrt{\frac{1}{L_r \bullet C_r}}$$

The peak current then is equal to I_{IN} plus the output voltage divided by the resonant circuit's characteristic impedance. Decreasing L_r or increasing C_r will increase the peak current. The inductor was designed using a Magnetics, Inc. MPP core 55209 with 33 turns for an inductance of 8µH. The inductor should be constructed with Litz wire or several strands of small magnet wire to minimize high frequency effects.

Resonant Capacitor

The resonant capacitor is sized to ensure a controlled dv/dt of the main switch. The effective resonant capacitor is the sum of the MOSFET capacitance and the external node capacitance. The APT5020BN has approximately 500pF of output capacitance, and an external capacitance of 500pF was added across the device. This capacitor limits the dv/dt at turn-off and consequently reduces the Miller effect. In addition, it reduces turn-off losses since the switch current is diverted to the capacitor. The capacitor must be a good high frequency capacitor, and low ESR and ESL are required. It must also be capable of handling the relatively large charging current at turn-off. Two good choices are polypropolene film or a ceramic material.

This combination of L and C yields a resonant quarter cycle of:

$$\frac{\pi}{2} \sqrt{L_r \bullet C_r} = 140\text{ns}$$

The resonant circuit's impact on the output voltage can now be calculated. Recall that to ensure discharge of the resonant inductor at high line:

$$D_{MIN} = \frac{t_{01} + t_{12} + t_{rr}}{T} \quad (1)$$

and for a boost converter:

$$V_{OMIN} = \frac{V_{INpk}}{1 - D_{MIN}} \quad (2)$$

Substituting (1) into (2) and solving for V_O produces:

$$V_{OMIN} = \frac{(L_r \bullet I_{INp} + V_{INp} \bullet T}{\left(T - t_{rr} - \frac{\pi}{2} \bullet \sqrt{L_r \bullet C_r}\right)} \quad (3)$$

Equation (3) can be solved using the previously established values and yields a minimum output voltage of 405V. This suggests a design value of 410V for V_O.

ZVT Switch and Rectifier Selection

The ZVT switch also experiences minimal turn-on loss due to the discharge of its drain-to-source capacitance. However, it doesn't experience high current and voltage overlap since the turn-on current is limited by the resonant inductor. The switch does experience turn-off and conduction losses however. Although the peak switch current is actually higher than the main switch current, the duty cycle is small, keeping conduction losses low. The ZVT switch will be one or two die sizes smaller than the main switch due to the low average drain current. The ZVT switch on-time is :

$$t_{ZVT} = \frac{I_{INp} \bullet L_r}{V_O} + \frac{\pi}{2} \bullet \sqrt{L_r C_r}$$

The peak ZVT switch current is equal to the peak ZVT inductor current. A conservative approximation of the switch RMS current is made by assuming a square wave signal. The RMS of the current is approximated by:

$$I_{RMS} \approx I_{L_{rpk}} \bullet \sqrt{\frac{t_{ZVT}}{T}}$$

This corresponds to a peak of approximately 14A at maximum load and maximum ZVT on-time, however, the RMS is only 3.9A. An appropriate device in this application is the Motorola MTP8N50E, a 500V, 8A device with an $R_{DS(ON)}$ of 0.8Ω. As with the main MOSFET, a 5.1Ω resistor is placed in series with the gate to damp any parasitic oscillations at turn on and a Schottky diode and resistor is placed in parallel with the resistor to speed up turn-off. A Schottky is also placed from ZVTOUT to ground to

prevent the pin from being driven below ground. This diode should be placed as close to the IC as possible.

The rectifiers needed for the ZVT circuit also experience relatively low RMS current. Diode D2 returns the energy stored in the resonant inductor during t_{ZVT} to the load. D2 should be an ultra-fast recovery diode and is usually chosen to be of similar speed as D1. The diode selected for D2 is a Motorola MURH860; a 600V device with a $t_{rr} \approx 35$ns.

Diode D3 blocks current from flowing up through the Q_{ZVT} body diode when the inductor resets, it sees the same peak and RMS current as Q_{ZVT}. D3 should be a fast recovery diode to decouple the drain to source capacitance of Q_{ZVT} from the resonant inductor. Energy stored in the D3 anode node capacitance will resonate with the ZVT inductor when the ZVT switch turns off. Minimizing this effect will reduce the amount of snubbing required at this node. The diode chosen here was the MUR460. This is a 600V, 4 amp device with $t_{rr} \approx 75$ns.

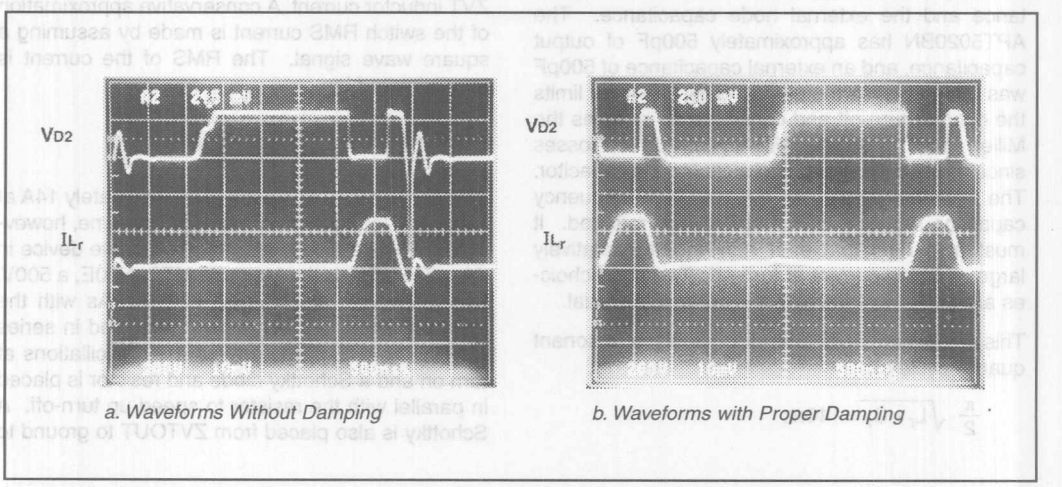
To summarize, both diodes in the ZVT circuit experience low RMS current. The main selection criteria in addition to the blocking voltage (in both cases equal to V_O) is reverse recovery time. Choosing devices with fast recovery times will reduce parasitic oscillations, losses, and EMI.

ZVT Snubber Circuit

The ZVT circuit requires some method for damping the parasitic oscillations that occur after the ZVT inductor current goes to zero. Figure 10a shows the ZVT inductor current and diode D2 anode voltage without adequate damping. The figure shows that as the inductor current begins to discharge (when Q_{ZVT} turns off) to the output, the anode voltage is at V_{OUT} (since D2 is conducting). As the inductor current passes through zero, the voltage rings negative since the opposite end of the inductor is clamped to 0V through the main switch body diode. The anode voltage can easily ring negatively to twice the output voltage. This increases the reverse voltage stress on the diode to three times the output voltage! Keeping the energy in the node capacitance to a minimum and using fast recovery diodes will reduce the ringing and improve the circuit performance.

Several methods of damping this oscillation have been proposed [4,7]. In this circuit two methods, the saturable reactor and resistive damping were investigated. A 51Ω, 10W noninductive resistor was connected through a diode from ground to the anode of D2. The saturable reactor was placed in series with the resonant inductor and implemented with 8 turns on a Toshiba saturable core SA 14 x 8 x 4.5. The resistive damping method prevents the node from oscillating. However, it does not prevent current from flowing in D2 while D1 is conducting (due to the dv/dt across L_r when Q_{MAIN} turns off). If current flows through D2 during this time it will experience reverse recovery current when Q_{ZVT} turns on. The saturable reactor prevents this current flow due to its high impedance. L_S also decouples L_r from the node capacitance, which prevents the node from oscillating.

The saturable reactor works well without the resistive damping and was the method chosen in this design. With the saturable reactor damping the circuit properly, the resistive damping can be eliminated. However, since L_S is designed to saturate each switching cycle, the core loss is largely material dependent and can cause significant temperature



a. Waveforms Without Damping

b. Waveforms with Proper Damping

Figure 11. ZVT Ringing Waveforms

rise of the core. In this circuit, heatsinking of the core was required. An alternative design was also tried using the larger MS 18 x 12 x 4.5 which ran cooler although it also required heatsinking. Optimization of this circuit can significantly reduce the losses in the ZVT circuit. In this design, damping network losses were approximately 2W. Figure 10b shows the same circuit condition with the node damped with L_S.

ZVS Circuit

The ZVS circuit components are chosen next. In this example, a 1kΩ resistor is used to pull up the ZVS pin. The capacitor chosen is 500pF. This combination will require approximately 200ns to charge up to the 2.5V threshold.

$$t = -R \bullet C \bullet ln\left(\frac{1-V_{THRESHOLD}}{V_{REF}}\right)$$

3. Oscillator Frequency

Calculate CT:

The switching frequency selected is 250kHz.

$$CT = \frac{1}{11200 \bullet 250kHz} = 357pF, \text{ use } 330pF$$

4. Multiplier/Divider Circuit

Calculate the VRMS resistor divider:

Set VRMS = 1.5V at low line ($85V_{RMS}$)

$$\text{divider} = \frac{85V_{RMS} \bullet 0.9}{1.5\ V_{DC}} = 51{:}1$$

The voltage divider can be solved if one of the resistors is defined (since there are two equations and three unknowns). Letting the lower resistor in the divider = 18kΩ:

$$R_{TOTAL} = 18k\Omega \bullet 51 = 918k\Omega$$

Letting R10 = 120kΩ, gives:

$$R9 = 918k\Omega - 120k\Omega - 18k\Omega = 780k\Omega$$

R9 is split into two resistors (each 390kΩ) to reduce their voltage stress.

Calculate the capacitor values to place the filter poles at 18Hz:

$$C5 = \frac{1}{2\pi \bullet f_P \bullet R11} = \frac{1}{2\pi \bullet 18Hz \bullet 18k\Omega}$$

$$= 0.49\mu F, \text{ use } 0.47\mu F$$

$$C4 = \frac{1}{2\pi \bullet f_P \bullet R_{eq}} = \frac{1}{2\pi \bullet 18Hz \bullet 117k\Omega}$$

$$= 75nF, \text{ use } 0.082\mu F$$

where $R_{eq} = R9||(R10 + R11) = 117k\Omega$

In order to consolidate capacitor values C4 could be chosen to be 0.1μF without degrading the system performance.

Calculate the IAC resistor:

Set $I_{IAC} = 500\mu A$ at high line.

$$R = \frac{\sqrt{2} \bullet 270V}{500\mu A} = 764k\Omega$$

Use 2, 390kΩ resistors in series to reduce voltage stress.

Calculate R_{IMO}:

At low line $I_{IAC} = 156\mu A$ and the output of the multiplier should equal 1V. With low line and maximum load, V_{EA} will be at its maximum of 6V, therefore, using the multiplier output equation:

$$\frac{1V}{R_{IMO}} = \frac{I_{IAC} \bullet (V_{EA} - 1.5)}{V_{VRMS}^2}$$

$$R_{IMO} = \frac{1.5^2}{156\mu A \bullet (6 - 1.5)} = 3.2k\Omega, \text{ use } 3.3k\Omega$$

A 1000pF capacitor is placed in parallel with R_{IMO} for noise filtering. Since the voltage across R_{IMO} is the output of the multiplier and is the reference for the current error amplifier, the RC pole frequency should be placed well above the 120Hz multiplier signal.

5. Current Synthesizer

First, chose a turns ratio for the current transformer. The current transformer is designed to produce 1V at peak input current. This allows sufficient margin before the current limit trip point (1.4V) is reached. If $I_{PK} = 9.5A$ a turns ratio of 50 : 1 would be appropriate. This turns ratio will keep the sense network losses less than 150mW and allow the use of a 1/4 watt resistor. Solving for the sense resistor yields:

$$R_S = \frac{1V}{\frac{I_{sw}}{N}} = \frac{1V}{\frac{9.5}{50}} \approx 5.1\Omega$$

Recall from the previous current synthesizer section that R_{VS} = 22kΩ. The current synthesizer capacitor can now be calculated:

$$CI = \frac{3 \bullet L \bullet N}{R_{VS} \bullet V_{OUT} \bullet R_s}$$

$$= \frac{3 \bullet 200\mu H \bullet 50}{22k\Omega \bullet 410V \bullet 5.1\Omega} = 633pF, \text{ use } 680pF$$

6. Control Loop Design

Small Signal Model

The small signal model of the ZVT PFC boost converter is similar to the standard PFC boost converter model. The two converters operate exactly the

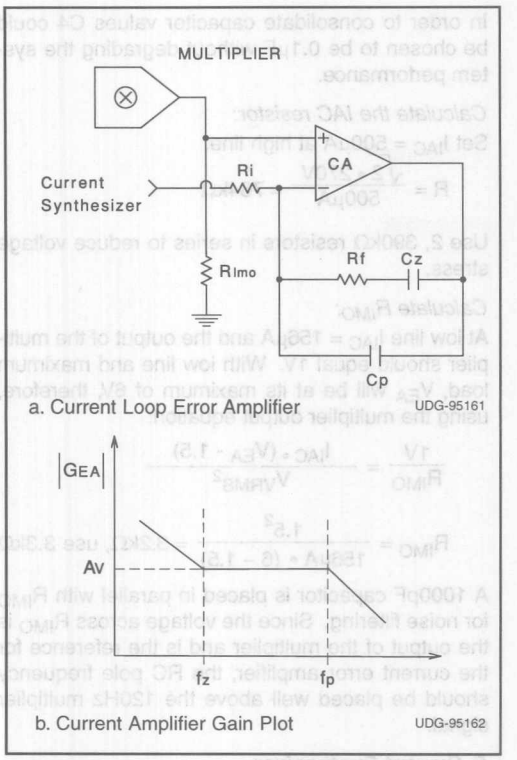


Figure 12. Current Error Amplifier Schematic

same throughout most of the switching cycle and only during the switching transitions is there any difference. This allows the design of the control loops to proceed following the standard techniques outlined in [9].

Current Loop Design

Excellent references on the current loop design are found in [5,9,11]. The design of the average current mode control loop begins with choosing a cross-over frequency. In this example the switching frequency is 250kHz, so the unity gain cross over frequency could be chosen to be as high as 40kHz (1/6 of the switching frequency). In this circuit however, the cross over is chosen to be 10kHz. Since the main job of the current loop is to track the line current, a 10kHz bandwidth is quite adequate for this application.

Once the cross over frequency (f_c) is known, the next thing to do is calculate the gain of the power stage. The small signal model of the power stage including the current sense network is given below. This model does not include the sampling effect at one half the switching frequency [12] but is a good approximation at the frequencies of interest.

$$G_{id}(s) = \frac{V_O \bullet R_{SENSE}}{s \bullet L \bullet V_{SE}}$$

The UC3855A/B has an oscillator ramp of $5.2V_{pp}$ (V_{SE}). The R_{SENSE} term, is the attenuation from actual input current to sensed current (i.e. it includes the current transformer turns ratio). Using the previously determined component values and solving for the power stage gain at f_c yields a gain of 0.63 at 10kHz. In order to have a gain of 1 at f_c, the error amplifier must have a gain of 1/0.63 at 10kHz. The error amplifier is shown in Figure 12a with the frequency response in Figure 12b. The resistor Ri is equal to 3.3kΩ so the feedback resistor is chosen to be 5.6kΩ. A zero is placed at the cross over frequency to give a phase margin of 45 degrees. To reduce switching noise a pole is placed at one-half the switching frequency. The following summarizes the design procedure.

1. $$|G_{id}(s)| = \frac{410V \bullet 0.10}{2 \bullet \pi \bullet 10kHz \bullet 200\mu H \bullet 5.2} = 0.63$$

2. $$G_{EA} = \frac{1}{|G_{id}(s)|} = 1.58 \Rightarrow Av = \frac{R_f}{R_i}$$

$$\therefore R_f = \frac{R_i}{|G_{id}(s)|} \approx 5.6k\Omega$$

3. $$f_z = f_c = \frac{1}{2 \bullet \pi \bullet R_f \bullet C_z}$$

$$C_Z = \frac{1}{2 \bullet \pi \bullet 10kHz \bullet 5.6k\Omega} \approx 2200pF$$

4. $$f_p = \frac{1}{2 \bullet \pi \bullet R_f \left(\frac{C_z \bullet C_p}{C_z + C_p}\right)} = \frac{1}{2 \bullet \pi \bullet R_f \bullet C_p}$$

$$C_p = \frac{1}{2 \bullet \pi \bullet 5.6k\Omega \bullet 125kHz} \approx 220pF$$

Voltage Loop Design

The design of the voltage loop follows the procedure given in [5]. The first step is to determine the amount of ripple on the output capacitor.

$$V_{Opk} = \frac{P_{IN} \bullet X_{Co}}{V_O}$$

$$V_{Opk} = \frac{525}{2 \bullet \pi \bullet 120 \bullet 410\mu \bullet 410} = 4.14V_{PK}$$
$$= 8.3V_{pp}$$

In order to meet the 3% THD specification, the distortion due to output ripple voltage feeding through the voltage error amplifier will be limited to 0.75%. This allows 1.5% from the multiplier and 0.75% from miscellaneous sources. A 1.5% second harmonic on the error amplifier will result in 0.75% 3 rd harmonic distortion at the input. At full load, the peak error amplifier ripple voltage allowed is:

$$V_{EApk} = \%\,ripple \bullet V_{VEA} = 0.015 \bullet (6 - 1)$$
$$= 0.075V$$

The error amplifier gain at 120Hz is the allowable error amplifier ripple voltage divided by the output ripple voltage, or 0.009 (–41 dB). The error amplifier input resistor was chosen to be 1.36MΩ to keep power dissipation low and allow a small value for the compensation capacitor. Two 681kΩ resistors in series are used to reduce the voltage stress. The voltage error amplifier schematic is shown in Figure 13, with the 120Hz gain determined by the integrator function of C_f and R_i. This network has a single pole role off and the capacitor value is easily found to give the desired gain at 120Hz.

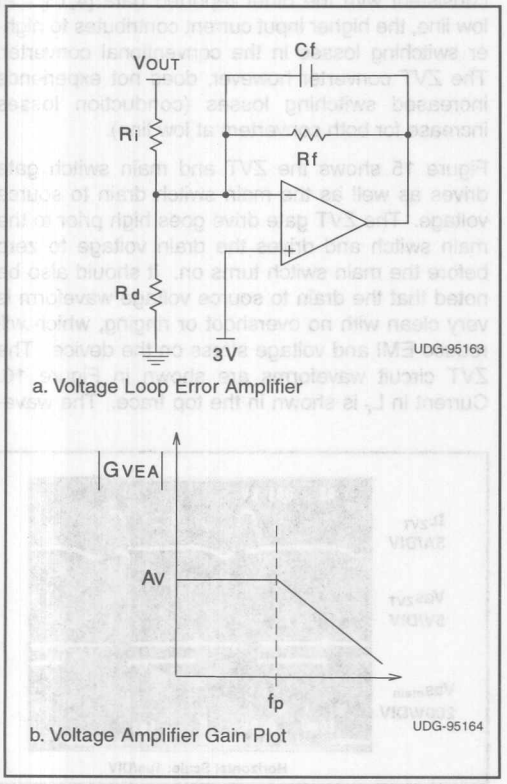


Figure 13. Voltage Error Amplifier

$$C_f = \frac{1}{2 \bullet \pi \bullet f \bullet G_{VEA} \bullet R_i}$$

$$C_f = \frac{1}{2 \bullet \pi \bullet 120Hz \bullet 0.009 \bullet 1.36M\Omega}$$

$$\approx 0.1\mu F$$

The crossover frequency can now be calculated recognizing that a pole (due to the combination of C_f and R_f) will be placed at the cross over frequency to provide adequate phase margin. The pole placement will determine the phase margin since the power stage has a single pole response with the associated 90 degree phase lag. If the error amplifier pole is placed at the crossover frequency, the overall loop gain will have a 45 degree phase margin. The power stage gain is given by:

$$G_{PS}(s) = \frac{V_o}{V_{VEA}} = \frac{P_{IN}}{\Delta V_{EA} \bullet V_o \bullet (s \bullet C_o)}$$

The voltage loop gain (T_V) is the product of the power stage gain and the error amplifier gain. To find the cross over frequency, solve for f and set equal to 1.

$$T_V = 1 = G_{PS}(s) \bullet G_{VEA}(s)$$

The error amplifier gain is:

$$G_{VEA} = \frac{-j}{2 \bullet \pi \bullet f \bullet R_i \bullet C_f} = \frac{-j \bullet 1.17}{f}$$

$$\therefore T_V = 1 = \frac{-j \bullet 92.6}{f} \bullet \left(\frac{-j \bullet 1.17}{f}\right) = \frac{108}{f^2}$$

The cross over frequency then is approximately 11Hz, so the resistor, R_f, can be calculated to place the pole at f_c.

$$R_f = \frac{1}{2 \bullet \pi \bullet 11Hz \bullet 0.1\mu F} \approx 140k\Omega$$

Finally, the resistor R_D (10kΩ) sets the DC output voltage to 410V.

7. OVP/ENABLE

An output voltage exceeding 450V is defined as an overvoltage condition. To trip the OVP comparator at 450V requires a divider of:

$$\frac{7.5V}{450V} = 60:1$$

Letting the lower resistor in the divider = 33kΩ, the top resistor then is 2MΩ, two 1MΩ resistors are

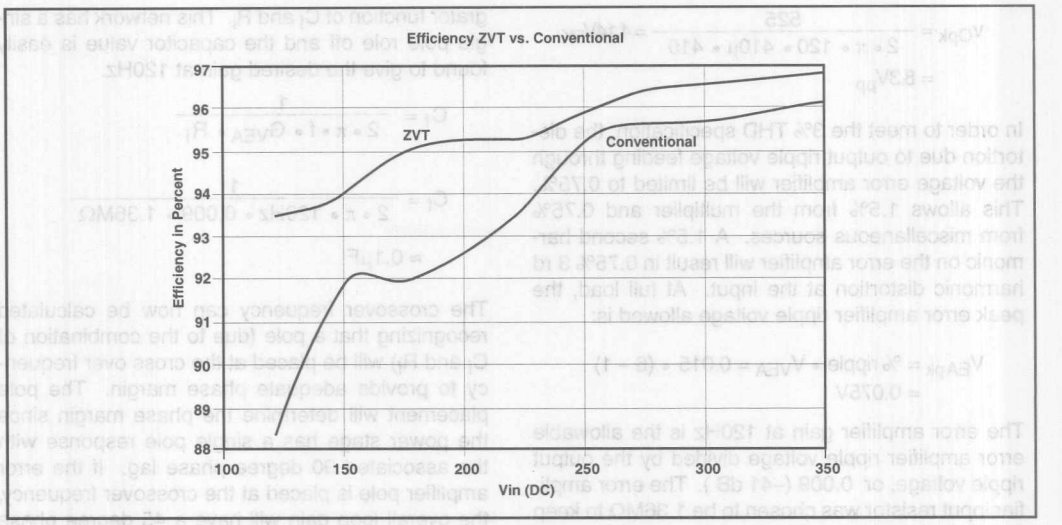


Figure 14. Efficiency Data

used in series to reduce the voltage stress. A 10nF capacitor is placed in parallel with the 33kΩ resistor for noise filtering.

With this divider the converter will start at $76V_{RMS}$, which will allow startup well below low line.

EXPERIMENTAL RESULTS

The example converter was constructed to demonstrate circuit performance. The circuit performed well and was tested over the full line and load ranges.

Figure 14 shows efficiency data for the ZVT vs. a conventional boost converter, which was derived by simply removing the ZVT components. The conventional circuit needed to be cooled with a fan in order to stabilize the power semiconductor temperatures. It can be seen from the data that the ZVT circuit has a significant advantage over the conventional converter at low line. At higher line voltages the advantage is reduced until the two power stages converge at high line. This is understandable and consistent with the other reported data [4,13]. At low line, the higher input current contributes to higher switching losses in the conventional converter. The ZVT converter however, does not experience increased switching losses (conduction losses increase for both converters at low line).

Figure 15 shows the ZVT and main switch gate drives as well as the main switch drain to source voltage. The ZVT gate drive goes high prior to the main switch and drives the drain voltage to zero before the main switch turns on. It should also be noted that the drain to source voltage waveform is very clean with no overshoot or ringing, which will reduce EMI and voltage stress on the device. The ZVT circuit waveforms are shown in Figure 16. Current in L_r is shown in the top trace. The wave-

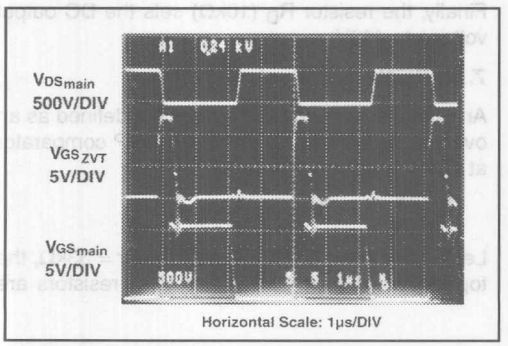


Figure 15. Power Stage Waveforms

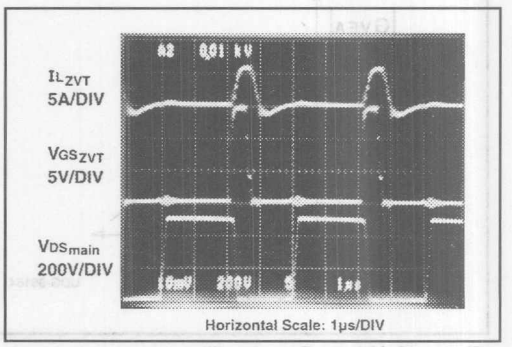


Figure 16. ZVT Waveforms

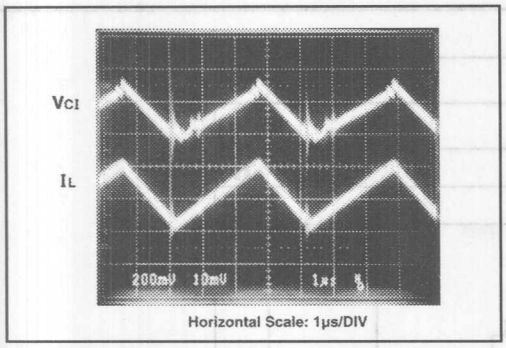


Figure 17. Current Synthesizer Waveforms

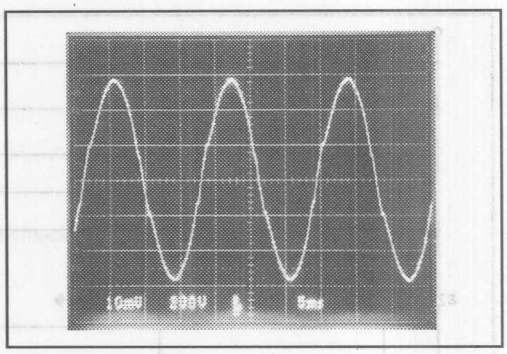


Figure 18. Line Current

forms are well damped with a peak current of approximately 6A. The current synthesizer waveforms are shown in Figure 17. The top waveform is the reconstructed waveform at CI and the bottom waveform is inductor current. The waveforms show good agreement. Any error between the reconstructed and actual waveform will be greatest at high line and is primarily caused by slight offset voltage errors in the synthesizer circuit.

Figure 18 shows the input line current at low line and maximum load, the THD and power factor are well within acceptable limits. Table 1 gives THD and pf measurements for several line and load conditions with the single stage current error amplifier clamp circuit. Table 2 shows THD and pf with the two stage clamp circuit shown in Figure 9B.

Line(VAC)	% THD	Pf
100	6.3	0.998
120	4.5	0.999
200	8.9	0.996
230	10	0.995

Table 1 THD and Pf vs. line, with single stage error amplifier clamp circuit.

Line(VAC)	% THD	Pf
100	4.95	0.999
120	5.30	0.998
200	5.45	0.998
230	5.83	0.998

Table 2 THD and Pf vs. line, with two stage error amplifier clamp circuit.

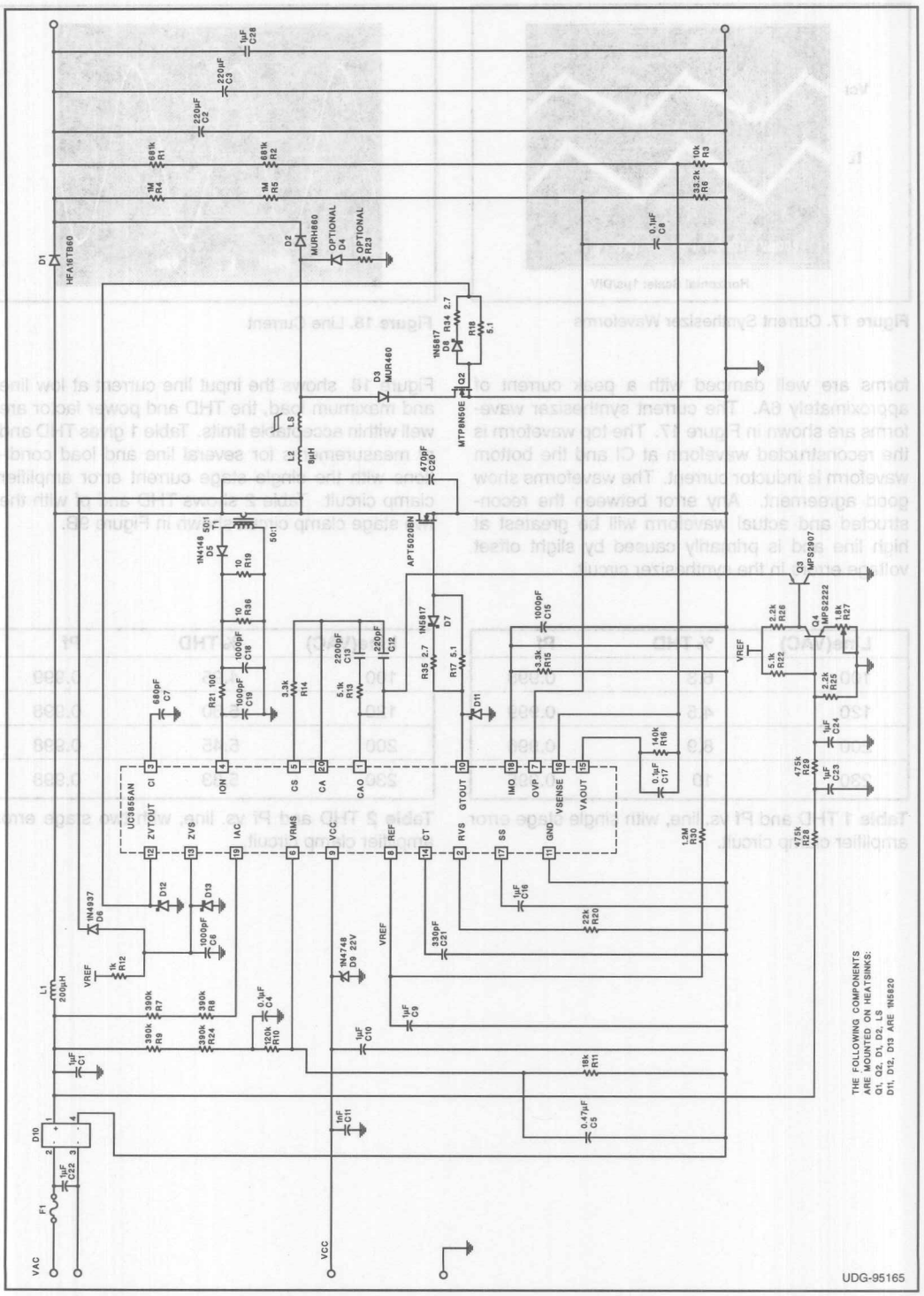


Figure 19. UC3855A/B Typical Application

POWER STAGE COMPONENT VENDORS

L1,L2	Magnetics, Butler, PA (412) 282-8282
Spike Killer	Toshiba, Westboro, MA (508) 836-3939
Q_{MAIN}	APT, Bend, OR (503) 382-8028
D1	International Rectifier, El Segundo, CA (310) 322-3331
Q_{ZVT}, D2, D3, D4	Motorola, Phoenix, AZ (602) 244-3550

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THE NEW UC3879 PHASE-SHIFTED PWM CONTROLLER SIMPLIFIES THE DESIGN OF ZERO VOLTAGE TRANSITION FULL-BRIDGE CONVERTERS

by Laszlo Balogh

INTRODUCTION

This Application Note will introduce the UC3879 integrated circuit and compare its performance to its predecessors, the UC3875/6/7/8 controller family. These integrated circuits provide all necessary control, decoding, protection and drive functions to successfully manage the operation of the full-bridge converter with phase-shifted control. This integrated solution greatly simplifies the design procedure and offers significant savings in development time and printed circuit board real-estate for the designer.

Using the conventional full-bridge topology with phase-shifted control technique has already demonstrated its superiority in medium to high power, DC-to-DC power conversion. This control method provides well controlled dv/dt values and zero-voltage switching of all primary side semiconductors in the power stage over nearly all operating conditions. Several publications [1-8] discussed the details of operation including equivalent circuits for the resonant transitions for both legs of the bridge converter, conditions for zero-voltage switching and describing further improvement possibilities. The major benefits offered by this approach are a simpler power stage than its hard switched counterpart, utilizing circuit parasitics instead of being penalized by them, improved efficiency and lower EMI level. These significant advantages are realized with a slightly more complex control algorithm.

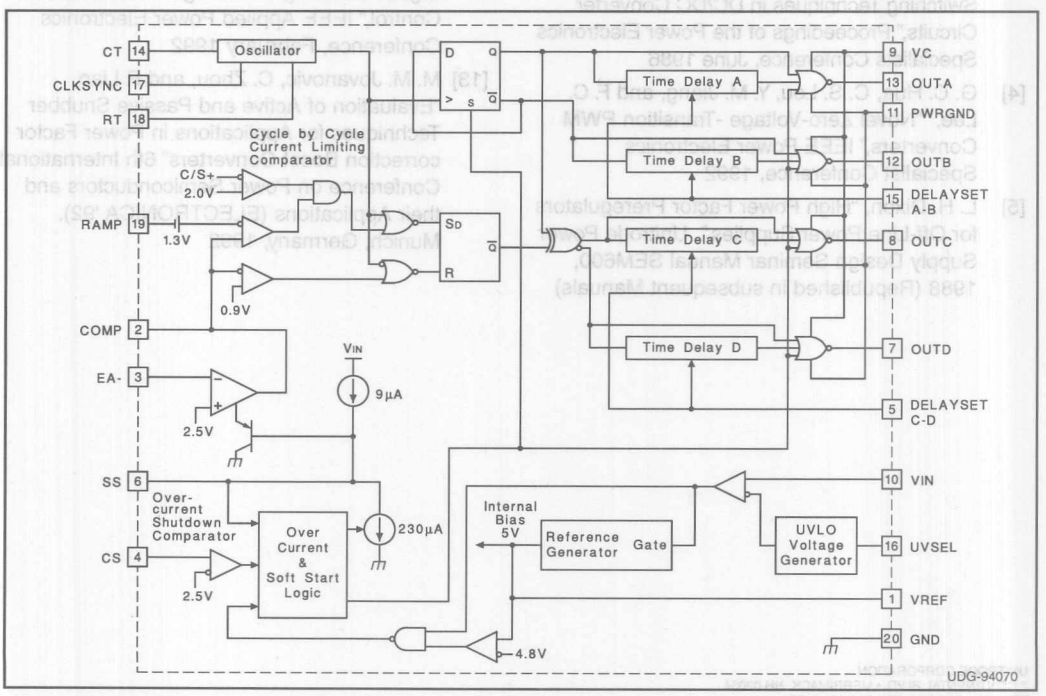


Figure 1. UC3879 Block Diagram

UNITRODE UC3879 PHASE-SHIFT PWM CONTROL IC - BLOCK DIAGRAM

The UC3879 is an improved version of the previously introduced UC3875 controller family. The internal architecture of the IC is shown in Figure 1.

The undervoltage lockout level of the UC3879 is user selectable by the UVSEL pin. Two predefined thresholds are available. If the UVSEL pin is floating, the chip starts running when the supply voltage exceeds 15.25V on the VIN pin. In case the UVSEL pin is externally connected to the VIN pin, operation starts at 10.75V. Independent of the selected start up option, the UC3879 goes to an undervoltage lockout mode when the input voltage falls below approximately 9.25V. The threshold levels reflect the two most commonly used auxiliary power generation methods; bootstrap or off-line.

The operating frequency of the synchronizable oscillator is programmed by two external components. The resistor from the RT pin to ground defines the charge current of the timing capacitor while the discharge current is internally fixed at 10mA. This way, the duty-cycle (D_{OSC}) of the oscillator, which corresponds to the duty ratio of the signal appearing on the CLKSYNC output of the IC, can be set accurately based on the relationship:

$$RT = \frac{2.5V}{0.01A \cdot D_{OSC}}$$

The minimum recommended pulse width for reliable operation is around 250nsec and for all practical applications it should not exceed 500nsec. Hence, D_{OSC} shall be determined based on the clock frequency as:

$$D_{OSC} = (250nsec...500nsec) \cdot f_{CLOCK}$$

The timing capacitor, connected between the CT pin and ground, in combination with the already defined RT value determines the clock frequency (f_{CLOCK}) by the following formula:

$$CT = \frac{(1 - D_{OSC})}{1.08 \cdot RT \cdot f_{CLOCK}}$$

In practice, the selection of proper capacitance values are much more difficult than those of the resistors. Therefore, one might first select the appropriate capacitor value to fulfill the requirement based on the following simple table:

Frequency Range	Capacitance
f_{CLOCK} < 30kHz	2.2nF
30kHz < f_{CLOCK} < 100kHz	680pF
100kHz < f_{CLOCK}	220pF

After choosing the value of the timing capacitor, the required resistance can be calculated as:

$$RT \cong \frac{0.47 + 0.07 \cdot \sqrt{47.17 - 5 \cdot 10^4 \cdot CT \cdot f_{CLOCK}}}{CT \cdot f_{CLOCK}}$$

Figure 2 shows the solution of the timing equations for the most commonly used frequency range. It offers a quick guide to estimate the required resistor value.

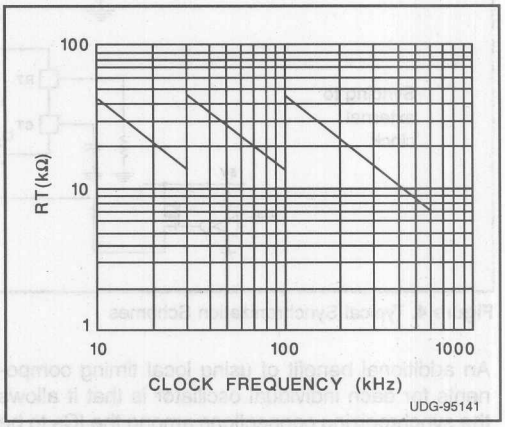


Figure 2. Timing Resistor (RT) vs. Oscillator Frequency

During free-running operation the capacitor voltage changes between nearly 0V and 2.9V linearly. Typical operating waveforms for free-running and synchronized operation are demonstrated in Figure 3.

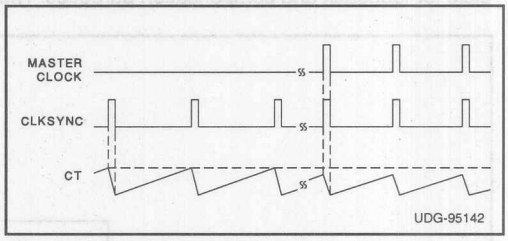


Figure 3. Oscillator Waveforms
a) Free-running; b) Synchronized Operation

Synchronization can be attained by driving the CLKSYNC pin from another UC3879 or by external circuitry as shown in Figure 4.

In both cases, all ICs will synchronize to the IC or external clock signal with the highest free-running frequency. The resistors R1 to Rn may be needed to properly terminate the synchronization bus and to keep the sync pulse narrow due to capacitance loading the line.

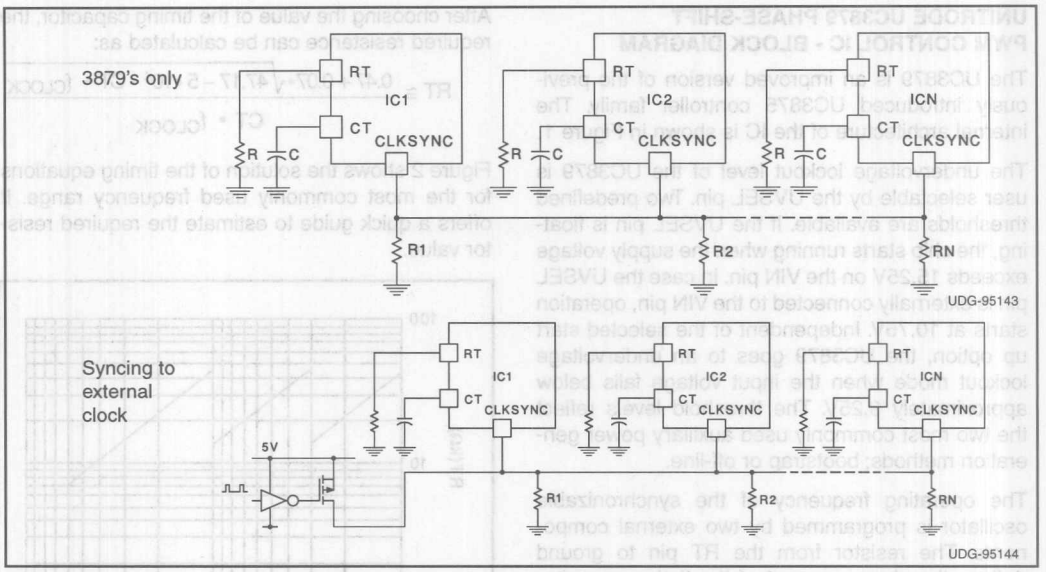


Figure 4. Typical Synchronization Schemes

An additional benefit of using local timing components for each individual oscillator is that it allows the synchronizing connections among the ICs to be broken without any local loss of functionality.

Output regulation is achieved using the 10MHz gain bandwidth on-board error amplifier. The noninverting input of the error amplifier is internally connected to a 2.5V reference. The inverting input (E/A–) and the output of the amplifier (E/A OUT) are accessible for feedback and compensation purposes. The output of the error amplifier is utilized to command the high speed PWM circuit. This signal is compared to the RAMP input of the IC having a usable input voltage range from zero to 2.9V.

Soft-start is accomplished with a capacitor from the soft-start pin (SS) to ground. During the soft-start period, the soft-start output of the error amplifier is clamped to the capacitor voltage which is gradually increased from zero to about 4.8V. It corresponds to pulse width, phase shift or peak current limiting

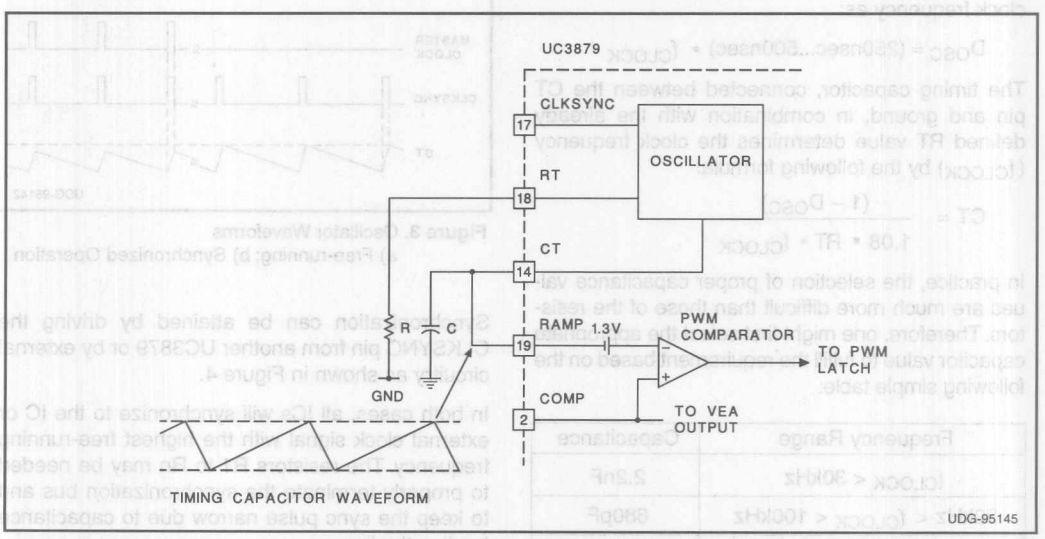


Figure 5. UC3879 with Voltage Mode Control

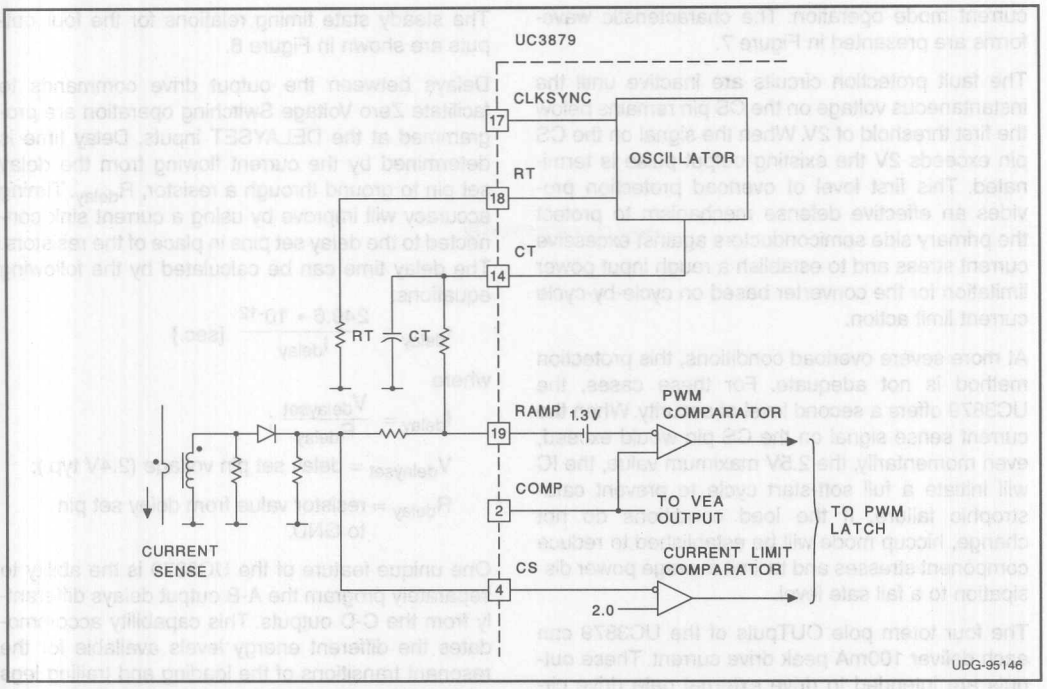


Figure 6. UC3879 with Peak Current Mode Control

depending on the exact implementation.

The UC3879 is equally suited for conventional voltage mode control or for peak current mode control. When used in voltage mode, the CT signal is directly fed to the RAMP terminal as indicated in Figure 5.

In current mode operation, the RAMP signal is the sum of the current sense signal and the slope compensation, derived from the voltage across the timing capacitor as it is shown in Figure 6.

Fault protection is established by two independent current limiting circuits which accept a 0V to 2.5V amplitude maximum current sense signal on their CS input pin. They provide cycle-by-cycle and shutdown type current limit protection in both voltage or

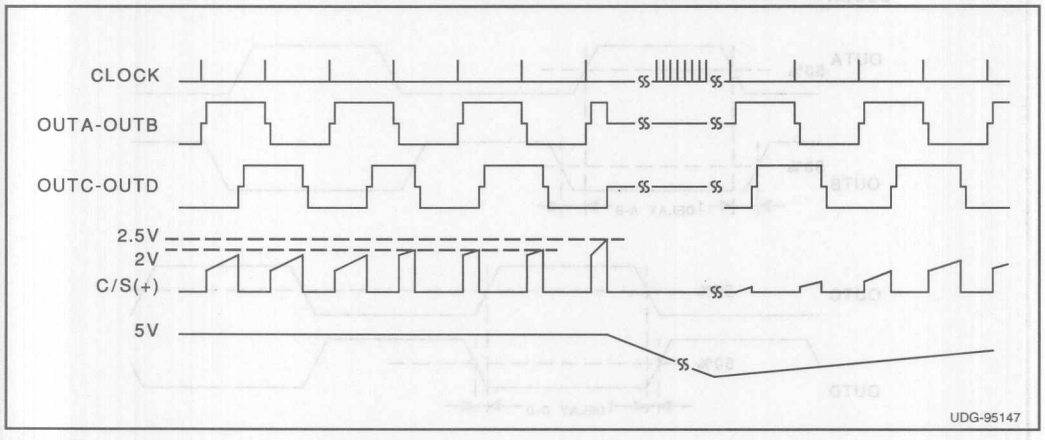


Figure 7. Operation of the Current Limiting Circuits (typical waveforms)

current mode operation. The characteristic waveforms are presented in Figure 7.

The fault protection circuits are inactive until the instantaneous voltage on the CS pin remains below the first threshold of 2V. When the signal on the CS pin exceeds 2V the existing output pulse is terminated. This first level of overload protection provides an effective defense mechanism to protect the primary side semiconductors against excessive current stress and to establish a rough input power limitation for the converter based on cycle-by-cycle current limit action.

At more severe overload conditions, this protection method is not adequate. For these cases, the UC3879 offers a second level of security. When the current sense signal on the CS pin would exceed, even momentarily, the 2.5V maximum value, the IC will initiate a full soft-start cycle to prevent catastrophic failure. If the load conditions do not change, hiccup mode will be established to reduce component stresses and to limit average power dissipation to a fail safe level.

The four totem pole OUTputs of the UC3879 can each deliver 100mA peak drive current. These outputs are intended to drive external gate drive circuits. This enhances the robustness of the overall design. To further reduce the noise transmitted back to the analog circuitry, the output section features its own collector power supply (VC) and ground (PGND) connections. Local decoupling capacitors and series impedance to the auxiliary supply improves performance even more.

The steady state timing relations for the four outputs are shown in Figure 8.

Delays between the output drive commands to facilitate Zero Voltage Switching operation are programmed at the DELAYSET inputs. Delay time is determined by the current flowing from the delay set pin to ground through a resistor, R_{delay}. Timing accuracy will improve by using a current sink connected to the delay set pins in place of the resistors. The delay time can be calculated by the following equations:

$$t_{delay} = \frac{249.6 \cdot 10^{-12}}{I_{delay}} \text{ [sec.]}$$

where

$$I_{delay} = \frac{V_{delayset}}{R_{delay}};$$

$V_{delayset}$ = delay set pin voltage (2.4V typ.);

R_{delay} = resistor value from delay set pin to GND.

One unique feature of the UC3879 is the ability to separately program the A-B output delays differently from the C-D outputs. This capability accommodates the different energy levels available for the resonant transitions of the leading and trailing legs of the bridge circuit [7-9]. Inability to optimize each of these durations will generally result in loosing zero voltage switching of the full-bridge converter switches under some operating conditions.

The optimum delay time, on the cycle-by-cycle basis, is the function of the actual current flowing in the primary winding of the transformer. This current

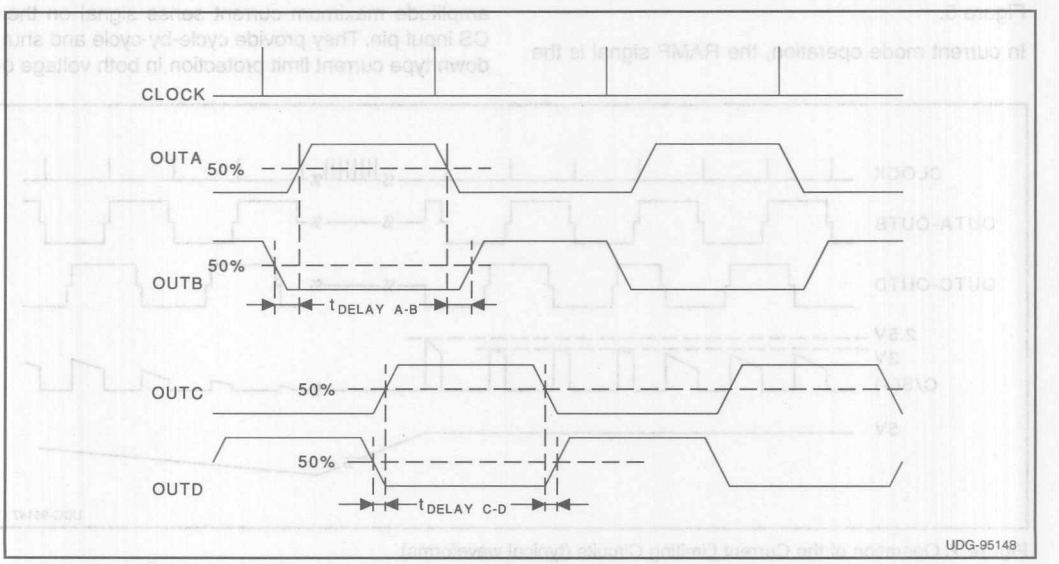


Figure 8. Output Timing Diagram for Steady State Operation

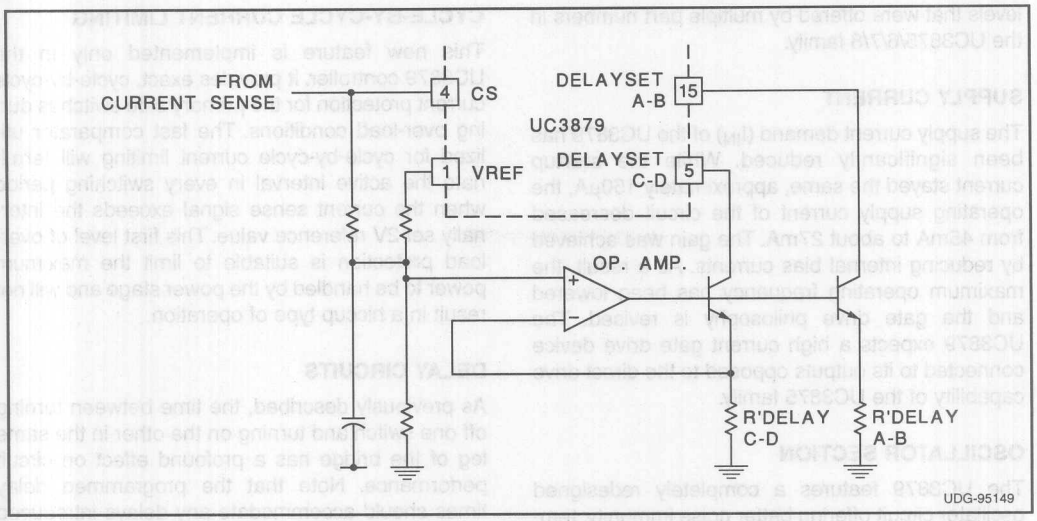


Figure 9. Adaptive Control of Delay Times

value can easily change by a factor of 10 to even 100 depending on load conditions. This causes a large variation in the required delay time, thus adaptive programming of delays might be desirable for certain applications.

Figure 9 introduces a simple external circuit to achieve variable delay times based on the momentary value of the sensed current.

The resistor network connected to the positive input of the operational amplifier determines the ratio of the minimum and the maximum delay times. The actual values of $t_{delayA-B}$ and $t_{delayC-D}$ can be scaled by the resistors between the emitters of the respective transistors and ground.

As these delays can be realized in several ways along the external gate drive circuits, setting zero delay is also offered by simply connecting the delay set inputs to the IC's 5.0V reference.

The precision, short circuit protected 5.0V bandgap reference is available for external functions as well.

UC3879 VS. UC3875/6/7/8

Although the UC3879 retained the operating principle and the basic architecture of the UC3875, it is still important to draw attention to the enhanced and added features of the new IC. The differences between the two controllers are summarized in Table 1. Their consequences for the circuit design will also be highlighted.

UNDERVOLTAGE LOCKOUT

The undervoltage lockout circuit utilizes a logic input (UVSEL) to select between the two available turn-on voltages (15.25V/10.75V). The advantage of this solution is that it can configure the undervoltage lockout threshold without external components. The UC3879 provides the same undervoltage lockout

Features	UC3875/6/7/8	UC3879
Undervoltage Lockout	Fixed at 15.25V/10.75V	Selectable
Supply Current	45mA typ.	27mA typ.
Oscillator Section	up to 2MHz operation	up to 600kHz operation
Error Amplifier	noninverting input accessible	noninverting input tied to 2.5V
Cycle-by-cycle Current Limiting	not available	implemented
Time Delay Circuits	60ns minimum delay	0 delay available
Output Drivers	4 x 2A totem-pole	4 x 100mA totem-pole

Table 1. Comparison of Unitrode's Phase-Shifted PWM Control ICs

levels that were offered by multiple part numbers in the UC3875/6/7/8 family.

SUPPLY CURRENT

The supply current demand (I_{IN}) of the UC3879 has been significantly reduced. While the startup current stayed the same, approximately 150μA, the operating supply current of the circuit decreased from 45mA to about 27mA. The gain was achieved by reducing internal bias currents. As a result, the maximum operating frequency has been lowered and the gate drive philosophy is revised. The UC3879 expects a high current gate drive device connected to its outputs opposed to the direct drive capability of the UC3875 family.

OSCILLATOR SECTION

The UC3879 features a completely redesigned oscillator circuit offering better noise immunity, temperature stability, and linearity. The charge current of the timing capacitor is constant, producing a linear, positive slope on the timing capacitor during the conduction period. The voltage level is tailored to provide ramp signal for voltage mode control directly. Likewise, slope compensation can be effortlessly accomplished using the voltage of the timing capacitor in case of peak current mode control. The operating frequency is programmed by the combination of RT and CT, which are connected to their separate pins.

ERROR AMPLIFIER

Both integrated circuits make use of a 10MHz gain bandwidth amplifier to regulate the output voltage. The noninverting input of the UC3879 error amplifier is internally wired to a 2.5V reference opposed to the UC3875 family where the reference is to be provided externally.

In constant output voltage applications, the UC3879 will save those components related to generating the reference for the feedback amplifier. Conversely, it will require more components and more elaborate solution if the programming of the output voltage, thus the reference, is required. Systems with isolation between the primary and secondary side controllers will not experience any difference in the design since the error amplifier of the control IC is usually configured as a voltage follower processing the error signal transmitted from the secondary side of the converter.

CYCLE-BY-CYCLE CURRENT LIMITING

This new feature is implemented only in the UC3879 controller. It provides exact, cycle-by-cycle current protection for the primary side switches during over-load conditions. The fast comparator utilized for cycle-by-cycle current limiting will terminate the active interval in every switching period when the current sense signal exceeds the internally set 2V reference value. This first level of overload protection is suitable to limit the maximum power to be handled by the power stage and will not result in a hiccup type of operation.

DELAY CIRCUITS

As previously described, the time between turning off one switch and turning on the other in the same leg of the bridge has a profound effect on circuit performance. Note that the programmed delay times should accommodate any delays introduced by the high current gate circuits and transformer.

Allowing zero delay between the outputs of the UC3879 provides greater freedom to the designer to implement those delays as desired. Possible other points to program the necessary delays are the inputs of the high current gate drivers or the secondary sides of the gate drive transformers. All these solutions have their pros and cons, and require careful considerations in sight of the actual application.

OUTPUT DRIVERS

The output totem pole drivers of both controllers have identical structures. They feature their own power rail connections and they are kept active low during undervoltage lockout. However, output current ratings are remarkably different. With its 2A peak current capability, the UC3875 family is prepared for direct drive of the gates or gate drive transformers of the most commonly used power switches. Yet, with the continuously increasing die sizes, separate driver chips can be advantageous to eliminate undesired power dissipation and noise generation from the sensitive analog control sections. In this regard, the UC3879 is designed to work with external high current gate drive circuits. Its fast outputs, with 100mA peak current capability, are especially appropriate to drive the TTL or MOSFET input stages of those devices.

Undervoltage Lockout		Delay Times		UC3879	UVSEL pin		DELAYSET pins	
Turn-ON	Turn-OFF	$\tau_D > 0$	$\tau_D = 0$	Old Part #	Float	$\rightarrow V_{CC}$	$\rightarrow V_{REF}$	R_{SET}
10.75V	9.25V	X		**UC3875**		X		X
15.25V	9.25V	X		**UC3876**	X			X
10.75V	9.25V		X	**UC3877**		X	X	
15.25V	9.25V		X	**UC3878**	X		X	

Table 2. Providing UC3875/6/7/8 functionality through the setup options of the UC3879 control IC.

UC3879 DESIGN FLEXIBILITY

Besides the several improved features and added functions, the UC3879 offers the greatest degree of design flexibility with the minimum number of external components. Table 2 shows the different setup possibilities to achieve the same functionality offered by four different part numbers in the UC3875 family.

SUMMARY

As demonstrated, the UC3875/6/7/8 and the UC3879 integrated circuits are dedicated to eliminate most of the difficulties associated with implementing the numerous auxiliary functions and the tedious control algorithm of the full bridge converters with phase-shifted control. The single chip solution with its carefully optimized signal levels and minimum number of external components provide the fast track in the controller design for one of today's most promising power conversion techniques.

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IMPLEMENTING MULTI-STATE CHARGE ALGORITHM WITH THE UC3909 SWITCHMODE LEAD-ACID BATTERY CHARGER CONTROLLER

By Laszlo Balogh

INTRODUCTION

Applications of lead-acid batteries for primary as well as backup power sources has been increased significantly. The reasons behind this growth are the continuously improving battery technology which provides higher and higher power densities, and the increased demand for wireless operation of different electronic devices and tools. Manufacturers of these equipment are frequently challenged to provide solutions for quick and efficient recharge of the cells and to maximize the capacity and life of the battery.

Although the task sounds simple, satisfying the various requirements associated with charging and maintaining lead-acid batteries often requires considerable intelligence from the battery charger circuit. The implementation of a well optimized charging process requires complex control circuitry, such as microprocessors, DSP chips or state machine type of controllers. Usually, these solutions require custom components, and significant hardware and software development time. The cost of these solutions are penalized, by the higher cost and software of the digital controller, interfacing to the analog part of the circuit, in addition to the increased part count and consequently higher manufacturing expense.

This Application Note will introduce a new, dedicated analog controller. The UC3909 Switchmode Lead-Acid Battery Charger integrated circuit provides a low cost solution to battery charging, without sacrificing the performance of the system.

Additionally, the paper will guide users, whose primary expertise is not switchmode power supply design, how to devise state of the art, multi-state battery charger, using the new IC. The step by step instructions incorporated in this Application Note will provide exact component values, reducing the time of the paper design to merely a few minutes.

BASICS OF LEAD-ACID BATTERIES

In order to efficiently discuss battery properties, some of the common terms used in the battery industry have to be defined.

Ampere-Hour (Ah) - is a measurement of electric charge computed as the integral product of current (in Amperes) and time (in hours).

Capacity - is the ability of the battery to store and discharge a given quantity of current over a specified period of time. The capacity of the battery is expressed in Ampere-Hours (Ah). A cell's capacity is a function of the discharge current and usually increases with lower current levels. The capacity of the battery listed in the datasheet usually corresponds to the measured capacity at C/10 discharge rate.

C Rate - is the charge or discharge current of the battery expressed in multiples of the rated capacity. For example, a 2.5Ah cell will provide 250mA for 10 hours. The C rate in this particular case is C/10. In the real world, however, a cell does not maintain the same rated capacity at all C rates.

Self Discharge - is the loss of useful capacity of a cell on storage due to internal chemical action.

Deep Discharge - is the discharge of the battery below the specified cutoff voltage, typically 1.7V-1.9V per cell at 25°C depending on the C rate, before the battery is recharged. It happens usually upon withdrawal at least 80% of the rated capacity of the cells.

Constant Voltage Charge - is a charging technique during which the voltage across the battery terminals is regulated while the charge current varies according to the state of charge of the battery.

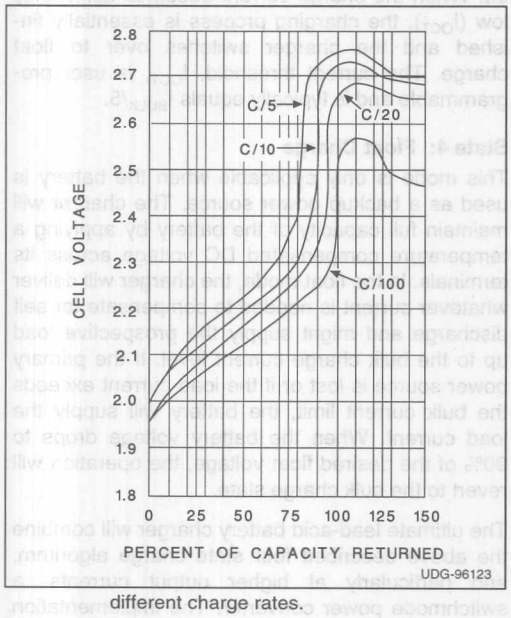
Constant Current Charge - is a charging method during which the current through the battery is maintained at a steady state value while the cell voltages will vary according to the state of charge of the battery.

Trickle-Charge - is a constant current charge of the battery. In this mode, a low current, typically in the range of C/100 or lower is applied to the battery to raise the voltage to the deep discharge threshold (cutoff voltage), a level corresponding to near zero capacity. The trickle charge current has to be determined to assure continuous operation without damaging the cells.

Bulk-Charge - is also a constant current mode of operation, to quickly replenish the charge to the battery. The battery manufacturers define the bulk charge current as the maximum charge current allowed for the cells. It can be applied to the batteries if their voltage is between the deep discharge and the over-charge limits. Typical bulk charge current varies between C/5 and 2·C depending on manufacturers and battery types.

Over-Charge - the term describes the chemical reactions taking place when the majority of the lead-sulfate has already been converted to lead, resulting in the generation of hydrogen and oxygen. The beginning of the over-charge reactions depends on the C rate, and it is indicated by the sharp rise in cell voltage as it is illustrated in Figure 1.

Figure 1. Typical over-charge characteristic at different charge rates.



For over-charge to coincide with the 100% return of capacity, the charge rate must be less than C/100. For higher charge rates, over-charge of lead-acid batteries is necessary to return the full capacity.

In a controlled **over-charge mode**, a constant voltage is applied. Its value is typically set between 2.45 V/cell and 2.65 V/cell, again depending on the C rate. Improper selection of the over-charge voltage will eventually result in dehydration of the battery and reducing its useful life span.

Float-Charge - is a constant voltage charge of the battery, after completing the charging process. This voltage maintains the capacity of the battery against self discharge. Even though providing a fixed output voltage is a simple task, to find the precise value of the float voltage has a profound effect on battery performance. For instance, 5% deviation from the optimum cell voltage in float mode, could result approximately 30% difference in the available capacity of the battery. Furthermore, the battery's temperature coefficient of typically -3.9mV/°C per cell, adds complication. If the float voltage is not compensated according to the battery temperature, loss of capacity will occur below the design temperature, and uncontrolled over-charging with degradation in life will happen at elevated temperature.

BATTERY CHARGER BASICS

What differentiates a battery charger from a conventional power supply is the capability to satisfy the unique requirements of the battery. Lead-acid battery chargers typically have two tasks to accomplish. The most important is to restore capacity as quickly as possible. The second one is to maintain capacity by compensating for self discharge and ambient temperature variations.

There are two fundamentally different charging methods for lead-acid batteries. In constant voltage charge, the voltage across the battery terminals is constant and the condition of the battery determines the charge current. Constant voltage charge is most popular in float mode application. The charging process is usually terminated after a certain time limit is reached.

Another technique is constant current charge, which is often used in cyclic applications because it recharges the battery in a relatively short time. As opposed to constant voltage charge, the constant current charge automatically equalizes the charge in the series cells. There are many varia-

tions of the two basic methods, well suited for switchmode battery charger circuits. Considering that well designed switchmode power converters are inherently current limited, the combination of constant current and constant voltage charge is an obvious choice.

The best performance of the lead-acid cells can be achieved using a four state charge algorithm. This method integrates the advantages of the constant current charge to quickly and safely recharge and equalize the lead-acid cells, with the constant voltage charge to perform controlled over-charge and to retain the battery's full charge capacity in float mode applications. The carefully tailored charging procedure maximizes the capacity and life expectancy of the battery.

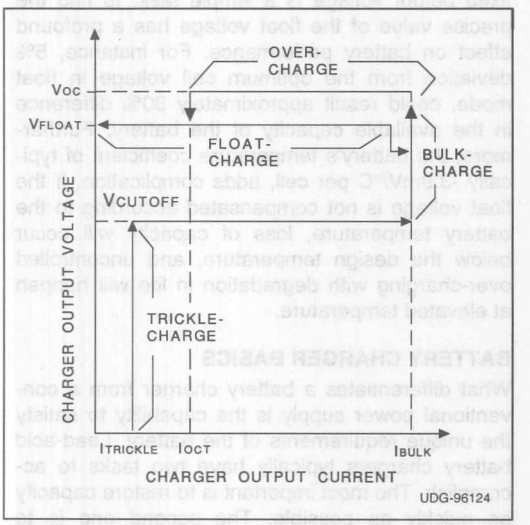


Figure 2. Four-state charge algorithm

The four states of the charger's operation are trickle charge, bulk charge, over-charge and float charge, as they are shown in Figure 2. Assuming a fully discharged battery, the charger sequences through the states as follows:

State 1: Trickle Charge

If the battery voltage is below the cutoff voltage, the charger will apply the preset trickle charge current ($I_{TRICKLE}$). In case of a healthy battery, as the charge is slowly restored, the voltage will increase towards the nominal range until it reaches the cutoff voltage. At that point the charger will advance to the next state, bulk charging.

In case of a damaged battery, e.g. one or more cells are shorted or the internal leakage current of the battery is increased above the trickle current value, the low value of the trickle charge current ensures safe operation of the system. In this case the battery voltage will stay below the deep discharge threshold (V_{CUTOFF}) preventing the charger from proceeding to the bulk charge mode.

When the battery voltage is above the cutoff voltage at the beginning of the charge cycle, the trickle charge state is skipped and the charger starts with the bulk charge mode.

State 2: Bulk Charge

In this mode the maximum allowable current (I_{BULK}) charges the battery. During this time, the majority of the battery capacity is restored as quickly as possible. The bulk charge mode is terminated when the battery voltage reaches the over-charge voltage level (V_{OC}).

State 3: Over-Charge

Controlled over-charge follows bulk charging to restore full capacity in a minimum amount of time. During the over-charge period, the battery voltage is regulated. The initial current value equals the bulk charge current, and as the battery approaches its full capacity the charge current tapers off. When the charge current becomes sufficiently low (I_{OCT}), the charging process is essentially finished and the charger switches over to float charge. The current threshold, I_{OCT}, is user programmable and is typically equals $I_{BULK}/5$.

State 4: Float Charge

This mode is only applicable when the battery is used as a backup power source. The charger will maintain full capacity of the battery by applying a temperature compensated DC voltage across its terminals. In the float mode, the charger will deliver whatever current is needed to compensate for self discharge and might supply the prospective load up to the bulk charge current level. If the primary power source is lost or if the load current exceeds the bulk current limit, the battery will supply the load current. When the battery voltage drops to 90% of the desired float voltage, the operation will revert to the bulk charge state.

The ultimate lead-acid battery charger will combine the above described four state charge algorithm, and particularly at higher output currents, a switchmode power converter. The implementation of a charger of this type usually requires several

integrated circuits. To minimize cost as well as complexity, a new integrated circuit had been developed to provide as much functionality and design flexibility as possible, while achieving these requirements.

THE UC3909 BLOCK DIAGRAM

The UC3909 Switchmode Lead-Acid Battery Charger controller combines the precision sensing and control of battery voltage and current, logic to sequence the charger through its various modes of operation, and the control and supervisory functions of a switching power supply. The integrated circuit comprises of two major sections. A dashed line shown in the middle of Figure 3 divides the circuit into two functional subsections. The PWM control circuit is commanded by the charge state logic depending on the condition of the battery.

The charge state logic is shown in the lower right corner of the block diagram, which is composed of several digital gates. It sequences the charger through the four possible states of operation depending on the battery voltage. Information about the actual operating mode of the charger is also provided. The status information can be easily interfaced to any logic family due to the open collector structure of the outputs of pin STAT0, STAT1, and STATLV. (See the datasheet for detailed pin descriptions.)

The precision voltage and current sensing circuits are shown in the lower left corner of the block diagram. The battery voltage is compared to the temperature compensated reference voltage by the voltage error amplifier and charge enable comparator. Accurate sensing of the charge current is achieved by the uncommitted current sense amplifier, connected to the CS+, CS- and CSO pins. The use of this amplifier requires a low value resistor for current measurement. Output regulation is accomplished by the current error amplifier. Its inverting and noninverting inputs are connected to the output of the current sense and voltage error amplifiers through external resistors. The output of the current error amplifier produces the appropriate control parameter for the PWM controller.

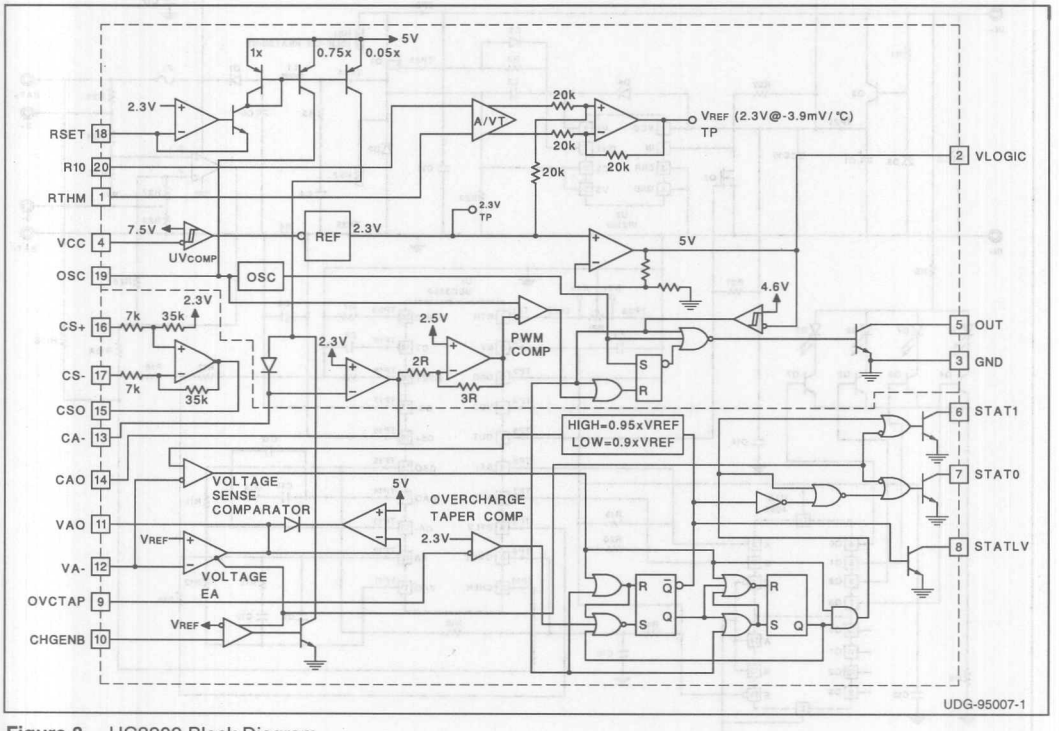


Figure 3. UC3909 Block Diagram

The PWM control section consists of a fast comparator, clock generator, latch and an open collector drive stage. The comparator circuit compares the output of the current error amplifier to the sawtooth derived from the timing capacitor waveform. A latch is set by the clock and reset by the comparator circuit in every switching cycle modulating the pulse width appearing at the output of the controller. This modulation of the output pulse width makes output voltage and output current regulation possible.

The remaining part of the block diagram performs numerous housekeeping functions, such as undervoltage lockout, internal bias and reference generation, temperature sensor linearization and compensation of the internal voltage reference according to the battery temperature.

UC3909 DEMONSTRATION CIRCUIT

To illustrate the capabilities of the new controller, a full featured, switchmode battery charger circuit has been developed and built for evaluation purposes.

The power stage is based on a simple buck topology, reflecting the most common solution used in battery chargers today. The buck converter offers size reduction and high efficiency, two important advantages of switchmode power conversion. Practical output power of this converter type is below 500W. In the case of off-line chargers, line isolation can be provided by 60Hz isolation transformer. For higher power levels the buck converter could be easily replaced by other isolated, buck derived topologies, like any variation of the forward or bridge type converters. Using one of these isolated conversion techniques will eliminate the bulky 60Hz transformer by integrating the isolation into the high frequency power stage. The design procedure, that will be presented in this Application Note for the buck configuration, can be easily adapted to the other power converters.

The usual elements of the buck converter can be recognized in Figure 4. They are Q1, D2, L1 and C5. Other components in the power stage pertain to additional, application specific requirements. D1 prevents the discharge of the battery by the con-

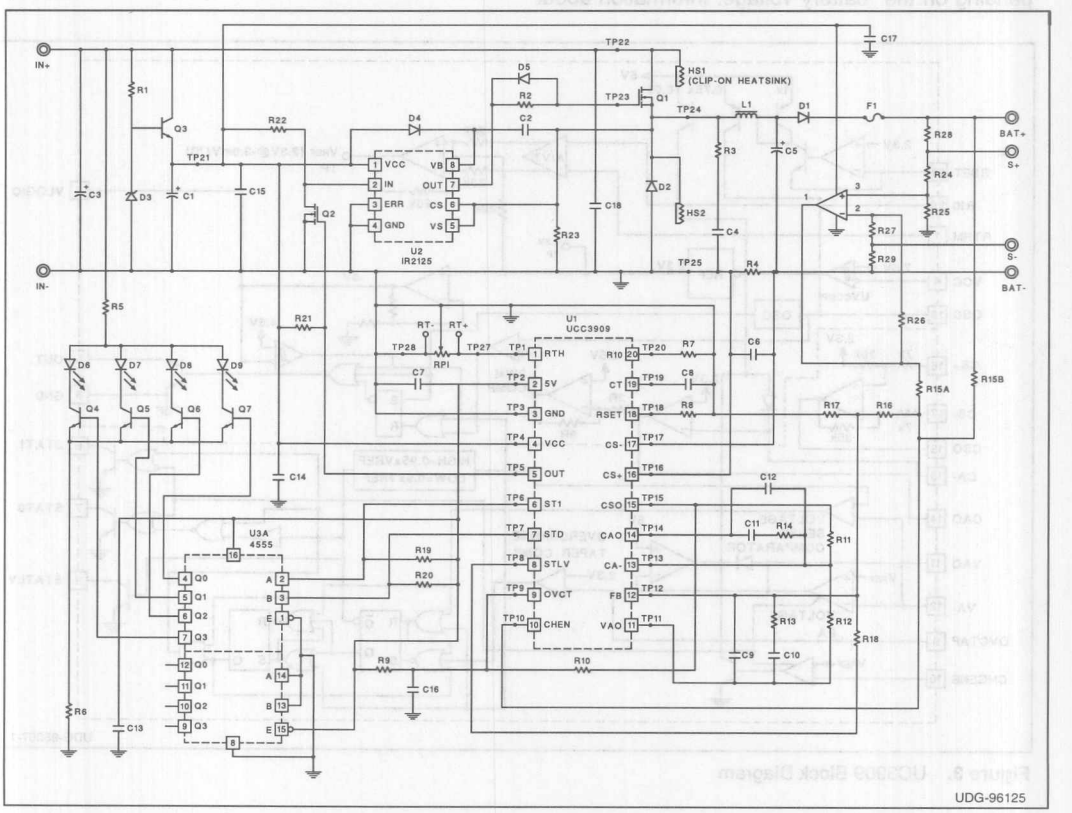


Figure 4. Demonstration Board Schematic

troller, when the primary power source is absent. An output fuse, F1, protects the circuit against the possible hazards when the battery is connected to the output terminals with reverse polarity. The charge current is measured by the resistor, R4 in the ground return path. The controller section consists of four well separable circuits. The first functional block is composed of R1, D3, Q3, and C1. These components provide a stabilized voltage for the rest of the control circuitry.

In the buck converter, the controlled switch, Q1, is located between the positive input terminal and the common node of the freewheeling diode, D2, and the output filter inductor, L1. There are many different components which could be used as a switch, yet for efficient operation and cost considerations, an N-channel MOSFET transistor has been selected. To interface the floating switch to the ground referenced controller, a high side driver is inevitable. The high side driver circuit consists of U2, D4, D5, R2, C2, Q2, R22 and R23. Its purpose is to level shift the output pulse of the control IC to the gate of the MOSFET transistor with minimum delays.

All the functions related to properly charging the battery are integrated in the UC3909 controller. The voltage and current levels which determine the actual values of the cutoff, over-charge and float voltages, as well as the trickle, bulk and taper threshold currents, are scaled appropriately by the resistor networks around the IC. The role of those components will be defined in the next chapter deliberating the design procedure.

The last section is the charge state decoder circuit. The coded information of the two outputs of the UC3909 is translated by U3, to display the actual operating mode of the battery charger.

BATTERY CHARGER DESIGN

The complete schematic drawing of the four state, switchmode battery charger is shown in Figure 4. In order to expedite the paper design, an easy to follow design procedure has been established. The step by step instructions can guide even the novice users through the calculations.

Battery Data

By the time the designer starts the circuit design, the type of the battery is already defined. The battery selection criteria are not detailed in this Application Note. Nevertheless, it is worthwhile to draw attention to some of the circumstances influencing the decision. Naturally, the most important parameters are the voltage and current requirements of the load as well as the time duration while the battery has to be able to supply the load current. Furthermore, the user has to consider whether the application requires frequent charge and discharge cycles or the battery is used in backup mode, where most of the time it will standby in its fully charged state. The available time for recharging the battery is also a significant factor to determine the applicable algorithm, and charge current rates. Combination of all these conditions will define the required battery and some of the battery charger parameters.

Once the battery is defined we can obtain the first set of input data. From the battery manufacturer's data sheet, more frequently through several telephone calls, and considering some application related conditions, the lines of Table 1 can be filled out.

For example, the demonstration circuit has been designed to charge a Dynasty JC1222 type sealed lead-acid battery from Johnson Controls. The nominal voltage is 12V, the capacity of the battery is 2.2Ah. Twelve volt batteries contain six cells connected in series. The battery has a temperature coefficient of -3.9mV/°C. Additional input parameters, like operating temperature range, float, cutoff and over-charge voltages as well as trickle, bulk, and over-charge terminate current levels can be determined from the application requirements and from the battery data sheet.

The completed Battery Data section is shown in Table 1. The trickle current level corresponds to the previously explained safety considerations and it equals C/100. A bulk charge current value of 800mA is given by the battery manufacturer [8] and is used instead of the C/2 value, noted in the respective equation in Table 1.

The over-charge period will be terminated when the current tapers off to one fourth of the bulk current. Maximum output power of the battery charger is listed in the last row of Table 1.

Parameter	Description	Definition	Value/Part#
Battery Data			**JC1222**
V	Nominal Battery Voltage		12V
NC	Number Of Cells	connected in series within the battery	6
C_{RATE}	Battery Capacity	use C/10 capacity; from battery datasheet	2.2 Ah
V_C	Cell Float Voltage	@25°C, fully charged; from battery datasheet	2.275V
$V_{C,MAX}$	Maximum Cell Voltage	@25°C, over-charge limit; from battery datasheet	2.43V
$V_{C,MIN}$	Minimum Cell Voltage	@25°C, fully discharged; from battery datasheet	1.75V
$I_{TRICKLE}$	Trickle Charge Current Limit	$I_{TRICKLE} = 0.01 \cdot C_{RATE}$; typical or use battery datasheet	22mA
I_{BULK}	Bulk Charge Current Limit	$I_{BULK} = 0.5 \cdot C_{RATE}$; typical or use battery datasheet	0.8A
I_{OCT}	Over-Charge Terminate Current Threshold	$I_{OCT} = 0.25 \cdot I_{BULK}$; typical or use battery datasheet	0.2A
TC	Cell Voltage Temperature Coefficient	typical value; the thermistor linearizer circuit is calibrated for this temperature coefficient	-3.9 mV/°C
T_{MIN}	Minimum Operating Battery Temperature	refer to your application requirements	-10°C
T_{MAX}	Maximum Operating Battery Temperature	refer to your application requirements	+50°C
V_{BAT}	Battery Float Voltage	$V_{BAT} = V_C \cdot NC$; nominal, @ 25°C battery temperature	13.65V
$V_{BAT,MIN}$	Minimum Battery Voltage	$V_{BAT,MIN} = \left[V_{C,MIN} + (T_{MAX} - 25) \cdot TC\right] \cdot NC$; @ T_{MAX}; fully discharged	9.92V
$V_{BAT,MAX}$	Maximum Battery Voltage	$V_{BAT,MAX} = \left[V_{C,MAX} + (T_{MIN} - 25) \cdot TC\right] \cdot NC$; @ T_{MIN}; fully charged	15.40V
$P_{CH,MAX}$	Maximum Output Power	$P_{CH,MAX} = I_{BULK} \cdot V_{BAT,MAX}$	12.3W

Table 1. Battery Charger Input Parameters

Buck Converter Operating Conditions

The battery charger circuit of the UC3909 is based on the buck topology. Before the component values of the power stage can be calculated, the basic operating parameters must be defined.

The output voltage range is listed in Table 1 as $V_{BAT,MIN}$ and $V_{BAT,MAX}$ determined primarily by the operating temperature range and the battery technology. On the other hand, input voltage variation depends on the power source. For this particular example, assume a 60Hz line isolation transformer with the optimized step down ratio. At minimum line voltage, it provides 18V DC voltage after rectification. Taking into account nominal tolerances, the input voltage of the converter at high line condition will be approximately 30V DC. From the minimum and maximum values of the input and output voltages, the steady state duty ratio limits are calculated (D=0.37 ... 0.89) as shown in Table 2.

At this point, the switching frequency of the converter has to be chosen. The trade-offs involved in the frequency selection are numerous. The primary factors are the speed of the prospective semiconductors, the capabilities of the controller, maintaining high efficiency in wide load current variations, power level and the size of the output inductor and capacitors.

Parameter	Description	Definition	Value/Part#
Buck Converter Operating Parameters			
$V_{IN,MIN}$	Minimum Input Voltage		18V
$V_{IN,MAX}$	Maximum Input Voltage		30V
f_S	Switching Frequency		50kHz
V_{D1F}	D1 Diode Forward Voltage Drop (estimate)	@100°C with I_{BULK}	0.59V
V_{D2F}	D2 Diode Forward Voltage Drop (estimate)	@100°C with I_{BULK}	0.73V
D_{MAX}	Maximum Duty Ratio	$D_{MAX} = \frac{V_{BAT,MAX} + V_{D1F} + V_{D2F}}{V_{IN,MIN} + V_{D2F}}$	0.89
D_{MIN}	Minimum Duty Ratio	$D_{MIN} = \frac{V_{BAT,MIN} + V_{D1F} + V_{D2F}}{V_{IN,MAX} + V_{D2F}}$	0.37

Table 2. Buck Converter Operating Parameters

For example, the upper limit of the operating frequency is bound to the capabilities of the slowest components. In the demonstration circuit, the high side gate driver circuit can be conveniently operated up to 150kHz operating frequency. Since the buck converter is a hard switched topology, the operating frequency has a significant effect on the efficiency. Considering that most of the time the charger supplies light output load, further reduction of the switching frequency is desirable to maintain decent efficiency in this operating modes.

While reducing the switching frequency has a beneficial effect on efficiency, at the same time the size of the output inductor and capacitors are increasing. The compromise between the size of the reactive circuit components and light load efficiency in trickle and float charge modes led to a moderate switching frequency selection of 50kHz.

Power Stage Design

Table 3 summarizes the design procedure of the power components. The bold entries shall be copied over to the part list directly. The respective equations are included, and they make use of variables defined in Table 1 and Table 2, or by the previous lines in Table 3.

Semiconductors

First, the three semiconductor devices are selected. Their voltage and current ratings are based on the maximum input and output voltages and on the bulk charge current. The minimum current ratings given in Table 3 assure appropriate margins for reliable operation. Using higher current components improves efficiency but also might increase cost.

After the part number is chosen, power dissipation estimates are given based on the actual voltage, current, and device parameters. The diode D1 carries the DC output current, therefore its dissipation is strictly conduction loss. The other two semiconductors are part of the switching circuit, hence their power dissipation is calculated by adding their respective conduction and switching losses.

Note that estimating switching losses on device parameters can be fairly inaccurate. This can cause a significant difference between the estimated and real switching losses especially at higher operating frequencies.

Output Inductor

The inductance of the output choke has been calculated by choosing the maximum ripple component of the inductor current. In a general purpose buck converter, unless extreme noise, core loss or application specific requirements would dictate otherwise, the rule of thumb is 25% to 35% of the DC current value is acceptable for ripple current content. Although battery manufacturers are concerned about using AC currents to charge the battery, they usually refer to frequencies below 1kHz. The DC output current with superimposed AC components of the switchmode chargers, at considerably higher frequencies, will be averaged by the slow chemical processes inside the battery.

Input Capacitor

The value of the input energy storage capacitor depends on the tolerable ripple and noise voltage at the input of the converter, and a function of the hold-up requirements. It is especially important for AC operated chargers where the energy is avail-

able in 120Hz repetitions, while the output has to be supplied continuously.

The situation is somewhat different if the charger is part of a distributed power system where an already regulated voltage with reasonable energy storage capability is available for the circuit. In this case, the ripple current handling capability of C3, and the noise requirements will determine the value of the input capacitor.

In Table 3, the value of the selected input capacitor is based on its rms current handling capability. The UC3909 demonstration circuit will operate properly when it is connected to a laboratory power supply, but will require a larger input capacitance in off-line applications.

Output Capacitor

There are numerous factors determining the output capacitor value. The various noise requirements at the output of the converter, the acceptable output voltage sag during the time interval when the capacitor contributes to supply the load current, and loop stability criteria. Fortunately, for all practical purposes, the output capacitor of a battery charger loses its importance since it is connected in parallel with the battery. The battery is considered as a low impedance voltage source with great high frequency filtering capabilities, taking over the traditional functions of the output capacitor.

The output capacitor, C5 of the demonstration circuit was chosen to handle the rms value of the ripple current component in the output inductor, L1 and to provide appropriate filtering in the absence of the battery.

RC Damping Circuit

Due to the nonideal nature of the switching action in all hard switching topologies, excessive switching spikes can develop across the semiconductors of the circuit during the switching time interval. The reduction of this voltage stress is accomplished by an RC snubber circuit consisting of R3 and C4 of the demonstration circuit. The complex optimization of the RC network is assisted by reference [6]. Proper operation of the snubber circuit also depends on the layout and the parasitic components of the switching circuit. Table 3 gives two equations to calculate the component values of R3 and C4 as a starting point. Further optimization of these component values might be desirable based on measurement results.

Note, that a tight layout of the critical components C18, Q1 and D2, and using an ultra fast rectifier diode are also essential to keep unwanted switching spikes under control.

Current Sense

The accurate control of the output current is one of the most important functions of the battery charger. It is achieved by the UC3909 control IC using average current mode control. An exact measurement of the current flowing in the output inductor, L1 is required. Therefore, a low value current sense resistor, R4 is placed in the ground return path, between the anode of D2 and the negative electrode of the output capacitor, C5. The voltage developed across R4 is proportional to the inductor current, and used by the controller to regulate the trickle and bulk charge current levels as well as to provide current limiting during overload operation.

The value of the current sense resistor is determined to satisfy two conditions. The first constraint is to limit the maximum voltage across R4 below 350mV when full output current is delivered. This is required by the UC3909 to prevent the current sense amplifier from saturation. The second restriction is the power dissipation of R4. In Table 3, the power dissipation of the current sense resistor was set to 1.5% of the maximum output power. This assumption was made to balance between two opposing requirements, namely to maintain high efficiency and to provide the highest signal level across R4, thus to improve noise immunity of the circuit. The maximum power dissipation equation of R4 might have to be revised, especially in higher power applications, due to component ratings and efficiency considerations.

Output Fuse

The fuse in series with the output of the battery charger is intended to prevent catastrophic failure if the battery is connected to the charger with reversed polarity. The fuse has to be selected with sufficient safety margin to carry the full charge current, but disconnect the output quickly in case of excessive currents drawn from the battery.

Parameter	Description	Definition	Value/Part#
Power Stage Design			
V_{RMM} (D1)	Diode Breakdown Voltage (minimum)	$V_{RRM} = 1.5 \cdot V_{BAT,MAX}$ (pick the next higher standard value)	(23.1V) 50V
$I_{O,MIN}$ (D1)	Diode Current Rating (minimum)	$I_{O,MIN} = 2 \cdot I_{BULK}$	1.6A
D1	Discharge Protection Diode	Select general purpose diode.	**GI750CT**
P_{D1}	Diode Power Dissipation (approximate value for heatsink selection)	$P_{D1} = I_{BULK} \cdot V_{D1F}$ (assuming 100°C junction temperature)	0.5W
V_{RMM} (D2)	Diode Breakdown Voltage (minimum)	$V_{RRM} = 1.5 \cdot V_{IN,MAX}$ (pick the next higher standard value)	(45V) 50V
$I_{O,MIN}$ (D2)	Diode Current Rating (minimum)	$I_{O,MIN} = 2 \cdot I_{BULK}$	1.6A
D2	Buck Freewheeling Diode	Select ultra fast switching diode.	**MUR610**
t_{RR}	Diode Reverse Recovery Time	catalog data; @ I_{BULK}; approximate value	35ns
I_{RRM}	Diode Peak Reverse Recovery Current	catalog data; @ I_{BULK}; approximate value	0.5A
P_{D2}	Diode Power Dissipation (approximate value for heatsink selection)	$P_{D2} = I_{BULK} \cdot (1 - D_{MIN}) \cdot V_{D2F} + 0.25 \cdot I_{RRM} \cdot V_{IN,MAX} \cdot t_{RR} \cdot f_S$	0.38W
V_{DSS} (Q1)	Switch Breakdown Voltage (minimum)	$V_{DSS} = 1.5 \cdot V_{IN,MAX}$ (pick the next higher standard value)	(45V) 50V
$I_{D,MIN}$ (Q1)	Transistor Current Rating (minimum)	$I_{D,MIN} = 4 \cdot I_{BULK}$	3.2A
Q1	Buck Main Switch	Select the MOSFET transistor	**IRFZ14**
R_{DSON} (Q1)	Switch ON Resistance	catalog data; @25°C, typical value	200mΩ
C_{OSS} (Q1)	Drain Source Capacitance	catalog data; typical value	160pF
I_{GATE}	Gate Charge/Discharge	approximate, average value	0.8A
Q_{GS} (Q1)	Gate-To-Source Charge	catalog data	3.1nC
Q_{GD} (Q1)	Gate-To-Drain Charge	catalog data	5.8nC
t_{OFF}; t_{ON}	Approximate Switching Times	$t_{OFF} = t_{ON} = \frac{Q_{GS} + Q_{GD}}{I_{GATE}}$	12ns
P_{Q1}	Switch Power Dissipation (approximate value for heatsink selection)	$P_{Q1} = I_{BULK}^2 \cdot D_{MAX} \cdot R_{DSON} \cdot 1.5 + 0.5 \cdot C_{OSS} \cdot V_{IN,MAX}^2 \cdot f_S + \frac{V_{IN,MAX} \cdot I_{BULK}}{2} \cdot (t_{OFF} + t_{ON} + t_{RR}) \cdot f_S$	0.21W
P_{HS}	Heatsink Power Dissipation	$P_{HS} = P_{D1} + P_{D2} + P_{Q1}$; worst case, estimate	1.1W
$\Delta I_{L,MAX}$	Inductor Ripple Current	$\Delta I_{L1,MAX} = 0.4 \cdot I_{BULK}$; typical value	0.32A
L1	Buck Inductance	$L1 = \frac{V_{IN,MAX}}{\Delta I_{L1,MAX} \cdot 4 \cdot f_S}$	(0.47mH) **0.4mH**
$I_{L1,PEAK}$	Inductor Peak Current	$I_{L1,PEAK} = I_{BULK} + \frac{V_{IN,MAX}}{8 \cdot L1 \cdot f_S}$	**1A**
L1	Buck Filter Inductor	Check vendor's list for off the shelf part number or design you inductor according to the values above	**PCV-2-400-05** (Coiltronics)

Parameter	Description	Definition	Value/Part#
V_{C3}	Input Capacitor Voltage Rating	$V_{C3} = 1.5 \cdot V_{IN,MAX}$ (pick the next higher standard value)	(45V) 50V
$I_{C3,RMS}$	Input Capacitor RMS Current	$I_{C3,RMS} = 0.5 \cdot I_{BULK}$ (worst case @ f_S; D=0.5)	0.4A
C3	Input Capacitor (electrolytic)	High frequency type, i.e. Panasonic HFQ series (see text for value considerations)	**680µF/35V**
C18	High Frequency Bypass Capacitor For Switches	Polypropylene or stacked metallized film. Minimum voltage rating equals V_{C3}.	**1µF/63V**
V_{C5}	Output Capacitor Voltage Rating	$V_{C5} = 1.5 \cdot V_{BAT,MAX}$ (pick the next higher standard value)	(23.1V) 25V
$I_{C5,RMS}$	Output Capacitor RMS Current	$I_{C5,RMS} = \frac{V_{IN,MAX}}{\sqrt{192} \cdot f_S \cdot L1}$	108mA
C5	Output Capacitor (electrolytic)	High frequency type, i.e. Panasonic HFQ series (see text for value considerations)	**470µF/25V**
$R_{C5,ESR}$	Output Capacitor's ESR	from datasheet	65mΩ
$P_{SN,MAX}$	Snubber Power Dissipation	$P_{SN,MAX} = P_{CH,MAX} \cdot 0.015$ assume 1.5% of full output power	0.185W
V_{C4}	Snubber Capacitor Voltage Rating	$V_{C4} = 1.5 \cdot V_{IN,MAX}$ (pick the next higher standard value)	(45V) 63V
C4	Snubber Capacitor (polypropylene or metallized film)	$C4 = \frac{2 \cdot P_{SN,MAX}}{V_{IN,MAX}^2 \cdot f_S}$ (pick the closest standard value)	(8.2nF) **10nF**
R3	Snubber Resistor (noninductive)	$R3 = \frac{1}{16 \cdot \pi \cdot f_S \cdot C4}$ (pick the closest standard value)	(39.8Ω) **39Ω**
$P_{R4,MAX}$	Current Sense Resistor Power Dissipation	$P_{R4,MAX} = P_{CH,MAX} \cdot 0.015$ assume 1.5% of full output power	0.185W
R4	Current Sense Resistor (RS) (noninductive)	$R4 \le \frac{0.35}{I_{L1,PEAK}}$ *AND* $R4 \le \frac{P_{R4,MAX}}{I_{BULK}^2}$ (pick the next lower standard value)	(291mΩ) **270mΩ** (RCD type: RSF1B)
F1	Output Fuse Rating (fast acting type)	$I_{F1} = 1.25 \cdot I_{BULK}$ (pick the next higher standard value)	(1.0A) **1A**

Table 3. Buck Converter Power Stage Components Design Sheet

Controller Design

The controller design is described in Table 4. Instructions are organized by the functional blocks of the circuit. This procedure is similar to the one explained in the power stage design. All the equations use parameters calculated or entered in the previous three tables or the preceding lines of Table 4.

Auxiliary Power Supply

The purpose of this circuit is to provide a stabilized voltage for the gate drive IC and for the UC3909 controller circuits. The auxiliary voltage has to be higher than 7.8V, the undervoltage lockout of the UC3909. Furthermore, the auxiliary voltage has to be suitable to drive the gate of the MOSFET switch directly, limiting the voltage level below 18V. The auxiliary voltage of the demonstration circuit is approximately 14.5V, to satisfy both requirements with appropriate margins.

The circuit configuration shown in Figure 4 assumes that the minimum input voltage is higher than the auxiliary voltage. In this case, R1 biases D3 to the zener voltage, and provide the base current to Q3. The auxiliary voltage will be equal to the zener voltage minus the base emitter voltage

of Q3. The advantage of this solution is that the controller supply current flowing through Q3, is independent from the input voltage.

For completeness, it should be mentioned that there are other solutions to power the controller section of the battery charger. The actual solution has to take into account the operating input voltage range, the selected gate drive technique and the type of semiconductor used in place of Q1. For example, using a P-channel MOSFET transistor will require a different gate drive technique but will allow the user to omit the auxiliary supply and to power up the UC3909 directly from the input voltage. Note that even in this case auxiliary power supply might be necessary if the maximum input voltage exceeds the VCC rating of the controller.

MOSFET Gate Drive

The gate drive circuit is based on the IR2125, High Voltage High Side Gate Driver integrated circuit from International Rectifier. The different considerations for designing the circuit are outlined in the IR2125 datasheet, [7], and are used in the component selection. The given part values are applicable for switching frequencies above 10kHz and limited below approximately 150kHz. Using the IR2125 is possible for input voltages below 500V due to the voltage rating of the device.

There is one design aspect regarding the gate drive circuit which needs to be clarified. The IR2125 like all other high side driver IC working with the bootstrapping principle monitors the voltage across the bootstrap capacitor to ensure sufficient voltage for turning on the MOSFET transistor. The first pulse appears at the gate when both voltages, VCC with respect to ground and VB with respect to the VS pin are above their respective undervoltage lockout thresholds. Thus, precharging the bootstrap capacitor, C2 is imperative to get the circuit initially running. During normal operation, C2 is charged instantaneously through the conducting rectifier diode, D2. Conversely, at startup D2 will prevent charging the bootstrap capacitor. Fortunately the problem can be solved by a large value resistor, R23 connected between the VS pin of the IR2125 and the ground of the circuit.

Differential Output Voltage Sense

The differential voltage sense block is optional. Several trade-offs will be discussed in a later chapter together with other practical considerations. Adding a simple operational amplifier and a couple of resistors provides tighter output voltage regulation and remote sensing capability to the charger.

The design of the differential voltage sense circuit has to satisfy two conditions. The gain of the amplifier must be higher than the reciprocal value of the number of cells connected in series in the battery. This assures that the output voltage of the differential amplifier is compatible with the voltages expected by the UC3909. A second condition is given in Table 4 ensures that the inputs of the differential amplifier stage will be kept within their common mode voltage range at any possible battery voltage. The actual gain, within these two limits, can be determined by the user.

Note that the gain of the amplifier, "A", will be used in the subsequent lines of Table 4. Therefore, even if the differential amplifier stage is omitted, the value of "A" shall be made equal to 1, and used for the rest of the calculations.

Housekeeping and Battery Temperature Sensing

The oscillator frequency is set by C8 and R8, and the UC3909 datasheet contains the exact timing equations. In Table 4, the timing equation is already solved for easily available capacitor values and for the most common frequency range. First the user selects the appropriate capacitor value based on the switching frequency defined in Table 2. Then the value of R8 is calculated, since resistor values are available in much finer steps than those of the capacitors.

In the demonstration circuit the battery temperature variation is simulated by the RP1 potentiometer. For actual temperature compensation, it shall be substituted by a L1005-5744-103-D1 type thermistor from Keystone Carbon Co. [11] or equivalent. Since the resistance of the thermistor should represent the battery temperature, it is usually mounted on or in the vicinity of the battery. To facilitate this, a two pin header, P4 is provided for convenient connection of the temperature sensor.

Current Limitation

Four resistors R9, R10, R11, and R12 program the three critical current levels, as defined in Table 1. A battery charger operates in current limited mode during trickle and bulk charge. The corresponding two current levels are the trickle current, $I_{TRICKLE}$

and the bulk charge current, I_{BULK}. A third distinct current level is the taper current threshold, I_{OCT} where the IC will switch from over-charge to float charge regime.

The accuracy of the different current levels depends on component tolerances and on some of the parameters of the control IC. Tolerances of the external resistors can be controlled by the appropriate part selection but the internal offsets and tolerances of the UC3909 are out of hand for the designer. The largest error term inside the IC is the offset of the current sense amplifier. Its effect is especially significant in trickle charge mode and at low current levels when the measured current signal is in the same order of magnitude than the input offset of the operational amplifier. For that reason, the initial accuracy of the trickle charge current limit can be in the neighborhood of ±30%. As the output current increases the accuracy improves rapidly and it is around ±5% at full current assuming 1% resistor tolerances.

Fortunately, in the battery charger application, only the bulk charge current has to be controlled precisely. The tolerances of the other two current values might influence the transitions between the charge regimes but do not represent a danger to the battery.

Setting The Output Voltages

The deep discharge threshold or cutoff voltage, over-charge voltage and float voltage are defined by the resistor network of R15, R16, R17, and R18, connected to the feedback pin of the UC3909. There are two different setup possibilities depending on whether the differential voltage sense circuit is used or omitted. With differential sensing, the calculated value of R15 resistor is placed in the position marked R15A, using the signal of the output of the operational amplifier, U4, for voltage regulation. In case of direct sensing of the output, the position R15B must be used instead. In order to provide tight tolerances of the three voltage levels, using 1% resistors is recommended.

Closing The Current Loop

"Closing the loop" is a frightening topic for many power supply designers. The detailed analysis of how to implement optimum loop compensation of the average current mode controller is beyond the scope of this Application Note. Nevertheless some excellent reference materials and design guide are listed in the Reference section of this paper [3], [4] and [5]. These articles cover not only the design criteria of the average current control loop used in the UC3909, but also explain the critical issues related to closing the voltage loop of the controller.

Using the procedure outlined in [3], closed form equations can be derived for all feedback components and they are given in Table 4.

Voltage Loop Compensation

The voltage loop of the demonstration circuit is compensated very conservatively for stability under wide operating conditions by introducing a dominant, low frequency pole to the system. The voltage loop crossover frequency is designed to be around 1kHz, which will result in a quite slow response to fast output voltage variations. However, the circuit performance is still acceptable since battery charging does not impose severe transient requirements on the power supply.

Note, that the equations given in Table 4 are suitable to implement stable voltage loop compensation but far from achieving the maximum bandwidth or best transient behavior.

Charge State Decoder

The battery charger progresses through four different operating modes which are related to the status of the charging process and to the replaced capacity of the battery. This information can be further processed to reveal vital information about the condition of the battery, to estimate the remaining charge time, and possibly to record the history of the battery. The UC3909 can signal the actual charge state in binary coded form on the STAT0 and STAT1 outputs. A truth table for decoding the status bits is given in the datasheet.

For the users convenience, a simple charge state decoder is implemented in the demonstration circuit. The decoding function is performed by an inexpensive integrated circuit, U3. According to the STAT0 and STAT1 outputs of the UC3909, one of its outputs are activated, which will cause one of the four transistors of Q4 - Q7, and respective light emitting diodes to turn on. Each LED corresponds to one of the four charge states as marked on the printed circuit board. The resistors R6 and R5 are intended to set the LED currents and to reduce the voltage across the collector and the emitter terminals of the transistors.

Parameter	Description	Definition	Value/Part#
Controller Part Values			
C6, C7, C13, C14, C15, C16,C17	Bypass Capacitors	X7R monolithic ceramic capacitors. Minimum voltage rating 25V.	**100nF/63V**
Auxiliary Power Supply			
D3	Auxiliary Voltage Stabilizer	**V_Z = 15V;** zener diode; 1W / 5%	**1N4744A**
V_{CEO} (Q3)	Collector Emitter Breakdown Voltage	$V_{CEO} = 1.5 \cdot (V_{IN,MAX} - V_Z)$ (select the next higher standard value)	(22.5V) 30V
Q3	Auxiliary Power Bypass	Select general purpose NPN transistor.	**2N3904**
R1	Zener Bias Resistor	$R1 = \frac{V_{IN,MIN} - V_Z}{2 \cdot 10^{-3}}$	**1.5kΩ**
P_{R1}	Zener Bias Resistor Power Dissipation	$P_{R1} = \frac{(V_{IN,MAX} - V_Z)^2}{R1}$	0.15W
C1	Auxiliary Power Storage Capacitor	Aluminum electrolytic capacitor. Minimum voltage rating 25V.	**82µF/25V**
Gate Drive			
U2	International Rectifier	High Voltage High Side MOS Gate Driver	**IR2125**
C2	Bootstrap Capacitor	Stacked metallized film capacitor. Minimum voltage rating 25V.	**0.15µF/50V**
D4, D5	Switching Signal Diodes	Select high speed signal switching diodes.	**1N4148**
Q2	Gate Drive Inverter	Select small signal MOSFET transistor.	**2N7000**
R2	Gate Resistor for Q1		**4.7Ω**
R21, R22	Gate Drive Pull Up Resistors		**1kΩ**
R23	Bootstrap Precharger		**1kΩ**
R30	Gate Pull Down Resistor		**10kΩ**
Differential Voltage Sense - Optional			
U4	National Semiconductor	Dual Single Supply Operational Amplifier	**LM358N**
$I_{FB,MAX}$	Maximum Current Through Feedback Resistors		150µA
R24, R27	Voltage Sense Resistors	$R24 = R27 = \frac{V_{BAT}}{I_{FB,MAX}}$	**91kΩ**
R28, R29	Voltage Sense Resistors	$R28 = R29 = 0.001 \cdot R24$	**91Ω**
R25, R26	Voltage Sense Divider	$R25 = R26 = A \cdot R24$; where A must be $\frac{1}{NC} < A < \frac{V_Z - 3}{V_{BAT,MAX}}$	**30kΩ**
A	Gain Of Voltage Sense Amplifier	$A = \frac{R25}{R24 + R28}$; A=1 if amplifier is omitted.	0.3297
Charger Control Section - IC Setup - Housekeeping And Temperature Sensing			
U1	Unitrode	Switchmode Lead-Acid Battery Charger IC	**UC3909N**
C8	Timing Capacitor, CT	f_S < 25 kHz 5.6nF 25 kHz < f_S < 50 kHz 3.3nF 50 kHz < f_S < 110 kHz 1.5nF 110 kHz < f_S < 220 kHz 680pF	**1.5nF**
R8	RSET Oscillator	$R8 = \frac{1}{1.2 \cdot C8 \cdot f_S}$	**11kΩ**

Parameter	Description	Definition	Value/Part#
R7	Reference Resistor For The Thermistor Linearizer	Select 1%, low temperature coefficient type.	**10kΩ**
RP1	Thermistor Emulation Potentiometer	Select 10 turns potentiometer for fine resolution. (Set initial value to 10kΩ before putting it in.)	**50kΩ**
Charger Control Section - IC Setup - Current Levels			
R9	OVCTAP Set Resistor (ROVC2)	Noncritical; use:	**100kΩ**
R10	OVCTAP Set Resistor (ROVC1)	$R10 = 1.8518 \cdot I_{OCT} \cdot R4 \cdot R9$	**10kΩ**
R11	Trickle Current Limit Set Resistor (RG1)	$R11 = 43.4783 \cdot I_{TRICKLE} \cdot R4 \cdot R8$	**2.7kΩ**
R12	Bulk Current Limit Set Resistor (RG2)	$R12 = \frac{0.54 \cdot R11}{I_{BULK} \cdot R4}$	**6.8kΩ**
Charger Control Section - IC Setup - Voltage Levels			
R15	Battery Voltage Divider (RS1) ±1% recommended	$R15 = \frac{V_{C,MAX}}{I_{FB,MAX}} \cdot \frac{V_{C,MIN} \cdot A \cdot NC - 2.3}{V_{C,MIN}}$	**11kΩ**
R16	Battery Voltage Divider (RS2) ±1% recommended	$R16 = \frac{2.3}{I_{FB,MAX}} \cdot \frac{V_{C,MAX} - V_{C,MIN}}{V_{C,MIN}}$	**6.2kΩ**
R17	Battery Voltage Divider (RS3) ±1% recommended	$R17 = \frac{2.3}{I_{FB,MAX}} \cdot \frac{V_{C,MAX} \cdot A \cdot NC - 2.3}{V_C \cdot A \cdot NC - 2.3}$	**18kΩ**
R18	Battery Voltage Float Adj. (RS4) ±1% recommended	$R18 = \frac{2.3}{I_{FB,MAX}} \cdot \frac{V_{C,MAX} \cdot A \cdot NC - 2.3}{(V_{C,MAX} - V_C) \cdot A \cdot NC}$	**130kΩ**
Charger Control Section - IC Setup - Current Error Amplifier			
R14	Current Error Amplifier Compensation Resistor	$R14 = \frac{0.28 \cdot f_S \cdot L1}{V_{BAT,MAX} + V_{D1F} + V_{D2F}} \cdot \frac{R11}{R4}$	**3.3kΩ**
C11	Current Error Amplifier Compensation Capacitor	$C11 = \frac{10}{2 \cdot \pi \cdot f_S \cdot R14}$	**10nF**
C12	Current Error Amplifier Compensation Capacitor	$C12 = \frac{1}{2 \cdot \pi \cdot f_S \cdot R14}$	**1nF**
Charger Control Section - IC Setup - Voltage Error Amplifier			
f_0	Voltage Loop Cross-Over Frequency	Dominant pole; noncritical requirements.	1kHz
R13	Voltage Error Amplifier Compensation Resistor	$R13 = \frac{0.625 \cdot V_{IN,MAX} \cdot (R15 + R16)}{A \cdot I_{BULK} \cdot f_S \cdot L1 \cdot V_{BAT,MAX}} \cdot \sqrt{\frac{1 + \left(16 \cdot \pi \cdot f_0 \cdot f_S \cdot L1 \cdot C5 \cdot \frac{V_{BAT,MAX}}{V_{IN,MAX}}\right)^2}{1 + (2 \cdot \pi \cdot f_0 \cdot R_{C5,ESR} \cdot C5)^2}}$	**910kΩ**
C9	Voltage Error Amplifier Compensation Capacitor	$C9 = \frac{C5 \cdot R_{C5,ESR}}{R13}$	**33pF**
C10	Voltage Error Amplifier Compensation Capacitor	$C10 = \frac{8 \cdot f_s \cdot L1 \cdot C5 \cdot V_{BAT,MAX}}{R13 \cdot V_{IN,MAX}}$	**47nF**
Charge State Decoder			
U3	Motorola	Dual Binary To 1-of-4 Decoder/Demultiplexer	**MC14555BCP**
D6, D7, D8, D9	Status Indicator LED's	Quad green LED assembly.	**IDI 5640H5**

Parameter	Description	Definition	Value/Part#
Q4, Q5, Q6, Q7	LED Driver Transistors	Minimum V_{CEO} equals $V_{IN,MAX}$ value	2N3904
R6	LED Current Set Resistor	$R6 = \frac{4.3}{0.01}$ assuming 10 mA LED current.	430Ω
R5	Voltage Limiter of the LED Driver Transistors	$R5 = \frac{V_{IN,MIN} - 7}{0.01}$	1.1kΩ
R19, R20	Pull Up Resistors	Noncritical; use:	10kΩ

Table 4. Four State Battery Charger Controller Design Sheet

PARTS LIST

The following Bill Of Material was generated from the calculated part values listed in Table 3 and 4. The part designators correspond to the Demonstration Board component positions.

C1	82µF,	25V	electrolytic
C2	0.15µF	50V	met.film / polypropylene
C3	680µF	35V	electrolytic
C4	10nF	50V	met.film / polypropylene
C5	470µF	25V	electrolytic
C6	0.1µF	50V	ceramic
C7	0.1µF	50V	ceramic
C8	1.5nF	50V	ceramic
C9	33pF	50V	ceramic
C10	47nF	50V	ceramic
C11	10nF	50V	ceramic
C12	1.0nF	50V	ceramic
C13	0.1µF	50V	ceramic
C14	0.1µF	50V	ceramic
C15	0.1µF	50V	ceramic
C16	0.1µF	50V	ceramic
C17	0.1µF	50V	ceramic
C18	1.0µF	63V	met.film / polypropylene
D1	GI750CT		100V, 6A, general
D2	MUR610CT		100V, 6A, ultrafast
D3	1N4744A		15V,1W zener
D4	1N4148		75V, 200mA, switching
D5	1N4148		75V, 200mA, switching
D6-D9	L20355		LED assembly,IDI
L1	375µH	4A	Coilcraft
Q1	IRFZ14		60V, 10A, NMOS
Q2	2N7000		60V, 500mA, NMOS
Q3	2N3904		40V, 200mA, NPN
Q4	2N3904		40V, 200mA, NPN
Q5	2N3904		40V, 200mA, NPN
Q6	2N3904		40V, 200mA, NPN
Q7	2N3904		40V, 200mA, NPN
R1	1.5kΩ	5%, 0.25W	
R2	4.7Ω	5%, 0.25W	
R3	39Ω	5%, 0.6W	metal film
R4	270mΩ	5%, 1W	RCD-RSF1B
R5	1.1kΩ	5%, 0.25W	
R6	430Ω	5%, 0.25W	
R7	10kΩ	5%, 0.25W	
R8	11kΩ	5%, 0.25W	
R9	100kΩ	5%, 0.25W	
R10	10kΩ	5%, 0.25W	
R11	2.7kΩ	5%, 0.25W	
R12	6.8kΩ	5%, 0.25W	
R13	910kΩ	5%, 0.25W	
R14	3.3kΩ	5%, 0.25W	
R15A	11kΩ	1%, 0.25W	
R16	6.2kΩ	1%, 0.25W	
R17	18kΩ	1%, 0.25W	
R18	130kΩ	1%, 0.25W	
R19	10kΩ	5%, 0.25W	
R20	10kΩ	5%, 0.25W	
R21	1kΩ	5%, 0.25W	
R22	1kΩ	5%, 0.25W	
R23	1kΩ	5%, 0.25W	
R24	91kΩ	1%, 0.25W	
R25	30kΩ	1%, 0.25W	
R26	30kΩ	1%, 0.25W	
R27	91kΩ	1%, 0.25W	
R28	91Ω	5%, 0.25W	
R29	91Ω	5%, 0.25W	
R30	10 kΩ	5%, 0.25W	
RP1	50kΩ	0.25W	10 turns potentiometer
U1	UC3909N		Battery Charger Controller
U2	IR2125		High Side Driver
U3	MC14555BCP		Binary to 1-of-4 Decoder
U4	LM358N		Operational Amplifier

MEASUREMENT RESULTS

Checking Out The Circuit

To safely bring the circuit into operation, the following precautions shall be exercised to prevent catastrophic failures at the first turn on. Use sockets for all integrated circuits and do not plug them in until the auxiliary power supply is checked.

All voltages given in the rest of this chapter are with respect to circuit ground unless otherwise noted.

Step 1.

Connect the input of the circuit to your DC power source. Increase the input voltage slowly up to the minimum input voltage value used in Table 2. Check the auxiliary supply voltage at the test point, TP21. The correct value should be 0.7V less than the V_Z voltage listed in Table 4, approximately 14.3V for this example. The same voltage should be measured at pin 4 of U4, pin 1 of U2 and pin 8 of U4 integrated circuits. When all voltages are correct, remove the input power.

Step 2.

Install U1, and connect the input voltage again. Measure the reference voltage of the UC3909. The correct voltage on pin 2 (TP2) is 5V. Next, check the oscillator. Measure and compare the timing capacitor and output waveforms, TP19 and TP5 respectively, to the oscillogram shown in Figure 5.

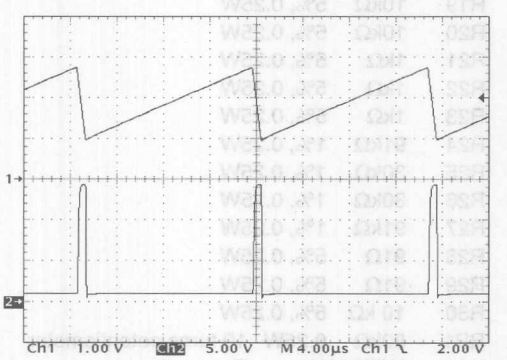


Figure 5. Trace 1: Timing Capacitor Waveform; Trace 2: OUT pin of UC3909

Compare the operating frequency to the expected value listed in Table 2. Disconnect the input voltage.

Step 3.

Populate the remaining of the IC sockets, by installing U2, U3, and U4 integrated circuits. Connect a resistive load to the output terminals. The load resistor shall be calculated as:

$$R_{LOAD} = \frac{2 \cdot V_{BAT}}{I_{OCT}}$$

Slowly raise the input voltage of the circuit while continuously monitoring the output voltage. The output voltage shall increase together with the input voltage until the output equals the float voltage, V_{BAT}. For further increases of the input voltage, the output should be regulated at the float charge voltage. If the output is not regulating, stop increasing the input voltage. Check the component values in the feedback divider, and the operating conditions of the UC3909. Convenient test points are provided in the demonstration board, for easy access to the pins of the integrated controller. The descriptions and typical voltages of the individual pins are included in the datasheet of the UC3909.

Step 4.

Once the output voltage is stabilized, check the switching waveforms of the converter. Typical waveforms of gate drive (U2/pin2), Q1 drain current, TP24, and the output inductor current, measured at full load, are shown in Figure 6.

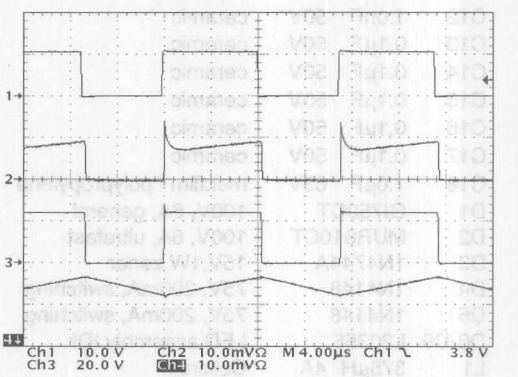


Figure 6. Switching waveforms of the converter: Trace 1: OUT pin; Trace 2: I_{o1} (1A/div); Trace 3: TP24; Trace 4: I_L (0.5A/div)

Step 5.

The final test of the circuit is to check the bulk charge current limit, the float and over-charge voltage levels. The load resistor defined in step 2 ensures float mode operation of the charger. Note the

float voltage then gradually increase the load current until the charger reverts to bulk charge mode. At this point the output current should be equal to I_{BULK}. By slowly reducing the load current, the charger will sequence to the next state, over-charging. In this mode of operation the output voltage equals to $V_{BAT,MAX}$, the over-charge voltage. Verify the numbers against the values in Table 1.

Charge Characteristic

The ultimate test of the circuit is to charge a battery. The demonstration circuit has been designed to charge a 12V, 2.2Ah sealed lead-acid battery. During the charge cycle, the battery voltage and current, and the displayed operating states have been recorded. The result is shown in Figure 7.

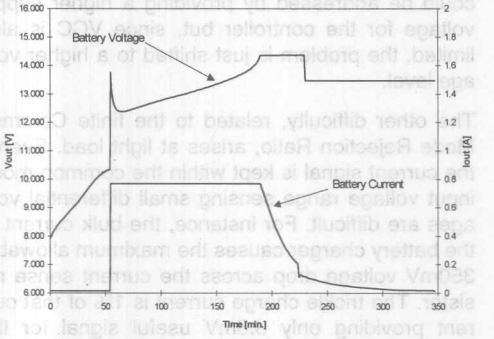


Figure 7. JC1222 Charge Characteristic

The chart shows the change of the battery voltage and charge current as a function of time and the exact values of the characteristic parameters. As can be seen, the charger started with trickle charge mode. When the battery voltage reached the cutoff voltage, the charger switched over to bulk charging. The sharp peak in the battery voltage at the switch over is caused by the high internal impedance of the battery. The majority of the battery capacity is replenished in about two hours in bulk charge mode. Bulk charge is followed by the controlled over-charge of the battery. Note that the over-charge LED is turned on before the voltage loop is satisfied because the threshold of the voltage sense comparator is intentionally set 5% below the reference of the voltage error amplifier. This way, the turn on of the over-charge LED coincides with the onset of the chemical over-charge process indicated by the gradient change in the voltage curve. The battery charging process concludes in float mode when the current tapers off to near zero.

Efficiency

The efficiency of a converter is usually measured as a function of load current at a fixed output voltage and at different input voltages. While this method is really informative in DC-to-DC applications, it is very difficult to assess the efficiency of a battery charger this way. Since the load current and the output voltage of the converter vary continuously during charging, one single efficiency number carries very little information about the circuit.

To demonstrate the effect, three different efficiency graphs are given below. The first one shows the effect of the output voltage variation on the efficiency. The second one is the traditional efficiency chart at a fixed output voltage.

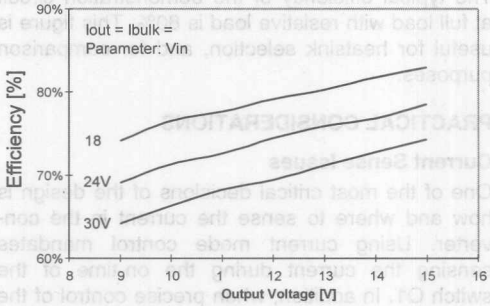


Figure 8. Efficiency vs. Output Voltage

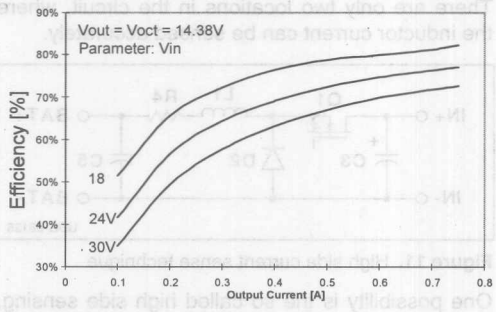


Figure 9. Efficiency vs. Load Current

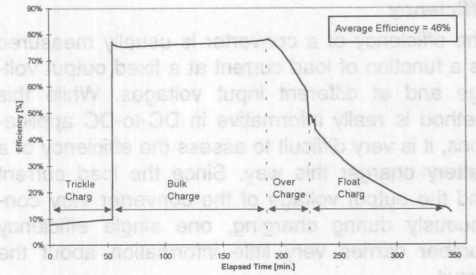


Figure 10. Efficiency vs. Time During Battery Charging

The third one presents the efficiencies during the entire charge cycle and the calculated average efficiency of the battery charger.

The typical efficiency of the demonstration circuit at full load with resistive load is 80%. This figure is useful for heatsink selection, and for comparison purposes.

PRACTICAL CONSIDERATIONS

Current Sense Issues

One of the most critical decisions of the design is how and where to sense the current in the converter. Using current mode control mandates sensing the current during the on-time of the switch Q1. In addition, when precise control of the output current is necessary, knowing the exact output current is inescapable. The output current of the buck converter equals the output inductor current, leaving very little choice to the designer. There are only two locations in the circuit, where the inductor current can be sensed accurately.

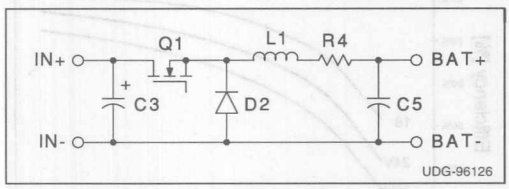


Figure 11. High side current sense technique

One possibility is the so called high side sensing, where the current sense resistor is placed in series with the output inductor as shown in Figure 11. For reliable operation it is important to put the resistor at the output capacitor side of the inductor, to avoid having a large switching component added to the inherently small current sense signal. Even with this precaution taken into account, the signal sits on top of a large common mode DC voltage (appr. V_{BAT}) which represents a problem for the current sense amplifier.

The amplifier has a limited Common Mode Input Voltage Range and a finite Common Mode Rejection Ratio which both confine its capability and its precision when the measured signal contains a significant common mode component. To illustrate the problem, look at the demonstration circuit.

When the battery is close to its fully charged state the current signal is superimposed on a 16V DC signal. At the same time, the supply voltage of the UC3909 is approximately 14.5V. In this case the Common Mode Input Voltage Range of the current sense amplifier is exceeded and the current information is either lost or erroneous. The problem could be addressed by providing a higher supply voltage for the controller but, since VCC is also limited, the problem is just shifted to a higher voltage level.

The other difficulty, related to the finite Common Mode Rejection Ratio, arises at light load. Even if the current signal is kept within the common mode input voltage range sensing small differential voltages are difficult. For instance, the bulk current of the battery charger causes the maximum allowable 350mV voltage drop across the current sense resistor. The trickle charge current is 1% of that current providing only 3.5mV useful signal for the amplifier. Assume that the output voltage is 10V and the CMRR of the current sense circuit is 60dB. There will be two components determining the output voltage of the amplifier. The amplified current signal, 17.5mV, is added to a 10mV error signal, developed from the 10V common mode components, present at the inverting and noninverting inputs of the current sense amplifier. As demonstrated, the error caused by the common mode component is rather significant, it is in the order of 35%.

The other possibility to monitor the inductor current is in the ground return path, as it is done in the demonstration circuit. This solution eliminates both problems related to the common mode properties of the amplifier since one end of the current sense resistor is actually grounded. The disadvantage of this technique is that the input and output grounds of the charger are not the same potential any more.

The low side current sensing offers two places for grounding the controller. The GND pin of the UC3909 can be connected either to the output side of the current sense resistor, or to its node com-

mon to the input of the buck regulator. When the IC is grounded at the output side, the output voltage is regulated perfectly. On the other hand the supply current of the UC3909 has to flow through the current sense resistor causing an error in the current measurement. The ICC of the controller has a wide tolerance which made the design of the trickle charge current very inaccurate.

Finally, the solution used in the demonstration circuit grounds the controller to the input side of the current sense resistor. It gives the best result to closely control the currents from no load to full current. The only factor influencing the accuracy of the current measurement is the input offset voltage of the current sense amplifier.

Until now, the effect of the current sense amplifier was neglected. Note that this offset is not specific to the low side sensing technique, and it would have further deteriorated the accuracy of any previously mentioned current sense method.

The current sense amplifier of the UC3909 possesses a 15mV maximum input offset voltage. This 15mV is comparable to the current signal in trickle charge mode. This explains the rather loose tolerance of the trickle charge current limit, mentioned earlier in the design chapter.

Although this approach exhibits the optimum properties to control the output current, it introduced a problem for the voltage regulation. Since the regulated voltage appears between the positive output terminal and the circuit ground, the output of the battery charger is not tightly controlled. The error is caused by the voltage drop across R4, proportional to the output current. At full current, at the beginning of the over-charge period the output voltage will be 350mV lower than the calculated over-charge voltage level, and as the current tapers off the error is diminishing. In float charge mode the output current, hence the voltage deviation from the designed value is negligible.

Differential Voltage Sense Advantages

By using the two inputs of the differential amplifier stage, the output voltage can be regulated between any two points of the output, independently from the grounding of the controller. When the two inputs are connected to the solder joints of the output connector, the effect of resistive voltage drops across the current sense resistor and on the printed circuit board traces can be eliminated. Furthermore, the user can compensate for the external voltage drop on the wiring between the output of the charger and the battery nodes using the two remote sense connections.

Driving A P-channel MOSFET Switch

The demonstration circuit takes advantage of the lower cost and better efficiency of an N-channel MOSFET. However, using a P-channel transistor can also be accomplished easily. Figure 12 shows a possible implementation of the P-channel MOSFET switch, driven by the UC3909.

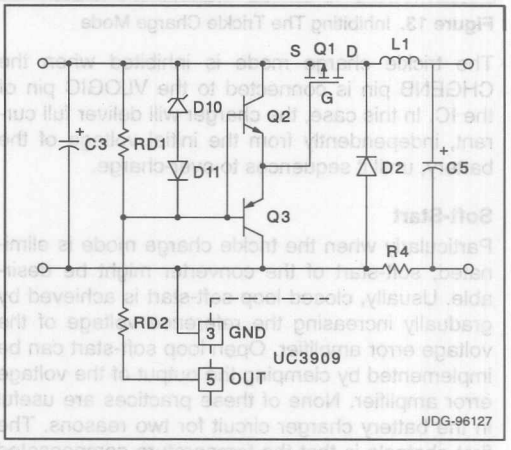


Figure 12. P-channel MOSFET Drive

The disadvantage of this technique is the relatively high power loss in the level shift circuit. The switching speed of the high side P-channel MOSFET is determined by the two series resistors connected to the output of the controller. To achieve acceptable turn-off speed the resistor values can not be increased. Therefore, the losses are especially high at elevated input voltages and at higher switching frequencies.

Skipping The Trickle Charge Mode

Depending on the battery type and the application, the trickle charge mode might not be necessary. Particularly, the new lead-acid batteries built from pure lead plates can accept full charge current from the beginning of the charge cycle. This requirement can be effortlessly accommodated by the UC3909 as shown in Figure 13.

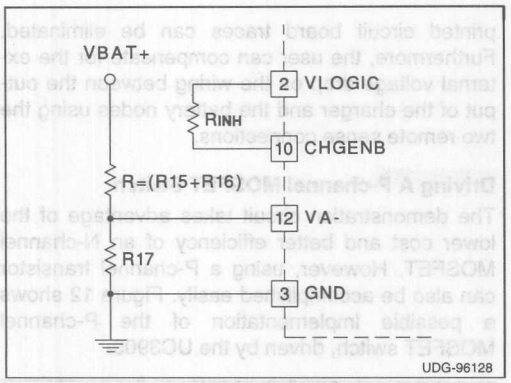


Figure 13. Inhibiting The Trickle Charge Mode

The trickle charge mode is inhibited when the CHGENB pin is connected to the VLOGIC pin of the IC. In this case, the charger will deliver full current, independently from the initial voltage of the battery, until it sequences to over-charge.

Soft-Start

Particularly when the trickle charge mode is eliminated, soft-start of the converter might be desirable. Usually, closed loop soft-start is achieved by gradually increasing the reference voltage of the voltage error amplifier. Open loop soft-start can be implemented by clamping the output of the voltage error amplifier. None of these practices are useful in the battery charger circuit for two reasons. The first obstacle is that the temperature compensated reference of the error amplifier is not available for external manipulations. The second problem is that the battery is already connected at turn on.

Since the battery is discharged at the beginning of the charging process, the voltage error amplifier is saturated and the converter operates in current limited mode. Therefore, soft-start can be introduced only in the current control loop. In general purpose buck converters this would result in output voltage overshoot during start-up, but with the battery connected to the output, this problem does not exist. The following circuit, shown in Figure 14 can be added to provide a simple soft-start solution for the battery charger.

The output current of the buck converter will ramp up gradually to the full bulk current value according to the RC time constant in Figure 14. This solution requires extreme cautions to ensure that precharging of the bootstrap capacitor is accomplished well before the charging of the soft-start capacitor is complete.

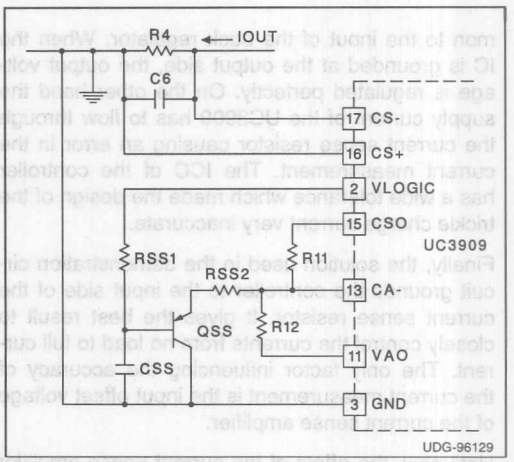


Figure 14. Soft-Start Of The UC3909

Eliminate Float Charge

The majority of the applications use the lead-acid batteries as backup power sources. In case of losing the primary power source, the system relies on the availability of the entire battery capacity. The float mode operation of the battery charger is intended to ensure that the battery is in its fully charged state during the stand by period.

As was mentioned earlier, finding the appropriate float voltage is critical to maintain 100% capacity of the battery. An easy way to avoid the problems related to float charge is to terminate the charging process upon completion of the over-charge process.

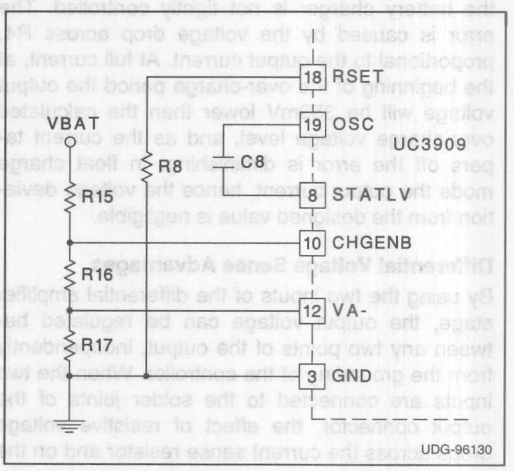


Figure 15. Disabling Float Charge State

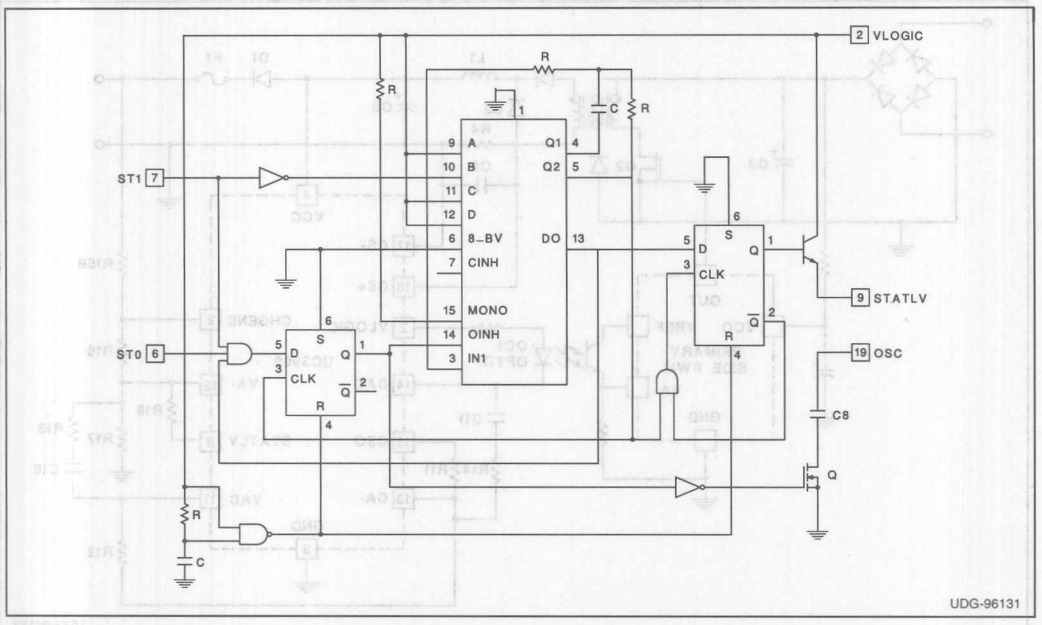


Figure 16. Implementing The Timed Charge Method

The solution shown in Figure 15 eliminates the float mode operation by disabling the oscillator. The advantage of this approach is that the IC will recover to bulk charge mode automatically if the battery voltage drops 10% below its nominal float voltage value.

Note that there are numerous other applications which also do not require float charging the batteries. For instance, batteries in hand held tools and portable equipment are recharged quickly while the primary power source is available, but do not employ float mode operation.

Incorporating Timed Algorithms

The constant voltage charge of the lead-acid batteries necessitates combining voltage monitoring and time measurement. It requires applying constant output voltage across the battery terminals for a certain time interval. Although the UC3909 is not optimized for these algorithms, the circuit diagram in Figure 16 shows how to combine the timer with the controller.

Off-line Configurations

Very often battery chargers are operated from the AC line. Figure 17 shows line isolation with a 60Hz transformer. This technique provides a low cost, competitive solution for low power applications. Furthermore, it can be advantageous for medium power, stationary applications because of its simplicity.

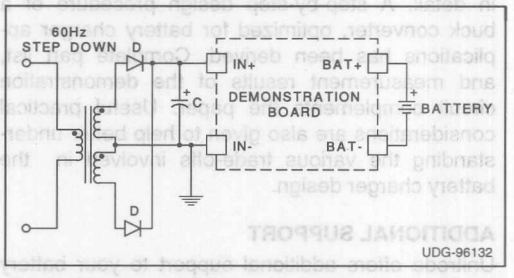


Figure 17. Isolated Off-Line Charger With 60Hz Step-Down Transformer

At higher output power, or in portable applications, the 60Hz isolation transformers become bulky. In this situation, line isolation is frequently obtained in the switchmode power stage. The forward converter, shown in Figure 18 is the isolated version of the buck topology. The components of the demonstration circuit can be easily recognized in the schematic drawing.

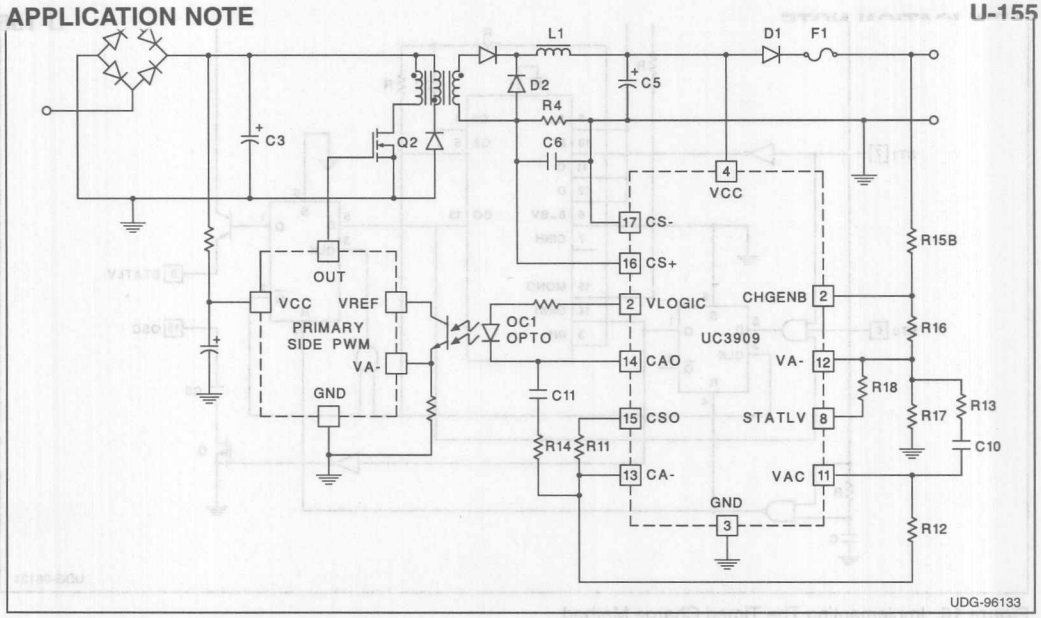


Figure 17. Forward Converter With Line Isolation

SUMMARY

This Application Note introduced the UC3909 Switchmode Lead-Acid Battery Charger controller in detail. A step-by-step design procedure of a buck converter, optimized for battery charger applications has been derived. Complete part list, and measurement results of the demonstration circuit complements the paper. Useful practical considerations are also given to help better understanding the various trade-offs involved in the battery charger design.

ADDITIONAL SUPPORT

Unitrode offers additional support to your battery charger project. The Appendix contains the MathCad® design file used to perform all calculations for Table 1 - 4. In addition, a printed circuit board of the fully functional battery charger circuit, useful upto 4A of continuos charge current is available for further evaluation.

For more information on the UC3909 Switchmode Lead-Acid Battery Charger controller or to order the demonstration circuit, please contact your Unitrode representative or the factory directly at (603) 424-2410.

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APPENDIX

This MathCad file calculates the parameters and part values of the
UC3909 Switchmode Lead-Acid Battery Charger demonstration circuit.

NOTES:
- names ending to an "E" (i.e. R1E) are results of the respective calculations and they require manual entry of standard component values before continuing the calculations.

TABLE 1.

Input parameters:

NC := 6	Number of cells connected in **series** within the battery.
Cr := 2.2	Capacity of the battery.
Vc := 2.275	Cell float voltage at 25°C.
Vcmax := 2.43	Maximum cell voltage during controlled over-charge at 25°C.
Vcmin := 1.75	Minimum cell voltage at full discharge on 25°C.
It := 0	Trickle charge current. Enter the data from the battery datasheet or 0 for the default value (Itrickle=0.01*Cr).
Ib := 0.8	Bulk charge current. Enter the data from the battery datasheet or 0 for the default value (Ibulk=0.5*Cr).
Io := 0	Over-charge taper current threshold. Enter the data from the battery datasheet or 0 for the default value (Ioct=0.25*Ibulk).
TC := - 0.0039	Battery Temperature coefficient.
Tmin := - 10	Minimum operating temperature of the battery.
Tmax := 50	Maximum operating temperature of the battery.

Equations:	**Calculated paprameters:**
$Itrickle := if(It=0, 0.01 \cdot Cr, It)$	Itrickle = 0.022
$Ibulk := if(Ib=0, 0.4 \cdot Cr, Ib)$	Ibulk = 0.8
$Ioct := if(Io=0, 0.25 \cdot Ibulk, Io)$	Ioct = 0.2
$Vbat := Vc \cdot NC$	Vbat = 13.65
$Vbatmin := (Vcmin + (Tmax - 25) \cdot TC) \cdot NC$	Vbatmin = 9.915
$Vbatmax := (Vcmax + (Tmin - 25) \cdot TC) \cdot NC$	Vbatmax = 15.399
$Pchmax := Vbatmax \cdot Ibulk$	Pchmax = 12.319

TABLE 2.

Input parameters:

$Vinmin := 18$	Minimum input voltage of the battery charger.
$Vinmax := 30$	Maximum input voltage of the battery charger.
$fs := 50000$	Switching frequency of the converter.
$Vd1f := 0.59$	Forward voltage drop of D1 at Ibulk and 100°C junction temperature.
$Vd2f := 0.73$	Forward voltage drop of D2 at Ibulk and 100°C junction temperature.

Equations:

$$Dmax := \frac{Vbatmax + Vd1f + Vd2f}{Vinmin + Vd2f}$$

$$Dmin := \frac{Vbatmin + Vd1f + Vd2f}{Vinmax + Vd2f}$$

Calculated paprameters:

$Dmax = 0.893$

$Dmin = 0.366$

TABLE 3.

Input parameters:

$trr := 35 \cdot 10^{-9}$	Reverse recovery time of D2 at Ibulk (estimate).
$Irrm := 0.5$	Peak reverse recovery current of D2 (estimate).
$Rdson := 0.2$	Channel resistance of Q1 at 25°C (the catalog data).
$Coss := 160 \cdot 10^{-12}$	Q1 drain source capacitance.
$Igate := 0.8$	Average gate current during turning on and off Q1.
$Qgs := 3.1 \cdot 10^{-9}$	Gate-to-source charge of Q1.
$Qgd := 5.8 \cdot 10^{-9}$	Gate-to-drain charge of Q1.

Equations:

$VrmmD1 := 1.5 \cdot Vbatmax$

$IminD1 := 2 \cdot Ibulk$

$Pd1 := Ibulk \cdot Vd1f$

$VrmmD2 := 1.5 \cdot Vinmax$

$IminD2 := 2 \cdot Ibulk$

Calculated paprameters:

$VrmmD1 = 23.099$

$IminD1 = 1.6$

$Pd1 = 0.472$

$VrmmD2 = 45$

$IminD2 = 1.6$

$Pd2 := Ibulk \cdot (1 - Dmin) \cdot Vd2f + 0.25 \cdot Irrm \cdot Vinmax \cdot trr \cdot fs$ $Pd2 = 0.377$

$VdssQ1 := 1.5 \cdot Vinmax$ $VdssQ1 = 45$

$Idmin := 4 \cdot Ibulk$ $Idmin = 3.2$

$tonoff := \frac{Qgs + Qgd}{Igate}$ $tonoff = 1.113 \cdot 10^{-8}$

$Pq1 := (Ibulk)^2 \cdot Dmax \cdot Rdson \cdot 1.5 + 0.5 \cdot Coss \cdot (Vinmax)^2 \cdot fs + \frac{Vinmax \cdot Ibulk}{2} \cdot (2 \cdot tonoff + trr) \cdot fs$ $Pq1 = 0.209$

$Phs := Pd1 + Pd2 + Pq1$ $Phs = 1.058$

$dImax := 0.4 \cdot Ibulk$ $dImax = 0.32$

$L1E := \frac{Vinmax}{4 \cdot dImax \cdot fs}$ $L1E = 4.687 \cdot 10^{-4}$ $L1 := 400 \cdot 10^{-6}$

$IL1peak := Ibulk + \frac{Vinmax}{8 \cdot L1 \cdot fs}$ $IL1peak = 0.988$

$Vc3 := 1.5 \cdot Vinmax$ $Vc3 = 45$

$Ic3rms := 0.5 \cdot Ibulk$ $Ic3rms = 0.4$

$Vc5 := 1.5 \cdot Vbatmax$ $Vc5 = 23.099$

$Ic5rms := \frac{Vinmax}{\sqrt{192} \cdot fs \cdot L1}$ $Ic5rms = 0.108$

$Psn := 0.015 \cdot Pchmax$ $Psn = 0.185$

$Vc4 := 1.5 \cdot Vinmax$ $Vc4 = 45$

$C4E := \frac{2 \cdot Psn}{(Vinmax)^2 \cdot fs}$ $C4E = 8.213 \cdot 10^{-9}$ $C4 := 10 \cdot 10^{-9}$

$R3E := \frac{1}{16 \cdot \pi \cdot fs \cdot C4}$ $R3E = 39.789$ $R3 := 39$

$Pr4max := 0.015 \cdot Pchmax$ $Pr4max = 0.185$

$R4E1 := \frac{0.35}{IL1peak}$ $R4E1 = 0.354$ $R4E2 := \frac{Pr4max}{(Ibulk)^2}$ $R4E2 = 0.289$

$R4E := if(R4E1 > R4E2, R4E2, R4E1)$ $R4E = 0.289$ $R4 := 0.27$

$Pr4rated := (Ibulk)^2 \cdot R4 \cdot 5$ $Pr4rated = 0.864$

$If1 := 1.25 \cdot Ibulk$ $If1 = 1$

TABLE 4.

Input parameters:

$Vref := 2.3$	Internal reference voltage of the UC3909.
$Vlogic := 5$	The voltage on the VLOGIC pin of the UC3909.
$Vz := 15$	Zener voltage of D3.
$Ifbmax := 150 \cdot 10^{-6}$	Maximum current of the voltage feedback divider. This current always loads the battery.
$Ae := \frac{30}{91}$	Guess value of the gain (A) of the voltage sense amplifier.
$C8 := 1.5 \cdot 10^{-9}$	Timing capacitor value.
$C5 := 470 \cdot 10^{-6}$	Output capacitor value.
$Rc5esr := 65 \cdot 10^{-3}$	Equivalent series resistance of the output capacitor, C5.
$R9 := 100 \cdot 10^{3}$	Free parameter.
$f0 := 1000$	Voltage loop cross-over frequency.

Equations:		**Calculated paprameters:**
$VceoQ3 := 1.5 \cdot (Vinmax - Vz)$		$VceoQ3 = 22.5$
$R1E := \frac{Vinmin - Vz}{0.002}$	$R1E = 1.5 \cdot 10^{3}$	$R1 := 1500$
$Pr1 := \frac{(Vinmax - Vz)^2}{R1}$		$Pr1 = 0.15$
$R24E := \frac{Vbat}{Ifbmax}$	$R24E = 9.1 \cdot 10^{4}$	$R24 := 91 \cdot 10^{3}$
$R28 := 0.001 \cdot R24$		$R28 = 91$
$R25E := Ae \cdot R24$	$R25E = 3 \cdot 10^{4}$	$R25 := 30 \cdot 10^{3}$
$A := \frac{R25}{R24 + R28}$		$A = 0.329$
$R8E := \frac{1}{1.2 \cdot C8 \cdot fs}$	$R8E = 1.111 \cdot 10^{4}$	$R8 := 11000$
$R10E := 1.8518 \cdot Ioct \cdot R4 \cdot R9$	$R10E = 1 \cdot 10^{4}$	$R10 := 10000$
$R11E := 43.4783 \cdot Itrickle \cdot R4 \cdot R8$	$R11E = 2.841 \cdot 10^{3}$	$R11 := 2700$
$R12E := \frac{0.54 \cdot R11}{Ibulk \cdot R4}$	$R12E = 6.75 \cdot 10^{3}$	$R12 := 6800$

$$R15E := Vcmax \cdot \frac{Vcmin \cdot A \cdot NC - Vref}{Ifbmax \cdot Vcmin} \qquad R15E = 1.072 \cdot 10^{4} \qquad R15 := 11000$$

$$R16E := \frac{Vref}{Ifbmax} \cdot \frac{Vcmax - Vcmin}{Vcmin} \qquad R16E = 5.958 \cdot 10^{3} \qquad R16 := 6200$$

$$R17E := \frac{Vref}{Ifbmax} \cdot \frac{Vcmax \cdot A \cdot NC - Vref}{Vc \cdot A \cdot NC - Vref} \qquad R17E = 1.747 \cdot 10^{4} \qquad R17 := 18000$$

$$R18E := \frac{Vref}{Ifbmax} \cdot \frac{Vcmax \cdot A \cdot NC - Vref}{(Vcmax - Vc) \cdot A \cdot NC} \qquad R18E = 1.252 \cdot 10^{5} \qquad R18 := 130000$$

$$R14E := \frac{0.28 \cdot fs \cdot L1}{Vbatmax + Vd1f + Vd2f} \cdot \frac{R11}{R4} \qquad R14E = 3.349 \cdot 10^{3} \qquad R14 := 3300$$

$$C12E := \frac{1}{2 \cdot \pi \cdot fs \cdot R14} \qquad C12E = 9.646 \cdot 10^{-10} \qquad C12 := 1000 \cdot 10^{-12}$$

$$C11 := 10 \cdot C12 \qquad C11 = 1 \cdot 10^{-8}$$

$$R13E := \frac{0.625 \cdot Vinmax}{A \cdot Ibulk \cdot fs \cdot L1 \cdot Vbatmax} \cdot \sqrt{\frac{1 + \left(16 \cdot \pi \cdot f0 \cdot fs \cdot L1 \cdot C5 \cdot \frac{Vbatmax}{Vinmax}\right)^{2}}{1 + (2 \cdot \pi \cdot f0 \cdot Rc5esr \cdot C5)^{2}}} \cdot (R15 + R16)$$

$$R13E = 9.466 \cdot 10^{5} \qquad R13 := 910 \cdot 10^{3}$$

$$C9E := \frac{C5 \cdot Rc5esr}{R13} \qquad C9E = 3.357 \cdot 10^{-11} \qquad C9 := 33 \cdot 10^{-12}$$

$$C10E := \frac{C5 \cdot Vbatmax}{R13 \cdot Vinmax} \cdot 8 \cdot fs \cdot L1 \qquad C10E = 4.242 \cdot 10^{-8} \qquad C10 := 47 \cdot 10^{-9}$$

$$R6E := \frac{Vlogic - 0.7}{0.01} \qquad R6E = 430 \qquad R6 := 430$$

$$R5E := \frac{Vinmin - 7}{0.01} \qquad R5E = 1.1 \cdot 10^{3} \qquad R5 := 1100$$

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THE UC3886 PWM CONTROLLER USES AVERAGE CURRENT MODE CONTROL TO MEET THE TRANSIENT REGULATION PERFORMANCE OF HIGH END PROCESSORS

by Larry Spaziani
Applications Engineer

ABSTRACT

The continuing development of high performance processors is imposing stringent requirements on their respective power systems. Intel's Pentium®Pro power system specification, for instance, demonstrates the industry trend to operate at lower voltages and at higher currents, with tight regulation and fast transient response. To meet these requirements, the UC3886 Average Current Mode PWM Controller is introduced. This application note highlights the features of the UC3886 and details how this IC is ideal for creating the optimal switching regulator for low voltage processor applications.

UC3886 FEATURES AND BENEFITS

- Average Current Mode Control direct from a sense resistor
  - No slope compensation networks required
- High Gain-Bandwidth Amplifiers for a fast transient response
- Programmable Current Sense Amplifier
  - Interfaces to a low power sense resistor
  - Accurate Over Current Protection
- On-board Reference for Standalone operation
- Direct Drive for Buck regulator NMOS high side switch
  - Eliminates need for separate Driver IC

INTRODUCTION

The Intel Pentium®Pro microprocessor specifications underscore an ongoing trend in high end digital systems. Clock frequencies are increasing for improved throughput and the number of transistors is increasing as manufacturing technology improves. Power management both within the processor and power to the processor has been elevated to a significant architectural design consideration.

The consequence of these advances for the power system is requirements that strike fear in the most hardy power supply designers. Load current increases as the number of transistors and the clock frequency increase whereas operating voltage decreases to limit the power dissipation on the processor. Noise immunity decreases as well under these conditions resulting in much tighter regulation requirements. High efficiency must be maintained even though currents are increasing and output voltages are decreasing. Load current transients become exceedingly fast as the processor goes into and out of sleep modes of operation. Operating voltage is no longer a standard but must be programmable for variations from supplier to supplier, or even within a product line, such as with the Intel Pentium®Pro. Of course, simplicity must be maintained in order to keep parts count low and cost down.

The UC3886 Average Current Mode PWM Controller has been created to meet these requirements. The UC3886 is a full featured PWM controller which offers excellent performance, yet can be configured as a basic Buck regulator with a low external parts count. Excellent regulation accuracy can be realized through the high gain of Average Current Mode Control and by the very low offset voltage and current amplifiers used in the UC3886, which contribute negligible error to the output voltage. High efficiency is maintained by providing a direct drive to an efficient, low $R_{DS(ON)}$ N-MOSFET. A variable output voltage power supply can be controlled simply by supplying a command voltage to the UC3886 from a programmable reference, such as the UC3910 4-Bit DAC and Voltage Monitor IC.

The high gain of Average Current Mode control offers several advantages which help the designer to meet the regulation requirements of a widely varying load current as well as the extremely fast transient requirements. High current loop gain can be maintained at low operating currents with a regulator in continuous or discontinuous modes of operation. Average Current Mode control also allows optimal high bandwidth loop compensation which can maintain regulation during high current transients. The UC3886 obtains this current information from a low value resistor, and requires no transformers or slope compensation circuitry. The highly accurate current limiting of the UC3886 reduces the need to electrically and thermally overdesign the power components for short circuit fault considerations.

THE UC3886 AVERAGE CURRENT MODE PWM CONTROLLER IC

A block diagram of the UC3886 is shown in Figure 1.

The UC3886 Average Current Mode PWM Controller is ideally suited for a basic Buck regulator configuration, as shown in Figure 2, where a low processor voltage is generated from +5V typically. Appendix 1 provides a review of the operation of the typical Buck regulator shown in Figure 2.

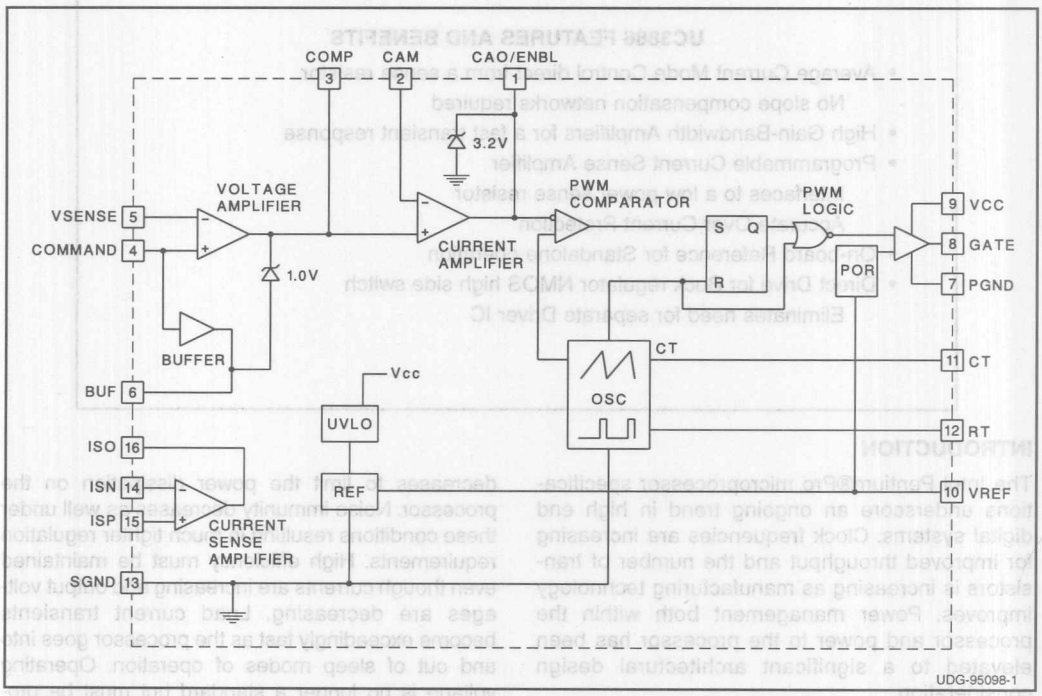


Figure 1. UC3886 Average Current Mode PWM Controller

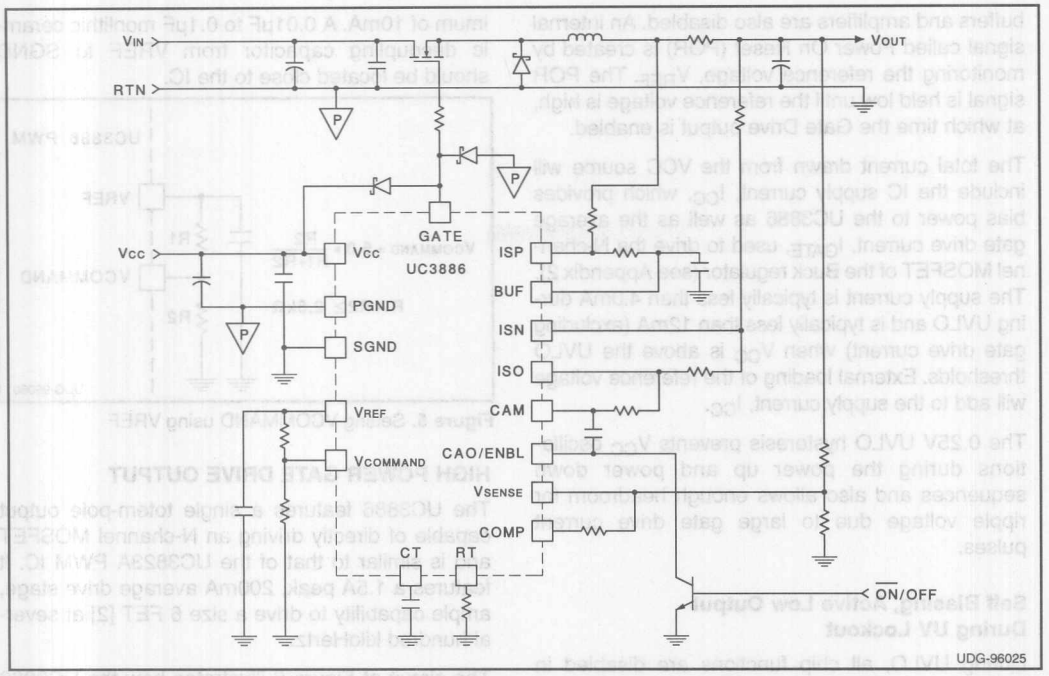


Figure 2. UC3886 Configured in a Typical Buck Regulator

UC3886 - SUPPLYING POWER

The UC3886 is constructed using a bipolar process allowing V_{CC} to be as high as 20V, however, the circuitry is optimized for a supply voltage of 12V. Minimum operating voltage is 10.3 volts. The supply voltage provides power directly to the reference voltage and the Gate Drive circuitry. It is also used to create an internal 7.3V bias voltage that supplies power to the Buffer, Voltage Amplifier, Current Amplifier, Current Sense Amplifier and the PWM comparator. The reference voltage is used to provide power directly to the PWM logic and to the Oscillator. Figure 3 shows the power distribution scheme within the UC3886.

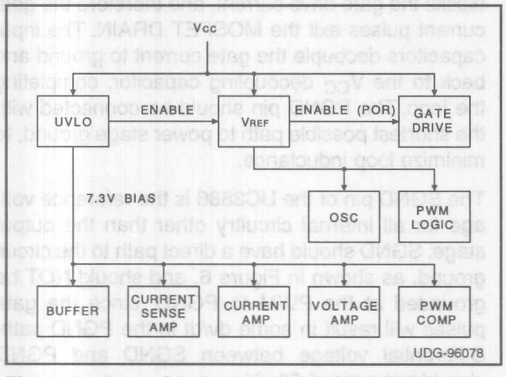


Figure 3. - Power Distribution within the UC3886

VCC should be decoupled to PGND closely to the IC with a low ESR capacitor to provide holdup during the gate pulses. Also add a 0.01µF to 0.1µF monolithic ceramic capacitor from VCC to SGND to provide high frequency signal decoupling.

UNDERVOLTAGE LOCKOUT

The UC3886 features an undervoltage lockout protection circuit for controlled operation during power up and power down sequences. Figure 4 shows typical V_{CC} thresholds of the UC3886 UVLO circuitry.

During UVLO, V_{REF} is kept off, which disables the oscillator, the PWM logic, and the Gate Drive. The

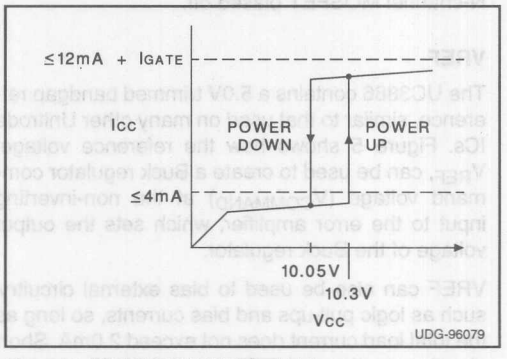


Figure 4. UC3886 UVLO Typical Values

buffers and amplifiers are also disabled. An internal signal called Power On Reset (POR) is created by monitoring the reference voltage, V_{REF}. The POR signal is held low until the reference voltage is high, at which time the Gate Drive output is enabled.

The total current drawn from the VCC source will include the IC supply current, I_{CC}, which provides bias power to the UC3886 as well as the average gate drive current, I_{GATE}, used to drive the N-channel MOSFET of the Buck regulator (see Appendix 2). The supply current is typically less than 4.0mA during UVLO and is typically less than 12mA (excluding gate drive current) when V_{CC} is above the UVLO thresholds. External loading of the reference voltage will add to the supply current, I_{CC}.

The 0.25V UVLO hysteresis prevents V_{CC} oscillations during the power up and power down sequences and also allows enough headroom for ripple voltage due to large gate drive current pulses.

Self Biasing, Active Low Output During UV Lockout

During UVLO, all chip functions are disabled in order to keep operating current at a minimum. The Gate Drive output, however, cannot be allowed to "float" high during this condition, because the Buck regulator N-channel MOSFET may inadvertently turn on.

An active low, self biasing totem-pole design is incorporated into the UC3886 Gate Drive output, which is very similar to that used in the UC3823A and is described in detail in U-128 [1]. The result of the self biased output is that during UVLO, the Gate Drive output is held low without drawing power from the supply voltage. No supply current is drawn because the self biasing output derives its power from the MOSFET gate voltage which is attempting to rise. This feature also negates the need for a gate-to-source resistor to keep the N-channel MOSFET biased off.

VREF

The UC3886 contains a 5.0V trimmed bandgap reference, similar to that used on many other Unitrode ICs. Figure 5 shows how the reference voltage, V_{REF}, can be used to create a Buck regulator command voltage ($V_{COMMAND}$) at the non-inverting input to the error amplifier, which sets the output voltage of the Buck regulator.

VREF can also be used to bias external circuitry, such as logic pull-ups and bias currents, so long as the total load current does not exceed 2.0mA. Short circuit protection on VREF protects the IC at a minimum of 10mA. A 0.01µF to 0.1µF monlithic ceramic decoupling capacitor from VREF to SGND should be located close to the IC.

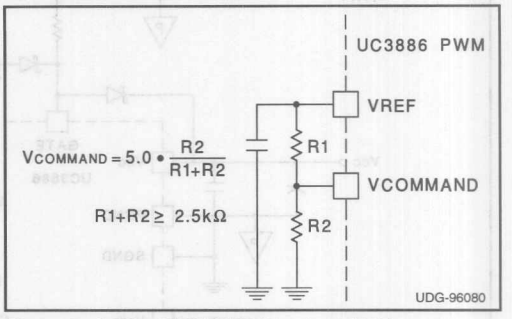


Figure 5. Setting VCOMMAND using VREF

HIGH POWER GATE DRIVE OUTPUT

The UC3886 features a single totem-pole output capable of directly driving an N-channel MOSFET and is similar to that of the UC3823A PWM IC. It features a 1.5A peak, 200mA average drive stage, ample capability to drive a size 6 FET [2] at several hundred kiloHertz.

The circuit of Figure 6 illustrates how the UC3886 Gate signal is used to drive a MOSFET for a low output voltage BUCK regulator.

Grounding with PGND and SGND

The PGND pin is a dedicated ground pin for the UC3886 output drive stage. The UC3886 Gate signal provides the high current gate pulses required during the MOSFET turn-on and turn-off times. These high current pulses should be decoupled by a low ESR capacitor placed closely to the IC as shown in Figure 6.

The current path for the gate pulses originates from the decoupling capacitor, passes through the totem-pole output of the UC3886 and enters the MOSFET gate. In a Buck regulator configuration, the inductor blocks the gate drive current, and therefore the gate current pulses exit the MOSFET DRAIN. The input capacitors decouple the gate current to ground and back to the V_{CC} decoupling capacitor, completing the loop. The PGND pin should be connected with the shortest possible path to power stage ground, to minimize loop inductance.

The SGND pin of the UC3886 is the reference voltage for all internal circuitry other than the output stage. SGND should have a direct path to the circuit ground, as shown in Figure 6, and should NOT be grounded at the PWM to PGND, since the gate pulses will result in some dv/dt in the PGND path. Differential voltage between SGND and PGND should not exceed 50mV.

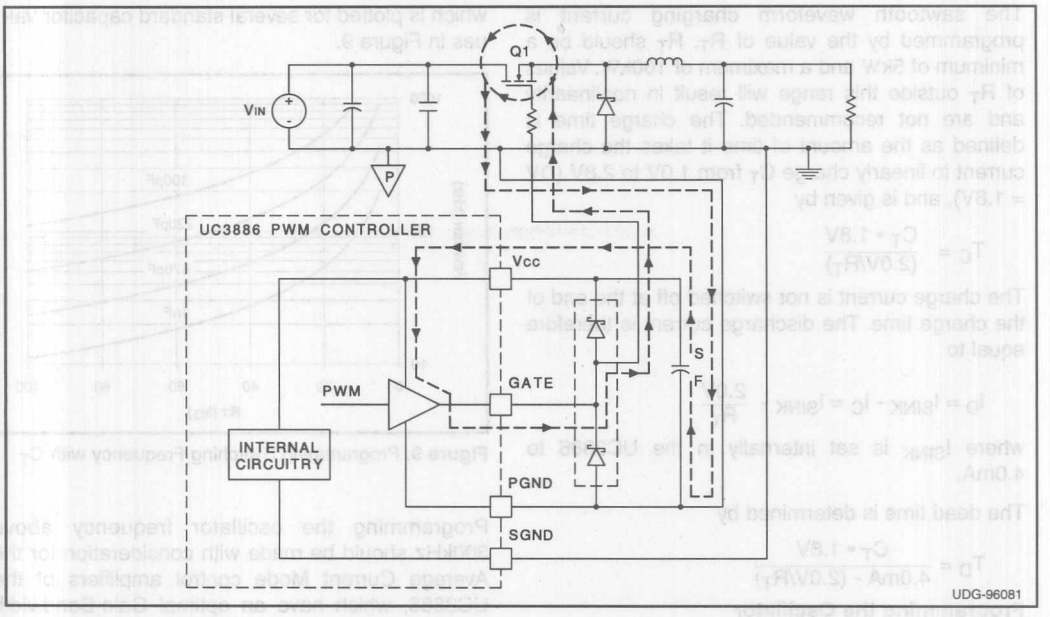


Figure 6. Driving a BUCK MOSFET with the UC3886

Schottky Clamping Diodes

The high di/dt characteristics of the gate drive pulse can cause undesirable ringing in the gate circuit, due to circuit trace inductance. A detailed explanation of why this occurs is available in Unitrode Application Note U-111 [2].

The use of low voltage schottky clamps, as shown in Figure 6, will protect the circuit from these effects. Use of 1N5821, 3A schottky diodes is recommended. The UC3612 is a dual schottky diode made specifically for this purpose and is available in an 8-pin DIP or SOIC package.

OSCILLATOR

The UC3886 oscillator is a sawtooth oscillator that is externally programmable (R_T, C_T) as shown in Figure 7. The oscillator switching period, T_S, consists of a charge time, T_C, and a discharge time or deadtime, T_D, such that

$$T_S = T_C + T_D \text{ [seconds]}$$

as shown in sawtooth waveform of Figure 7.

Oscillator equations presented below use the following units:

Resistance in ohms
Capacitance in farads
Currents in amperes
Time in seconds
Frequency in Hertz

The oscillator switching frequency, F_S, is given by

$$F_S = \frac{1}{T_S}$$

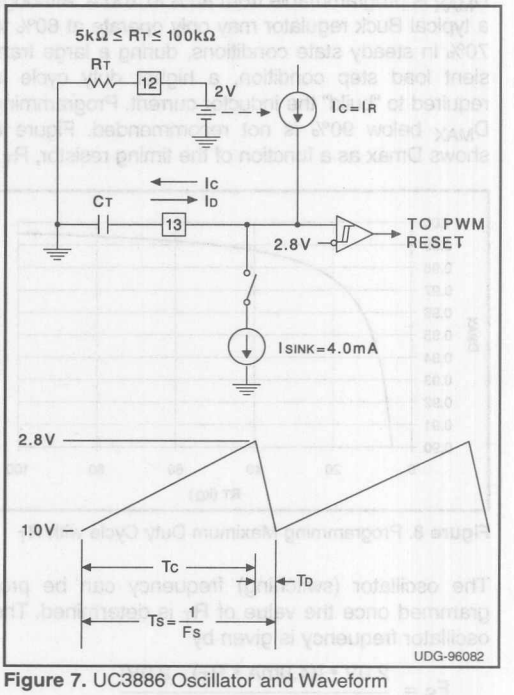


Figure 7. UC3886 Oscillator and Waveform

and are not recommended. The charge time is defined as the amount of time it takes the charge current to linearly charge C_T from 1.0V to 2.8V (DV = 1.8V), and is given by

$$T_C = \frac{C_T \bullet 1.8V}{(2.0V/R_T)}$$

The charge current is not switched off at the end of the charge time. The discharge current is therefore equal to

$$I_D = I_{SINK} - I_C = I_{SINK} - \frac{2.0V}{R_T}$$

where I_{SINK} is set internally in the UC3886 to 4.0mA.

The dead time is determined by

$$T_D = \frac{C_T \bullet 1.8V}{4.0mA - (2.0V/R_T)}$$

Programming the Oscillator

The first step in programming the oscillator is to choose a maximum operating duty cycle, D_{MAX}, given by

$$D_{MAX} = \frac{T_C}{T_C + T_D} = 1 - \frac{2.0V}{(R_T \bullet 4.0mA)}$$

D_{MAX} is programmable from 90% to 100%. Although a typical Buck regulator may only operate at 60% to 70% in steady state conditions, during a large transient load step condition, a higher duty cycle is required to "build" the inductor current. Programming D_{MAX} below 90% is not recommended. Figure 8 shows Dmax as a function of the timing resistor, R_T.

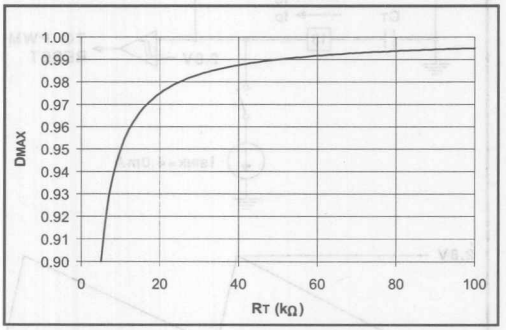


Figure 8. Programming Maximum Duty Cycle with R_T

The oscillator (switching) frequency can be programmed once the value of R_T is determined. The oscillator frequency is given by

$$F_S = \frac{2.0V \bullet [(4.0mA \bullet R_T) - 2.0V]}{C_T \bullet 1.8V \bullet R_T^2 \bullet 4.0mA}$$

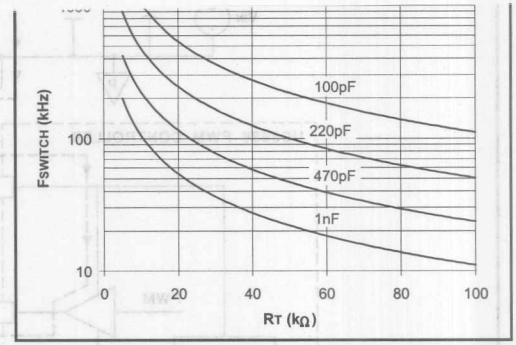


Figure 9. Programming Switching Frequency with C_T

Programming the oscillator frequency above 300kHz should be made with consideration for the Average Current Mode control amplifiers of the UC3886, which have an optimal Gain-Bandwidth product for operation below 300kHz.

The deadtime is plotted in Figure 10 as a function of R_T and C_T.

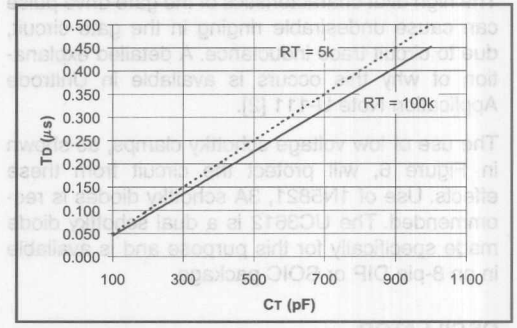


Figure 10. Deadtime vs C_T, R_T

Synchronizing the UC3886

Synchronizing the UC3886 can be achieved by superimposing a narrow voltage pulse on the PWM Ramp signal, as shown in Figure 11. The UC3886 oscillator should be programmed to freerun approximately 15% lower than that of the synchronizing frequency. A 1.0V amplitude pulse with a rise time of £ 10ns and a duration between 10ns and $T_D/2$ is recommended. Note that when synchronized, the dead time is the sum of the synchronizing pulse width and the oscillator discharge time. An excessively wide synchronizing pulse will result in less usable duty cycle, which may be required for large signal response. A very slow rising edge on the syn-

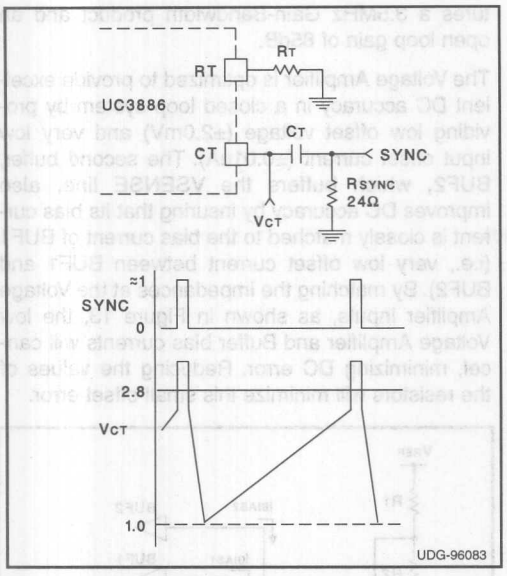


Figure 11. Synchronizing the UC3886

chronizing pulse should be avoided as well, as the PWM gain may be reduced.

Details of PWM oscillator operation, waveforms and synchronization is covered extensively in U-111 [2]. Synchronizing multiple UC3886 PWM controllers can be implemented using the UC3803 circuit as detailed in U-133A [3].

UC3886 - AVERAGE CURRENT MODE CIRCUIT BLOCK DESCRIPTION

The UC3886 Average Current Mode circuit blocks consist of the Voltage Amplifier, Buffer, Current Sense Amplifier, Current Amplifier and PWM Comparator. These blocks are shown in Figure 12 configured for Average Current Mode control in a Buck regulator.

The Dynamics of Average Current Mode Control with the UC3886

An understanding of the dynamics of Average Current Mode control as shown in Figure 12 is necessary to better understand the individual blocks which make up the system.

A simple but important fact must be understood up front; the ***load*** current of the Buck regulator is not the same as the ***inductor*** current of the Buck regulator. The ***load*** current is made up of the ***inductor*** current plus the current from the output capacitance. Average current mode control programs the ***inductor*** current. This is especially important when considering transient behavior and the dynamics involved.

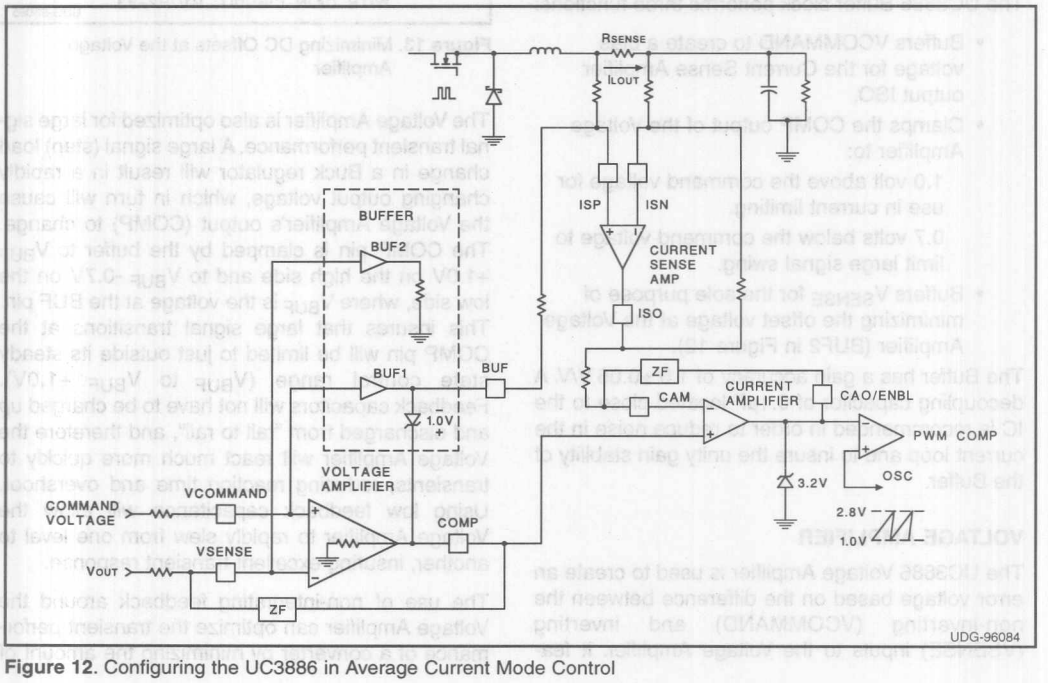


Figure 12. Configuring the UC3886 in Average Current Mode Control

The purpose of Average Current Mode Control is to program the Buck regulator (output inductor) to supply an average current to the load, such that the proper output voltage is maintained. The proper output voltage is programmed by the VCOMMAND pin on the UC3886.

A change in the load current of the Buck regulator will change the output voltage incrementally, which in turn will change the output of the Voltage Amplifier, COMP. Changing COMP will change the output of the Current Amplifier, CAO/ENBL, which is a direct input to the PWM comparator. Duty cycle will change as a result of CAO/ENBL changing. Note that at this point, the average inductor current has not changed yet, only the LOAD current. This means that until this point, the output capacitor has supplied the change in load current.

A duty cycle change will cause the average current to change through the inductor. The inductor current is converted to a voltage signal by the sense resistor, and is then amplified by the Current Sense Amplifier and is seen at the inverting input of the Current Amplifier, CAM. When the amplified current signal of the Current Amplifier's non-inverting input is equal to the COMP pin, the circuit settles into a steady state condition, where the average current into the load results in the proper output voltage.

BUFFER

The UC3886 Buffer block performs three functions:

- Buffers VCOMMAND to create a bias voltage for the Current Sense Amplifier output ISO.
- Clamps the COMP output of the Voltage Amplifier to:
  - 1.0 volt above the command voltage for use in current limiting.
  - 0.7 volts below the command voltage to limit large signal swing.
- Buffers V_{SENSE} for the sole purpose of minimizing the offset voltage at the Voltage Amplifier (BUF2 in Figure 12).

The Buffer has a gain accuracy of 1.0 ±0.05 V/V. A decoupling capacitor of 0.1µF located close to the IC is recommended in order to reduce noise in the current loop and to insure the unity gain stability of the Buffer.

VOLTAGE AMPLIFIER

The UC3886 Voltage Amplifier is used to create an error voltage based on the difference between the non-inverting (VCOMMAND) and inverting (VSENSE) inputs to the Voltage Amplifier. It features a 3.5MHz Gain-Bandwidth product and an open loop gain of 85dB.

The Voltage Amplifier is optimized to provide excellent DC accuracy in a closed loop system by providing low offset voltage (±2.0mV) and very low input offset current (±0.01uA). The second buffer, BUF2, which buffers the VSENSE line, also improves DC accuracy by insuring that its bias current is closely matched to the bias current of BUF1 (i.e., very low offset current between BUF1 and BUF2). By matching the impedances at the Voltage Amplifier inputs, as shown in Figure 13, the low Voltage Amplifier and Buffer bias currents will cancel, minimizing DC error. Reducing the values of the resistors will minimize this small offset error.

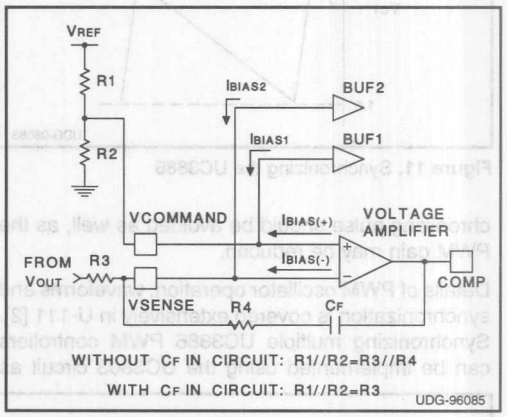


Figure 13. Minimizing DC Offsets at the Voltage Amplifier

The Voltage Amplifier is also optimized for large signal transient performance. A large signal (step) load change in a Buck regulator will result in a rapidly changing output voltage, which in turn will cause the Voltage Amplifier's output (COMP) to change. The COMP pin is clamped by the buffer to V_{BUF} +1.0V on the high side and to V_{BUF} -0.7V on the low side, where V_{BUF} is the voltage at the BUF pin. This insures that large signal transitions at the COMP pin will be limited to just outside its steady state control range (V_{BUF} to V_{BUF} +1.0V). Feedback capacitors will not have to be charged up and discharged from "rail to rail", and therefore the Voltage Amplifier will react much more quickly to transients, reducing reaction time and overshoot. Using low feedback capacitance will allow the Voltage Amplifier to rapidly slew from one level to another, insuring excellent transient response.

The use of non-integrating feedback around the Voltage Amplifier can optimize the transient performance of a converter by minimizing the amount of

capacitance on the COMP pin, and by intentionally limiting DC voltage regulation. Non-integrating compensation is discussed in Appendix 3.

CURRENT SENSE AMPLIFIER

The UC3886 Current Sense Amplifier is used to amplify a differential current sense signal across a low value current sense resistor, R_{SENSE}. It features a 2.5MHz Gain-Bandwidth product and an open loop gain of 85dB. This amplifier must be set up as a differential amplifier as shown in Figure 14. A differential amplifier configuration will amplify only the difference voltage across the sense resistor, R_{SENSE}, and will not amplify or carry common-mode information.

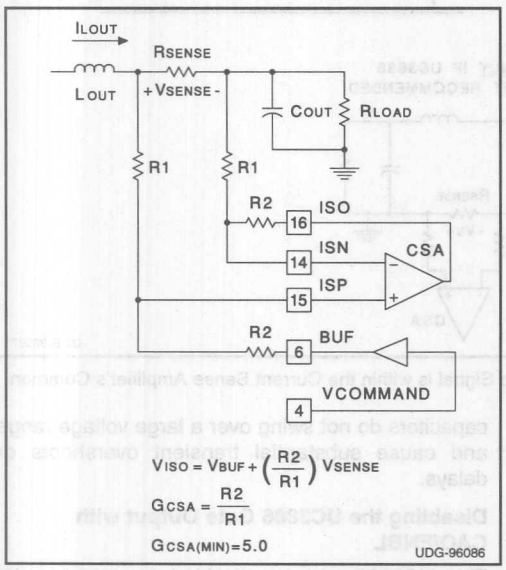


Figure 14 . Configuring the Current Sense Amplifier of the UC3886

The Current Sense Amplifier gain must be programmed (by external resistors) to be greater than or equal to 5.0 (14dB), as this amplifier ***is not stable*** with gain below 5.0. The Current Sense Amplifier gain is limited on the high side by its Gain-Bandwidth product of 2.5MHz. Therefore, the gain of the Current Sense Amplifier, G_{CSA}, must be programmed between

$$G_{CSA_MIN} = 5.0 \text{ and } G_{CSA_MAX} = 2.5MHz/F_{SWITCH}$$

where F_{SWITCH} is the oscillator switching frequency.

Equations governing a Differential Amplifier are contained in Appendix 4.

R_{SENSE}, the current sense resistor, is used to measure the output inductor current, which is necessary for the proper operation of Average Current Mode Control. The Current Sense Amplifier features a common mode input range from 0.0 to 4.5Vdc. This allows the current sense resistor to be placed directly in series after the output inductor in low output voltage converters.

R_{SENSE} should not be placed before the output inductor because the current sense signal will be outside the common mode range of the Current Sense Amplifier. Likewise, R_{SENSE} should not be placed in the return path unless a ground difference can exist between the UC3886 and the load, which may be detrimental to voltage regulation. Figure 15 illustrates these points.

CURRENT AMPLIFIER AND PWM COMPARATOR

The Current Amplifier is used to create a current error voltage based on the difference between the amplified inductor current and the Voltage Amplifier output, COMP. It features a 3.5MHz Gain-Bandwidth product and an open loop gain of 85dB. Using an integrating feedback compensating network around the Current Amplifier presents two advantages of Average Current Mode control over Peak Current Mode Control [4]. Higher DC gain is the first advantage. The second is the ability to compensate the loop, whereas Peak Current Mode Control has a fixed gain.

The output of the Current Amplifier, CAO/ENBL, is compared to the PWM ramp with the result being a duty cycle varying as a function of the inductor current and the commanded voltage. Ideal PWM comparator waveforms are shown in Figure 16. By observing the waveforms of Figure 16, the noise immunity advantage of Average Current Mode control over Peak Current Mode control can be seen. At the beginning of each switching cycle, the Ramp signal is at its lowest point, and therefore the PWM comparator is less susceptible to turn on spikes. Also, since an Average Current Mode control system samples the Inductor current, and not the switch current, there are no parasitic turn on spikes to compensate for or filter.

The Current Amplifier output, CAO/ENBL, is compared to the ramp waveform generated at the timing capacitor, C_T, at the high speed PWM Comparator. The ramp waveform is a fixed frequency ramp ranging from 1.0V to 2.8V. Figure 16 shows that the output of the Current Amplifier is clamped to approximately 3.2V, which is above the steady state range of the PWM comparator (2.8V). Large signal transient conditions may cause the Current Amplifier output to swing high and clamp to this upper limit. Clamping the Current Amplifier output allows a fast transient response, as the feedback

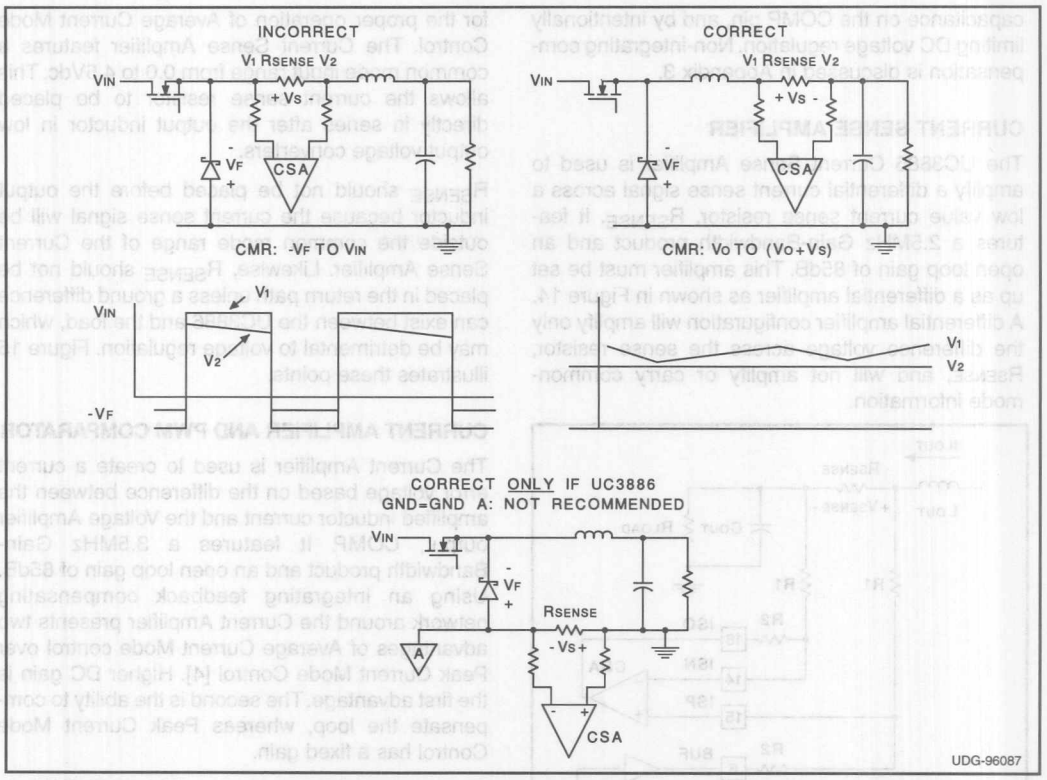


Figure 15. Sense Current AFTER the Inductor to Insure the Signal is within the Current Sense Amplifier's Common Mode Range

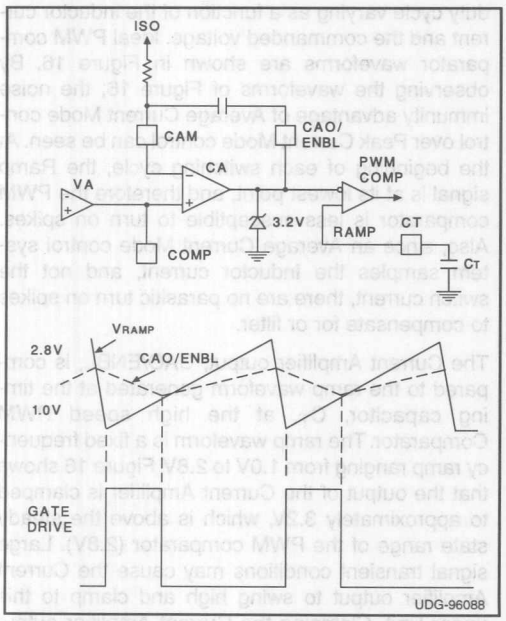


Figure 16. The Current Amplifier Output is compared to the PWM Ramp Signal

capacitors do not swing over a large voltage range and cause substantial transient overshoots or delays.

Disabling the UC3886 Gate Output with CAO/ENBL

The UC3886 can be disabled by bringing the CAO/ENBL pin below 0.8V, as shown in Figure 17. The CAO/ENBL pin is one input to the PWM comparator, and the oscillator ramp waveform is the other. Bringing the CAO/ENBL pin below 0.8V will force the Gate Drive duty cycle to 0%.

The CAO/ENBL is the output of the Current Amplifier and will be compensated for loop control. The signal to the CAO/ENBL pin must therefore be a true open collector so that during the HIGH (open) state, there is no effect on the amplifier's performance. The open collector signal must be capable of sinking ³ 250µA and remain below 0.8V. Figure 17 shows R1 which is recommended if the enable signal is located at a significant distance from the power supply. A long circuit board signal run can couple noise into the current loop if it resides close to noisy signals. R1 acts as a high impedance block to noise signals. R1 should be

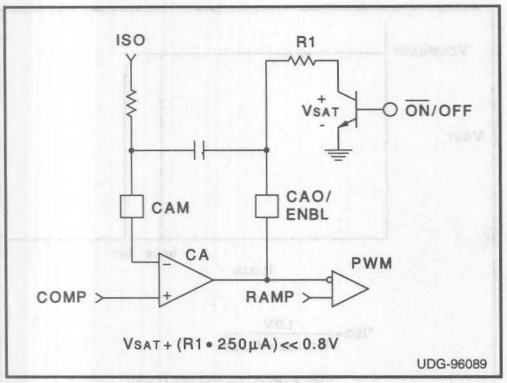


Figure 17. Disabling the UC3886

small enough however to insure that the disabling signal at CAO/ENBL is less than 0.8V. A 1kW resistor is recommended.

No features of the UC3886 are powered down during the disabled output state other than the Gate Drive output.

CLOSING THE LOOP WITH AVERAGE CURRENT MODE CONTROL

The fundamental principles of Average Current Mode Control are presented in Unitrode Application Note U-140 [4]. Compensating both the current loop and voltage loop is further detailed in Unitrode Seminar Topic "Switching Power Supply Control Loop Design" [5].

Figure 18 is a modification of the models presented in the two referenced application notes where the addition of the Current Sense Amplifier is the fundamental change.

Closing the Loop in a Variable Output Power Supply

The above mentioned references on closing the loop using Average Current Mode control show a critical limitation on the inductor current slope during the switch OFF time. A variable output power supply must consider the maximum operating output voltage, where the inductor current OFF time slope is maximized. The result will be less than optimal gain at the lower operating voltages.

CURRENT LIMITING WITH THE UC3886

The output of the Current Sense Amplifier, ISO, is determined by the differential gain equation (see Appendix 4) and is biased by the voltage at the BUF pin, V_{BUF}, as shown in Figure 14, such that

$$ISO = V_{BUF} + V_{SENSE} \bullet G_{CSA} \text{ [Volts]}$$

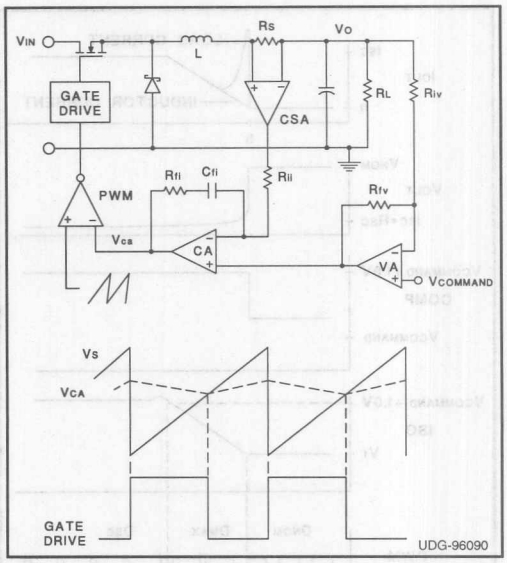


Figure 18. Average Current Mode Control Circuit and Waveforms for the UC3886 ACM Controller

where

$$V_{SENSE} = I_{LOUT} \bullet R_{SENSE} \text{ and}$$

$$G_{CSA} = \frac{R2}{R1} \text{ as shown in Figure 14.}$$

An increase in load current will force the power supply output voltage to decrease as the output capacitor discharges. This will force the Voltage Amplifier output (COMP) upward, the Current Amplifier output (CAO/ENBL) higher, will increase the duty cycle and thus will increase the inductor current.

COMP is clamped to V_{BUF} + 1.0V by the buffer. As the average output inductor current continues to rise, to raise the output voltage, the output of the Current Sense Amplifier, ISO, exceeds the value of COMP. This occurs when

$$I_{SC} \bullet R_{SENSE} \bullet G_{CSA} = 1.0 \text{ Volt}$$

or at a short circuit current limit, I_{SC}, of

$$I_{SC} = \frac{1.0 \text{ Volt}}{R_{SENSE} \bullet G_{CSA}} \text{ [Amperes]}$$

When ISO exceeds the value of COMP, the Current Amplifier, configured for high DC gain, swings to its minimum value, resulting in a lower short circuit duty cycle, D_{SC}. D_{SC} is high enough only to maintain the average current through the inductor.

Figure 19 graphically represents the dynamics of a short circuit placed across the output of the Buck regulator of Figure 12 at time t_1.

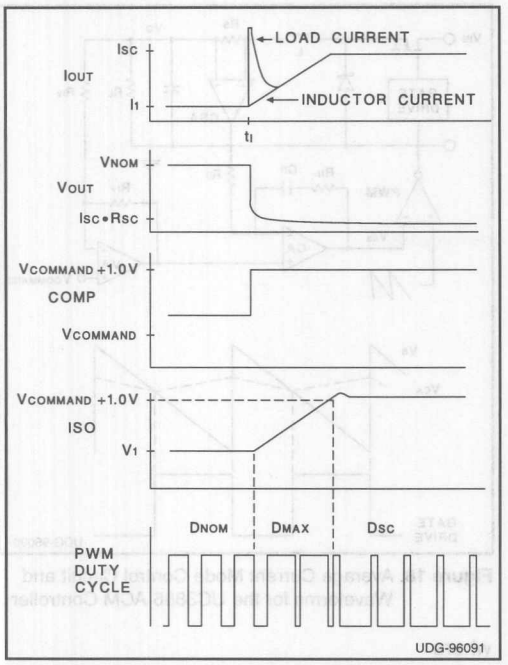


Figure 19. Dynamics of Short Circuit Protection with the UC3886

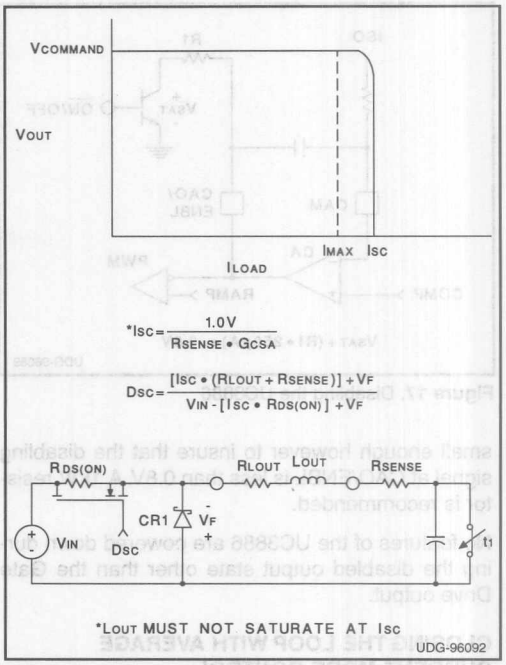


Figure 20. UC3886 Current Limit Load Line in a Buck Regulator

Current Limit Load Line

Current limiting in the UC3886 follows a "square knee" load line, where current is not disabled or folded back. Figure 20 shows this load line.

The voltage at the output of the Buck regulator of Figure 20 falls proportionally to the value of the short circuit, usually measured in milliohms. Many regulators, under a short circuit of extremely low resistance, will demonstrate a condition where Ipeak can be much larger than I_{SC}, often referred to as "tail-out". Safety and reliability issues may arise should the value of Ipeak not be well understood and controlled.

The simplified Buck regulator shown in Figure 20 shows several key parasitic elements, along with the value of R_{SENSE}, which limit the current to I_{SC}, preventing tail-out. See Appendix 5 for a detailed example of programming the current limit using the UC3886 ACM Controller.

AVERAGE CURRENT MODE CONTROL IN DISCONTINUOUS MODE

Average current mode control offers the advantage of being able to function while the regulator is running in a discontinuous mode of operation where the output inductor, and therefore the current signal, runs dry.

With peak current mode control, during discontinuous mode, the peak/average current error becomes unacceptably large, a result of the fixed and limited gain in peak current mode control. The high gain of the Current Amplifier used in Average Current Mode control allows the large changes in duty cycle required for load changes. The Average Current Mode gain, however, is limited.

There is a slope limitation criteria of Average Current Mode control (U-140 [4]) which is: *The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input.* This slope criteria directly limits the amount of gain obtainable in the Current Amplifier at the switching frequency.

The criteria mentioned above can be equated as

$$\frac{V_O + V_F}{L_{OUT}} \bullet R_S \bullet G_{CSA} \bullet G_{CA} \leq \frac{V_S}{T_S - T_D}$$

where, in the model of Figure 18

V_S = Oscillator Ramp [V]

T_S = Switching Period [s]

T_D = Oscillator Deadtime [s]

V_O = Output Voltage [V]

V_F = Freewheeling Diode Forward Voltage [V]

L_{OUT} = Output inductor [H]

R_S = Sense Resistor [W]

G_{CSA} = Gain of the Current Sense Amplifier

G_{CA} = Gain of the Current Amplifier at the switching Frequency.

It can be shown from the above equation that the Current Amplifier gain is directly proportional to the Inductor value, and is constant at a given output voltage.

$$\frac{G_{CA}}{L_{OUT}} = \frac{V_S}{T_S - T_D} \bullet \frac{1}{R_S \bullet G_{CSA}} \bullet \frac{1}{V_O + V_F} = K$$

Decreasing L_{OUT} must result in a decrease in G_{CA}, and therefore the Average Current Mode gain. This lower current gain will adversely effect large signal response of the circuit, although a smaller inductor value will improve large signal response. Even with this limitation on the gain G_{CA}, Average Current Mode Control can achieve much higher gains than Peak Current Mode control.

STARTUP AND SOFT STARTING WITH THE UC3886

Soft starting a power supply is defined as bringing the output voltage up to its specified value in a slow, controlled manner. Typical power supplies soft start in 10ms to 100ms.

The need for soft starting a power supply is often associated with overshoot. The output voltage of a power supply will often ring over its specified value when the power supply is "snapped" on, as the control loop often lags the rise of the output voltage. The overshoot can be destructive if it is not clamped or controlled. Slowly ramping up the output voltage will minimize the overshoot.

The fast transient response of the UC3886 Average Current Mode controller helps eliminate the need for soft starting the DC/DC converter. At startup, the Average Current Mode control directly controls the inductor current. As long as the output voltage is less than the required voltage, the current loop forces the UC3886 to supply current limited to I_{SC}, the short circuit limit. Once the proper output voltage is reached, the very fast transient response of the UC3886 Voltage and Current Amplifiers will cut back on the duty cycle, thus eliminating the voltage overshoot associated with a slow loop response. A large output capacitance on the DC/DC converter will insure that a slight overshoot in inductor current results in negligible overshoot in the output voltage.

A soft start capacitor can be added to the VCOMMAND pin as shown in the circuit of Figure 21, should a slow, controlled start up be required. The values or resistors R1 and R2 should be chosen to (a) create the proper voltage at VCOMMAND, (b) draw less than 2.0mA from VREF and (c) equal the impedance seen by the inverting input of the UC3886 Voltage Amplifier, V_{SENSE}, to cancel bias current effects. Once the resistors are chosen, then C_{SS} should be chosen for the proper time constant.

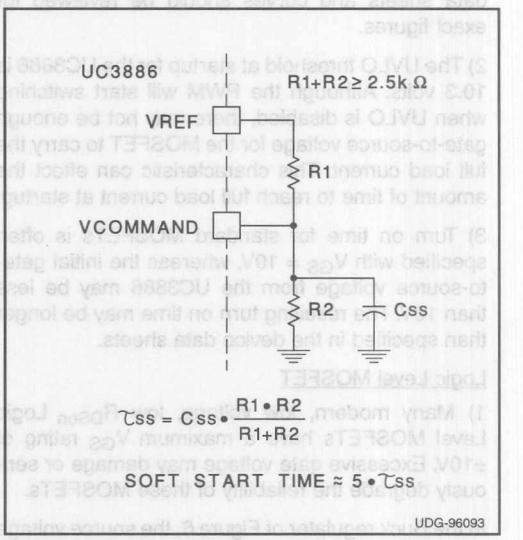


Figure 21. Soft Starting the UC3886

DRIVING A HIGH SIDE N-CHANNEL MOSFET WITH THE UC3886

The UC3886 is designed to drive an N-Channel MOSFET in a Buck configuration, as shown in Figure 6. There are circuit and MOSFET factors to be considered in order to properly drive the MOSFET. The circuit factors include the values of V_{IN}, V_{CC}, UVLO, the UC3886 totem-pole gate voltage and ringing voltages on the Gate and Source nodes. The MOSFET factors include V_{GSmin}, V_{GSmax}, R_{DSon} vs V_{GS}, and the type of MOSFET used, standard or Logic Level. A MOSFET's on and off characteristics are controlled by the gate-to-source voltage, V_{GS}.

There are many sources of literature [6, 7, 8, 9] which discuss MOSFET drive circuits and parameters. This application note will highlight several considerations in using the UC3886 GATE output in dri-

ving standard and Logic Level MOSFETs in a Buck regulator.

Standard MOSFET

1) Given a 5 volt input and a 12 volt V_{CC} source to the UC3886 (Figure 6), V_{GS} is only 7 volts nominally. R_{DSon} for standard MOSFETs is often specified with V_{GS} = 10V. A survey of several 60 volt low R_{DSon} MOSFETs shows that R_{DSon} is higher by a factor of approximately 1.35 when these MOSFETs are driven with only 7 volts V_{GS}. Specific data sheets and curves should be reviewed for exact figures.

2) The UVLO threshold at startup for the UC3886 is 10.3 volts. Although the PWM will start switching when UVLO is disabled, there may not be enough gate-to-source voltage for the MOSFET to carry the full load current. This characteristic can effect the amount of time to reach full load current at startup.

3) Turn on time for standard MOSFETs is often specified with V_{GS} = 10V, whereas the initial gate-to-source voltage from the UC3886 may be less than 10V. The resulting turn on time may be longer than specified in the device data sheets.

Logic Level MOSFET

1) Many modern, low voltage, low R_{DSon} Logic Level MOSFETs have a maximum V_{GS} rating of ±10V. Excessive gate voltage may damage or seriously degrade the reliability of these MOSFETs.

In the Buck regulator of Figure 6, the source voltage is rising from $-V_F$ to $+V_{IN}$ during turn on. At the beginning of the cycle, the gate-to-source voltage, V_{GS}, is equal to $V_{GATE}+V_F$, which may be well in excess of 10V. At the end of the cycle, V_{GS} is less, as the source voltage has risen to approximately the input voltage. The gate-to-source voltage dynamic characteristics are dependent on the value of series gate resistance, R_{GATE}, as well as circuit load characteristics. R_{GATE} can be increased to insure that during the turn-on pulse, the source voltage has risen to the input voltage well in advance of V_{GS} reaching its maximum value. The cost of this approach may be in switching power losses.

A gate-to-source zener diode can be used as shown in Figure 22 to insure that excessive V_{GS} is not reached.

Low R_{DSon} - Low Voltage MOSFETs

Several MOSFET processes have increased the density of MOSFET cells in order to optimize R_{DSon} and current handling capabilities. One result of this is the reduction of a good Gate metal path to individual cells. The result of this is higher internal gate resistance and inductance, which effects the switching performance of the MOSFET.

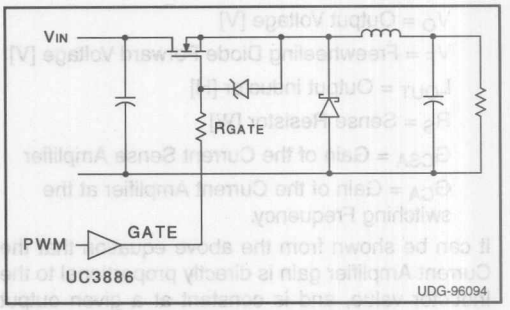


Figure 22. Clamping V_{GS} with a Zener Diode

A noticeable effect of these parasitics is the difference between the Turn-On delay and the Turn-Off delay. At turn-on, as soon as a small number of cells are turned on, drain current begins to conduct. At turn-off however, the gate charge must be removed from all MOSFET cells, resulting in a substantial delay in turning off the drain current, as illustrated in Figure 23. MOSFET Turn-on and Turn-off delays will vary based on supplier processes. Supplier data sheets should be consulted.

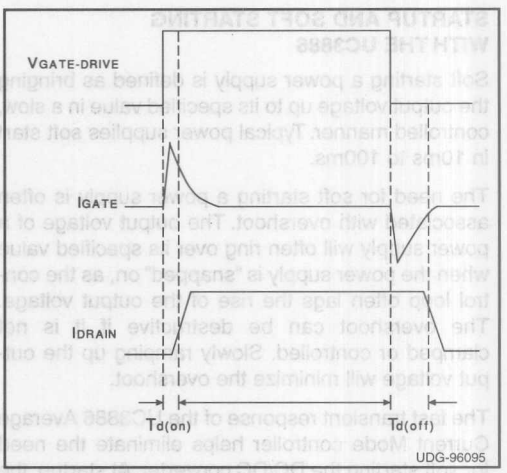


Figure 23. MOSFET Turn-On and Turn-Off Delays

USING THE UC3886 WITH THE UC3910 FOR A COMPLETE Pentium®Pro SOLUTION

The UC3886/UC3910 Chip Pair is shown in Figure 24 as configured in a typical Buck regulator. The programmable DAC output of the UC3910 is simply fed into the VCOMMAND pin of the UC3886 to provide a programmable PWM controlled power supply.

Using this chip pair offers significant benefits when providing power to today's microprocessors. The two IC's can be configured, as shown in Figure 24, to provide all functions required to interface with,

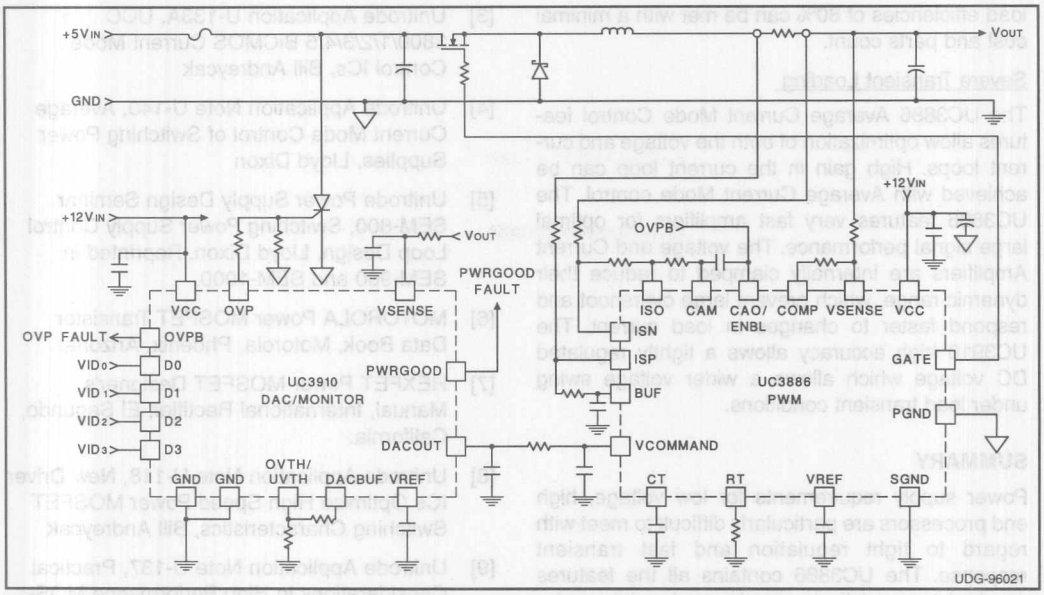


Figure 24. UC3886/UC3910 Interconnection Diagram

control, and monitor the performance of the Intel Pentium®Pro and other high end processors. Together, the chip pair meets the critical requirements of the Pentium®Pro with a simple, accurate and efficient switching regulator which meets the difficult transient regulation requirements with Average Current Mode Control.

For additional information on the UC3910 4-BIT DAC and Voltage Monitor IC, refer to application note U-158 [10]. For additional information on a detailed circuit design and performance of the UC3886/UC3910 chip pair, refer to application note U-157 [11].

Features of the UC3886/UC3910 Chip Pair

Simplicity

The UC3886/UC3910 is configured to drive a basic Buck regulator. The ICs integrate all control and monitoring functions, so that external parts count is reduced. Circuit boards can use fewer layers, fewer interconnects and fewer components.

The UC3886 features a direct output NMOS drive, eliminating the need for creating high voltages and allowing the use of an efficient N-Channel MOSFET.

The programmable voltage feature of the UC3910 allows system designers to directly interface with Intel's Pentium®Pro to create one power supply that will meet all voltage requirements, and thus reducing all the logistics associated with single output power supplies.

The UC3910's DAC and unique voltage monitoring architecture directly replaces discrete components including a precision reference, a DAC, complicated resistive networks, multiple window comparators and an SCR Driver. The UC3910's tracking fault windows are simply programmable with two external resistors.

The UC3886 can directly monitor the inductor current through a low value resistor, eliminating the need for a current transformer or complicated waveform synthesis circuitry.

The accuracy and true "square-knee" characteristic of the UC3886 over current limit programming eliminates the need to over-design the power components for operation in an indefinite short circuit.

Accuracy

The typical ±0.5% accuracy of the UC3910 is not corrupted by the UC3886, as the UC3886 uses a very low offset Voltage Amplifier, has very low bias currents, and offsets the bias currents within the IC. The combined system accuracy is ±1%. This high DC accuracy negates the need for trimming the power supply output voltage in manufacturing.

Efficiency

The high current drive of the UC3886 allows the use a high end low R_{DSon} N-channel MOSFET. Full

load efficiencies of 80% can be met with a minimal cost and parts count.

Severe Transient Loading

The UC3886 Average Current Mode Control features allow optimization of both the voltage and current loops. High gain in the current loop can be achieved with Average Current Mode control. The UC3886 features very fast amplifiers for optimal large signal performance. The voltage and Current Amplifiers are internally clamped to reduce their dynamic range, which prevent large overshoot and respond faster to changes in load current. The UC3910 high accuracy allows a tightly regulated DC voltage which allows a wider voltage swing under load transient conditions.

SUMMARY

Power supply requirements for low voltage, high end processors are particularly difficult to meet with regard to tight regulation and fast transient response. The UC3886 contains all the features required to meet these requirements while maintaining high efficiency and a low external parts count. Average current mode control offers excellent regulation and fast transient response, accurate current limiting reduces electrical and thermal overdesign, and high side N-MOSFET drive helps create a simple and high efficiency power circuit.

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[10] Unitrode Application Note U-158, The UC3910 Combines Programmability, Accuracy and Integrated Functions to Control and Monitor High End Processor Power Supplies, Larry Spaziani

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APPENDIX 1: BUCK REGULATOR BASICS

A schematic of a basic Buck regulator power stage is shown in Figure 1A . Several parasitic elements are included for the reasons described below.

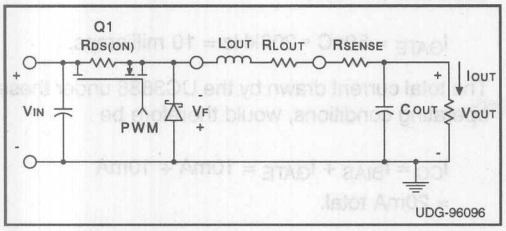


Figure 1A - Buck Regulator Power Stage

The transfer function of a Buck regulator is often simplified as

$$V_{OUT} = V_{IN} - D \qquad \text{Simple Approximation}$$

where D is the duty cycle of the Pulse Width Modulator (PWM).

Parasitic elements such as series resistance and even the diode drop, V_F, are often assumed to be negligible, especially when the output voltage is large compared to these voltage drops, and current is low.

For a low voltage, high current Buck regulator, a more exact transfer function is necessary to insure proper operation.

The basic operation of a Buck regulator with PWM control is this: a PWM controlled rectangular waveform is created by the switch, Q1, and is averaged by the output LC power stage. The inductor must balance volt-seconds during both the ON time and the OFF time in order for this averaging function to occur. Volt-seconds is defined as the product of the voltage across the inductor and the time which that voltage is present.

The equation for the volt-second product across the inductor during the ON and OFF times are given by:

$$VOLT_SEC_ON = (V_{IN} - I_{OUT} \bullet (R_{DSON} + R_{LOUT} + R_{SENSE}) - V_{OUT}) \bullet T_{ON}$$

$$VOLT_SEC_OFF = (V_{OUT} + I_{OUT} \bullet (R_{LOUT} + R_{SENSE}) + V_F) \bullet T_{OFF}$$

Equating the volt seconds gives

$$(V_{IN} - I_{OUT} \bullet (R_{DSON} + R_{LOUT} + R_{SENSE}) - V_{OUT}) \bullet T_{ON} = (V_{OUT} + I_{OUT} \bullet (RL_{OUT} + R_{SENSE}) + V_F) \bullet T_{OFF}$$

Duty cycle D is defined as T_{ON}/T, where T is the switching period. Therefore, T_{OFF}/T can be defined as 1-D, resulting in

$$\frac{T_{ON}}{T_{OFF}} = \frac{D \bullet T}{(1\text{-}D) \bullet T} =$$

$$\frac{V_{OUT} + [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] + V_F}{V_{IN} - [I_{OUT} \bullet (R_{DSON} + R_{LOUT} + R_{SENSE})] - V_{OUT}}$$

giving the governing equation for the output voltage

$$V_{OUT} = (D \bullet V_{IN}) - (D \bullet I_{OUT} \bullet R_{DSON}) - [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] - [V_F \bullet (1 - D)]$$

and the governing equation for duty cycle

$$D = \frac{V_{OUT} + [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] + V_F}{V_{IN} - (I_{OUT} \bullet R_{DSON}) + V_F}$$

Duty Cycle for Buck Regulator

Example:

V_{IN} = 5.0V

V_{OUT} = 3.1V

R_{LOUT} = 0.010W

R_{SENSE} = 0.010W

R_{DSON} = 0.025W

I_{OUT} = 1A min to 10A max

V_F = 0.4V @ 1A, 0.5V @ 10A

Estimate Duty cycle based on the simple duty cycle approximation:

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{3.1V}{5.0V} = 62\%$$

Calculate Duty cycle based on the complete equation:

$$D = \frac{3.1V + [10A \bullet (0.01W + 0.01W)] + 0.5V}{}$$

$$= 72.4\%@10A$$

$$D = \frac{3.1V + [1A \bullet (0.01W + 0.01W)] + 0.4V}{5.0V - (110A \bullet 0.025W) + 0.4V}$$

$$= 65.5\%@1A$$

The results show that simplifying the transfer function can result in a substantial error when low voltages and high currents are considered.

APPENDIX 2: CALCULATING AVERAGE GATE DRIVE CURRENT, I_{GATE}

A MOSFET gate requires a total gate charge, Q_G, which is specified in the manufacturer's data sheet, in order to effectively turn on. Understanding gate drive requirements and dynamics is discussed in detail in U-118 [8] and in U-137 [9]. The MOSFET gate is charged up at turn-on by a peak current waveform, often limited by the driver output impedance as well as series resistance. Over many cycles, the peaks of current can be averaged. This average current must be supplied to the UC3886 from the V_{CC} source.

Figure 2A shows an N-channel MOSFET in a Buck regulator configuration. The input voltage is 5V, and the gate driver is powered from 12V. The effective Gate-to-Source voltage is therefore 7V.

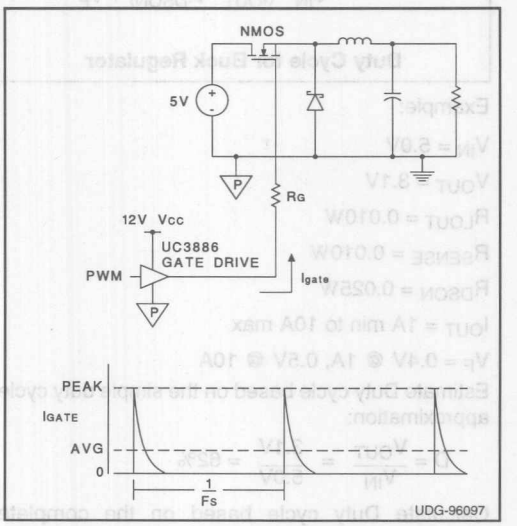


Figure 2A. Calculating Average Gate Current

Figure 2B is a generic example of a manufacturer's "Gate-Source Voltage vs Gate Charge" curve, found in most MOSFET data sheets. The charge required is a direct function of the Gate-to-Source voltage which drives the MOSFET. Using this curve, the required gate charge for the circuit in Figure 2A can be read off of the curve.

Gate charge and current are related by

$$Q_G = I_{GATE} \bullet T_S$$

where I_{GATE} is the AVERAGE gate current and T_S is $1/F_S$ or one switching period.

Average gate current, I_{GATE}, can therefore be calculated by using

$$I_{GATE} = Q_G / T_S = Q_G \bullet F_S.$$

As an example, an IRFZ48 MOSFET requires approximately 50 nanocoulombs total gate charge (Q_G) with 7 volts V_{GS} drive. The average current drawn by the gate at an operating frequency of 200kHz is therefore

$$I_{GATE} = 50nC \bullet 200kHz = 10 \text{ milliamps.}$$

The total current drawn by the UC3886 under these operating conditions, would therefore be

$$I_{CC} = I_{BIAS} + I_{GATE} = 10mA + 10mA$$
$$= 20mA \text{ total.}$$

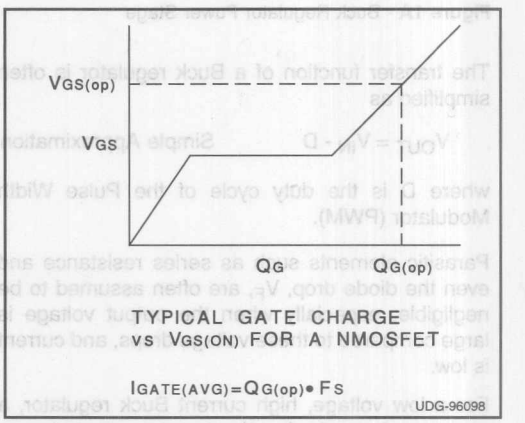


Figure 2B. Using Total Gate Charge to Calculate Gate Current

APPENDIX 3: MANAGING REGULATION AT THE LOAD WITH NON-INTEGRATING GAIN

A model of an Average Current Mode controlled Buck regulator is shown in Figure 3A. The Average Current Mode control loop can be modeled as a simple transconductance amplifier, which converts the Voltage Amplifier's error voltage into the required average output current.

The parasitic resistive and inductive elements shown in the circuit will have the following effects:

- The resistive elements will cause a steady state load regulation error proportional to resistance and load current
- The resistive elements will cause a transient voltage drop proportional to resistance and amplitude of the change in load current
- The inductive elements will cause a transient voltage drop proportional to inductance and the rate of change, di/dt.

Sensitive loads, such as high end Processor ICs, require regulation at the load to be extremely tight under load variations. Load regulation specifica-

tions can consist of a window of voltage regulation which includes variations of steady state load current, load transient conditions, voltage ripple and DC regulation tolerances.

The allowed transient voltage deviation, when considering low voltage processors with very fast transients rates, can be extremely difficult to meet, and may require an excessive amount of output capacitance in order to keep the total capacitor's ESR and ESL low enough to meet the regulation requirements. Excess capacitance is bulky and expensive.

Managing the regulation at the load can be summarized by the following goals and methods to meet the goals.

Goals

1. Meet ±5% regulation at the load under all operating conditions
2. Minimize the amount of output capacitance required at the power supply output in order to minimize cost and size

Methods

1. Use parallel, low impedance pins at the power supply connector.
2. Use power and ground planes from the power supply to the load.
3. Maximize local decoupling at the load.
4. Minimize ripple to maximize use of the regulation window.
5. Compensate for the I • R voltage drop to the load with positive DC offset at the power supply output.
6. Maximize allowable transient voltage swing by providing positive DC offset at the power supply output when operating at the minimum load, and providing negative DC offset at the power supply output when operating at the maximum load. This can be accomplished by using Non integrating gain (resistive, not capacitive feed back) about the Voltage Amplifier.

Methods 1 through 4 consist of good electronic layout and filtering practices. Methods 5 and 6 are steps which can be taken at the power supply, and are discussed below.

Figure 3B illustrates the output voltage effects resulting from load transients when integrating and non-integrating feedback is utilized as well as the effects of a DC offset voltage.

Integrating gain utilizes a DC blocking capacitor in the feedback, and therefore results in a very high

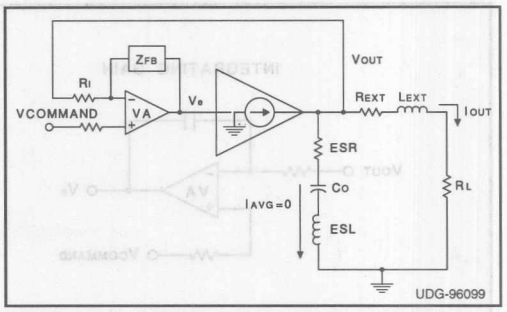


Figure 3A. Average Current Mode Controlled Regulator Output Model

DC gain. The result is excellent load regulation, where the output voltage is nominally equal to the command voltage. This is typical of most power supplies.

Non-integrating gain utilizes a resistive feedback path instead of capacitive. The result is that the output voltage will decrease as the load current increases. This provides an INTENTIONAL negative load regulation characteristic.

The use of the DC offset, achieved simply by the voltage divider formed by R_I and R_D of Figure 3B, centers the output voltage at nominal load.

These points are best shown by an example.

EXAMPLE

Buck regulator using UC3886/UC3910 Chip Pair

V_{OUT} = 2.4V to 3.4V.

Regulation window = ±5% including load, line, ripple and transient conditions.

Ripple = ±1%

DC Regulation Tolerance plus Line Regulation = ±1%

I • R Voltage Drop from power supply to load = -1% at Imax

Imin = 0.5A = Minimum normal operating current

Imax = 10A = Maximum normal operating current

I_Limit = 12A = Short circuit current limit

Goal: Determine and set V_{OUT} vs I_{OUT} such that the ±5% Regulation requirement is met with maximum allowed transient voltage swings (minimum output capacitance).

Step 1: Establish a regulation goal.

The specified window is ±5%. V_{RIPPLE} and DC Error, which are each ±1%,

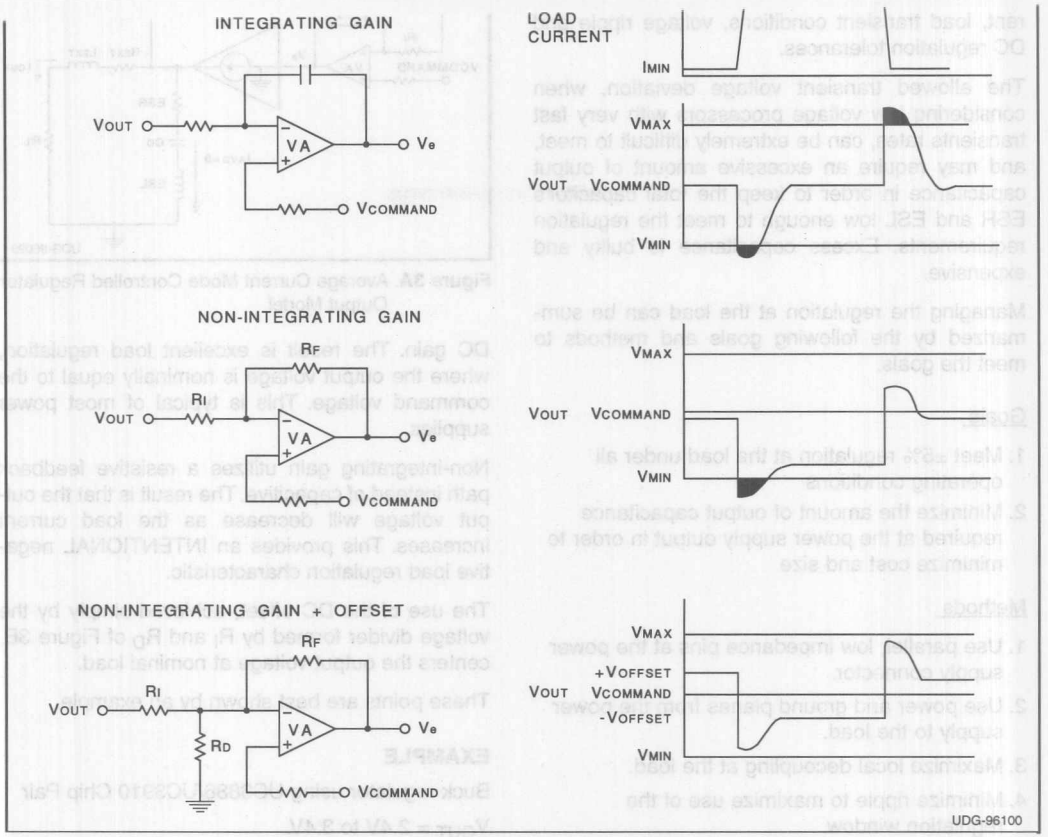


Figure 3B. Integrating vs Non-Integrating Gain in the Voltage Error Amplifier of the UC3886

reserve ±2% of the specified window. This leaves ±3% of the window for load regulation.

Figure 3C illustrates the regulation window.

Based on the regulation of integrating gain, a load step from Imin to Imax may only cause a -3% voltage excursion and still insure that the ±5% window requirement is met. The load regulation set as a goal will double the allowed voltage excursion from -3% to -6%.

Step 2: Determine the voltage-to-current gain of the closed loop Average Current Mode circuit.

The UC3886 error voltage, COMP, swings from Vcommand at 0.0 amperes load current, to $V_{COMMAND}$ +1.0V at the short circuit current limit point, I_Limit, set by the Current Sense Amplifier gain. The voltage-to-current gain is therefore equal to

$$V_to_I_Gain = \frac{I_Limit}{DVe} = \frac{12\ A}{1.0\ V} = 12$$

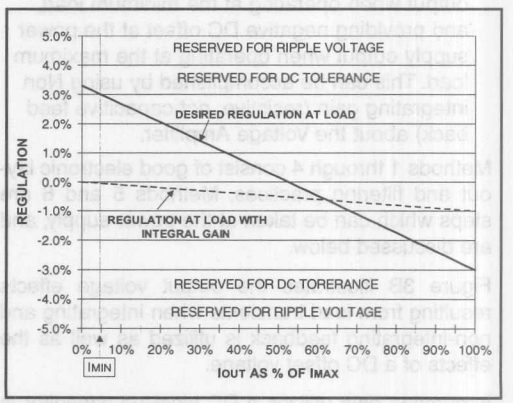


Figure 3C. Load Regulation for Example Circuit

Step 3: Determine the swing in the UC3886 error voltage, COMP, at Imax.

$$DVe = \frac{Imax}{I_Limit} \bullet 1.0 = \frac{10.0\ A}{12\ A} \bullet 1.0$$

$$= 0.833\ Volts$$

From the desired load regulation curve, determine the swing in output voltage associated with the change from 0 Amps (Not Imin in this case) to Imax. Subtract the I • R drop intrinsic to the circuit.

The desired regulation swing is -6.3% - (-1.0%) = -5.3% from 0A to Imax. At the lowest operating output voltage, this is equivalent to:

$$DV_{OUT} = 2.4V \bullet 5.3\% = 0.127\ Volts$$

Step 4: Determine the gain around the Voltage Amplifier to achieve the desired voltage swing over the operating load range.

$$DVout = \frac{DVe}{Gain} = \frac{DVe}{R_F/R_I}$$

and therefore $R_F/R_I = \frac{0.833V}{0.127V} = 6.56$

Where R_F is the feedback resistor and R_I is the input resistor, as in Figure 3B. Let R_F = 20.0kW, then R_I = 3.09kW and the gain about the Voltage Amplifier = 6.47.

Step 5: Determine the DC offset required from the Resistive Divider and calculate the value of R_D.

The resistive divider must offset the output voltage by the desired offset at 0.0 Amps of +3.3%.

Using a voltage divider resistor, R_D with R_I, as shown in Figure 3B:

$$\frac{R_D}{R_I + R_D} = 1 - 0.033 \text{ so}$$

$$R_D = \frac{R_I \bullet (1\text{-}0.033)}{0.033} = 90.9kW$$

Figure 3D illustrates the resulting load regulation at the output of the power supply and at the load.

Step 6: Determine the effects of a variable output voltage

The DC offset fixed by the voltage divider of R_I and R_D is setting an offset percentage, which is constant at 3.3%.

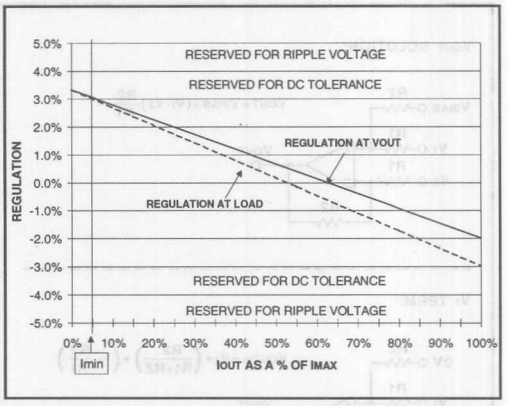


Figure 3D. Load Regulation for Example Circuit -2.4V Output

Therefore, at 0.0A all output voltages will start at +3.3% offset.

The gain of the Voltage Amplifier, set by R_F and R_I, is also fixed, and will therefore have a smaller effect at output voltages larger then 2.4V. At 3.4V, the change in output voltage is fixed at -0.127 Volts, which is only -3.74% of the nominal output. The higher voltages will therefore operate within a narrower voltage regulation window than 2.4V and the voltage regulation requirements will be met.

APPENDIX 4: DIFFERENTIAL AMPLIFIER EQUATIONS

The amplifier shown in Figure 4A is configured as a differential amplifier, with a DC bias. The output voltage of this configuration is given by

$$V_{OUT} = V_{BIAS} + (V1 - V2) \bullet \frac{R2}{R1}$$

This result can be derived from the principal of superposition, by adding the portion of the output voltage due to each input voltage, V1, V2 and V_{BIAS}.

V1 term: Set V_{BIAS} and V2 to GND, find V_{OUT}:

The voltage at the non-inverting input to the amplifier V(+) is derived from the voltage divider of R2 and R1, and is then multiplied by the non-inverting op-amp non-inverting gain formula.

$$V(+) = V1 \bullet \left(\frac{R2}{R1+R2}\right)$$

$$V_{OUTV1} = V(+) \bullet \left(1 + \frac{R2}{R1}\right)$$

$$= V1 \bullet \left(\frac{R2}{R1+R2}\right) \bullet \left(1 + \frac{R2}{R1}\right)$$

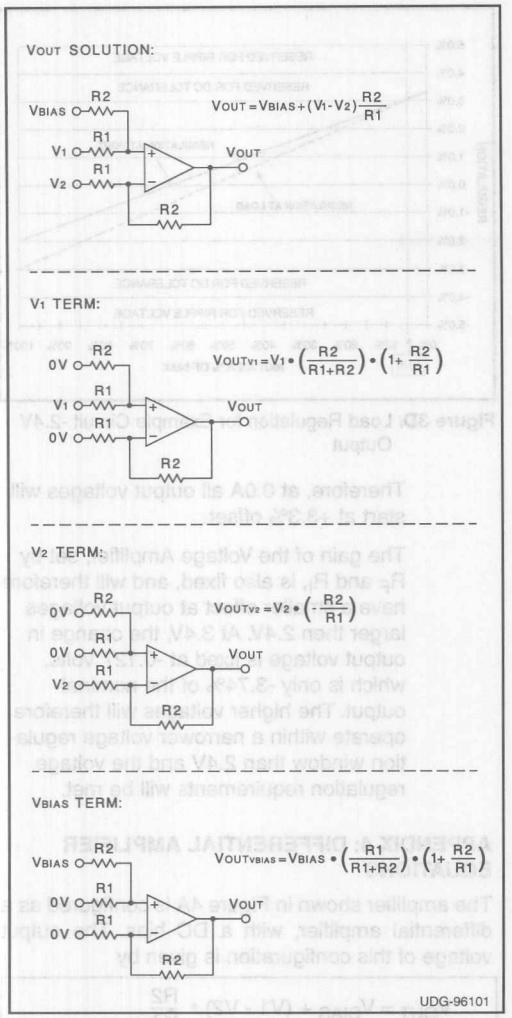


Figure 4A. Differential Amplifier Configuration with DC Bias

V2 term: Set V_{BIAS} and V1 to GND, find V_{OUT}:

The voltage at the non-inverting input to the amplifier is 0 volts. The configuration is therefore a standard inverting op-amp configuration which gives

$$V_{OUTV2} = V2 \bullet \left(-\frac{R2}{R1}\right)$$

V_{BIAS} term: Set V1 and V2 to GND, find V_{OUT}:

The voltage at the non-inverting input to the amplifier is derived from the voltage divider of R1 and R2, and is then multiplied by the non-inverting op-amp non-inverting gain formula.

$$V(+) = V_{BIAS} \bullet \left(\frac{R1}{R1+R2}\right)$$

$$V_{OUTVBIAS} = V(+) \bullet \left(1 + \frac{R2}{R1}\right)$$

$$= V_{BIAS} \bullet \left(\frac{R1}{R1+R2}\right) \bullet \left(1 + \frac{R2}{R1}\right)$$

when factored gives

$$V_{OUTVBIAS} = V_{BIAS}$$

V_{OUT} Solution: Sum the 3 terms together

$$V_{OUT} = V1 \bullet \left(\frac{R2}{R1+R2}\right) \bullet \left(1 + \frac{R2}{R1}\right)$$

$$+ V2 \bullet \left(-\frac{R2}{R1}\right) + V_{BIAS}$$

which yields

$$V_{OUT} = V_{BIAS} + (V1 - V2) \bullet \frac{R2}{R1}$$

The DC Bias is the value of V_{BIAS}, and the gain of the differential amplifier which multiplies the difference voltage (V1 - V2) is given by

$$\text{Gain} = \frac{R2}{R1}$$

APPENDIX 5: PROGRAMMING THE SHORT CIRCUIT LIMIT

From the short circuit current equation

$$I_{SC} = \frac{1.0 \text{ volt}}{R_{SENSE} \bullet G_{CSA}}$$

it can be seen that the product of the sense resistor and the gain of the Current Sense Amplifier must be

$$R_{SENSE} \bullet G_{CSA} = \frac{1.0 \text{ Volt}}{I_{SC}}$$

The value of G_{CSA} is bounded to

$$G_{CSA_MIN} = 5.0 \text{ and } G_{CSA_MAX} = \frac{2.5MHz}{F_{SWITCH}}$$

which in turn, bounds the value of R_{SENSE}, since the product is a constant.

Several considerations must be used to select R_{SENSE}:

- Type - 2 Wire vs 4 Wire: With very low value sense resistors, as the UC3886 allows, the resistance of the solder joint becomes a major contributor to resistance. A 4 wire Kelvin connection removes the error due to the solder joint. A 2 wire is more cost effective. A compromise may be in using a surface mount 2 wire resistor and splitting the pads to simulate a 4 wire connection. Beware that paralleling 4 wire

resistors for reduced power dissipation can result in an imbalance between the resistors.

- Value - Minimum and Maximum possible values: The upper value is limited by the minimum G_{CSA} value, and the lower value by the maximum G_{CSA} value. Higher values dissipate more power. Lower values typically have a higher temperature coefficient, resulting in less accuracy over temperature and have a higher cost factor.
- Efficiency and Power Dissipation: The lower the value of R_{SENSE}, the less power dissipation and the higher the regulator's efficiency. Power dissipation must be considered under both normal maximum operating current, Imax, as well as under short circuit conditions, I_{SC}.
- Operating Voltages and Duty Cycle: Given a low input voltage and an output voltage close to V_{IN}, such as 3.3V input, 2.9V output, the operating duty cycle can be quite high. A large voltage drop across R_{SENSE} may be unacceptable.
- Self-Inductance: A low inductance type of resistor should be used. Inductance of the resistor will result in an inductive "step" voltage superimposed on the ramp voltage. The step voltage will not contribute to error as the average current measurement is not effected, but may contribute to instability due to the very high slope of the inductive step. Refer to Unitrode Application Note U-140 [4] regarding slope limitations in Average Current Mode Control.

The following example illustrates the selection process in choosing R_{SENSE} and in setting the value of G_{CSA}.

F_{SWITCH}: 200kHz

Imax: 10.0A

I_{RIPPLE}: 1.0Ap-p

R_{LOUT} 0.01W

V_F 0.5V @ 12A

V_{IN} 5.0V

$R_{DS(on)}$ 0.025W

Step 1: Find the bounds of the Current Sense Amplifier gain G_{CSA}.

Minimum gain = 5.0 By specification

$$\text{Maximum gain} = \frac{2.5\text{MHz}}{200\text{kHz}} = 12.5$$

Step 2: Choose the short circuit limit. This limit should insure that tolerances and ripple current do not inadvertently trip the over current threshold.

Figure 5A illustrates the limitations on the sense resistor based on the bounds of the gain. Choosing a value of Isc as low as possible will limit the power dissipation in the sense resistor.

Select I_{SC} = 12.0 Amps.

Step 3: Choose a value of R_{SENSE}

From Figure 5A, a 12.0A I_{SC} implies that Rsense must lie between 0.007W and 0.017W. Choose 0.010W as the lowest standard value.

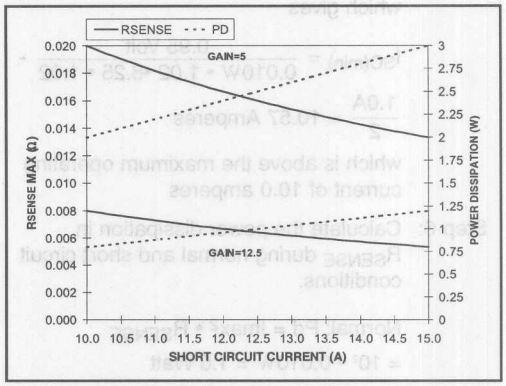


Figure 5A. R_{SENSE} and Power Dissipation Boundaries

Step 4: Program the gain of the Current Sense Amplifier.

$$G_{CSA} = \frac{1.0\text{ Volt}}{I_{SC} \bullet R_{SENSE}}$$

$$= \frac{1.0\text{ Volt}}{12.0\text{A} \bullet 0.01\text{W}} = 8.33$$

Choose large enough resistors so as not to load down the output of the Current Sense Amplifier. Refer to Figure 14 of this application note to configure the Current Sense Amplifier.

Select R2 = 36.5kW

$$R1 = \frac{36.5\text{kW}}{8.33} = 4.42\text{kW (closest}$$

1% value)

$$G_{CSA} = \frac{36.5}{4.42} = 8.25$$

Step 5: Solve for the minimum AVERAGE short circuit current limit.

The tolerance of the UC3886 current limit clamping mechanism is 1.0V ±0.05V.

Assume R_{SENSE} and G_{CSA} each have a tolerance of ±2% over temperature and life. 1/2 of I_{RIPPLE} will add to the AVERAGE current value of I_{SC}, and should not cause the UC3886 to clamp into over current.

Then

$$I_{SC(min)} + \frac{I_{RIP}}{2} = \frac{0.95\ Volt}{R_{SENSE} \bullet 1.02 \bullet G_{CSA} \bullet 1.02}$$

which gives

$$I_{SC(min)} = \frac{0.95\ Volt}{0.010W \bullet 1.02 \bullet 8.25 \bullet 1.02} - \frac{1.0A}{2} = 10.57\ Amperes$$

which is above the maximum operating current of 10.0 amperes

Step 6: Calculate the power dissipation in R_{SENSE} during normal and short circuit conditions.

Normal: $Pd = Imax^2 \bullet R_{SENSE}$

$= 10^2 \bullet 0.010W = 1.0$ Watt

Short Circuit: $Pd = I_{SC}^2 \bullet R_{SENSE}$

$= 12^2 \bullet 0.010W = 1.44$ Watt

Calculating the Short Circuit Duty Cycle

During a short circuit condition in a Buck regulator, the duty cycle becomes small and the free-wheeling diode conducts current for most of each switching cycle. The free-wheeling diode's average current is almost equivalent to the short circuit current in this condition, resulting in much higher power dissipation.

To calculate the power dissipated in the diode, the short circuit duty cycle, D_{SC}, must be calculated.

The governing equation of the Buck regulator is derived in Appendix 1, where the output voltage is given by

$$V_{OUT} = D \bullet (V_{IN} - I_{OUT} \bullet (R_{DSon}) - [I_{OUT} \bullet (R_{LOUT} + R_{SENSE})] - [V_F \bullet (1\text{-}D)]$$

where D is the operating duty cycle. Under a true (0.0W) short circuit condition, the output voltage is 0.0 volts and the operating duty cycle will be D_{SC}. Using 0.0V in the formula above and solving for I_{SC} and D_{SC} gives

$$I_{SC} = \frac{D_{SC} \bullet (V_{IN} + V_F) - V_F}{D_{SC} \bullet R_{DSon} + R_{LOUT} + R_{SENSE}}$$

$$\text{and } D_{SC} = \frac{I_{SC} \bullet (R_{LOUT} + R_{SENSE}) + V_F}{V_{IN} - I_{SC} \bullet R_{DSon} + V_F}$$

Continuing from the above example, the short circuit duty cycle is

$$Dsc = \frac{12A \bullet (0.01W + 0.01W) + 0.5V}{5.0V - 12A \bullet 0.025W + 0.5V} = 12\%$$

The resulting diode average current is therefore

$$I_{DIODE} = (100\%\text{-}12\%) \bullet 12A = 10.56$$

Amperes.

The output inductor, L_{OUT}, must be designed not to saturate at the short circuit current. Should L_{OUT} saturate, excessive current can result which is only limited only by the parasitic resistances, which can result in reliability or safety problems.

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FUELING THE MEGAPROCESSOR - A DC/DC CONVERTER DESIGN REVIEW FEATURING THE UC3886 AND UC3910

by Larry Spaziani
Applications Engineer

ABSTRACT

This application note provides a detailed account of design tradeoffs and procedures for the development of a Voltage Regulator Module (VRM) for the Intel Pentium®Pro processor. This voltage regulator features Unitrode's UC3886 Average Current Mode PWM Controller and UC3910 4-BIT DAC and Voltage Monitor ICs configured in a Buck Regulator. Test results and waveforms are provided which show how the VRM power supply meets stringent requirements imposed by Intel.

INTRODUCTION

Intel's Pentium®Pro power system specification demonstrates the industry trend to operate at lower voltages and at higher currents, with tight regulation and fast transient response. Meeting these requirements demands the most of both the power stage and the control system of the power supply. Unitrode's UC3886 and UC3910 are specifically designed for optimizing the control loop, the dynamic response and the DC accuracy required by the Pentium®Pro. The power stage inductor and capacitors are critical as well in meeting the extremely tight voltage regulation during a Pentium®Pro load transient.

This application note will detail the design of a complete VRM power supply. This design review will detail the critical VRM specifications, power supply architecture tradeoffs, power stage design details and equations and finally design specifics used to configure the UC3886 and UC3910. The complete current and voltage loops will then be closed, and performance results of the power supply will be shown.

This design review will reveal the many advantages of using the UC3886 and UC3910, which include:

- Direct output NMOS drive, eliminating the need for creating high voltages and allowing the use of an efficient N-Channel MOSFET.
- High DC accuracy negates the need for voltage trimming and insures the overall regulation will be met.
- Direct interface with INTEL's PENTIUM™ PRO VID programming codes.
- The UC3910's DAC and unique voltage monitoring architecture directly replaces discrete components including a precision reference, a DAC, complicated resistive networks, multiple window comparators and an SCR Driver.
- Accurate and true "square-knee" current limiting eliminates the need to over-design the power components for operation in an indefinite short circuit.
- Optimization of the loop performance due to large signal changes due to transient loading effects.

The Unitrode VRM demonstration kit is shown in Figure 1. The VRM's schematic is shown in Figure 2 and the parts are described in Table 1.

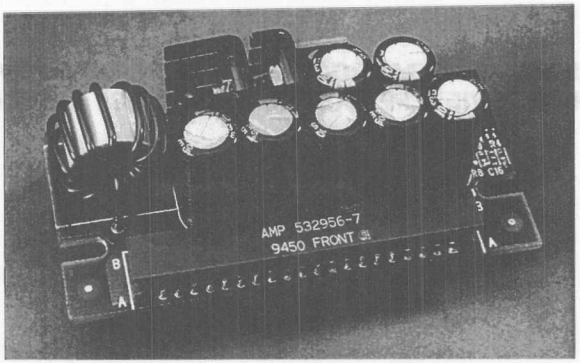


Figure 1. Unitrode's VRM Demonstration Kit

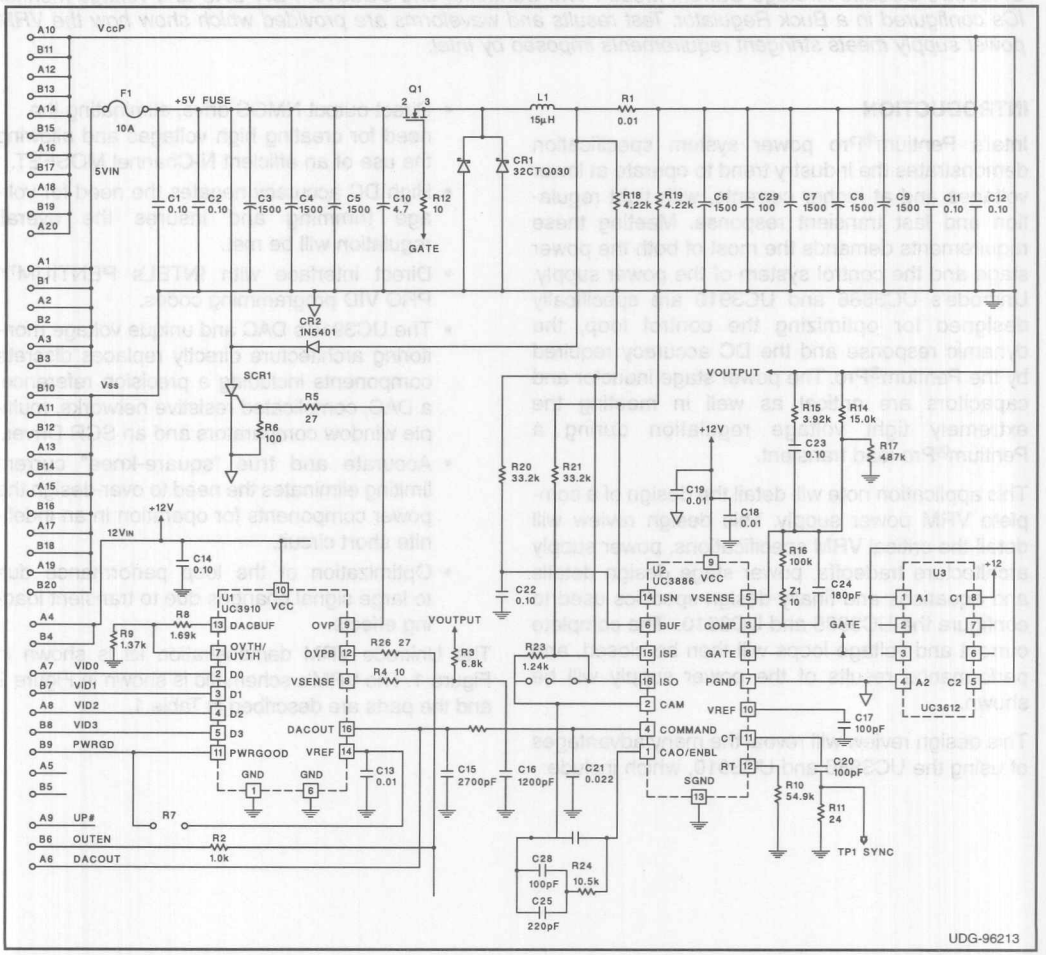


Figure 2. Schematic Diagram

POWER SUPPLY SPECIFICATIONS

The requirements for the DC/DC converter which will provide power to Intel Pentium®Pro are contained in Intel's application note AP-523 [1], Section 10. These power supply requirements consist of required specifications, expected specifications and design guidelines, some of which are summarized below.

Input Voltages:	5.00V ±5% 12.00V ±5%
Output Voltage:	Variable from 2.4V to 3.4V programmable per INTEL VID codes, 100mV increments.
Minimum Current:	0.3A
Maximum Current:	11.2A
Regulation:	±5% Including initial tolerance, setpoints, drift, transients and ripple/noise.
Load Transient:	Minimum to maximum or maximum to minimum current at a rate ≤30.3A/µs.
Input Current Rate:	±0.1A/µs maximum during a load transient.
Power-Good:	Open Collector output LOW signal when the output voltage is not within ±10% of nominal.
Output Enable:	Open Collector input signal with a LOW state disabling the DC/DC converter.
Ripple/Noise:	±1% to 20MHz.
Overshoot:	≤10% above the initial setpoint at application or removal of input power.
Efficiency:	≥80% at maximum current, ≥40% at minimum current
Temperature:	+10°C to +60°C, ≥100 LFM air cooling along connector axis.
Over Voltage:	Self shut down when the output exceeds 10% to 20% of nominal.
Short Circuit:	Continuous short circuit mode-without damage or overstress to the unit.

TABLE 1 - PENTIUM®PRO VRM DEMONSTRATION KIT BILL OF MATERIALS

UNITRODE PENTIUM®PRO VRM DEMONSTRATION KIT			
REF.DES.	**DESCRIPTION**	**PACKAGE**	**NOTES**
U1	Unitrode UC3910DP 4-BIT DAC and Voltage Monitor	SOIC-16	
U2	Unitrode UC3886DP ACM PWM Controller	SOIC-16	
U3	Unitrode UC3612DP Dual Schottky Diode	SOIC-8	
C01	0.10µF Ceramic	1206 SMD	
C02	0.10µF Ceramic	1206 SMD	
C03	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C04	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C05	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C06	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C07	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C08	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C09	Sanyo 6MV1500GX, 1500µF, 6.3V, Aluminum Electrolytic	10x20mm Radial Can	
C10	Sprague/Vishay 595D475X0016A2B, 4.7µF 16V Tantalum	SPRAGUE Size A	
C11	0.10µF Ceramic	1206 SMD	
C12	0.10µF Ceramic	1206 SMD	
C13	0.10µF Ceramic	1206 SMD	
C14	0.10µF Ceramic	1206 SMD	
C15	2700pF Ceramic	0603 SMD	
C16	1200pF Ceramic	0603 SMD	
C17	1000pF Ceramic	0603 SMD	
C18	0.01µF Ceramic	0603 SMD	
C19	0.10µF Ceramic	1206 SMD	
C20	100pF NPO Ceramic	0603 SMD	
C21	0.022uF Ceramic	0603 SMD	
C22	0.10µF Ceramic	1206 SMD	
C23	0.10µF Ceramic	1206 SMD	

TABLE 1 - PENTIUM®PRO VRM DEMONSTRATION KIT BILL OF MATERIALS (cont.)

REF.DES.	DESCRIPTION	PACKAGE	NOTES
C24	180pF NPO Ceramic	0603 SMD	
C25	220pF NPO Ceramic	0603 SMD	
C26	NOT USED	0603 SMD1	
C27	180pF NPO Ceramic	0603 SMD	
C28	1000pF NPO Ceramic	0805 SMD	
C29	Sprague/Vishay 593D107X9010D2, 100µF, 6.3V Tantalum	EIA Size D SMD	
SCR1	Motorola MCR12D, 12A SCR	TO-220AB	2
CR1	International Rectifier 32CTQ030 30V, 30A Schottky Diode	TO-220AB	
CR1-HS	AAVID 577002 TO-220 Heat Sink		
CR2	1N5401CT, 3A 100V Diode	DO-201AD	2
F1	Littlefuse R451010, 10A Fast Blow	SMD Square	2
J1	AMP 532956-7 40 Pin Connector		
L1	Coilcraft S6030-B, 10µH to 20µH	Radial Toroid	
Q1	International Rectifier IRL3103, 30V, 56A	TO-220AB	
Q1-HS	AAVID 577202 TO-220 Heat Sink		
R01	Dale/Vishay WSR-2 0.01W 1%	SMD Power Package	3
R02	1.00kW, 1%, 1/16 Watt	0603 SMD	
R03	6.8kW, 5%, 1/16 Watt	0603 SMD	
R04	10W, 5%, 1/16 Watt	0603 SMD	4
R05	27W, 5%, 1/16 Watt	0603 SMD	2
R06	100W, 5%, 1/16 Watt	0603 SMD	2
R07	NOT USED	0603 SMD	5
R08	1.69kW, 1%, 1/16 Watt	0603 SMD	
R09	1.37kW, 1%, 1/16 Watt	0603 SMD	
R10	54.9kW, 1%, 1/16 Watt	0603 SMD	
R11	24W, 5%, 1/16 Watt	0603 SMD	8
R12	10W, 5%, 1/16 Watt	0603 SMD	
R13	10kW, 5%, 1/16 Watt	0603 SMD	
R14	15.0kW, 1%, 1/16 Watt	0603 SMD	
R15	3.92kW, 1%, 1/16 Watt	0603 SMD	
R16	100kW, 1%, 1/16 Watt	0603 SMD	
R17	487kW, 1%, 1/16 Watt	0603 SMD	
R18	4.22kW, 1%, 1/16 Watt	0603 SMD	
R19	4.22kW, 1%, 1/16 Watt	0603 SMD	
R20	33.2kW, 1%, 1/16 Watt	0603 SMD	
R21	33.2kW, 1%, 1/16 Watt	0603 SMD	
R22	NOT USED	0603 SMD	1
R23	1.24kW, 1%, 1/16 Watt	0603 SMD	
R24	10.5kW, 1%, 1/16 Watt	0603 SMD	
R25	NOT USED	0603 SMD	
R26	27W, 5%, 1/16 Watt	0603 SMD	6
Z1	10W, 5%, 1/16 Watt	0603 SMD	7

Notes:
1) R22 and C26 are not required. These parts can be used for alternative compensation schemes.
2) These parts are related to the overvoltage protection SCR firing circuit.
3) Simulate a "4 wire" connection using PCB etch for best results.
4) R04 used for debug purposes. R04 is not required in a production unit.
5) R07 can be used to pull up the PWRGOOD signal internally to the VRM
6) R26 is not required for proper operation. R26 is used as a "jumper".
7) Z1 used for debug purposes. Z1 can be used for alternative compensation, or shorted in a production unit.
8) R24 is not required for production unless synchronization is used.

POWER CONVERSION ARCHITECTURE

Topology: Single Switch Buck Regulator

Power conversion from either +5 volts or +12 volts to the lower voltages required by the Pentium®Pro can be accomplished by either a linear regulator or by a myriad of switching converter topologies. Linear regulation is not appropriate because of its inherently poor efficiency. Transformer coupled switching topologies are not required, and not desired, because of the common input and output grounding system. Either a single switch or a synchronous rectifier (two switch) buck regulator are the most appropriate choices for this application. Higher efficiency can be achieved with synchronous rectification, but is not required in this application because the efficiency goal is 80%. The added cost and complexity of a second N-MOSFET is therefore not justified.

Input Voltage: +5 Volts Provides Power, +12 Volts provides Bias and Drive

Either the +5 volt or the +12 volt power bus can be used for this single switch Buck regulator. An N-channel MOSFET is chosen as the switch because of the efficiency of low R_{DSon} N-MOSFETs. The +12 volt bus can be used to drive the N-MOSFET in a +5V input Buck regulator, whereas a +12V input Buck regulator would require a higher voltage (17-20 volts) to provide drive to the switch. Several other considerations are made in choosing the input voltage, including:

- +12V input would require a larger output inductor for a given ripple current.
- +5V input operates at higher duty cycles, reducing power in the freewheeling diode, whereas +12V input operates at lower duty cycles, reducing power in the MOSFET.
- The combined power dissipated of the freewheeling diode plus the MOSFET is less with a +5V input than with a +12V input.
- +5V typically has better power distribution on a motherboard, and within a system, even considering the higher DC currents involved when converting power from +5V.
- The input capacitors will see the same RMS switching current at either voltage.
- +5V has six dedicated input pins whereas +12V has only two. Using +5V as an input voltage will result in fewer amps/pin and a lower impedance path to the source.
- +12V busses can often withstand larger voltage deviations due to the loading effects of the Pentium®Pro.

Control Method - Average Current Mode Control Using the UC3886

Average Current Mode control, as implemented with the UC3886, offers the advantages of optimization of the control loop, very fast amplifiers for a fast transient response, and accurate current limiting. Application Note U-140 [2] discusses the many advantages of Average Current Mode control over both Peak Current Mode control and Voltage Mode control.

Switching Frequency - 200kHz

Several considerations in choosing 200kHz as the switching frequency are:

1. An upper bound on frequency is derived from the gain required by the UC3886 Average Current Mode control current sense amplifier. This upper bound will be shown to be 312kHz.
2. A high switching frequency is desired for
   - Minimum output inductor size
   - Maximum control loop bandwidth
3. A low switching frequency is desired for
   - Keeping switching losses low, although switching losses in the semiconductors is not a significant factor in this application because the input voltage (+5V) is very low.
   - Reducing noise when using a 2-layer printed circuit board.
4. The use of Aluminum Electrolytic capacitors is favored for both input and output capacitors in this application because of the height allowed, their high Capacitance-to-ESR and Capacitance-to-ESL ratios and their ripple current capabilities. Surveying several suppliers of Aluminum Electrolytic capacitors revealed that they have significantly low impedance and optimal ripple current handling at 100kHz to 200kHz, where ESR is minimal.

POWER STAGE COMPONENT SELECTION

The power stage components consist of the input and output capacitors, switch, freewheeling diode, output inductor and sense resistor, and are chosen to be leaded devices for the most part because of the height allowed in this design. The semiconductors are first chosen to meet a full load efficiency goal of 80% and to provide reliable operation at full load. The output inductor is then chosen to provide low output current ripple into the capacitors and for continuous mode operation of the

Buck regulator. The output capacitors are chosen to provide an extremely low output impedance for low voltage ripple and low voltage droop during and output load transient. Finally, the input capacitors are chosen to handle the high level of ripple current demanded by the Buck regulator and to heavily filter the input voltage from both high and low load transients.

Efficiency/Power Dissipation Budget

The desired efficiency goal of ≥80% at full load operation will govern how many of the power stage components are selected. Efficiency goals are set at a nominal input voltage of +5.00V, an output voltage of 3.1V, +25°C ambient temperature and at a maximum load current of 11.2A.

The nominal output power of the power supply is equal to 3.1V • 11.2A = 34.72 Watts. From the desired efficiency, the input power at full load is

$$P_{IN} = \frac{P_{OUT}}{0.8} = \frac{34.72W}{0.8} = 43.4 \text{ Watts}$$

The power dissipated is 8.68 Watts, at full load. An example efficiency budget is shown in Table 2.

Power Stage Component Design Details

Freewheeling Diode: CR1

International Rectifier 32CTQ030 or equivalent, 2 legs paralleled

$V_F \approx 0.35V$ @ $T_J = 115°C$

$T_{Jmax} = 150°C$

Heat Sink = AAVID P/N 577002 or equivalent

Low voltage schottky technology is chosen to maximize the efficiency of the power supply, based on its lower forward voltage and lack of reverse recovery losses.

The operating duty cycle for this Buck converter is derived based on the equation[3]

$$D = \frac{V_O + I_O \bullet (R_{SENSE} + R_{LOUT}) + V_F}{V_{IN} - (I_O \bullet R_{DSon}) + V_F}$$

Likewise, the short circuit operating duty cycle is given by

$$D_{SC} = \frac{0.0V + I_{SC} \bullet (R_{SENSE} + R_{LOUT}) + V_F}{V_{IN} - (I_{SC} \bullet R_{DSon}) + V_F}$$

Given R_{SENSE} = 0.01

R_{LOUT} = 0.012 at 25°C, full load current

V_F = 0.35V at full load, 0.25 at minimum load

I_{SC} = 12.5A Nominal Short Circuit Current

V_{IN} = 5.00V Nominal

R_{DSon} = 0.025 at 110°C

V_O = 3.10V Nominal

Then typical duty cycles will be approximately:

Operating: ≈ 73% at Full load, 25°C T_A

≈ 64% at minimum load, 25°C T_A

Short Circuit: ≈ 13%

The maximum operating power dissipation at the diode's maximum operating junction temperature of 110°C is given by

$$P_{Dmax} = V_F \bullet I_{Omax} \bullet (1 - D_{max})$$
$$= 0.35V \bullet 11.2A \bullet (1 - 0.73) = 1.06W$$

The power dissipation under short circuit conditions, however, is substantially larger

$$P_{Dsc} = V_F \bullet I_{sc} \bullet (1 - D_{sc}) = 0.35V \bullet 1.12A \bullet (1 \bullet 0.73) = 1.06W$$

Let T_{Jmax} = 115°C under operating conditions and 150°C under short circuit conditions (Rated T_{Jmax} for device)

The two governing formulas defining the heat sink requirements (thermal impedance RθHS) are

$115°C = 50°C + 1.06W \bullet (3.0 + R\theta HS)$,
$R\theta HS = 58°C/W$

$150°C = 50°C + 3.80W \bullet (3.0 + R\theta HS)$,
$R\theta HS = 23.3°C/W$

The short circuit operation must be used to choose the heat sink. AAVID P/N 577002 with 100LFM of airflow meets the heat sink requirement of ≤23°C/W. Note that the accurate current limit set

TABLE 2 - POWER DISSIPATION BUDGET

Description	Power Dissipated [W]	Budget Remaining [W]
Budgeted Power		8.68
Estimated 3% Power Distribution (I^2R) Losses	1.1	7.58
Diode Losses	1.1	6.48
Sense Resistor	1.25	5.23
Output Inductor (I^2R)	1.3	3.93
Output Inductor (Core)	0.1	3.83
Input Capacitance Ripple Current Losses	0.5	3.33
UC3886 + UC3910 + Bias loads	0.3	3.03
MOSFET (Switching, Conduction, Gate Drive)	3.03	0.00

point achieved by the UC3886 allows for a minimum heat sink solution.

MOSFET Switch: Q1

International Rectifier IRL3103

$R_{DSon} \approx 0.025\Omega$ Estimated at $V_{GS} = 7V$, $T_J = 115°C$

Q_G (Total Gate Charge) ≈ 50nC estimated at $V_{GS} = 7V$

Heat Sink ≈ AAVID P/N 577202 or equivalent

From the power budget, the MOSFET should be chosen to achieve the desired losses, including the gate drive losses. Choosing a Logic Level MOSFET or a standard threshold voltage MOSFET is discussed in U-156[3]. This application will utilize a Generation 5 MOSFET from International Rectifier because of its combination of low R_{DSon} at low V_{GS} as well as rated V_{GS} of ±20V.

The power dissipation of the MOSFET consists of 4 components; (a) Gate drive, (b) C_{OSS}, (c) Crossover losses, and (d) Conduction losses

a) Gate Drive losses are given by

$$P_{GATE} = I_{GATEavg} \bullet V_{GS}$$

From the IRL3103 charge curve, with $V_{GS} = 7$ volts, the required total charge, Q_G, is estimated to be 50nC. The average current is given by

$$I_{GATEavg} = Q_G \bullet F_S = 50nC \bullet 200kHz = 10mA$$

$$P_{GATE} = 0.010 \text{ Amps} \bullet 12 \text{ Volts} = 0.12 \text{ Watts}$$

b) Coss losses are due to the discharge of the energy stored in the capacitance Coss each cycle, equivalent to

$$P_{COSS} = 0.5 \bullet Coss \bullet (V_{IN} + V_F)^2 \bullet F_S$$

From the IRL3103 capacitance curve, Coss is estimated to be 2400pF. Therefore,

$$P_{COSS} = 0.5 \bullet 2400pF \bullet (5.35V)^2 \bullet 200kHz = 0.007W.$$

c) Crossover (turn-on and turn-off) losses can be estimated as

$$P_{CROSSOVER} = \frac{1}{6} \bullet (V_{IN} + V_F) \bullet I_O \bullet \frac{T_{RISE/FALL}}{T_S}$$

where $T_{RISE/FALL}$ is the MOSFET current rise and fall time, estimated to be approximately 150ns, and T_S is the switching period. This loss occurs once at turn-on, and once at turn-off, and therefore, for this application

$$P_{CROSSOVER} = 2 \bullet \frac{1}{6} \bullet 5.35V \bullet 11.2A \bullet \frac{150ns}{5\mu s} = 0.6 \text{ Watts}$$

d) Conduction losses are determined by

$$P_{COND} = I_O^2 \bullet R_{DSon} \bullet D_{MAX}$$

and are worst at the maximum operating junction temperature, where R_{DSon} is highest. For the IRL3103, this loss is

$$P_{COND} = 11.2^2 \bullet 0.025\Omega \bullet 0.73 = 2.29 \text{ Watts}$$

$$Pd_Total_FET = 2.29W + 0.6W + 0.007W + 0.12W = 3.02W$$

The MOSFET heat sink requirements are determined from

$$115°C = 50°C + 3.02W \bullet (2.0 + R_{\theta HS}),$$

$$R_{\theta HS} = 19.5°C/W$$

AAVID P/N 577202 with 100LFM of airflow provides ≤14°C/W, exceeding the heat sink requirement.

Output Inductor: L1

Coilcraft P/N S6030-B

20µH @ 0 Adc

10µH @11.2 Adc

13 Turns, # 16AWG on Micrometals T60-52D Core

$R_{DC} \leq 0.008\Omega$ max, 20°C Ambient

$T_{RISE} \approx 40°C$ at maximum load

The output inductor of a Buck regulator is often chosen to maintain continuous current in the inductor under minimum load conditions. The ripple current in the inductor under minimum DC current conditions is equal to $2 \bullet I_{MIN}$ for this rule to apply. For this power supply, L_{OUT} is determined by

$$L_{OUT} = \frac{(V_{IN} - V_{OUT}) \bullet Duty}{2 \bullet I_{MIN} \bullet F_S} = \frac{(5V - 3.1V) \bullet 0.64}{2 \bullet 0.3A \bullet 200kHz} = 10.1\mu H \text{ @ Low Load}$$

A second condition for choosing the output inductor value is to limit the input current to the power supply during a step change in current from I_{MIN} to I_{MAX}. After a step change in load current, the duty cycle of the Buck regulator responds by assuming a maximum duty cycle of 100%. The input current therefore equals the output inductor current. To limit the input current rate to the required 0.1A/µs, the output inductor is chosen by

$$L_{OUT} = \frac{(V_{IN} - V_{OUT})}{di/dt} = \frac{(5V - 3.1V)}{0.1A/\mu s} = 19\mu H$$

A toroidal inductor design is used to meet these needs. The form factor allows a component height of 0.800", thus allowing a sizable inductor that can be designed for low cost and simple winding techniques. The inductance vs DC current is shown in Figure 3. The inductor must not saturate with DC

current equal to the power supply short circuit current limit, or the current limiting will not be effective.

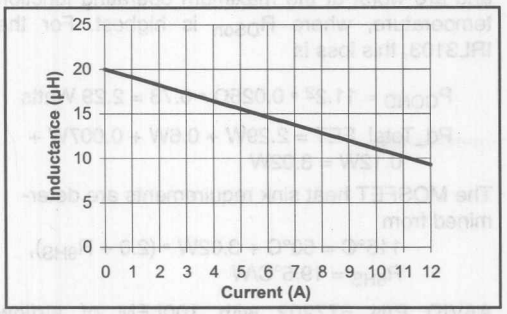


Figure 3. Output Inductor Performance vs DC Current - No AC Flux

The in-circuit inductance will tend to be higher due to the AC Flux imposed by the volt-seconds product of the Buck regulator. Micrometals -52 material's permeability increases substantially with AC Flux. This same effect of AC Flux on the permeability of the -52 material plays a major role during the transient load response of the power supply. During a transient load response, the voltage differential across the output inductor is approximately V_{IN}-V_{OUT}. The duration of the transient response, in excess of 100µs, means that the AC Flux on the core for this time is given by

$$\Delta B_{AC} = \frac{(V_{IN} - V_{OUT}) \bullet T_{LOUT} \bullet 10^8}{N \bullet Ae}$$

$$= \frac{(5V - 3.1V) \bullet 100\mu s \bullet 10^8}{13Turns \bullet 0.374\ cm^2}$$

$$= 3908\ Gauss$$

which, according to Micrometals [3] results in multiplying the output capacitance by approximately 260%. This results in a dynamic inductance, during a load step, of approximately 26µH. This feature will play an important role in the selection of the output capacitors to meet the transient load performance.

Output Capacitors: C06-C09, C11, C12, C29

SANYO - 6MV1500GX - 4 in Parallel
C = 1500µF
Form Factor = 10x20mm, Radial
ESR = 0.044Ω
ESL ≈ 4nH (Estimated)
Ripple Current Rating = 1.25A @ 105°C, 100kHz

Choosing the output capacitors for this regulator may be the single most important decision with regards to meeting the transient load behavior of the Pentium®Pro. The transient load step of the Pentium®Pro is so large and so fast that there is no control loop which can respond quickly enough and maintain regulation. Capacitance, providing a low impedance output, is therefore the best solution to maintaining the proper output voltage.

Understanding the Response to a Step Load

During a step load change from minimum to maximum current, the output of the power supply can be modeled as shown in Figure 4. Prior to the change in load current, the average current in the output inductor is I_{MIN} and the average current in the output capacitor is 0 amperes. Once the load current changes from Imin to I_{MAX}, the parasitic components shown in Figure 4 have a large affect on the output voltage.

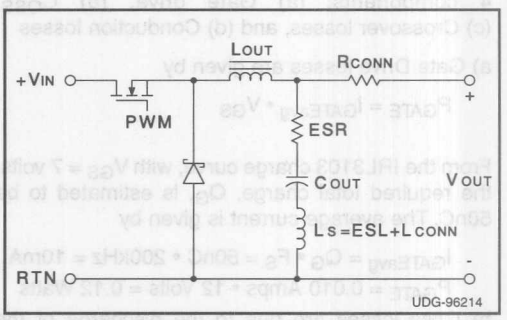


Figure 4. Large Signal Transient Model of Power Supply Output Stage

The VRM connector pins have parasitic resistance and inductance termed R_{CONN} and L_{CONN}. The parasitic inductance of the connector and the output capacitors (ESL) are summed together as L_S. ESR and R_{CONN} cannot be combined in the capacitor path as this would result in a DC load regulation error.

Figure 5 below illustrates the complexity of the output voltage waveform during a step in the output load current. A power supply with excellent load regulation is assumed for the purposes of understanding these dynamics. Reducing the load regulation through non-integrating [3] voltage loop gain will be discussed later in this application note. The output voltage responds to the load current step in four distinct phases, T_{STEP}, T_{LOOP}, T_{LOUT} and T_{CHARGE}.

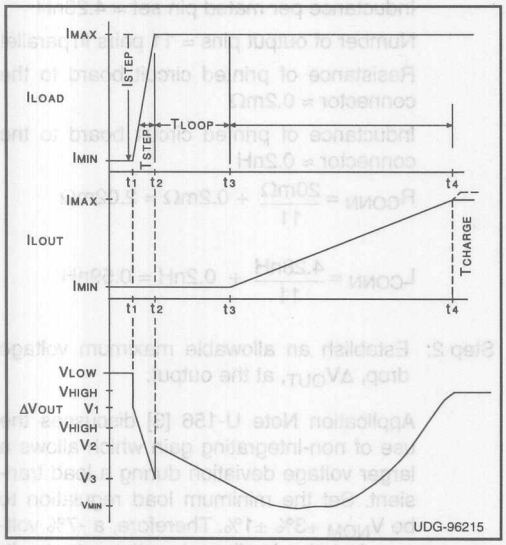


Figure 5. Dynamics of a Step Load

Phase 1, the step current phase from t_1 to t_2 (T_{STEP}), is characterized by a specified change in current and rise time. The response of the output voltage consists of:

a) A voltage step proportional to the parasitic circuit inductance, L_S.
b) A ramp in voltage proportional to the parasitic circuit resistance, R_S, where $R_S = R_{CONN} + ESR$.
c) A droop in voltage proportional to the power supply output capacitance.

The response of the output voltage during the time t_1 to t_2 is therefore given by

$$\Delta V_{OUT} = L_S \bullet \frac{\Delta I}{\Delta T} + i(t) \bullet R_S + \frac{1}{C_{OUT}} \int_{t_1}^{t_2} i(t)dt$$

which, at the end of T_{STEP}, is equal to

$$\Delta V_{OUT} = I_{STEP} \bullet \left(\frac{L_S}{T_{STEP}} + \frac{T_{STEP}}{2 \bullet C_{OUT}} + R_S \right)$$

Phase 2, from t_2 to t_3 (T_{LOOP}), is the time where the load current has settled at its maximum value, I_{MAX}, but the power supply loop has not yet responded. The inductor current is therefore still set at I_{MIN} and the response of the output voltage is therefore determined by

a) A voltage proportional to R_S.
b) A droop in voltage proportional to the power supply output capacitance.

There is an initial discharge of the capacitor at the end of Phase 1 which is the initial condition for Phase 2, determined by

$$\Delta V_Phase1 = \frac{1}{C_{OUT}} \int_{t_1}^{t_2} \frac{I_{STEP}}{T_{STEP}} \bullet t \, dt$$

$$= \frac{I_{STEP} \bullet T_{STEP}}{2 \bullet C_{OUT}}$$

The response of the output voltage during the time t_2 to t_3 is therefore given by

$$\Delta V_{OUT} = \frac{I_{STEP} \bullet T_{STEP}}{2 \bullet C_{OUT}} + \frac{1}{C_{OUT}} \int_{t_2}^{t_3} i(t)dt + R_S \bullet$$

$$I_{STEP} = I_{STEP} \bullet \left(\frac{T_{STEP}}{2 \bullet C_{OUT}} + \frac{T_{LOOP}}{C_{OUT}} + R_S \right)$$

T_{LOOP}, for the UC3886 Average Current Mode Controller and the compensation components shown in Figure 2, is less than one switching cycle.

Phase 3, from t_3 to t_4 (T_{LOUT}), is the time when control loop has forced the Buck regulator to the maximum duty cycle (100% for the UC3886) and the inductor current is ramping from I_{MIN} to I_{MAX}. The output inductor current during this phase is given by

$$iL_{OUT(t)} = \frac{(V_{IN} - V_{OUT})}{L_{OUT}} \bullet t$$

Since the inductor current is ramping up during Phase 3, the capacitor current is ramping down, and is given by

$$iC_{OUT(t)} = I_{STEP} - IL_{OUT(t)}$$

$$= I_{STEP} - \frac{(V_{IN} - V_{OUT})}{L_{OUT}} \bullet t$$

The change in output voltage during Phase 3 consists of

a) A voltage drop proportional to ESR and R_{CONN}.
b) A droop in voltage proportional to the output capacitance.

During Phase 3, the voltage drop due to the ESR and the capacitance is changing because the capacitor current decreases. The voltage drop due to R_{CONN} is constant, as it is set by the constant value of R_{CONN} and the maximum load current, I_{STEP}. There is an initial discharge of the capacitor at the end of Phase 2 which is the initial condition for Phase 3, determined by

$$\Delta V_Phase2 = \frac{1}{C_{OUT}} \int_{t_1}^{t_2} \frac{I_{STEP}}{T_{STEP}} \bullet t \, dt + \frac{1}{Cout}$$

$$\int_{t_2}^{t_3} I_{STEP} \, dt = \left(\frac{Istep}{2} \right) \bullet \left(\frac{2 \bullet T_{LOOP} - T_{STEP}}{C_{OUT}} \right)$$

$$\Delta V_{OUT} = \left(\frac{I_{STEP}}{2}\right) \bullet \left(\frac{2 \bullet T_{LOOP} - T_{STEP}}{C_{OUT}}\right) +$$

$$\frac{1}{C_{OUT}} \int_{t_3}^{t_4} iC_{OUT(t)}dt + iC_{OUT(t)} \bullet ESR +$$

$$I_{STEP} \bullet R_{CONN}$$

Which yields

$$\Delta V_{OUT} = \left(\frac{I_{STEP}}{C_{OUT}}\right) \bullet$$

$$\left(t - \frac{T_{STEP}}{2} + T_{LOOP} - \frac{t^2}{2 \bullet T_{LOUT}}\right) +$$

$$I_{STEP} \bullet \left(EST - \frac{ESR \bullet t}{T_{LOUT}} R_{CONN}\right)$$

T_{LOUT} is defined as the time it takes for the inductor current to equal the change in load current, I_{STEP}.

$$T_{LOUT} = \left(\frac{I_{STEP}}{(V_{IN} - V_{OUT})}\right) \bullet L_{OUT}$$

Phase 4, T_{CHARGE}, is the time when the inductor current overshoots to reach the programmed short circuit current limit in order to replace charge lost by the output capacitor. At the end of phase 4, the output voltage drop settles to

$$\Delta V_{OUT} = I_{STEP} \bullet R_{CONN}$$

The duration of phase 4 is determined by

$$I_{Cout} = C_{OUT} \bullet \frac{dv}{dt}$$ which yields a time of

$$T_{CHARGE} = \frac{C_{OUT} \bullet \Delta V_Phase3}{(I_{SC} - I_{MAX})}$$

where I_{SC} is the programmed short circuit current limit, and ΔV_Phase3 is the voltage at the end of phase 3, determined by

$$\Delta V_Phase3 = \frac{I_{STEP}}{C_{OUT}} \bullet \left(\frac{T_{LOUT}}{2} - \frac{T_{STEP}}{2} + T_{LOOP}\right)$$

Procedure for Determining the Required Output Capacitor(s)

Step 1: Determine the parasitic values of R_{CONN} and L_{CONN}. The following are estimates based on the connector pair used and the printed circuit board.

Resistance per pin ≈ 10mΩ

Resistance per mated pin set ≈ 20mΩ

Resistance of printed circuit board to the connector ≈ 0.2mΩ

Inductance of printed circuit board to the connector ≈ 0.2nH

$$R_{CONN} = \frac{20m\Omega}{11} + 0.2m\Omega = 2.02m\Omega$$

$$L_{CONN} = \frac{4.28nH}{11} + 0.2nH = 0.59nH$$

Step 2: Establish an allowable maximum voltage drop, ΔV_{OUT}, at the output.

Application Note U-156 [3] discusses the use of non-integrating gain which allows a larger voltage deviation during a load transient. Set the minimum load regulation to be V_{NOM} +3% ±1%. Therefore, a -7% voltage deviation is allowed on the output voltage while still meeting a minimum overall voltage of -5%. Voltage ripple is not considered during this transient response as the duty cycle is effectively 100%, and there is no voltage ripple. These limits are illustrated in Figure 6.

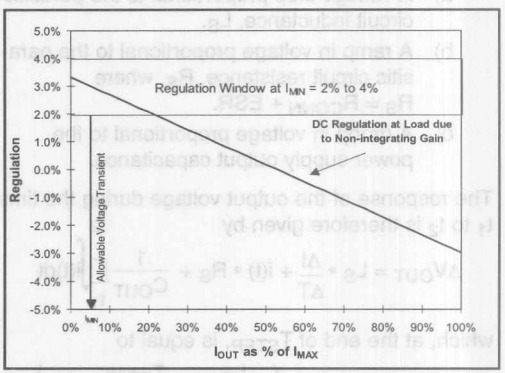


Figure 6. Setting the Regulation and Voltage Transient Requirements

$$\Delta V_{OUT} = 0.07 \bullet 3.1V = 0.217 \text{ volts}$$

Step 3: Estimate the total parasitic inductance, L_S, in order to derive a required value of R_S from the voltage step at the end of Phase 1. Aluminum electrolytic capacitors, size 10mm x 20mm, are estimated to have an ESL of approximately 4.0nH. Size 1206 ceramic chip capacitors are estimated to

have an ESL of approximately 1.9nH [1]. Assume that the combined ESL will be less than 0.51nH, for a total parasitic inductance

$L_S = 1.10nH$

This value must be insured to maintain overall regulation limits during the first phase, T_{STEP}.

Step 4: Equate the voltage deviation at the end of Phase 1 to the allowed voltage step. Assume that the change in voltage due to capacitive discharge is less than 1% of the overall change.

Therefore, the minimum value of C_{OUT} is equal to

$$C_{OUTmin} = \frac{10.9A \bullet 360ns}{2 \bullet 0.217V \bullet 0.01} = 904\mu F$$

Solving for the maximum value of R_S for a step of 11.2A – 0.3A = 10.9A yields,

$$R_S = \frac{(0.217V \bullet 0.99) - \left(10.9A \bullet \frac{1.1nH}{360ns}\right)}{10.9A}$$

$$= 16.6m\Omega$$

Step 5: Equate the voltage deviation at the end of Phase 2 to the allowed voltage step, from which a minimum value of C_{OUT} can be obtained

$$0.217V = \left(\frac{10.9A}{2}\right) \bullet \left(\frac{2 \bullet 5.0\mu s - 360ns}{C_{OUTmin}}\right) + (13.8m\Omega \bullet 10.9A)$$

$$C_{OUTmin} = \frac{\frac{10.9A}{2}(2.5\mu s \bullet 360ns)}{0.217V - (16.6m\Omega \bullet 10.9A)}$$

$$= 1457\mu F$$

Step 6: Choose a capacitor type, manufacturer(s) and values. Determine the number of capacitors required to meet the ESR requirements from Step 4 and the minimum capacitance requirements from Step 5. Add 20% margin for variations in ESR from 20°C down to 10°C (minimum operating temperature).

Radial, high frequency aluminum electrolytic capacitors are chosen based on the height allowed for this power supply VRM as well as their inherently low ESR and ESL. Many manufacturers offer 6.3V low ESR devices rated for 100kHz - 200kHz operation. Sanyo's MV-GX series of aluminum electrolytic capacitors are chosen based on their lower ESR specifications.

ESR Required = $16.6m\Omega \bullet 0.8 = 13.3m\Omega$

Sanyo MV-GX 1500µF, 10mm x 20mm, 6.3V device has a rated maximum ESR of 44mΩ. 4 devices are required, using 400mm² of board area. Sanyo MV-GX 1000µF, 8mm x 20mm, 6.3V device has a rated maximum ESR of 64mΩ. 6 devices are required, using 384mm² of board area. The 1500µF device is chosen to reduce the total parts count. The solution is:

$C_{OUT} = 1500\mu F \bullet 4 = 6000\mu F$

$ESR = 44m\Omega / 4 = 11.0m\Omega$

$ESL \approx 4nH / 4 = 1.0nH$

Step 7: Determine the voltage waveform at the output given this solution of output capacitors.

The current in the capacitor, during a transient, ramps up (or down) in a time determined by the output inductor. The output inductor, during a transient load step, is approximately 26µH.

$$T_{LOUT} = \left(\frac{I_{STEP}}{(V_{IN} - V_{OUT})}\right) \bullet L_{OUT}$$

$$= \left(\frac{10.9A}{(5.0V - 3.1V)}\right) \bullet 26\mu H = 149\mu s$$

The capacitor current is defined as

$$iC_{OUTt} = I_{STEP} - \frac{I_{STEP}}{T_{LOUT}} \bullet t$$

The voltage drop at the output of the power supply, during Phase 3 (T_{LOUT}) of the load transition, is determined by

$$\Delta V_{OUT} = \frac{I_{STEP}}{C_{OUT}} \bullet \left(t - \frac{T_{STEP}}{2} + T_{LOOP} - \frac{t^2}{2 \bullet T_{LOUT}}\right) + I_{STEP} \bullet \left(ESR - \frac{ESR \bullet t}{T_{LOUT}} + R_{CONN}\right)$$

The entire voltage response is plotted in Figure 7. Ceramic and tantalum capacitors (C11, C12, C29) are added in parallel to the aluminum output capacitors to reduce the overall ESL to less than the required

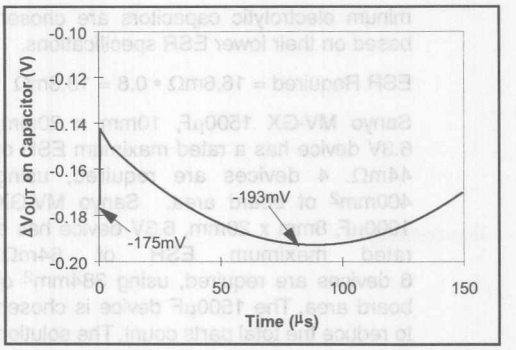


Figure 7. Voltage Droop on Power Supply Output during Load Transient

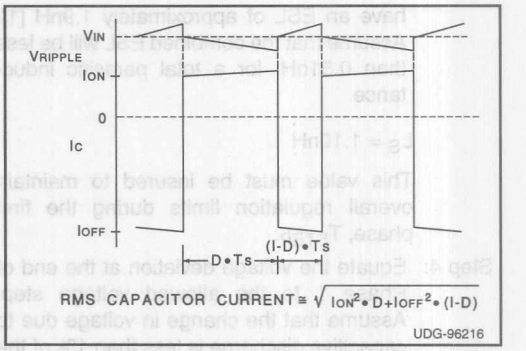


Figure 8. Input Capacitor(s) Current Waveform

0.51nH and to reduce high frequency noise to meet the ripple requirement of ≤2% peak-to-peak.

Input Capacitors: C01-C05

SANYO - 6MV1500GX - 3 in Parallel

C = 1500µF

Form Factor = 10 x 20mm, Radial

ESR = 0.044Ω

ESL ≈ 4nH (Estimated)

Ripple Current Rating = 1.25A @ 105°C, 100kHz

The input capacitance for a Buck regulator is chosen based on several criteria:

a) Ripple Current Handling at F_{SWITCH}
b) Ripple voltage at F_{SWITCH}
c) Maintaining Input voltage during load transients

The resulting solution must present a very low impedance to the input supply and to the Buck Regulator, resulting in a need for low ESR, large value capacitors.

Ripple Current and Voltage

The input capacitors are chosen primarily based on their switching frequency RMS current handling capability. With just 10's of nanohenries parasitic input inductance the input capacitors must handle virtually all of the 200kHz switching current.

Figure 8 shows the switching waveforms in the input capacitor(s). The average VRM power supply input current is calculated based on the maximum load of the power supply and the efficiency at maximum load.

$$I_{AVG} = \frac{P_{INPUTmax}}{V_{INPUT}} = \frac{I_{Omax} \bullet V_{OUT}}{Efficiency \bullet V_{INPUT}}$$

$$= \frac{11.2A \bullet 3.1V}{0.80 \bullet 5.0V} = 8.68A$$

During the MOSFET ON time, the input capacitors must provide the difference between the load current and the input current. During the MOSFET OFF time, the capacitor current is the complete input average current. Therefore,

$$I_{ON} = I_{Omax} - I_{AVG} = 11.2A - 8.68A = 2.52A$$
$$I_{OFF} = -I_{AVG} = -8.68A$$

The duty cycle at the maximum operating current is approximately 73%, and therefore the RMS current in the capacitors, assuming a rectangular waveform since the current ramp is very small, is given by

$$I_{RMS} = \sqrt{I_{OFF}^2 \bullet (1 - Duty) + I_{ON}^2 \bullet Duty}$$
$$= 5.0\ A_{RMS}$$

Three (3) Sanyo capacitors are chosen to maintain reliable operation while operating at this RMS current level.

Given the current waveform of Figure 8, the input voltage ripple will be proportional to the input capacitance and ESR, as shown in the voltage waveform of Figure 8. Low ESR and high capacitance will keep the ripple voltage low.

C01 and C02 ceramic capacitors are added to filter high frequency noise from the switching power supply from the +5V input power bus.

Filtering V_{INPUT} During Load Transients

During a low-to-high output load transient, the duty cycle goes to 100% until the output inductor current is equal to the load current, and the output inductor limits di/dt of the input current. During a high-to-low output load transient, however, there is no output

inductor limiting the input current rate because the input switch is opened (0% duty cycle). The result is the +5V bulk power supply will continue to source high current into this power supply for some time. Figure 9 illustrates the difference in the circuits between a low-to-high and a high-to-low load transient.

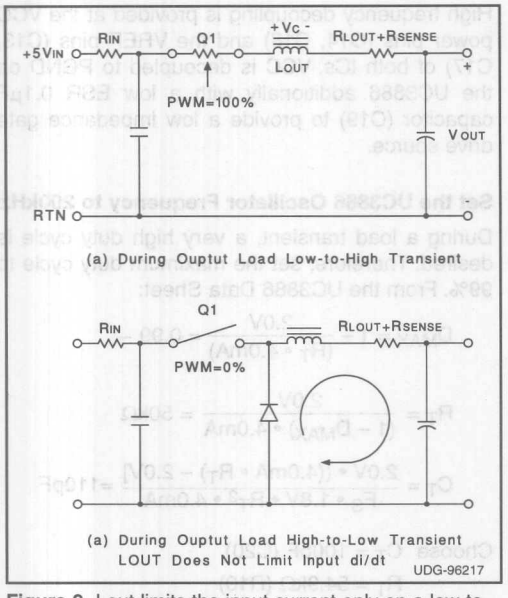


Figure 9. Lout limits the input current only on a low-to-high output current transient

Figure 10 shows typical current waveforms during a high-to-low load transient. The output current abruptly stops but the +5V bulk power supply takes a finite time to react to this change in load current, therefore sourcing energy into the input capacitors. Intel specifies that this input current must not change at a rate faster than 0.1A/µs.

The input capacitor(s) are chosen to limit the voltage surge on the input capacitors to less then 0.15

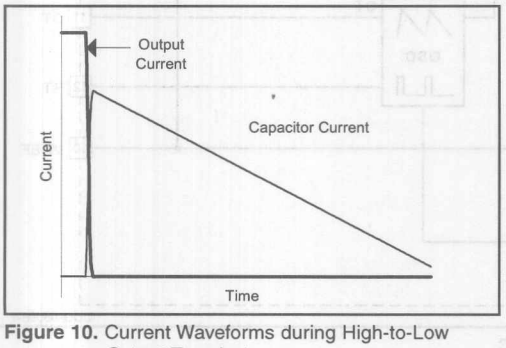


Figure 10. Current Waveforms during High-to-Low Output Transient

volts (3% of V_{IN}) during a high-to-low load transient. The current in the capacitor(s) is defined as

$$iC_{IN(t)} = I_{AVG} - I_{In_Rate} \bullet t$$
$$= 8.68A - (0.1A/\mu s) \bullet t$$

where I_{In_Rate} is defined as the rate at which the input current decays based on the +5V bulk power supply, assumed here to be 0.1A/µs, therefore decaying to 0.0A in 86.8µs.

The voltage surge on the input capacitance during this time is

$$vC_{IN(t)} = \frac{1}{C_{IN}} \int_0^{86.8\mu s} = iC_{IN(t)} + (ESR_{IN} \bullet iC_{IN(t)}) =$$

$$\left(\frac{8.68}{Cin} - (10^5 \bullet ESR)\right) \bullet t - \left(\frac{10^5 \bullet t^2}{2 \bullet C_{IN}}\right) + 8.68 \bullet ESR$$

which is plotted in Figure 11 for 3 Sanyo MV-GX type 1500µF, 0.044Ω Aluminum Electrolytic Capacitors.

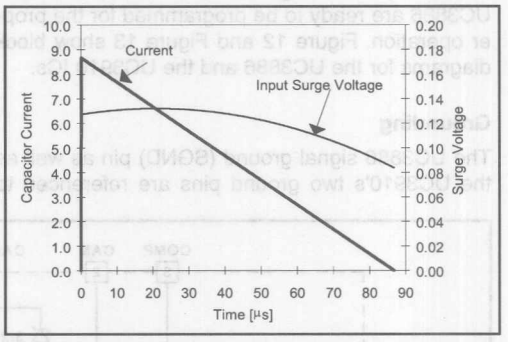


Figure 11. Input Capacitor Current and Surge Voltage During a High-to-Low Load Transient

Sense Resistor: R01

Dale P/N WSR-2 0.01Ω 1%

10mΩ, 2.0 watt 2 wire SMD sense resistor, ±75ppm TCR

The sense resistor is chosen by the criteria discussed in U-156, Appendix 5 [3]. R_{SENSE} is a 2-wire, 2 watt surface mount power product with very low inductance. The 2 watt rating (to ambient temperatures of 75°C) allows for 50% derating at the typical maximum current of 9.9 Amperes [1].

A short circuit current, I_{SC}, is chosen at a nominal 12.5 Amperes, more than 10% over the maximum current. The value of the UC3886 Current Amplifier's gain, G_{CSA}, is bounded to

$$G_{CSA_MIN} = 5.0 \text{ and } G_{CSA_MAX} = 2.5MHz/200kHz$$

I_{SC}

A 12.5A limit implies that Rsense must lie between 0.0064Ω and 0.016Ω. Choose 0.010Ω as the lowest standard value.

The power dissipation in R_{SENSE} during normal and short circuit conditions is

Normal:

$$P_D = I_{AVG}^2 \bullet R_{SENSE} = 9.9^2 \bullet 0.010\Omega$$

$$= 0.98 \text{ Watt} = 49\% \text{ of rated}$$

Short Circuit:

$$P_D = I_{SC}^2 \bullet R_{SENSE} = 12.5^2 \bullet 0.010\Omega$$

$$= 1.56 \text{ Watt} = 78\% \text{ of rated}$$

CONFIGURING THE UC3910 4-BIT DAC AND VOLTAGE MONITOR AND THE UC3886 AVERAGE CURRENT MODE PWM CONTROLLER

With the power stage chosen, the UC3910 and UC3886 are ready to be programmed for the proper operation. Figure 12 and Figure 13 show block diagrams for the UC3886 and the UC3910 ICs.

Grounding

The UC3886 signal ground (SGND) pin as well as the UC3910's two ground pins are referenced to is referenced to the input voltage return path, as discussed in U-156 [4], for best gate drive performance.

Decoupling

High frequency decoupling is provided at the VCC power pins (C14, C18) and the VREF pins (C13, C17) of both ICs. VCC is decoupled to PGND on the UC3886 additionally with a low ESR 0.1μF capacitor (C19) to provide a low impedance gate drive source.

Set the UC3886 Oscillator Frequency to 200kHz

During a load transient, a very high duty cycle is desired. Therefore, set the maximum duty cycle to 99%. From the UC3886 Data Sheet:

$$D_{MAX} = 1 - \frac{2.0V}{(R_T \bullet 4.0mA)} = 0.99 \rightarrow$$

$$R_T = \frac{2.0V}{(1 - D_{MAX}) \bullet 4.0mA} = 50k\Omega$$

$$C_T = \frac{2.0V \bullet ((4.0mA \bullet R_T) - 2.0V]}{F_S \bullet 1.8V \bullet R_T^2 \bullet 4.0mA} = 110pF$$

Choose C_T = 100pF (C20)

R_T = 54.9kΩ (R10)

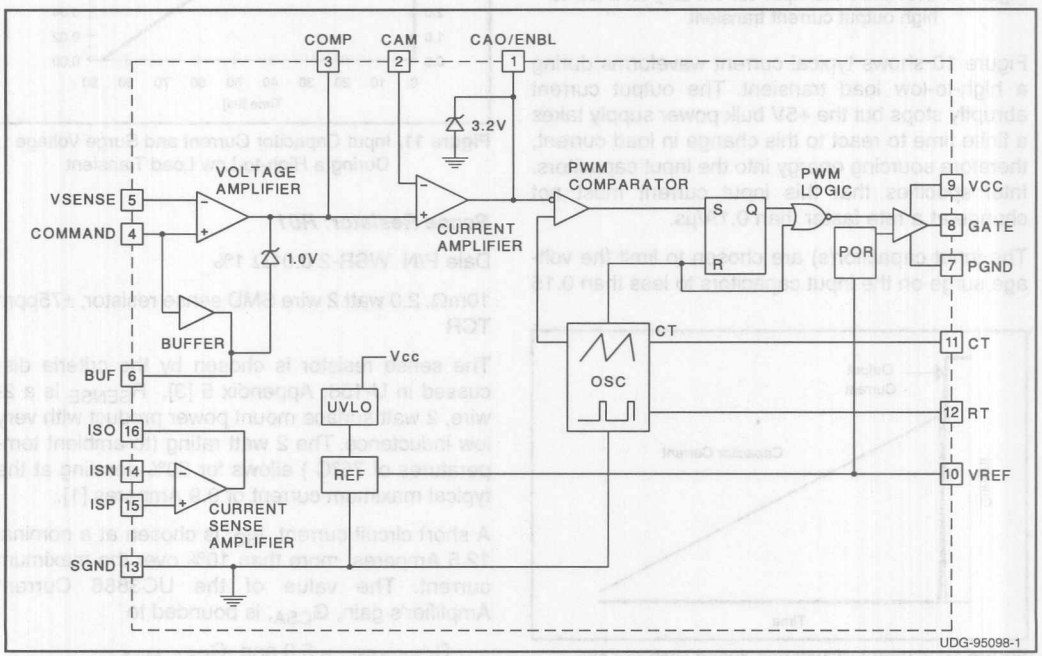


Figure 12. UC3886 Average Current Mode PWM Control IC

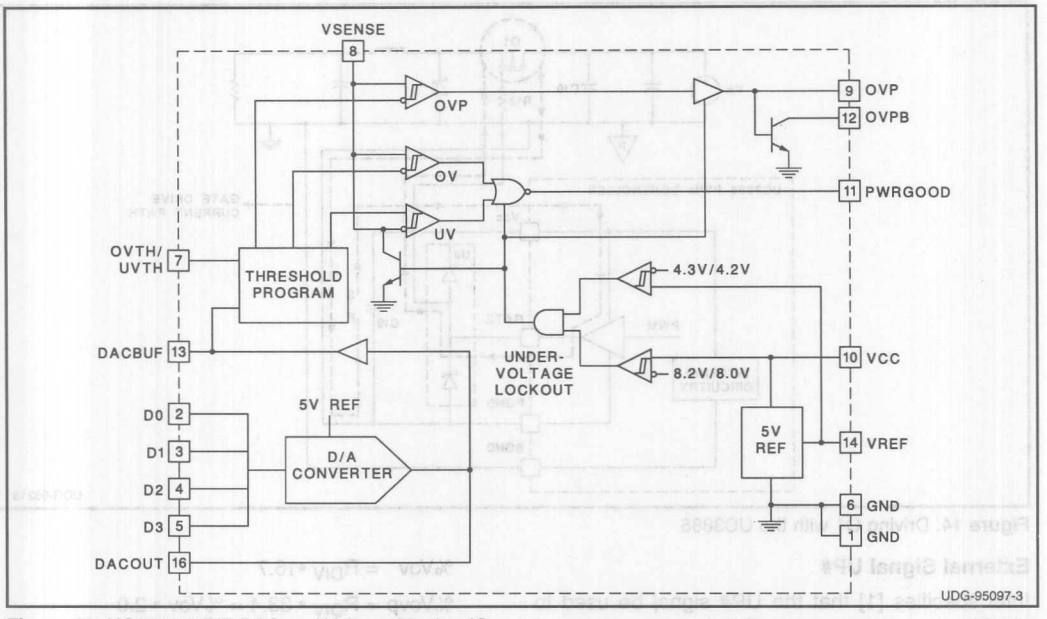


Figure 13. UC3910 4-BIT DAC and Voltage Monitor IC

Note that internal capacitance on the UC3886 CT pin adds approximately 10 to 15pF of capacitance. When using a capacitor as low as 100pF, a substantial frequency shift can result.

A 24Ω resistor and Test Point 1 (R11 and TP1) are provided to allow external synchronization of the unit from a narrow synchronizing pulse [3]. This resistor is not required unless external synchronization is desired.

Driving the MOSFET Gate from the UC3886 Gate Drive Output

A 10mΩ gate drive resistor (R12) is placed close to the MOSFET gate. The 10mΩ resistor limits the peak current and provides damping at the MOSFET gate to prevent oscillations. The power dissipation in this resistor is approximately 1.0mW based on an average current of 10mA.

Figure 14 shows that the current path for a gate drive signal originates from C19, a low decoupling capacitor located closely to the UC3886 GATE pin. C10 is added from the input voltage to the Power Ground (PGND) to decouple the high frequency current spike which exits the MOSFET from the DRAIN and must find a path back to PGND. C10 should be located as closely as possible to the MOSFET to prevent high frequency ringing at the MOSFET.

U3, the UC3612 dual schottky diode, is added to protect the UC3886 from inductive spikes above V_{CC} and below ground which may occur due to high gate drive spikes and parasitic inductance.

External Enable Signal

Intel specifies [1] that the Pentium®Pro power supply be enabled by an open collector, active high signal, OUTEN.

The UC3886 CAO/ENBL is connected to the input of the UC3886 PWM comparator (Figure 12), with the other side of the comparator attached to the oscillator ramp. The oscillator ramp is nominally a 1.0V to 2.8V peak ramp signal. The UC3886 gate drive is disabled by bringing the CAO/ENBL signal to a level below the oscillator ramp signal.

The external OUTEN signal is connected to the UC3886 CAO/ENBL signal through a 1.0kΩ resistor, R2. A 1.0kΩ resistor is recommended to provide a high impedance buffer between external noise and the output of the UC3886 Current Amplifier Output, to insure noise does not couple into the control loop. The CAO/ENBL pin may source up to 400μA. Using a 1.0kΩ resistor will result in a 400mV drop. A reasonable open collector output stage will be able to sink 400μA and maintain a saturation voltage less than 400mV, keeping the LOW level voltage at CAO/ENBL to less than 800mV.

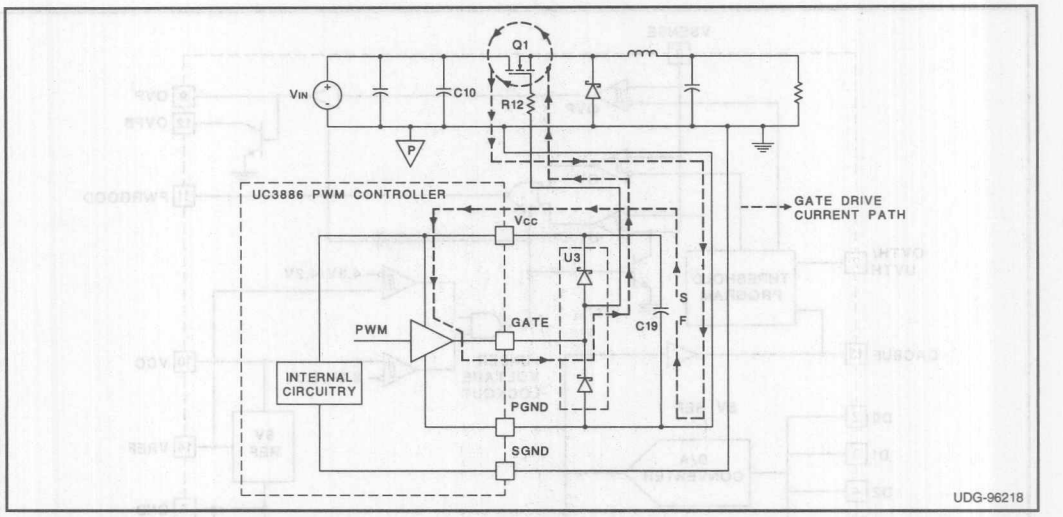


Figure 14. Driving Q1 with the UC3886

External Signal UP#

Intel specifies [1] that the UP# signal be used to disable the power supply if it is not capable of supporting an upgraded processor, either by varying the voltage or by supporting the higher load currents. The UP# signal is also an open collector signal, normally high, but pulled low when an Upgrade Processor is in place. By inserting a 0Ω jumper resistor for R25, the power supply will be disabled in the case of an upgrade processor.

> THE UNITRODE DEMONSTRATION KIT IS SHIPPED WITHOUT R25. UPGRADE PROCESSORS MAY EXCEED THE 12.5A CURRENT LIMIT OF THE DEMONSTRATION KIT. INSERT A 0Ω 0603 SMD JUMPER RESISTOR FOR R25 TO DISABLE THE POWER SUPPLY IN AN UPGRADE PROCESSOR APPLICATION

CONFIGURING THE UC3910 VOLTAGE MONITORING AND PROTECTION FEATURES

The regulation requirements for this power supply are set at ±5%. The PWRGD requirement is set to signal a voltage regulation failure when the output voltage is outside of the range of ±10%. The UC3910 Undervoltage and Overvoltage (UV, OV) thresholds are therefore chosen at midrange to be nominally ±7.5%.

The equations for setting the Voltage Monitoring thresholds (see U-158 [7]) are

$$\%V_{UV} = -\left(R_{DIV} \bullet \frac{3.34k\Omega}{20k\Omega}\right) \bullet 100 = -(R_{DIV} \bullet 16.7)$$

$$\%Vov = R_{DIV} \bullet 16.7$$

$$\%Vovp = R_{DIV} \bullet 33.4 = \%Vov \bullet 2.0$$

Setting $\%V_{UV}$ and $\%V_{OV}$ to ±7.55 yields a divider ratio R_{DIV} of 0.45.

R8 and R9 act as a voltage divider between the UC3910's DACBUF pin and OVTH/UVTH pin. R8 and R9 are chosen to draw approximately 1.0mA.

$$R8 = 1.69k\Omega,\ R9 = 1.34k\Omega,\ R_{DIV} = 0.448$$

The nominal thresholds are

Overvoltage Threshold = +7.48%

Undervoltage Threshold = –7.48%

Overvoltage Protection Threshold = +14.96%

PWRGD Signal:

Intel requires [1] the PWRGD signal to be an open collector active HIGH signal when the voltage is within specification. R7 is a 4.7kΩ resistor which can be added internally to the demonstration kit power supply for evaluation purposes. See the schematic of Figure 2.

> R7 IS NOT INSTALLED ON UNITRODE'S DEMONSTRATION KIT. USE A 4.7kΩ 1/10W 0603 SMD RESISTOR IF INTERNAL PULLUP IS DESIRED.

Overvoltage Protection:

The UC3910 provides both OVP and OVPB pins for protection in the case of overvoltage. OVP is capable of driving an SCR to perform a crowbar func-

tion. OVPB is an open collector, active low signal which is designed to pull down on the UC3886 CAO/ENBL signal to disable the UC3886 gate drive.

The Overvoltage Protection circuit consists of F1, SCR1, CR2, R05 and R06. Fuse F1 serves to protect the circuit under two circumstances: a MOSFET short circuit failure and when the crowbar SCR is fired. The fuse is chosen based on the maximum operating power and efficiency.

$$P_{OUTmax} = 3.4 \text{ Volts} \bullet 11.2 \text{ Amps} = 38 \text{ Watts}$$

$$I_{INmax} = \frac{38 \text{ Watts}}{0.80 \bullet 5.0V} = 9.5 \text{ Amperes}$$

A 10 Ampere SMD fuse is chosen.

Characterizing SCR's for Crowbar Applications is discussed extensively in Motorola's Thyristor Device Data book [5]. SCR1 is chosen based on its low gate trigger current, its On-State RMS current rating, and because it has to discharge a substantial amount of low ESR aluminum capacitors, its Peak Non-repetitive surge current rating.

SCR1 by itself will not protect the Pentium®Pro processor against an overvoltage except by causing the fuse F1 to open, which can take a substantial amount of time. CR2 provides an additional path to discharge the output capacitors directly in order to clamp the output voltage and protect the processor immediately. CR2 is connected before the sense resistor, R1, in order to use R1 as a current limiting resistor when the crowbar is fired. CR2 has a rated surge current of 200 Amperes.

Connecting an SCR as a crowbar to the output voltage may appear to be the best way to protect the Pentium®Pro processor in the case of an overvoltage failure. However, the UC3886 provides a current limiting mechanism, which would cause the SCR to sink the programmed current limit. An input fuse would not open under these circumstances because of the low output power being delivered. The SCR on the output would most likely fail thermally and open, thus defeating the protection mechanism.

Resistor R6 from the SCR gate to ground is chosen to protect the SCR against false firing due to dv/dt conditions. R6 will draw approximately 15mA when the SCR is fired, as the gate voltage is approximately 1.5 volts. R5 is chosen to limit the current from the UC3910 while insuring that the SCR gate trigger current is sufficient down to 10°C. The UC3910 will source at least 65mA when activated. R5 limits the current preventing excessive droop on VCC when the SCR is fired.

The open collector signal OVPB is also triggered during an overvoltage protection fault. This signal can be used to disable the UC3886 gate drive by connecting it directly to the UC3886 CAO/ENBL signal. R26 is installed in Unitrode's demonstration kit as a "jumper" only, to enable or disable this feature. Normal applications will directly connect the UC3886 CAO/ENBL pin to the UC3910 OVPB pin. Note that the OVPB signal is an open collector signal and therefore may be "OR';d" with the external open collector OUTEN and UP# signals.

Setting the RC Filters at VSENSE and DACOUT of the UC3910

The UC3910 VSENSE pin requires an R-C filter to isolate the pin from the power supply output [6]. The resistor acts both as part of an R-C filter and to limit the current into the VSENSE pin. During UVLO of the UC3910, VSENSE is actively pulled low in order to prevent false overvoltage protection signals.

The filter resistor R3 is chosen to limit the input current to ≤500µA under the maximum programmable voltage for the Pentium®Pro.

$$R3 \quad \frac{3.4V}{500\mu A} = 6.8k\Omega$$

The filter capacitor C16 is chosen to set the filter corner frequency at approximately $F_{SWITCH}/10$ in order to reduce the switching frequency ripple by 20dB.

$$C16 = \frac{1}{R3 \bullet 2 \bullet \pi \bullet (200kHz/10)} = 1170pF$$

Use R3 = 6.8kΩ

C16 = 1200pF as standard values

The filter capacitor at the output of DACOUT, C15, is chosen to insure that DACOUT rises at a faster rate than VSENSE. This prevents false OVP signals during V_{CC} brownout or glitch conditions.

$$R3 \bullet C16 > 3k\Omega \bullet C15 \rightarrow$$

$$C15 \leq \frac{R3 \bullet C16}{3k\Omega} \quad 2720pF$$

Use C15 = 2700pF as a standard value

Note that resistor R4 connected to the UC3910 VSENSE pin is used for debug purposes only and is not required for normal operation.

Programming the Current Limit with the Current Sense Amplifier of the UC3886

A nominal current limit of 12.5 Amperes is desired to protect the power supply under short circuit con-

in the freewheeling diode under short circuit conditions.

The gain of the current sense amplifier, G_{CSA}, is set based on the desired current limit and the value of the sense resistor [4], using:

$$G_{CSA} \bullet R_{SENSE} = \frac{1.0\ Volt}{I_{SC}} \rightarrow$$

$$G_{CSA} = \frac{1.0\ Volt}{12.5A \bullet 0.01\Omega} = 8.0$$

The current sense amplifier is configured as a differential amplifier using four external resistors, R18, R19, R20 and R21, with the gain equal to

$$G_{CSA} = 8.0 = \frac{R20}{R18} = \frac{R21}{R19}$$

R20 and R21 should not load down the UC3886 Current Sense Amplifier, and are chosen as 33.2kΩ. Therefore

Use R20 = R21 = 33.2kΩ
R18 = R19 = 4.22kΩ resulting in
G_{CSA} = 7.87 and a nominal short circuit current limit, I_{SC}, of 12.7 Amperes.

The BUF signal at pin 6 of the UC3886 must be filtered by C22 to insure a noise free bias voltage for the current sense signal ISO.

Programming the Non-Integrating Gain for the Voltage Amplifier of the UC3886

Managing the voltage regulation at the load, and maintaining regulation of ±5% involves the use of non-integrating gain about the UC3886 voltage amplifier. Without non-integrating gain, the number of output capacitors must increase. Application note U-156 [4], Appendix 3, details the goals and requirements for programming non-integrating gain.

The specified regulation window is ±5%. V_{RIPPLE} and DC Error, which are each ±1%, reserve ±2% of the specified window. This leaves ±3% of the window for load regulation. The desired regulation performance, versus load current, is shown in Figure 15. Setting the low load regulation to +3% nominally will allow the maximum voltage excursion during a load transient.

The UC3886 error voltage, COMP, will vary with load current from 0.0A to I_{SC} = 12.7A. The change in the error voltage will be

$$\Delta Ve = \frac{I_{MAX}}{I_{SC}} \bullet 0.95V = \frac{11.2\ Amps}{12.7\ Amps} \bullet 0.95V$$
$$= 0.834\ Volts$$

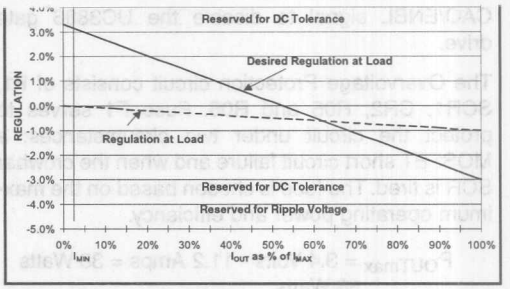


Figure 15. Load Regulation

A change in COMP of 0.95 volts is used because the change is 1.0V ±50mV, and under worst case the regulation window must be held.

Figure 15 shows that the load regulation due to parasitic resistances is –1% from no load to maximum load. From the desired load regulation curve, the swing in output voltage associated with the change from 0 Amps (Not I_{MIN} in this case) to I_{MAX} is determined to be –6.3%. The I • R drop intrinsic to the circuit is then subtracted and the desired regulation swing is set at –5.3%. From the lowest operating voltage, the change in the output voltage is

$$\Delta V_{OUT} = 2.4\ V \bullet 5.3\% = 0.127\ Volts$$

The gain around the Voltage Amplifier determined by the ratio of R16 to R14 is chosen to achieve the desired voltage swing over the operating load range.

$$\Delta V_{OUT} = \frac{\Delta V_E}{Gain} = \frac{\Delta V_E}{R16/R14} \text{ and}$$

$$\text{therefore } R16/R14 = \frac{0.88V}{0.127V} = 6.57$$

The feedback resistor is chosen very large to insure that there are no loading effects on the voltage amplifier output.

Use R16 = 100kΩ
R14 = 15kΩ resulting in the gain about the Voltage Amplifier of 6.67.

Non-Integrating gain has a negative regulation slope with regards to load current, and must be shifted up in order to swing ±3% about the nominal voltage. A DC offset is created by the resistive divider of R14 and R17 which shifts the regulation window up by +3.1%. R17 is chosen by

$$(V_{NOM} + 3\%) \bullet \frac{R17}{R14 + R17} = V_{NOM}$$

and therefore

$$\frac{R17}{R14 + R17} = \frac{1}{1.03}$$ yielding R17 = 487kΩ.

Filtering and Canceling Offset Current at the Command Pin of the UC3886

It is recommended that the decoupling capacitor, C21 be placed very close to the COMMAND pin of the UC3886, as this voltage is the voltage which commands the power supply output, and noise will directly couple to the power supply output. R13 is added in series between the UC3910 DACOUT pin and the UC3886 COMMAND pin in order to minimize DC errors due to offset currents in the UC3886 voltage amplifier. R13 is chosen to match the impedance at the V_{SENSE} input to the UC3886 voltage amplifier. Remember that the UC3910 DACOUT pin has an internal 3kΩ resistor. Therefore

$$R13 = \frac{1}{\frac{1}{R16} + \frac{1}{R14} + \frac{1}{R17}} - R_{DAC} =$$

$$= \frac{1}{\frac{1}{100k\Omega} + \frac{1}{15k\Omega} + \frac{1}{487k\Omega}} - 3k\Omega = 9.7k\Omega$$

Use R13 = 10kΩ

CLOSING THE LOOP WITH THE UC3886 AVERAGE CURRENT MODE PWM CONTROLLER

The basis for closing the Average Current and the Voltage loops of this circuit is found in Unitrode Application Note U-140 [2] and in the Unitrode Seminar Topic "Switching Power Supply Control Loop Design" [7]. This application note presents a step-by-step methodology solving for the loop compensation components found in Figure 2. The current loop is completed first with the voltage loop to follow.

The goal in closing the loops for this power supply is to obtain a stable closed loop response for the current and voltage loops, with an overall closed loop crossover frequency between 10kHz and

$$\frac{F_S}{2\pi} = 32kHz.$$

Closing the Current Loop

Step 1: Calculate the Oscillator Ramp as seen at the PWM Comparator input. From U-140, it is known that "The amplified inductor current downslope at one input of the PWM comparator must not exceed the oscillator ramp slope at the other comparator input".

From the oscillator timing equations, the ramp slope is

$$T_S = \frac{1}{F_S} = 5.0\mu s$$

$T_D \approx 50ns$ (Deadtime of oscillator)

Ramp = 2.8V – 1.0V = 1.8Vp-p

$$\text{Ramp Slope} = \frac{\text{Ramp}}{T_S - T_D} = \frac{1.8V}{4.95\mu s}$$

= 0.364 Volts/μs

Step 2: Calculate the inductor current downslope. The downslope occurs during the Buck regulator switch OFF time.

The inductor downslope is maximum at the maximum output voltage and with the minimum output inductance, which occurs at maximum load and maximum output voltage.

The diode forward voltage of CR1 is approximately 0.35V at 11.2A

V_{OUTmax} = 3.4V

L_{OUT} at the maximum operating current = 12μH

$$\text{Inductor di/dt} = \frac{3.4V + 0.35V}{12.0\mu H} = 0.313A/\mu s$$

Step 3: Convert the inductor current downslope to a voltage downslope as seen at the output of the Current Sense Amplifier.

$$\text{Inductor dv/dt} = 0.313A/\mu s \bullet 0.01\Omega \bullet \frac{33.2k\Omega}{4.22k\Omega} = 24.6mV/\mu s$$

Step 4: Set the gain from the Current Amplifier to meet the slope criteria. Reduce G_{CAmax} by 25% to account for amplified voltage ripple due to the ESR of the output capacitors. Reduce the gain by 15% more to account for Inductor and Oscillator variations.

The oscillator Ramp Slope = 0.364V/μs ≥ G_{CA} • Inductor dv/dt

where G_{CA} = The gain of the Current Amplifier at the switching frequency

Therefore:

$$G_{CA} \text{ at } F_{SWITCH} = \frac{364mV/ms}{24.6mV/ms} \bullet 0.60 = 8.9$$

Resistors R23 and R24 set the inverting

gain about the UC3886 Current Amplifier. Pick R24 to limit the loading on the Current Amplifier output. Then set R23 and R24 to program the Current Amplifier's inverting gain at F_{SWITCH}.

Use

R24 = 10.5kΩ

R23 = 1.24kΩ

as standard values

$G_{CA} = 8.47$

The GBW product for the UC3886 Current Amplifier is 3.5MHz and therefore a gain of 8.47 at 200kHz is within the device's GBW.

Step 5: Find the crossover frequency of the current loop gain by first finding the small signal control-to-output gain, G_P, of the buck regulator current loop power section. Consider the fact that the inductor, L_{OUT}, plays a key role in the equation for G_P, and that since L_{OUT} swings significantly with load current, so does G_P.

The small signal control-to-output gain is defined in U-140 from the CA output, V_{CA}, to the voltage across the sense resistor, V_{RS}. The UC3886 application however must add a gain stage factor for the Current Sense Amplifier gain. G_P is determined by

$$\frac{V_{RS}}{V_{CA}} = \left(\frac{Duty}{V_{CA}}\right) \bullet \left(\frac{V_{RS}}{I_{Lout}}\right) \bullet \left(\frac{I_{Lout}}{Duty}\right) \bullet G_{CSA}$$

$$= G_P$$

The change in duty cycle to change in Current Amplifier output is $100\%/V_S$, or

$$\frac{Duty}{V_{CA}} = \frac{1}{V_S}$$

where

V_S = The peak-to-peak voltage change of the oscillator ramp

The change in the resistor voltage to change in the inductor current is simply the value of the sense resistor, R_S (R_S = R1 in Figure 2).

$$\frac{V_{RS}}{I_{Lout}} = Rs$$

The change in inductor current per the change in duty cycle is a function of the input voltage. The small signal voltage applied at the inductor is simply the small signal changes in V_{IN} • Duty. The change in inductor current per the change in applied inductor voltage (small signal) is given by:

$$\frac{i}{v} = \frac{1}{Z_{OUT}} \text{ where } v = V_{IN} \bullet Duty$$

and therefore $$\frac{I_{Lout}}{Duty \bullet V_{IN}} = \frac{1}{Z_{OUT}}$$

which leads to the transfer function of

$$\frac{I_{Lout}}{Duty} = \frac{V_{IN}}{Z_{OUT}}$$

Z_{OUT} is dominated by the output inductor at frequencies above the L • C resonant frequency, and results in a single pole rolloff due to that inductor, which is what is shown in U-140 as the "$V_{IN/S}$ • L_{OUT}" term. The complete impedance function includes the output Inductor, Capacitor, Sense Resistor, Inductor Resistance, ESR, ESL and Load Resistance. The parasitic resistances will help dampen the response at the resonant frequency and should not be ignored.

The output impedance is given by:

$$Z_{OUT} = s \bullet L_{OUT} + R_S + RLout + \frac{\left(\frac{1}{s \bullet C} + ESR + s \bullet ESL\right) \bullet RL}{\left(\frac{1}{s \bullet C} + ESR + s \bullet ESL\right) + RL}$$

where

R_{Lout} = DC Resistance of output inductor

C = Output capacitance

ESR = Output capacitance ESR

ESL = Output capacitance ESL

R_L = Load Resistance

Now, solving for the control-to-output gain, G_P (of the Current Loop only),

$$G_p = \left(\frac{Duty}{V_{CA}}\right) \bullet \left(\frac{V_{RS}}{I_{Lout}}\right) \bullet \left(\frac{I_{Lout}}{Duty}\right) \bullet GCSA$$

can be simplified as

$$G_P = \left(\frac{1}{V_A}\right) \bullet (R_{SENSE}) \bullet \left(\frac{V_{IN}}{Z_{OUT}}\right) \bullet G_{CSA}$$

U-140 states to multiply the control-to-output power loop gain, Gp, by the gain of the Current Amplifier to achieve the overall current loop gain.

$$\text{Loop} = G_P \bullet G_{CA} = \left[\left(\frac{1}{V_S}\right) \bullet \left(\frac{V_{IN}}{Z_{OUT}}\right) \bullet (R_S) \bullet G_{CSA}\right] \bullet \left[\frac{V_S \bullet L_{OUT}}{(T_S - T_D) \bullet R_S \bullet (V_O + V_F) \bullet G_{CSA}}\right]$$

Equating the current loop gain to 1 will yield the loop crossover frequency, F_C.

$$1 = \left[\left(\frac{1}{V_S}\right) \bullet \left(\frac{V_{IN}}{Z(2 \bullet \pi \bullet F_C)}\right) \bullet (R_S) \bullet G_{CSA}\right] \bullet \left[\frac{V_S \bullet L_{OUT}}{(T_S - T_D) \bullet R \bullet (V_O + V_F) \bullet G_{CSA}}\right]$$

Z_{OUT} is dominated by the output inductor in the region of the crossover frequency, and therefore $Z_{OUT(fc)}$ can be replaced by $s \bullet L_{OUT}$

Solving for F_C and simplifying yields:

$$F_C = \frac{V_{IN}}{2 \bullet \pi \bullet (V_O + V_F) \bullet (T_S - T_D)}$$

Notice that L_{OUT} falls out of the equation, and therefore the only "Load" dependency is in the value of Vf. This is true ONLY if Lout is Constant with load current. If a swinging choke is used, then Lout cannot drop out of the equation.

The crossover frequency of the current loop can therefore be determined by

$$\frac{V_{IN} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet F_C \bullet L_{OUT}} \bullet G_{CSA} \bullet G_{CA} = 1$$

and therefore

$$F_C = \frac{V_{IN} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet L_{OUT}} \bullet G_{CSA} \bullet G_{CA}$$

The crossover frequency of the current loop will therefore vary as a function of load, with the minimum crossover frequency at the maximum input voltage and maximum value of L_{OUT}, or at minimum load.

Solving for the crossover frequency:

$$F_{Cmax} = \frac{V_{Imax} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet L_{OUTmin}} \bullet G_{CSA} \bullet G_{CA}$$

$$= \frac{5.25V \bullet 0.01\Omega}{1.8V \bullet 2 \bullet \pi \bullet 120mH} \bullet 7.87 \bullet 8.47$$

$$= 25\ .8kHz$$

$$F_{Cmin} = \frac{V_{Imin} \bullet R_S}{V_S \bullet 2 \bullet \pi \bullet L_{OUTmax}} \bullet G_{CSA} \bullet G_{CA}$$

$$= \frac{4.75V \bullet 0.01\Omega}{1.8V \bullet 2 \bullet \pi \bullet 24.0\mu H} \bullet 7.87 \bullet 8.47$$

$$= 11.7kHz$$

where the input voltage is +5V ±5%

Step 6: Add the pole-zero compensation into the Current Amplifier by solving for C_{ZERO} (C25 + C28) and C_{POLE} (C27), and solve for the current loop transfer function.

The zero should be placed at or below the minimum current loop crossover frequency, F_{Cmin}. The value of C_{ZERO} is determined by

$$Czero = \frac{1}{2 \bullet \pi \bullet F_{Cmin} \bullet R24}$$

$$= \frac{1}{2 \bullet \pi \bullet 11.7kHz \bullet 10.5k\Omega}$$

$$= 1296pF$$

Use C_{ZERO} = C25 + C28 = 1220pF (2 capacitors are used to allow tuning of this frequency)

The pole should be placed at $F_S/2$. The value of C_{POLE} is determined by

$$C_{POLE} = \frac{C_{ZERO}}{(2 \bullet \pi \bullet F_S/2 \bullet R24 \bullet C_{ZERO}) - 1}$$

$$= \frac{1220pF}{(2 \bullet \pi \bullet = 200kHz/2 \bullet 10.5k\Omega \bullet 1220pF) - 1}$$

$$= 173pF$$

Use C_{POLE} = C27 = 180pF

$$G_{CAs} = \frac{R24 \bullet (C_{POLE} + C_{ZERO}) \bullet s + 1}{s \bullet (C_{ZERO} \bullet R23 \bullet (R24 \bullet s \bullet C_{POLE} + 1)}$$

and the overall current loop is determined by multiplying the control-to-output transfer function by the current amplifier transfer function, or

$$Loop = G_P \bullet G_{CAs} = \left(\frac{1}{V_S} \bullet \frac{V_{IN}}{Z_{OUTs}} \bullet R_S \bullet G_{CSA} \right) \bullet G_{CAs}$$

which is plotted in Figure 16.

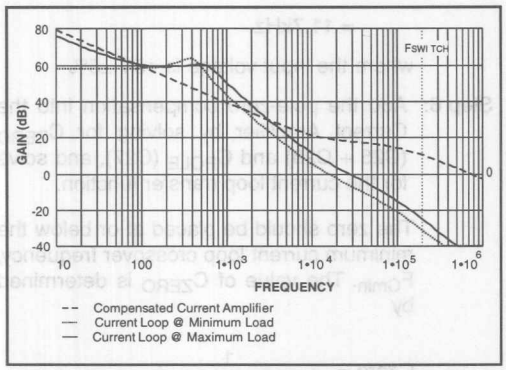


Figure 16. Current Amplifier and Current Loop Bode Plot - Minimum and Maximum Loads

The lower crossover frequency is above the estimated range of 11.7kHz because the gain of the compensated Current Amplifier is not a flat gain of 8.47 but is slightly higher due to the integrating feedback of the Current Amplifier.

The changes in loop gain at low frequencies is dominated by the changes in load resistance, while the variation at and around the crossover frequency is a function of the change in inductance vs current.

Closing the Voltage Loop:

The voltage loop must now be closed according to the guidelines in Unitrode Seminar Topic [7] "Switching Power Supply Control Loop Design". The compensation around the voltage amplifier of this circuit will differ from the seminar topic however by utilizing non-integrating gain [4].

The small signal current loop can be modeled as a fixed gain at low frequencies equal the transconductance forced by the current loop, and having a pole at the current loop crossover frequency, f_{CI}, as shown in Figure 17 below.

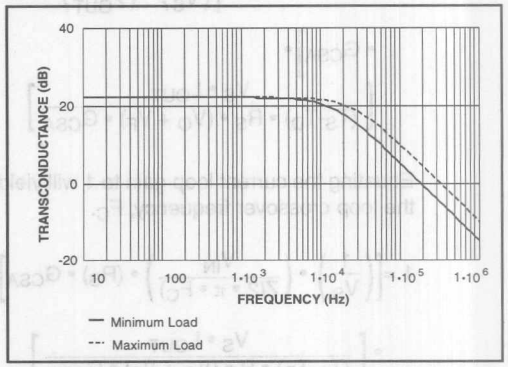


Figure 17. Small Signal Current Loop Transfer Function – Min and Max Loads

where the transconductance, TC(s) is determined by

$$T_{C(s)} = \frac{1}{R_S \bullet G_{CSA}} \bullet \left(\frac{1}{1 + \frac{s}{2 \bullet \pi \bullet f_{CL}}} \right)$$

The low frequency gain is the transconductance (remember, transconductance units is Ω^{-1})

$$Gain = \frac{1}{R_S \bullet G_{CSA}} = \frac{1}{0.01\Omega \bullet 7.87} = \frac{22.1dB}{\Omega}$$

Step 8: Determine the output impedance and power circuit gain, G_{Vs}.

The output impedance is determined by the output capacitance, its parasitics, and the load resistance.

$$Z_{Vout(s)} = \frac{\left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL \right) \bullet R_{LOAD}}{\left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL \right) + R_{LOAD}}$$

The power circuit gain equals the current loop transconductance times the output impedance, or

$$G_{Vs} = T_{C(s)} \bullet Z_{Vout(s)}$$

Step 9: Determine the gain required by the compensated voltage amplifier. Insure that gain at the switching frequency does not increase the PWM slope above the required amount due to ESR.

The resistors R14 and R16 around the voltage amplifier were determined by the requirements for non-integrating gain and are

$R14 = 15.0k\Omega$

$R16 = 100k\Omega$

The inductor current di/dt rate is known to be a maximum of 0.313A/µs. This inductor current ramp times the ESR of the output capacitor is multiplied by the gain of the voltage and current amplifiers and is seen at the PWM Comparator. The total contribution of ESR ripple contributed to the ramp at the PWM comparator is the limiting factor for the gain of the voltage amplifier, G_{VA}. Step 4 reduced G_{CAmax} by 25% to account for this factor. The gain of the Current Amplifier at the switching frequency, from Figure 16, is 3.3.

Therefore, from Step 4, and with an equivalent ESR of the output capacitors being 11.0mΩ

$$0.313A/\mu s \bullet ESR \bullet (1+G_{CA(Fs)}) \bullet G_{VAmax(Fs)} = 0.25 \bullet 0364V/\mu s$$

and therefore

$$G_{VAmax(Fs)} \frac{0.25 \bullet 0364V/\mu s}{0.313A/\mu s \bullet 0.011 \bullet (1 + 3.3)}$$

$$= 6.15$$

Since R16 and R14 set an inverting gain of 100kΩ/15kΩ = 6.67, then the voltage amplifier gain must be rolled off (add a pole) prior to the switching frequency to reduce the gain to less than $G_{VAmax(Fs)}$.

Step 10: Compensate the Voltage Amplifier to achieve desired loop gain and phase and to reduce the voltage amplifier gain at the switching frequency to below $G_{VAmax(Fs)}$.

The voltage loop gain is obtained by multiplying the power circuit gain, G_{Vs} by the Voltage Amplifier gain, G_{VAs}.

$$LoopV_S = G_{VAs} \bullet G_{Vs} = G_{VAs} \bullet T_{C(s)} \bullet \frac{\left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL\right) \bullet R_{LOAD}}{\left(\frac{1}{s \bullet C_{OUT}} + ESR + s \bullet ESL\right) + R_{LOAD}}$$

The voltage amplifier gain, without compensation, is simply R16/R14 = 6.67. The voltage loop gain is plotted in Figure 18, showing a very low crossover frequency.

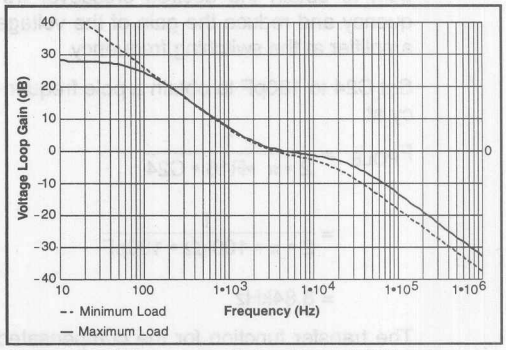


Figure 18. Voltage Loop Gain without Additional Voltage Amplifier Compensation

The voltage amplifier gain is compensated by adding a low frequency pole-zero pair in order to boost low frequency gain. Note however, that DC gain cannot be increased as it is limited by the requirements of non-integrating gain. Secondly, a high frequency pole is added to achieve the desired crossover frequency and to reduce the gain of the voltage amplifier beyond the crossover frequency.

Add C23 and R15 to add a low frequency pole-zero pair in order to boost low frequency (but NOT DC) gain, and therefore boost the crossover frequency. Set the zero at approximately 100Hz and the pole at approximately 400Hz.

The equations for the pole and zero are

$$F_{POLE} = \frac{1}{2 \bullet \pi \bullet C23 \bullet R15} \text{ and}$$

$$F_{ZERO} = \frac{1}{2 \bullet \pi \bullet C23 \bullet (R15 + R14)}$$

Set C23 to 0.1µF. Then

$$R15 = \frac{1}{2 \bullet \pi \bullet C23 \bullet F_{POLE}}$$

$$= \frac{1}{2 \bullet \pi \bullet 0.01\mu F \bullet 400} = 3.98k\Omega$$

Use R15 = 3.92kΩ as a standard value. The results are:

F_{POLE} = 406Hz
F_{ZERO} = 84Hz

Add C24 to add another pole to roll off the gain to obtain the desired crossover frequency and reduce the gain of the voltage amplifier at the switching frequency.

Set C24 to 180pF to obtain a pole frequency at

$$F_{POLE} = \frac{1}{2 \bullet \pi \bullet R16 \bullet C24}$$

$$= \frac{1}{2 \bullet \pi \bullet 100k\Omega \bullet 180pF}$$

$$= 8.84kHz$$

The transfer function for the compensated voltage amplifier is

$$GVA(s) = \frac{R16}{R14} \bullet \frac{s \bullet C23 \bullet (R14 + R15) + 1}{(s \bullet R16 \bullet C24 + 1) \bullet (s \bullet R15 \bullet C23 + 1)}$$

With this compensation, the voltage amplifier gain and the loop response for the Voltage Loop are plotted in Figure 19.

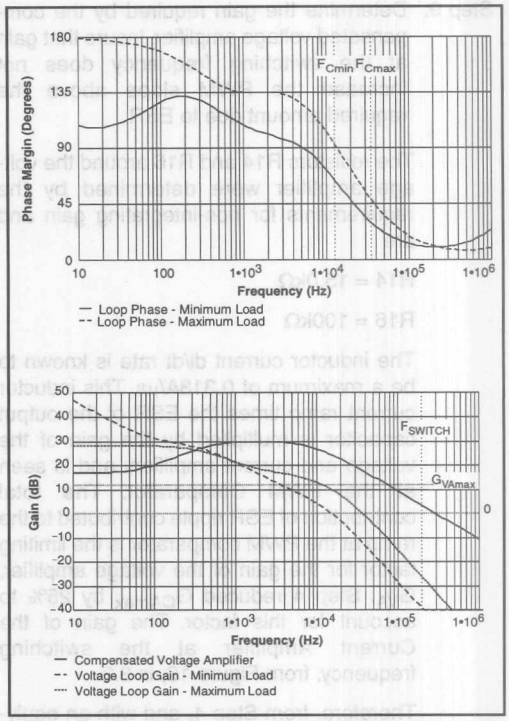


Figure 19. Final Voltage Loop Gain and Phase Plots

MEASURED RESULTS FROM THE VRM DEMONSTRATION KIT

Figure 20 provides the measured open loop response bode plots for the VRM power supply under a nominal 3.1V output at I_{Omax} = 11.2 Amperes.

Figure 21 shows the DC regulation measured at the load in a test configuration, with the nominal output voltage set to 3.100V. The measured test configuration DC impedance from the output of the connector to the resistive load is 1.50mΩ, which accounts for 17mV (0.54%) drop at full load. The load regulation curve matches the predicted non-integrating regulation curve.

Figure 22 shows the measured efficiency and power dissipation of the VRM in a test configuration, with the nominal output voltage set to 3.100V. The input voltage is fixed at 5.00V. The test board

COMPONENTS Z1, R22 AND C26 CAN BE USED FOR VARIATIONS IN THE COMPENSATION SCHEME. THE VRM DEMONSTRATION KIT IS SHIPPED WITH Z1=10Ω AND WITHOUT R22 AND C26.

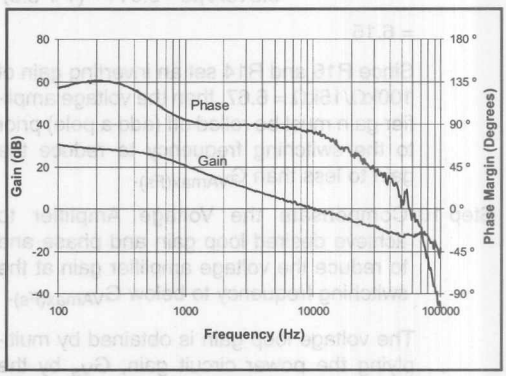


Figure 20. Open Loop Response with V_{OUT} = 3.1V, I_{OUT} = 11.2A

is subjected to 100LFM airflow at approximately 25°C ambient temperature. The full load efficiency is 83.6%.

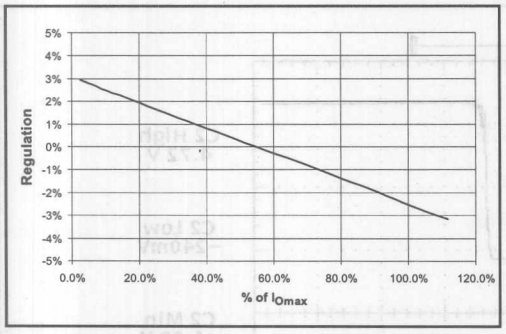


Figure 21. DC Regulation at V_{OUT} = 3.1V for VRM - Measured At Load

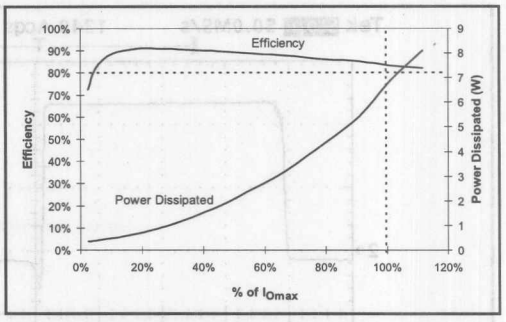


Figure 22. Efficiency and Power Dissipation vs Load for VRM Module with 3.100V nominal Output

The measured efficiency includes the power dissipated by the 12V bias power supply. The +12V current, I_{CC}, is measured to be 25.0mA during normal operation, and is fixed with varying load. With the OUTEN signal disabling the power supply, I_{CC} is measured at 18.5mA, supplying current only for the UC3886 and UC3910, but no gate drive. The average gate drive current is measured at 6.50mA.

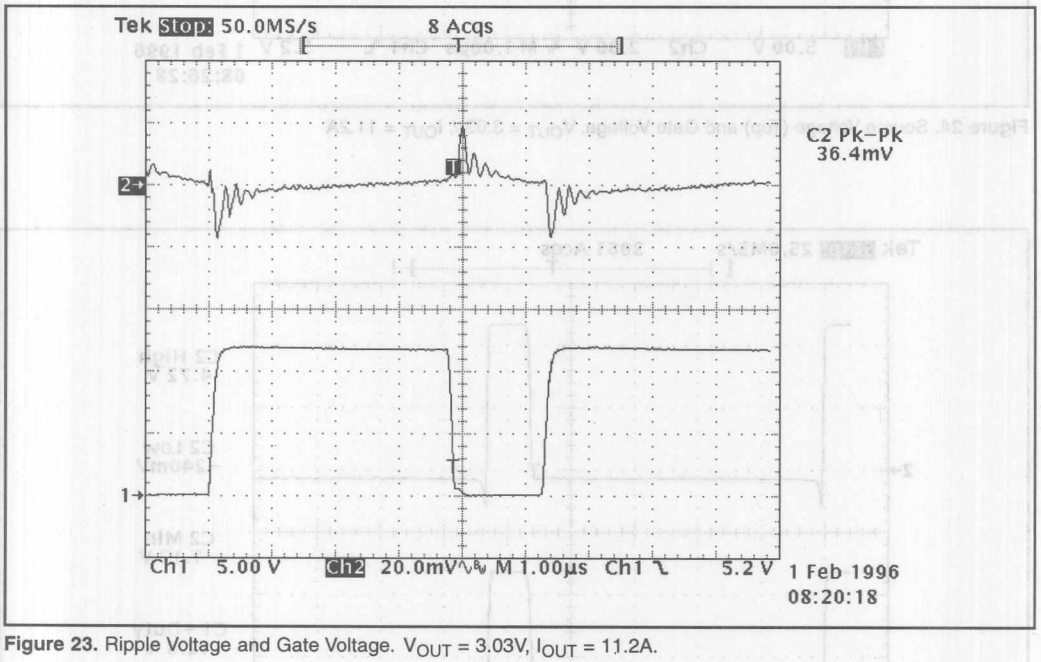


Figure 23. Ripple Voltage and Gate Voltage. V_{OUT} = 3.03V, I_{OUT} = 11.2A.

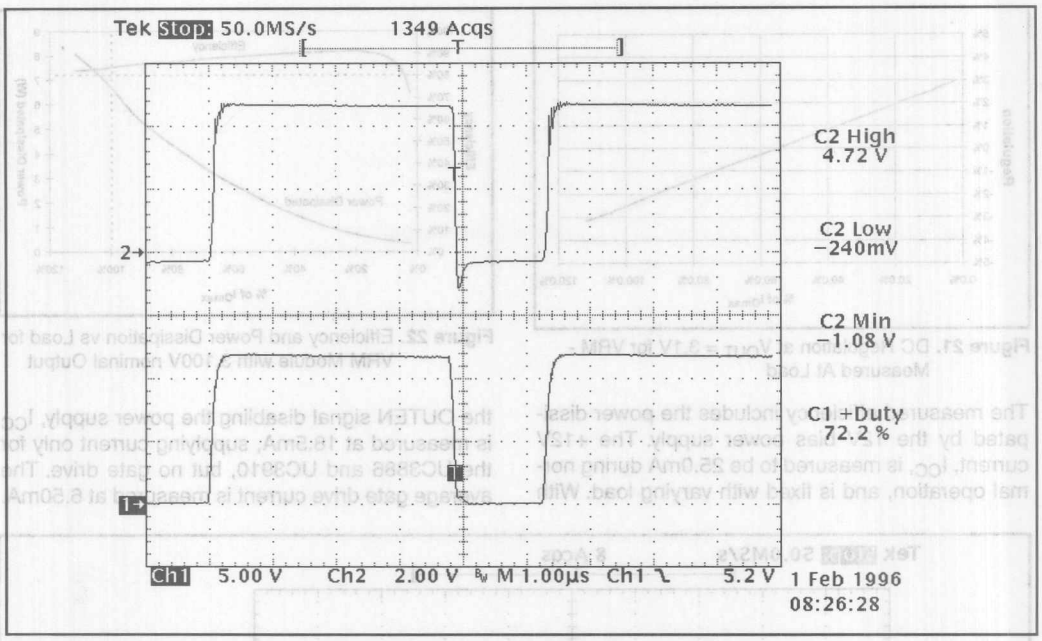


Figure 24. Source Voltage (Top) and Gate Voltage. V_{OUT} = 3.03V, I_{OUT} = 11.2A

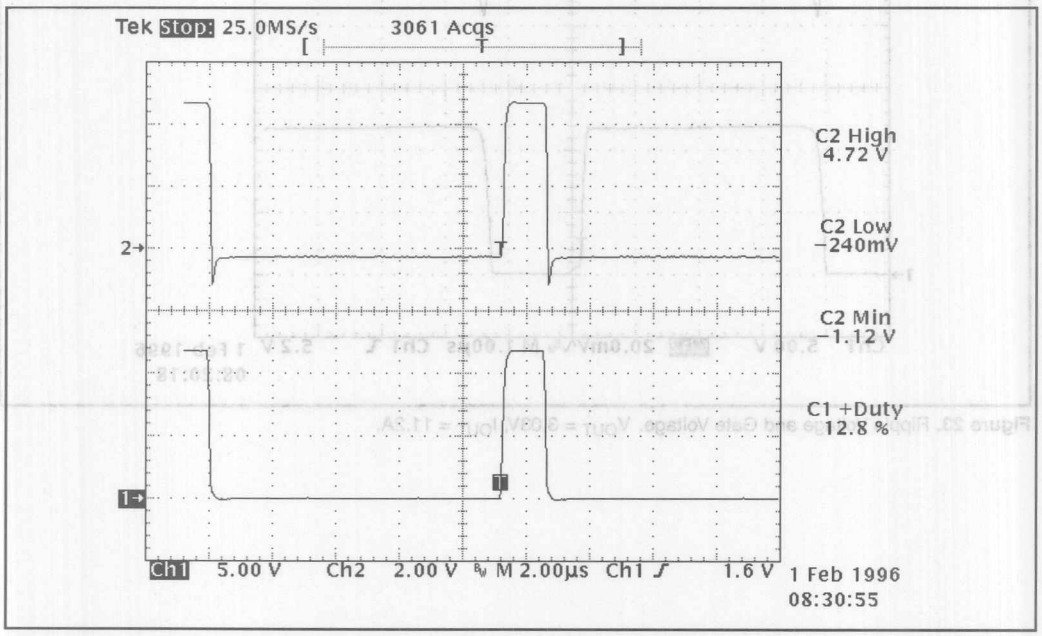


Figure 25. Short Circuit Source Voltage (Top) and Gate Voltage. V_{OUT} = 0.06V. The UC3886 skips cycles to maintain an accurate current limit.

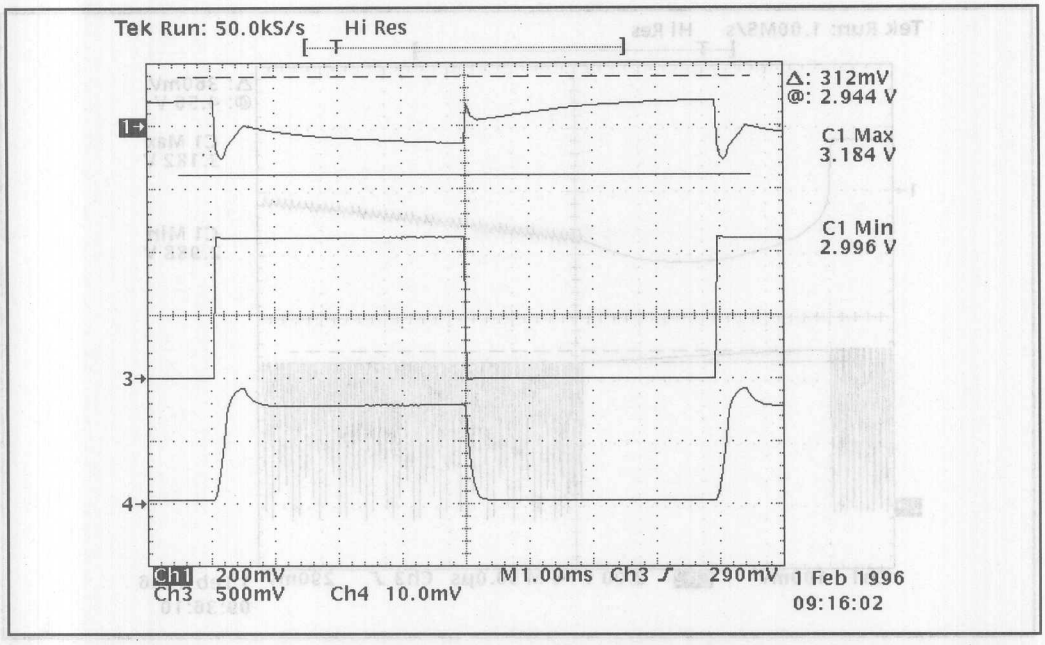


Figure 26. Transient Response to 125Hz, 0.3A to 11.2A to 0.3A Load Change. V_{OUT} (Top) centered about 3.10V, between ±5% cursors. Load current (Middle) @ 2A/div varies at 30A/µs. Input current (Bottom) @ 5A/div. overshoots to charge input and output caps after a load step.

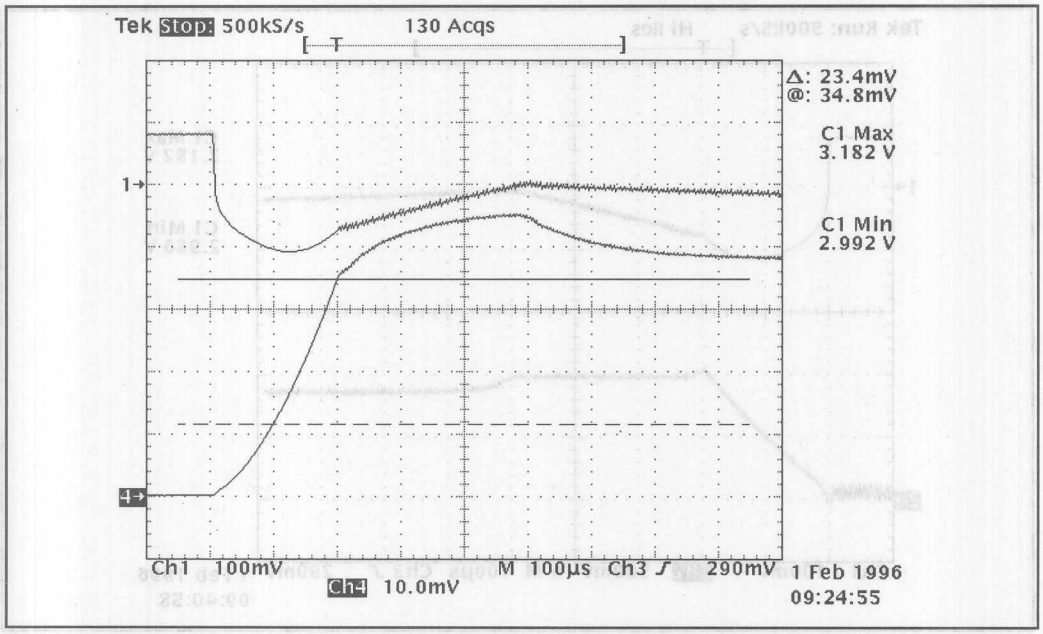


Figure 27. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 0.3A to 11.2A transient. Input current (Bottom, 2A/div) rises at 0.047A/µs during the load step.

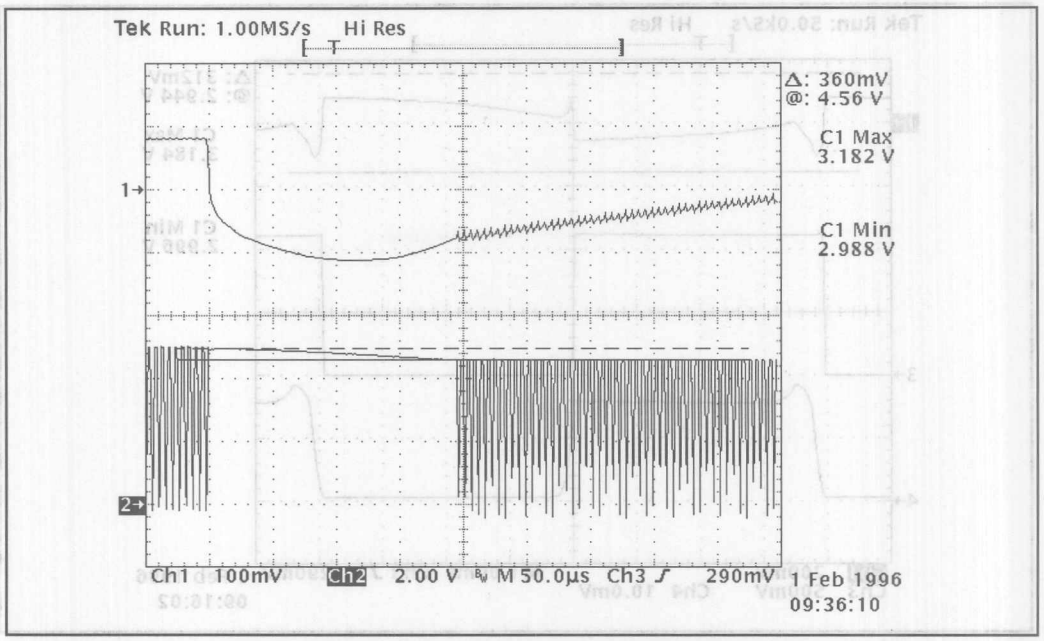


Figure 28. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 0.3A to 11.2A transient. Q1 Source (Bottom) shows 100% duty cycle as inductor current ramps to full load current. Slope in Source is due to Q1 R_{DSon}.

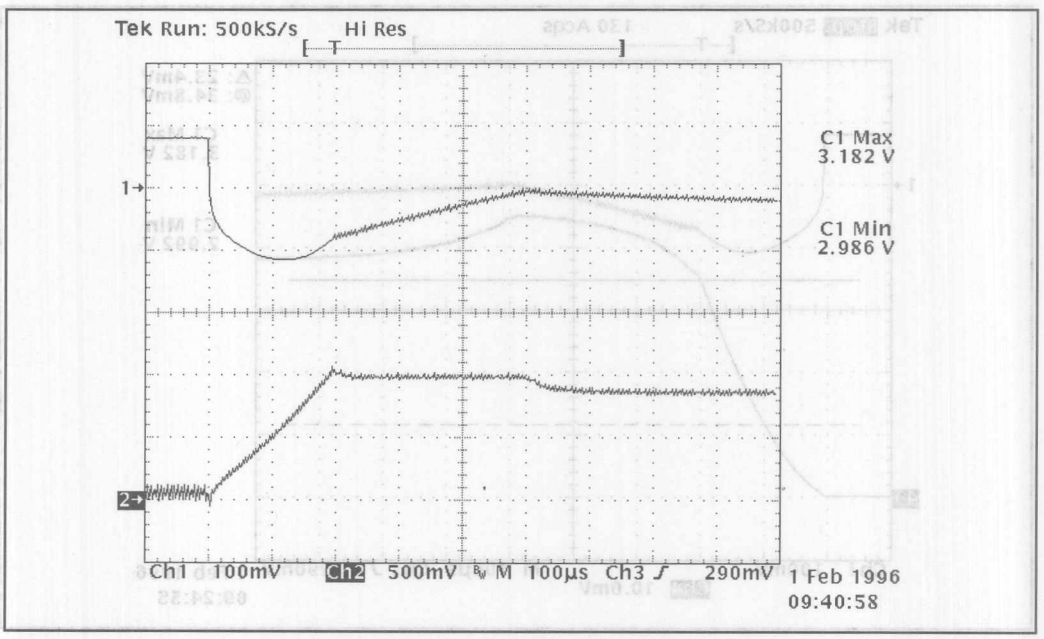


Figure 29. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 0.3A to 11.2A transient. ISO, UC3886 Pin 16 (Bottom) swings from 3.10V (Marker 2) to 4.10V at a measured 12.6A short circuit current. The output inductor is calculated to be 27µH during this swing due to high AC Flux.

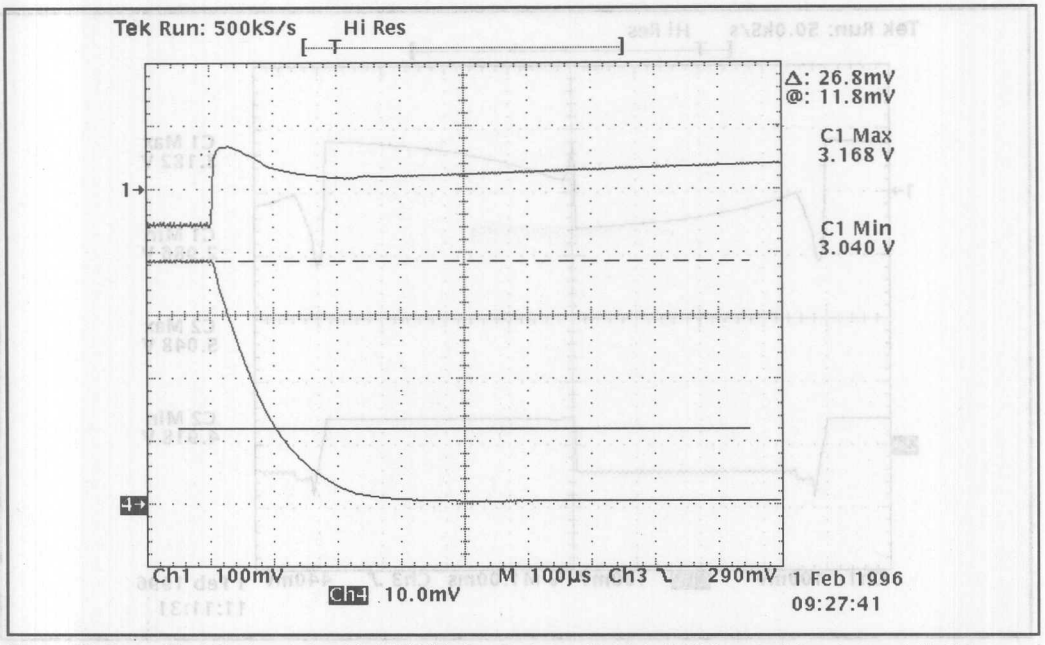


Figure 30. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 11.2A to 0.3A transient. Input current (Bottom, 2A/div) falls at 0.054A/µs during the load step.

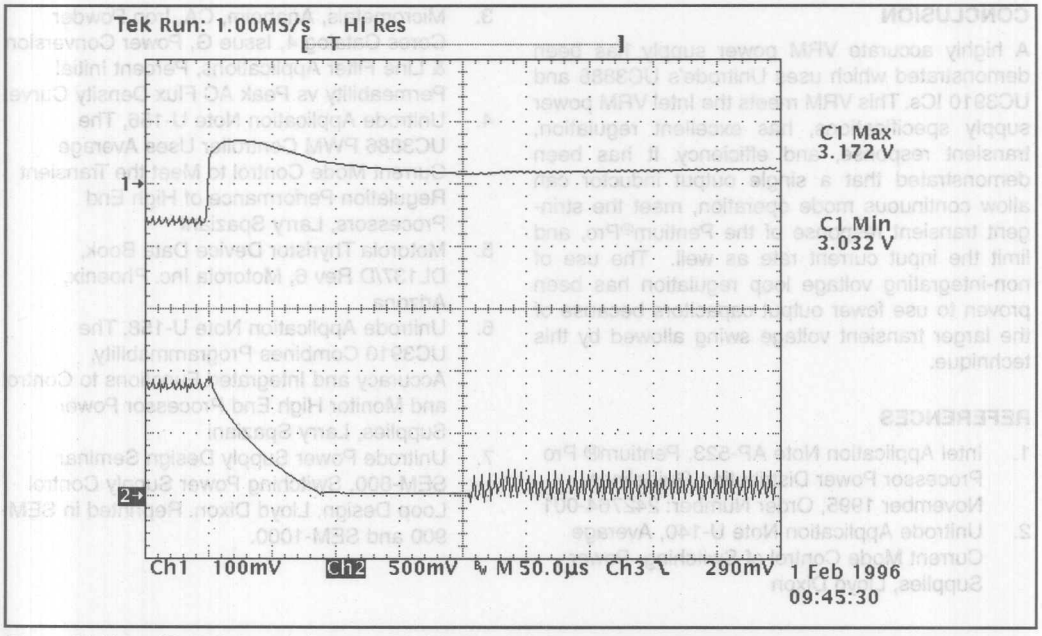


Figure 31. V_{OUT} (Top) Centered about 3.100V (Marker 1) during 11.2A to 0.3A transient. ISO, UC3886 Pin 16 (Bottom) swings from 4.00V (Marker 2) to 3.10V. The output inductor is calculated to be 28uH during this swing due to high AC Flux.

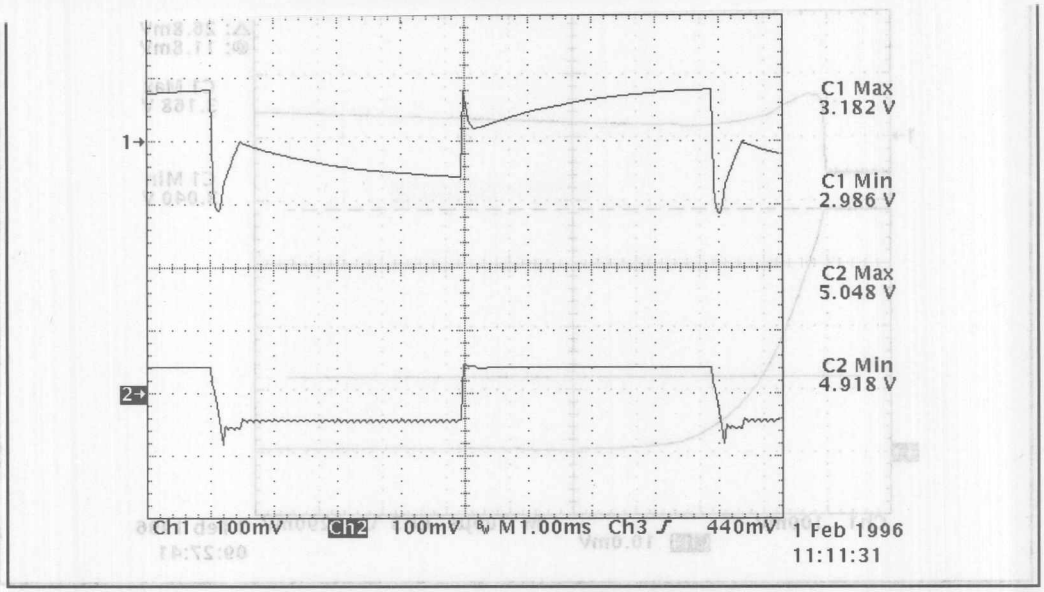


Figure 32. Transient Response to 125Hz, 0.3A to 11.2A to 0.3A Load Change. V_{OUT} (Top) centered about 3.10V. Input voltage (Bottom) shows only 130mV deviation during load steps without input inductor, due to low impedance VRM input capacitors.

CONCLUSION

A highly accurate VRM power supply has been demonstrated which uses Unitrode's UC3886 and UC3910 ICs. This VRM meets the Intel VRM power supply specifications, has excellent regulation, transient response, and efficiency. It has been demonstrated that a single output inductor can allow continuous mode operation, meet the stringent transient response of the Pentium®Pro, and limit the input current rate as well. The use of non-integrating voltage loop regulation has been proven to use fewer output capacitors because of the larger transient voltage swing allowed by this technique.

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2. Unitrode Application Note U-140, Average Current Mode Control of Switching Power Supplies, Lloyd Dixon
3. Micrometals, Anaheim, CA, Iron Powder Cores Catalog 4, Issue G, Power Conversion & Line Filter Applications, Percent Initial Permeability vs Peak AC Flux Density Curve.
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5. Motorola Thyristor Device Data Book, DL137/D Rev 6, Motorola Inc. Phoenix, Arizona
6. Unitrode Application Note U-158, The UC3910 Combines Programmability, Accuracy and Integrated Functions to Control and Monitor High End Processor Power Supplies, Larry Spaziani
7. Unitrode Power Supply Design Seminar SEM-800, Switching Power Supply Control Loop Design, Lloyd Dixon. Reprinted in SEM-900 and SEM-1000.

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THE UC3910 COMBINES PROGRAMMABILITY, ACCURACY AND INTEGRATED FUNCTIONS TO CONTROL AND MONITOR HIGH END PROCESSOR POWER SUPPLIES

by Larry Spaziani

ABSTRACT

As high performance processors continue to develop, their respective power supply requirements become more stringent, often requiring low, custom voltages and increasingly tighter regulation. Intel's Pentium®Pro power system specification, for instance, demonstrates the need for tight regulation, programmable power supply voltage and programmable voltage monitoring for status reporting to the processor. To help meet these requirements, the UC3910 4-BIT DAC and Voltage Monitor IC is introduced. This application note discusses the architecture and features of the UC3910 and details how this IC is used for an optimal Pentium®Pro power supply solution.

UC3910 4-BIT DAC AND VOLTAGE MONITOR

- High Precision Reference for tight regulation
  0.5% Typical combined DAC/Reference precision
- 4-BIT DAC directly compatible with Intel's Pentium®Pro VID function
  Sixteen steps from 2.0V to 3.5V in 100mV increments
- Undervoltage and Overvoltage Fault Windows
  User programmed with 2 external resistors
  Proportional to DAC programmed voltage over the entire operating range
- Overvoltage Protection Comparator
  Proportional to DAC programmed voltage over the entire operating range
  Directly drives an external SCR
- Undervoltage Lockout

INTRODUCTION

The UC3910 4-BIT DAC and Voltage Monitor IC contains a 4-BIT Digital to Analog converter which is used to program a precise DC voltage for use in commanding a power supply voltage. The actual power supply voltage is compared against user programmable thresholds, with the comparators providing logic status to the system or protecting the power supply with a crowbar SCR. This IC has been developed to interface with Intel's Pentium® Pro processor, but has widespread uses where precise control and monitoring of a power supply voltage is required.

The high DC accuracy of the UC3910 reference and DAC, typically ±0.5%, makes this IC ideal for controlling and monitoring tightly regulated power supplies, such as high end processors or bus termination voltages. Tight regulation of power supplies can be met without adjusting the power supply voltage at manufacturing. The programmable output can also be used to digitally adjust a power supply voltage in test or manufacturing, allowing a single power supply design to accommodate multiple uses.

The UC3910 offers substantial advantages over discrete solutions when meeting Intel's Pentium®Pro power supply requirements. Its 4-BIT Digital-to-Analog Converter output voltage varies from 2.0V to 3.5V in 100mV increments for direct

compatibility with Intel's VID codes. The many integrated features and the programmability of the UC3910 allow power supply designers to replace discrete components including a precision reference, a DAC, complicated resistive networks, multiple window comparators and an SCR Driver. Tight regulation can be met directly because of the excellent DC accuracy of the UC3910 combined DAC and reference voltages.

THE UC3910 4-BIT DAC AND VOLTAGE MONITOR

A block diagram of the UC3910 is shown in e 1.

The UC3910 is ideally suited to create a programmable, precision system reference for low voltage power supplies. Figure 2 shows the UC3910 configured with the UC3886 Average Current Mode PWM Controller IC to provide a solution for the

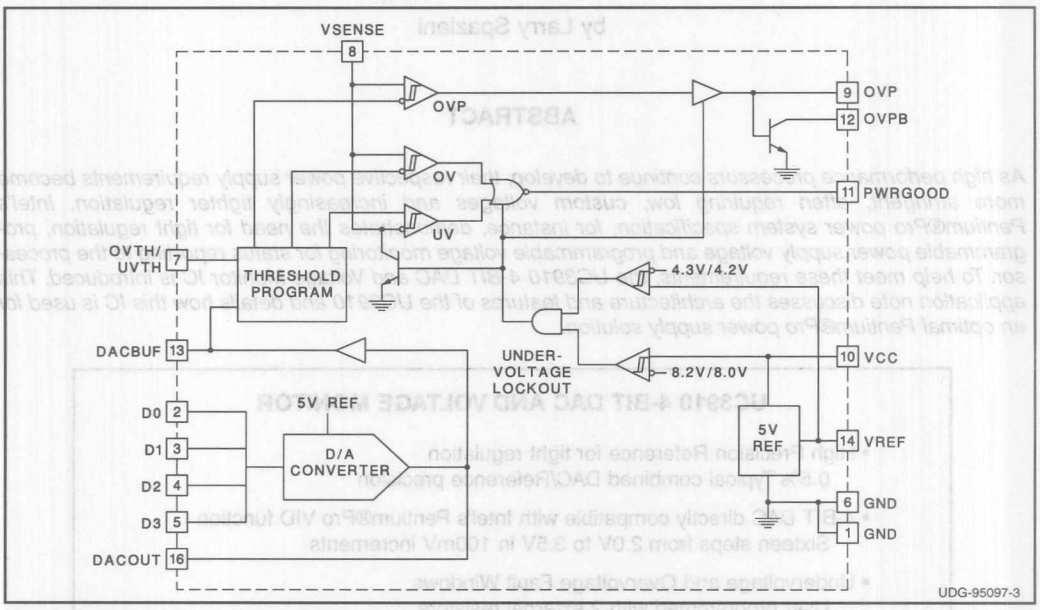


Figure 1. UC3910 4-BIT DAC and Voltage Monitor

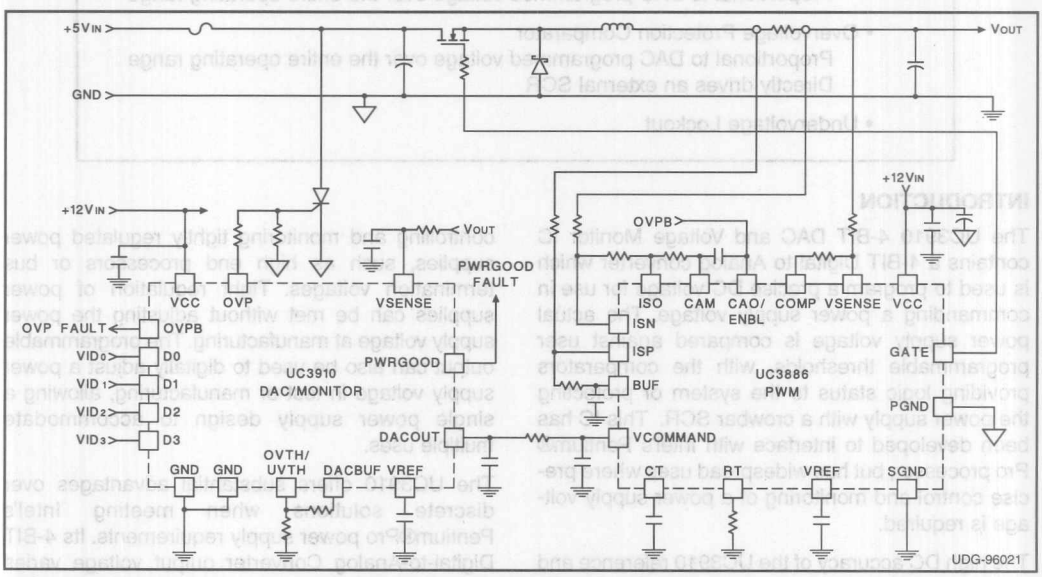


Figure 2. UC3910 Configured with the UC3886 for a Pentium®Pro DC/DC Converter

complex power system requirements of Intel's Pentium®Pro processor. The UC3910 is directly compatible with Intel's Voltage Identification (VID) code as shown in Figure 2.

UC3910 - SUPPLYING POWER

The UC3910 is constructed using a bipolar process allowing the input supply voltage, V_{CC}, to be as high as 20V. Minimum operating voltage is 8.2 volts. The supply voltage provides internal biasing of all circuit blocks including the high precision reference voltage, V_{REF}, which provides a precision reference voltage for the Digital to Analog Converter (DAC). VCC should be decoupled to ground with a 0.1µF to 1.0µF ceramic capacitor located in close proximity to the IC.

Grounding the UC3910

The UC3910 utilizes two ground pins to optimize the layout of the high precision DAC and Reference circuitry. Both ground pins must be connected to ground close to the IC and to each other.

UNDERVOLTAGE LOCKOUT

The UC3910 features an undervoltage lockout protection circuit for controlled operation during power up and power down sequences. Figure 3 shows typical V_{CC} thresholds of the UC3910 UVLO circuitry.

The supply current, I_{CC}, is typically less than 3mA during UVLO and is typically less than 10mA when V_{CC} is above the UVLO thresholds. External loading of the reference voltage will add to the supply current, I_{CC}. The 0.2V hysteresis prevents V_{CC} oscillations during the power up and power down sequences.

During UVLO, V_{REF} and the DAC output, DACOUT, are disabled, the threshold circuitry is disabled and the sense pin, VSENSE, is actively held low. The PWRGOOD signal is actively held LOW, the OVPB signal is forced HIGH (open) and the OVP signal's drive is disabled to insure no false control signals are generated during power up and power down sequencing.

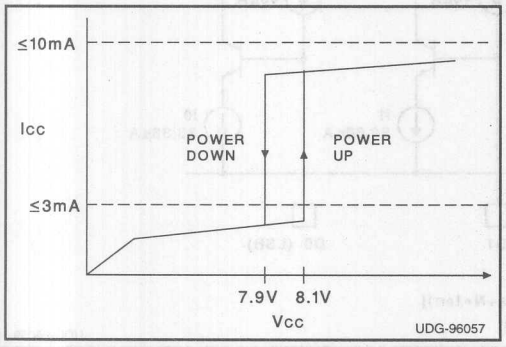


Figure 3. UC3910 UVLO Typical Values

VREF

The UC3910 contains a 5.0V precision trimmed bandgap reference, based on similar technology as that used on many other Unitrode ICs, but is enhanced by the use of precision thin film resistors. Thin film resistors exhibit excellent performance with voltage and temperature variations, and don't shift in value due to packaging stresses. These enhancements result in a reference voltage tolerance of ±0.5% from 0°C to 70°C. V_{REF} provides bias directly to the DAC circuitry, and plays a major role in the precision of the DAC output.

The reference can be used to bias external circuitry, can source up to 10mA and has internal short circuit protection. VREF should be decoupled with a 0.1µF to 1.0µF monolithic ceramic capacitor located close to the IC. Load circuits with high noise content should be avoided, or decoupled very well, as noise on V_{REF} will directly couple to the DACOUT pin.

VREF COMPARATOR

The reference voltage is internally monitored as shown in Figure 4. The 0.1V hysteresis prevents V_{REF} oscillations during the V_{REF} power up and power down sequences. While the reference voltage is below the V_{REF} threshold, VSENSE, PWRGOOD, OVP and OVPB are disabled in the same manner as they are during undervoltage lockout.

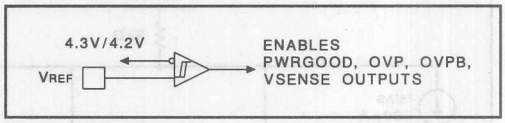


Figure 4. UC3910 V_{REF} Comparator

A typical power up sequence is shown in Figure 5. The voltage monitoring outputs are not enabled until time t_1 at which time V_{CC} and V_{REF} are above their respective thresholds.

PROGRAMMABLE DIGITAL-TO-ANALOG CONVERTER

The UC3910 contains a 4-Bit Digital to Analog Converter with an architecture shown in Figure 6. The DAC output (DACOUT) is a high impedance precision output programmed by the 4 programming pins, D0 (LSB) through D3 (MSB). Each programming bit pin controls a current source which is precisely trimmed to achieve the proper output voltage.

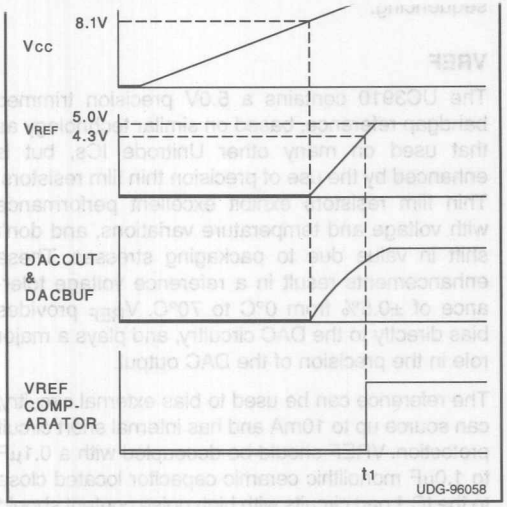


Figure 5. Power Up Sequence

DACOUT

The accuracy of the DACOUT pin, including the tolerance of the reference voltage, V_{REF} (combined accuracy), is typically ±0.5% and is ±0.9% from 0°C to 70°C worst case. DACOUT cannot be loaded externally since it is a high impedance (3kΩ) output. It should be decoupled locally with a 0.01µF to 0.1µF monolithic ceramic capacitor. A larger capacitor and the external decoupling capacitor form an RC time constant.

DACBUF

The DACBUF pin is a low impedance, buffered output of the DACOUT pin with a total gain/offset error of ±25mV. This pin is used by the UC3910 to set the overvoltage, undervoltage and overvoltage protection comparator threshold voltages. DACOUT cannot be used for this function since the threshold circuitry requires current and DACOUT cannot be loaded. The buffer is internally compensated for unity gain and cannot be decoupled externally. Good decoupling of the DACOUT and VCC pins will insure that the DACBUF signal is not corrupted by noise. DACBUF is internally clamped to 1 diode drop above ground during undervoltage lockout.

PROGRAMMING THE DAC

The DACOUT voltage is directly compatible with Intel's Pentium®Pro coding requirements, as shown in Table 1. The D0-D3 pins are directly equivalent to Intel's VID0 - VID3 signals. Intel requires programmable steps from 2.4V to 3.4V in 100mV increments, whereas the values of 2.0V to 2.3V and 3.5V are optional. The UC3910 DAC is programmable in 100mV increments, from 2.0V to 3.5V, where each decreasing bit represents a 100mV step, as shown Table 1.

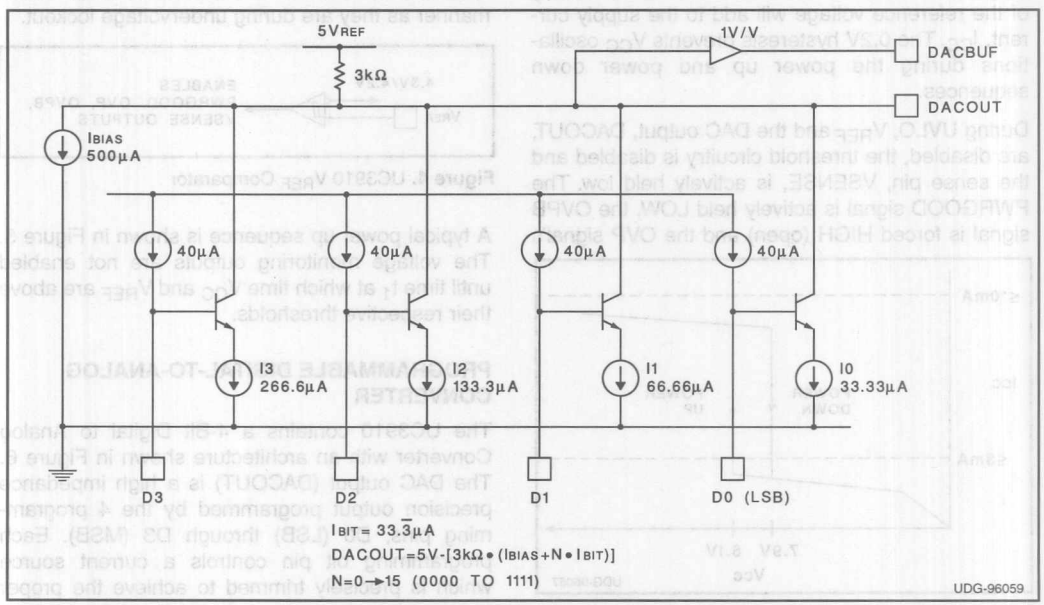


Figure 6. UC3910 Digital to Analog Converter (DAC) Architecture

Decimal Code	D3	D2	D1	D0	DACOUT Voltage	Pentium®Pro Specification	
15	1	1	1	1	2.0	No Processor	
14	1	1	1	0	2.1	2.1	
13	1	1	0	1	2.2	2.2	
12	1	1	0	0	2.3	2.3	
11	1	0	1	1	2.4	2.4	Intel's
10	1	0	1	0	2.5	2.5	I
9	1	0	0	1	2.6	2.6	I
8	1	0	0	0	2.7	2.7	I
7	0	1	1	1	2.8	2.8	↓
6	0	1	1	0	2.9	2.9	Operating
5	0	1	0	1	3.0	3.0	I
4	0	1	0	0	3.1	3.1	I
3	0	0	1	1	3.2	3.2	I
2	0	0	1	0	3.3	3.3	↓
1	0	0	0	1	3.4	3.4	Region
0	0	0	0	0	3.5	3.5	

Table 1. Programming the DACOUT Voltage

Figure 6 shows that each decimal code (0 through 15) represents an addition of 33.33μA of current through the 3kΩ resistor, which results in 100mV steps for each bit. A bias current of 500μA is used to set DACOUT to 3.5V when all four bits are 0s.

Programming pins D0-D3 are designed to accept OPEN = Logic 1 and SHORT = Logic 0 levels, as required by Intel, and will also accept open collector logic inputs. Each bit is pulled up internally to approximately 4.8V by a 40μA current source, as shown in Figure 6.

Some systems may want to control the D0-D3 pins from standard logic gates rather than open collector logic. The UC3910 will accept logic level inputs to the D0-D3 programming pins only if the logic HIGH level is ≥ 3.0 volts. The logic family should be well understood to insure that the driver can sink 40μA even when it is a logic HIGH.

Intel's specification for the Pentium®Pro processor includes all "1s" as an indicator that no processor is present. The UC3910 generates 2.0V on the DACOUT pin when all "1s" are present, thus insuring a safe low voltage level is present in a system should the programming pins be opened for any reason.

Dynamically Programming the DAC

The UC3910 is designed to accept the 4 bits as hardwired inputs prior to or at the same time power is applied to the UC3910. Dynamically changing the 4 bits is not recommended, as the characteristics (response time, overshoot, etc.) of the UC3910 DAC output under these conditions is highly dependent on external components. The time constant of the internal 3kΩ resistor and the DACOUT decoupling capacitor directly affect the rate at which DACOUT can dynamically change.

Changing the DAC Voltage Increments/Range

The UC3910 is designed to meet the Intel Pentium®Pro specification which requires programmable voltages from 2.4V to 3.4V in 100mV steps. Some systems may require exact power supply voltage outputs in ranges or increments other than those above in order to compensate for losses or to fine tune performance.

Upon inspection of Figure 6, a designer may opt to place an external resistor from DACOUT to VREF or to GND to adjust the DACOUT voltage up or down, respectively, as shown in Figure 7. This method, however, is NOT recommended. The UC3910 DAC is precisely trimmed to achieve it's accuracy, but the internal 3kΩ resistor IS NOT a precision resistor, and may be only accurate to ±20%. Designing an offset based on this internal resistor may therefore result in large errors. Should this method be used, the programmed voltage increment is no longer 100mV, but is proportional to the value of the external resistor used.

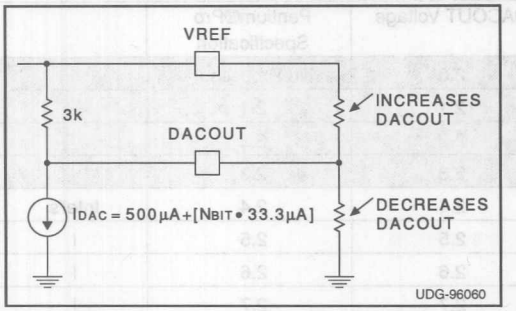


Figure 7. Using External Resistors to Adjust DACOUT is NOT recommended

A power supply's output voltage, controlled by the UC3910, may be adjusted when used in conjunction with the UC3886 PWM controller, as shown in Figures 8 (a) and (b). Increasing the voltage as shown in Figure 8 (a) can be accomplished with good accuracy by using precision resistors. Decreasing the voltage, as shown in Figure 8 (b) however, results in less accuracy, as the DACBUF buffered output includes gain/offset error of ±25mV (DACBUF = DACOUT ±25mV).

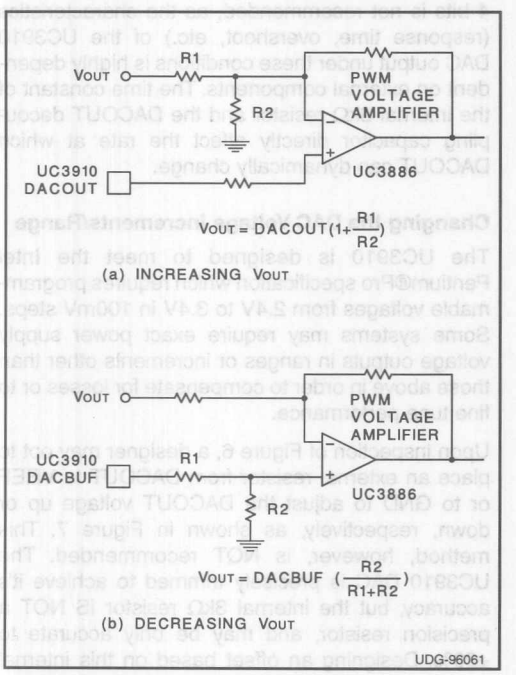


Figure 8. Recommended Methods for Adjusting a Power Supply's Output Voltage

VOLTAGE MONITORING SECTION

The UC3910's voltage monitoring section contains programmable window comparators which enable a power supply's output voltage to be closely monitored. The power supply's output voltage, as seen at the UC3910 VSENSE pin, is compared to three programmable thresholds; undervoltage, overvoltage, and overvoltage protection. The undervoltage and overvoltage comparators control the PWRGOOD signal to indicate that the output voltage is within a specified operating range. The overvoltage protection comparator controls the OVPB and OVP signals, which can be used to disable the power supply or to fire an external crowbar SCR.

The undervoltage, overvoltage, and overvoltage protection thresholds are programmed as a percentage above and below the programmed output (DACOUT), so that as the UC3910 DAC output voltage varies (various Pentium®Pro voltages for instance), so do the thresholds as a percentage of the DACOUT voltage.

Figure 9 shows a simplified schematic of the internal voltage monitor section. The voltage monitor section is programmable by the external resistors RS1 and RS2 at the threshold programming pin, OVTH/UVTH. RS1 and RS2 set the internal voltage thresholds which become inputs to the overvoltage, undervoltage and overvoltage protection comparators. The buffered DAC output, DACBUF, is used as the reference for the voltage monitoring thresholds.

VSENSE

The sense pin, VSENSE, is one input to the overvoltage, undervoltage and overvoltage protection comparators (OV, UV and OVP) which is compared to the set thresholds, as shown in Figure 9. VSENSE is typically connected to the output of the power supply which is controlled by the UC3910's precision output, DACOUT.

The hysteresis levels on the voltage monitor comparators can be as low as 20mV. VSENSE should be filtered externally with an RC filter, as shown in Figure 9, to insure that noise and ripple voltage does not cause false signals at the PWRGOOD and OVP pins. A filter frequency of 1/10th the power supply switching frequency is recommended, to reduce switching ripple by 20dB. The filter resistor and capacitor product is therefore

$$R_F \bullet C_F = \frac{1}{2 \bullet \pi \bullet (F_{SWITCH}/10)}$$

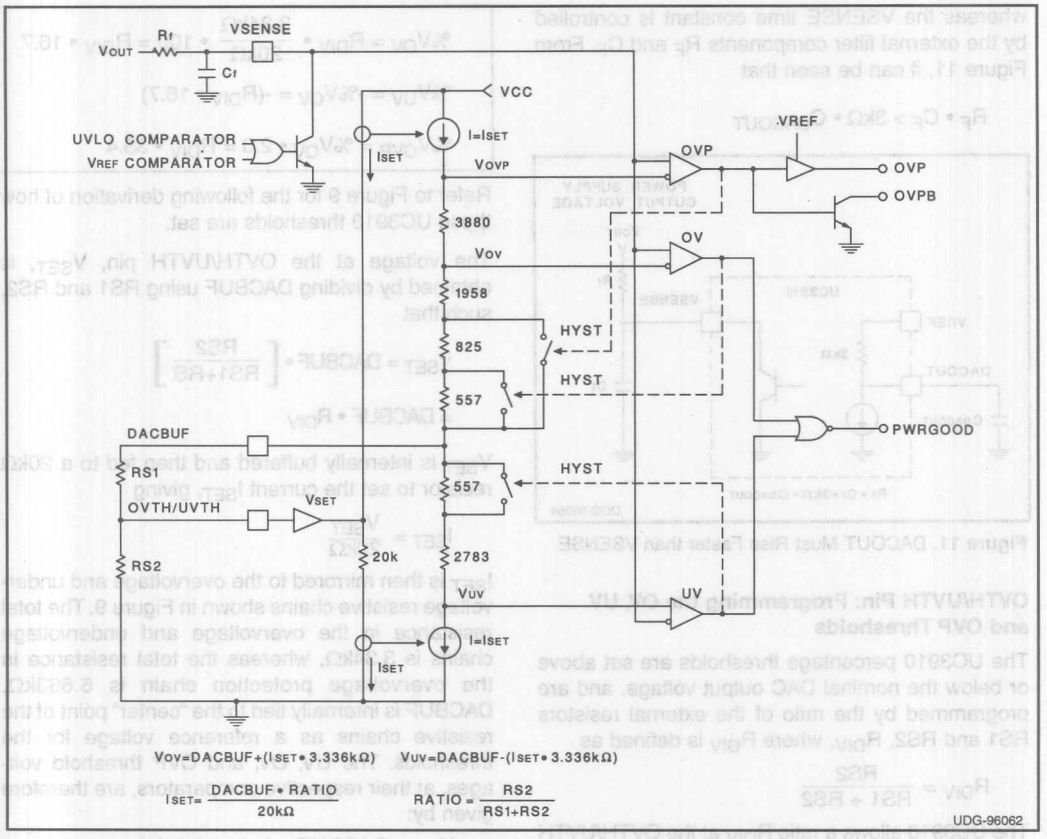


Figure 9. Voltage Monitor Section

VSENSE During UVLO - Protecting Against False OVP Signals

The UC3910 is designed to actively pull down VSENSE until V_{CC} and V_{REF} are above their respective thresholds during startup of the UC3910. This feature insures that during V_{CC} "brown-out" conditions, or when power supplies are powered up onto a live output bus, that the value of VSENSE will be below the DAC voltage, and will not trigger a false overvoltage protection signal. A V_{CC} "brown-out" situation is illustrated in Figure 10.

VSENSE can actively sink up to 500µA. The external filter resistor must therefore limit the current into VSENSE, such that

$$R_F \geq \frac{V_{OUT}}{500\mu A}$$

To insure that VSENSE does not falsely trigger an OVP condition, DACOUT must rise to its programmed level faster than VSENSE can rise. This restriction governs the two time constants on the VSENSE and the DACOUT pins. The DACOUT time constant is determined by the internal 3kΩ resistor and the DACOUT decoupling capacitor,

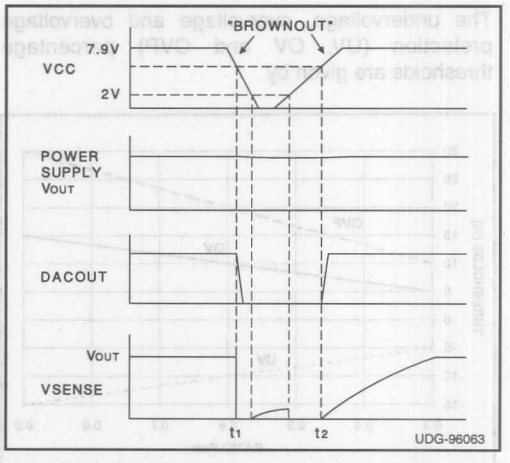


Figure 10. VSENSE is Pulled Low During UVLO Insuring that no False OVP Conditions Occur

whereas the VSENSE time constant is controlled by the external filter components R_F and C_F. From Figure 11, it can be seen that

$$R_F \bullet C_F > 3k\Omega \bullet C_{DACOUT}$$

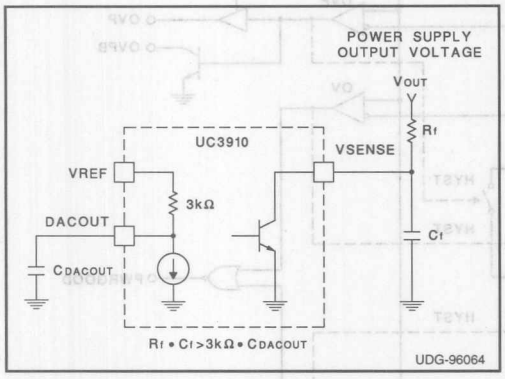


Figure 11. DACOUT Must Rise Faster than VSENSE

OVTH/UVTH Pin: Programming the OV, UV and OVP Thresholds

The UC3910 percentage thresholds are set above or below the nominal DAC output voltage, and are programmed by the ratio of the external resistors RS1 and RS2, R_{DIV}, where R_{DIV} is defined as

$$R_{DIV} = \frac{RS2}{RS1 + RS2}$$

The UC3910 allows a ratio R_{DIV} at the OVTH/UVTH pin from 0.3 to 0.9, which corresponds to overvoltage and undervoltage percentage thresholds from 5% to 15% and an OVP percentage threshold from 10% to 30%. These thresholds are shown in Figure 12.

The undervoltage, overvoltage and overvoltage protection (UV, OV and OVP) percentage thresholds are given by

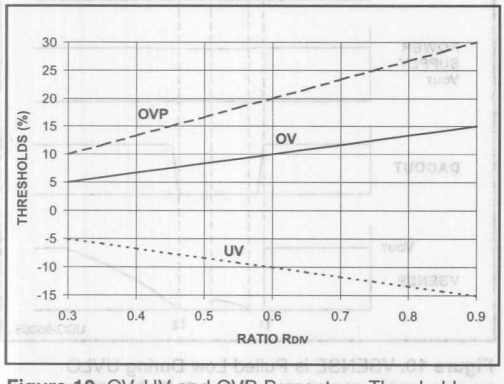


Figure 12. OV, UV and OVP Percentage Thresholds as a Function of the Divider Ratio R_{DIV}

$$\%V_{OV} = R_{DIV} \bullet \frac{3.34k\Omega}{20k\Omega} \bullet 100 = R_{DIV} \bullet 16.7$$

$$\%V_{UV} = -\%V_{OV} = -(R_{DIV} \bullet 16.7)$$

$$\%V_{OVP} = \%V_{OV} \bullet 2.0 = R_{DIV} \bullet 33.4$$

Refer to Figure 9 for the following derivation of how these UC3910 thresholds are set.

The voltage at the OVTH/UVTH pin, V_{SET}, is obtained by dividing DACBUF using RS1 and RS2, such that

$$V_{SET} = DACBUF \bullet \left[\frac{RS2}{RS1+RS}\right]$$

$$= DACBUF \bullet R_{DIV}$$

V_{SET} is internally buffered and then fed to a 20kΩ resistor to set the current I_{SET}, giving

$$I_{SET} = \frac{V_{SET}}{20k\Omega}$$

I_{SET} is then mirrored to the overvoltage and undervoltage resistive chains shown in Figure 9. The total resistance in the overvoltage and undervoltage chains is 3.34kΩ, whereas the total resistance in the overvoltage protection chain is 6.663kΩ. DACBUF is internally tied to the "center" point of the resistive chains as a reference voltage for the thresholds. The UV, OV, and OVP threshold voltages, at their respective comparators, are therefore given by:

$$V_{OV} = DACBUF + I_{SET} \bullet 3.34k\Omega$$

$$V_{UV} = DACBUF - I_{SET} \bullet 3.34k\Omega$$

$$V_{OVP} = DACBUF + I_{SET} \bullet 6.663k\Omega$$

These threshold voltages can be expressed in terms of percentages above or below the nominal DACBUF voltage since they are all biased by the programmed DACBUF voltage. The overvoltage percentage is determined by

$$\%V_{OV} = \left(\frac{V_{OV} - DACBUF}{DACBUF}\right) \bullet 100$$

which can be simplified to

$$\%V_{OV} = \left(R_{DIV} \bullet \frac{3.34k\Omega}{20k\Omega}\right) \bullet 100 = R_{DIV} \bullet 16.7$$

Likewise, the undervoltage and overvoltage protection percentage thresholds can be expressed as

$$\%V_{UV} = -(R_{DIV} \bullet 16.7) \text{ and}$$

$$\%V_{OVP} = R_{DIV} \bullet 33.4 = \%V_{OV} \bullet 2.0$$

(The OVP threshold percentage is 2.0 times the OV threshold percentage)

These percentage thresholds are shown graphically in Figure 12.

Hysteresis and Tolerances in the OV, UV and OVP Thresholds:

Each of the UV, OV and OVP threshold circuits in the resistive chain of Figure 9 contains a hysteresis resistor, which is switched in or out by the output of the respective comparator. The result is that the threshold voltages change (in voltage, not percent) by

$$UV_{HYS} = -(I_{SET} \bullet 557\Omega)$$

$$OV_{HYS} = I_{SET} \bullet 557\Omega$$

$$OVP_{HYS} = I_{SET} \bullet 1382\Omega$$

I_{SET} is proportional to both the programmed DAC voltage DACBUF as well as the ratio R_{DIV} which sets the thresholds. For an Intel Pentium®Pro application with voltages ranging from 2.4V to 3.4V and R_{DIV} ranging from 0.3 to 0.9, the hysteresis can range from 20mV to 85mV on OV and UV and from 50mV to 211mV on OVP. The effects of hysteresis are shown graphically in Figure 13.

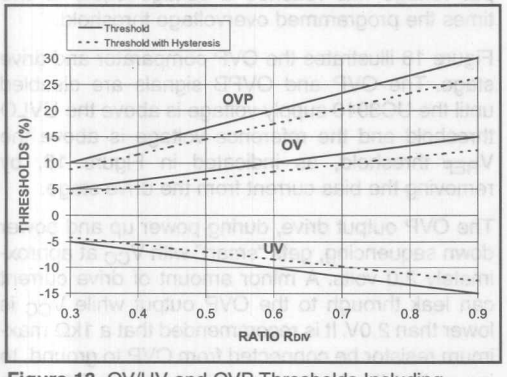


Figure 13. OV/UV and OVP Thresholds Including Hysteresis

There are tolerance factors that a circuit designer should consider when programming the voltage monitor threshold percentages. They are:

- UC3910 DACBUF error of ± 25mV
- UC3910 OV, UV and OVP Comparator off set voltages of ±10mV
- UC3910 Bias current from the OVTH/UVTH pins of ±30% of the value Iset
- UC3910 Threshold detection tolerance of ±10% of the percentage set
- External Resistor tolerances
- Non-ideal External resistor Values (The perfect divider ratio may not be achievable)

The designer can reduce the error due to external resistors by using precision values. Errors due to bias current from the OVTH/UVTH pin can also be minimized by using external values which draw approximately 1.0mA from DACBUF (presents a low impedance to the leakage current source), or

$$\frac{DACBUF}{RS1 + RS2} \approx 1.0mA$$

Unitrode has performed a Worst Case and an Root Sum Square (RSS) error analysis including all the abovementioned factors, for a set Ratio of R_{DIV}=0.45 (7.5% OV/UV thresholds), and using 1% resistors, with the results shown in Figure 14.

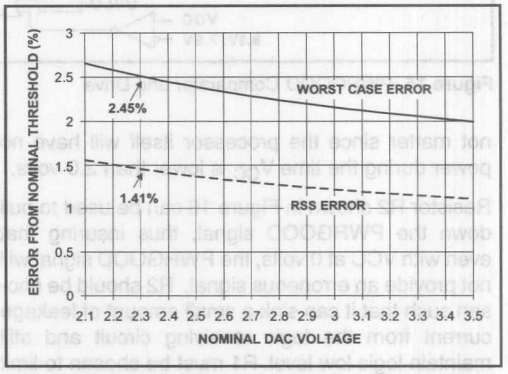


Figure 14. Error Analysis for a Nominal 7.5% OV/UV Threshold Setting - Varies with V_{OUT}

Should higher accuracy be required for the thresholds, the stability of the offset voltages and bias currents of the UC3910 with life and temperature is such that a voltage divider, RS1 and RS2, can be set up at manufacturing to set the thresholds very precisely, with little drift expected over the life of the power supply.

PWRGOOD

The PWRGOOD signal is an open collector logic level that is HIGH when the voltage at the UC3910 VSENSE pin is above the UV threshold and below the OV threshold, as indicated in Figure 9. The PWRGOOD signal must be pulled up externally to a voltage less than V_{CC}(max) and can sink 10mA.

Figure 15 illustrates the PWRGOOD comparator and drive stage. PWRGOOD is held low until the UC3910 supply voltage is above the UVLO threshold and the reference voltage is above the V_{REF} threshold, as indicated in Figure 15.

The PWRGOOD comparator output, during power up and power down sequencing, gets "smart" with V_{CC} at approximately 2.0 volts. Until V_{CC} reaches this level, there is not enough bias current (Figure 15, I1) to keep the PWRGOOD signal held in its low state. In most systems, where the PWRGOOD signal will act as the reset for the processor, this will

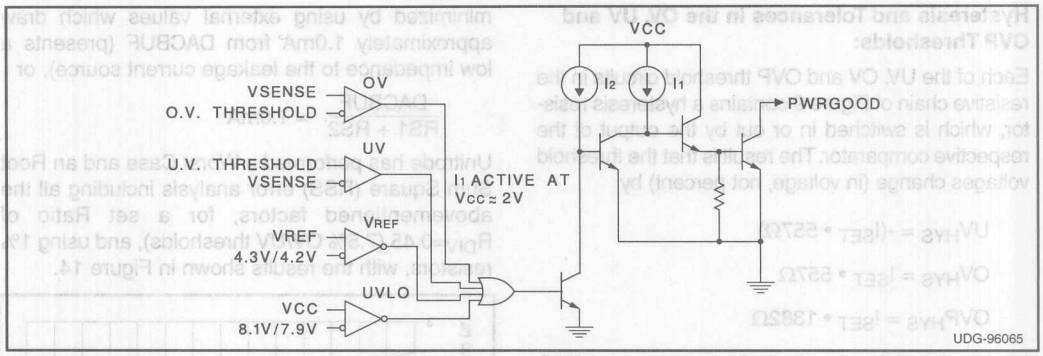


Figure 15. PWRGOOD Comparator and Drive

not matter since the processor itself will have no power during the time V_{CC} is lower than 2.0 volts.

Resistor R2 shown in Figure 16 can be used to pull down the PWRGOOD signal, thus insuring that even with VCC at 0 volts, the PWRGOOD signal will not provide an erroneous signal. R2 should be chosen such that it can sink a small amount of leakage current from the logic receiving circuit and still maintain logic low level. R1 must be chosen to limit the current into PWRGOOD to less than 10mA, and also to provide the proper level HIGH voltage. V_{REF} is disabled during UVLO, thus insuring there will be no pull-up voltage. Low voltage logic families can also be accommodated by using the circuit of Figure 16.

The PWRGOOD signal may be used as a reset signal to processor which is controlled by the UC3910 itself. A reset delay may be added to allow the processor to boot some time after the PWRGOOD signal. A typical reset circuit is shown in Figure 17.

OVP and OVPB Overvoltage Protection Signals

The OVP output signal is designed to directly trigger a silicon controlled rectifier (SCR) thyristor when a severe overvoltage condition occurs. OVPB is an open collector signal designed to go LOW under the same conditions, which can be used to disable a PWM such as the UC3886. The OVP comparator (see Figure 9) is tripped when the output voltage has reached a voltage equal to two times the programmed overvoltage threshold.

Figure 18 illustrates the OVP comparator and drive stage. The OVP and OVPB signals are disabled until the UC3910 supply voltage is above the UVLO threshold and the reference voltage is above the V_{REF} threshold, as indicated in Figure 18, by removing the bias current from the drive stage.

The OVP output drive, during power up and power down sequencing, gets "smart" with V_{CC} at approximately 2.0 volts. A minor amount of drive current can leak through to the OVP output while V_{CC} is lower than 2.0V. It is recommended that a 1kΩ maximum resistor be connected from OVP to ground, to insure that this leakage current does not charge an external SCR gate.

Figure 19 shows the UC3910 driving an external SCR. The UC3910 OVP signal, when high, will source a minimum of 65mA. Many SCRs require a

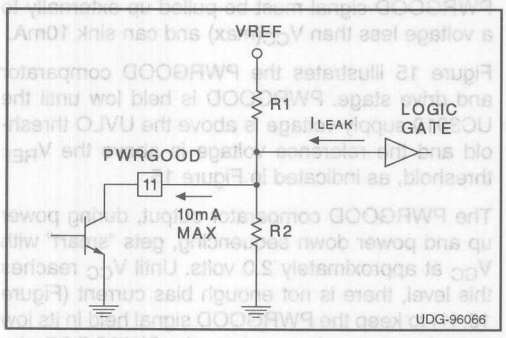


Figure 16. Add a Pull-down Resistor to PWRGOOD to Insure Proper Signal at $V_{CC} \leq 2$ Volts

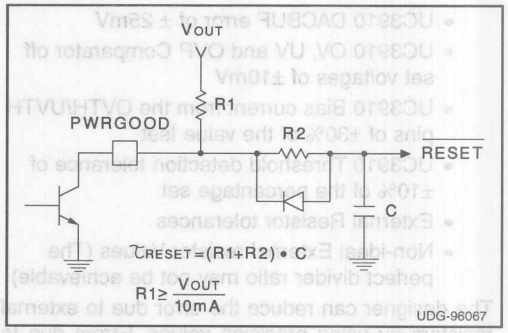


Figure 17. Using PWRGOOD to Reset the Processor

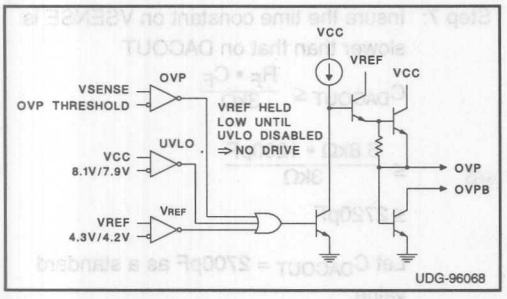


Figure 18. OVP Comparator and Drive

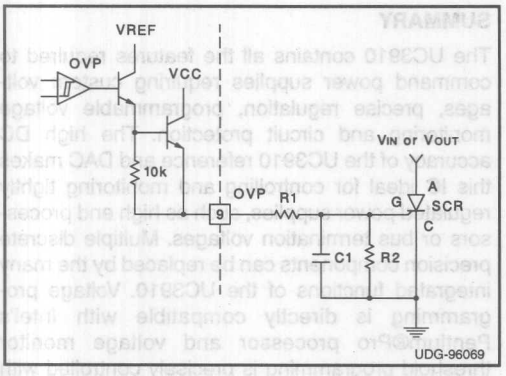


Figure 19. Driving an SCR using the UC3910 OVP Signal

gate trigger current (IGT) between 30mA and 50mA. The output high voltage will be approximately 4.3V maximum. The OVP signal is not pulled low internally to the UC3910.

Resistor R1 in Figure 19 is chosen to limit the gate current to minimize current draw on V_{CC} while insuring that the rated gate current is met. Resistor R2 is required to insure that the SCR is not inadvertently fired due to dc leakage currents or parasitic dv/dt effects through the SCR itself. C1 can be used to provide additional gate filtering, but should not be so large that the SCR gate signal is significantly delayed.

There are many tradeoffs to consider when choosing which SCR to use and where to use it to best protect critical electronics. SCR theory and various crowbar circuits are discussed extensively in literature [1] and in device data books [2].

The OVPB signal can be used to disable a power supply through a logic disable signal. This is easily accomplished when the UC3910 is used in conjunction with the UC3886 PWM controller IC, as demonstrated in Figure 20.

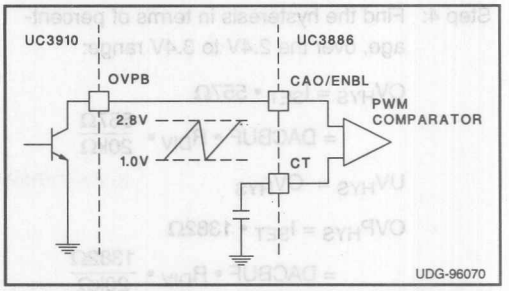


Figure 20. Disabling the UC3886 Switching Using the OVPB Signal

Circuit Example - Programming the Voltage Monitor Thresholds

Refer to Figure 9 and Figure 11, and program the UC3910 Voltage Monitor Section for the following requirements:

V_{OUTPUT} ranges from 2.4V to 3.4V (i.e., Pentium®Pro application)

F_{SWITCH} = 200kHz

Ripple voltage = 2% peak-to-peak

OV and UV Thresholds must be ±5% MINIMUM

OVP is to be set at 20% Maximum

Step 1: Choose to set the nominal overvoltage and undervoltage thresholds at 7.5% to insure that the ±5% thresholds are met.

Step 2: Calculate the ratio R_{DIV}, based on the desired 7.5%:

$$R_{DIV} = 7.5/16.7 = 0.45$$

Step 3: Find nominal values for RS1 and RS2

Let RS1 + RS2 draw ≈ 1.0mA at the maximum DACBUF voltage. Therefore

$$RS1+RS2 \approx \frac{3.4V}{1.0mA} \approx 3.4k\Omega$$

$$R_{DIV} = 0.45 = \frac{RS2}{RS1+RS2}$$

$$RS2 = 1.54k\Omega \qquad RS1 = 1.91k\Omega$$

$$RS1+RS2 = 3.45k\Omega \qquad R_{DIV} = 0.446$$

Step 4: Find the hysteresis in terms of percentage, over the 2.4V to 3.4V range:

$$OV_{HYS} = I_{SET} \bullet 557\Omega$$

$$= DACBUF \bullet R_{DIV} \bullet \frac{557\Omega}{20k\Omega}$$

$$UV_{HYS} = -OV_{HYS}$$

$$OVP_{HYS} = I_{SET} \bullet 1382\Omega$$

$$= DACBUF \bullet R_{DIV} \bullet \frac{1382\Omega}{20k\Omega}$$

The OV and UV hysteresis is 30mV @ 2.4V and 42mV @ 3.4V

The OVP hysteresis is 74mV @ 2.4V and 105mV @ 3.4V

Hysteresis on the OV and UV is ± 1.25%, and on the OVP is ± 3.1%

Step 5: Find V_{SENSE} filter components and calculate effective ripple at the VSENSE pin.

$$R_F \geq \frac{V_{OUTmax}}{500\mu A} \geq \frac{3.4V}{500\mu A} \geq 6.8k\Omega$$

Let $R_F = 6.8k\Omega$ as a standard 5% value.

$$C_F \geq \frac{1}{2 \bullet \pi \bullet (F_{SWITCH}/10)}$$

$$\geq \frac{1}{2 \bullet \pi \bullet (200kHz/10) \bullet 6.8k\Omega}$$

$$\geq 1170pF$$

Let $C_F = 1200pF$ as a standard value, giving a filter corner frequency of < 20kHz.

V_{RIPPLE} = 2% peak-to-peak • 1/10 = 4.8mV to 6.8mV peak to peak. This is well below the hysteresis ranges found in step 4.

Step 6: Solve for the thresholds. Use Figure 14 to estimate tolerances.

Nominal: $UV = -R_{DIV} \bullet 16.7 = -7.45\%$

$OV = R_{DIV} \bullet 16.7 = 7.45\%$

$OVP = OV \bullet 2.0 = 14.9\%$

Minimum OV/UV 7.45% - 2.45% = 5.00%

Maximum OV/UV 7.45% + 2.45% = 9.90%

Maximum OVP: 14.9% + 2.45% =17.35%

Step 7: Insure the time constant on VSENSE is slower than that on DACOUT

$$C_{DACOUT} \leq \frac{R_F \bullet C_F}{3k\Omega}$$

$$\leq \frac{6.8k\Omega \bullet 1200pF}{3k\Omega}$$

$$\leq 2720pF$$

Let $C_{DACOUT} = 2700pF$ as a standard value.

SUMMARY

The UC3910 contains all the features required to command power supplies requiring custom voltages, precise regulation, programmable voltage monitoring and circuit protection. The high DC accuracy of the UC3910 reference and DAC makes this IC ideal for controlling and monitoring tightly regulated power supplies, such as high end processors or bus termination voltages. Multiple discrete precision components can be replaced by the many integrated functions of the UC3910. Voltage programming is directly compatible with Intel's Pentium®Pro processor and voltage monitor threshold programming is precisely controlled with only two external resistors. Protecting the load against overvoltage can be performed with a logical shutdown or by driving a crowbar SCR.

Together with the UC3886 Average Current Mode PWM Controller IC, an optimal power supply can be designed to meet the stringent requirements of the Intel Pentium®Pro processor. For additional information on the UC3886 Average Current Mode PWM Controller IC, refer to application note U-156 [3]. For additional information on a detailed circuit design and performance of the UC3886/UC3910 chip pair, refer to application note U-157 [4].

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[4] U-157 Fueling the Megaprocessor - A DC/DC Converter Design Review Featuring the UC3886 and UC3910, L. Spaziani

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BOOST POWER FACTOR CORRECTOR DESIGN WITH THE UC3853

by Philip C. Todd

ABSTRACT

The UC3853 is designed to provide high performance power factor correction (PFC) for low to medium power applications with minimal complexity. It provides power supplies in the range of 10 to 200 watts with a low distortion, power factor corrected input current, a regulated output voltage and operation over a wide range of input voltages. The UC3853 uses average current mode control and works with either a boost or flyback converter. It was developed from the UC3854 family of PFC control circuits and has the same functionality in an 8-pin package. Much of the information available for the UC3854 family of integrated circuits is also applicable to the UC3853. In particular, Unitrode Application Note U-134 provides a good general introduction to power factor correction. U-134 contains an extended description of power factor correction, the boost PFC and the control circuits necessary to provide the correct programming of the current waveform. The reader is urged to review that note as well as this one before designing a boost power factor corrector.

This Application Note describes the features and functions of the UC3853 in detail. The design process for a boost power factor corrector is presented and the design details for a 100W output boost power factor corrector with a "universal" input voltage range of 80-270VAC are included. A table that extends the 100W boost converter example over the range of 25W to 200W is featured. A step-by-step summary of the design process is also provided so that the boost converter circuit may be customized for any application.

ABOUT THE UC3853 PFC CONTROLLER

The UC3853 has many similarities to the UC3854 based family of devices. It contains an average current mode control loop for a low distortion input current waveform, a multiplier to program an accurate current waveform and a voltage error amplifier to regulate the output voltage. The UC3853 also contains over-voltage protection for the output and has a fixed frequency internal oscillator which is synchronizable.

A block diagram of the UC3853 is shown in Figure 1. Due to its 8-pin simplicity, some pins serve more than one function and some functions are brought inside the chip altogether. The UC3853 begins operation when the voltage at the VCC pin is greater than 11.5V. An undervoltage lockout function (UVLO) keeps the device from operating before this voltage is reached. The UC3853 enters the UVLO state again when VCC drops below 9.5V. The hysteresis in the UVLO allows the device to be started from a capacitor which is trickle charged directly from the input voltage. When in UVLO, most of the internal circuits are not powered so the supply current is less than 500μA (250μA typical). The reference voltage in the UC3853 is internal to the device and is not brought out to a pin. The reference is divided down to 3.0V at the non-inverting input to the voltage error amplifier. The reference is trimmed to an accuracy of better than 2% at the FB pin of the voltage error amplifier so the reference voltage specification includes the offset of the amplifier. The total variation of the reference over temperature, including the set point accuracy, is 3.0V ±3.5%. For a typical 400V output the accuracy translates into an output variation of ±8V at room temperature, which is comparable to the ripple voltage amplitude on the output at full power.

The output of the UC3853 supplies 500mA peak current to the gate of the power MOSFET switch. A simplified schematic of the output driver is shown in Figure 2. The VCC pin provides the voltage feedforward signal needed by the multiplier/divider/squarer circuit and thus it has a wide input voltage range under normal operation. The output voltage

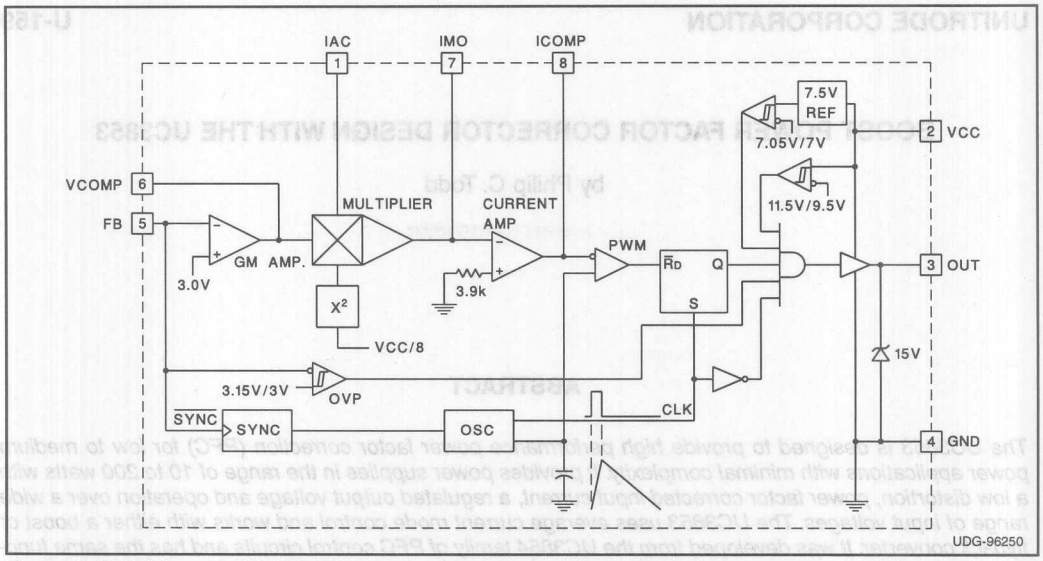


Figure 1. Block Diagram of UC3853

is therefore clamped near 15V to prevent the gate of the MOSFET switch from being driven beyond its breakdown voltage as VCC changes. When power is not applied to the device the output driver is self-biased to hold the output to within 1.5V of ground. When VCC is above the UVLO threshold the bias circuit is disabled and the output driver operates normally. This prevents the MOSFET from turning on when power is first applied to the converter. If the output were not held low, the gate to drain capacitance of the MOSFET would pull the gate high when power is applied and turn the device on, which often results in its destruction.

The PWM comparator uses the oscillator ramp and the output of the current amplifier to generate the gate drive output as shown in Figure 3. The output of the comparator is latched for the duration of the clock period to prevent false output pulses. The latch is set by the clock signal at the beginning of each clock period to drive the output high and is reset by the PWM comparator to drive the output low. The output is kept low by the status inputs to the AND gate that drives the output. The status inputs are the undervoltage lockout (UVLO), the reference valid and the output overvoltage status signal. The output is also held low during the clock interval.

The oscillator is internal to the UC3853, has a fixed 75kHz operating frequency and may be synchronized to an external source. The oscillator waveform is a reverse sawtooth because a negative slope ramp is required to provide the proper polarity for the PWM circuit and for the slope compensation of the average current loop. The current loop error amplifier inverts the current signal so the oscillator ramp must have a negative slope. The rel-

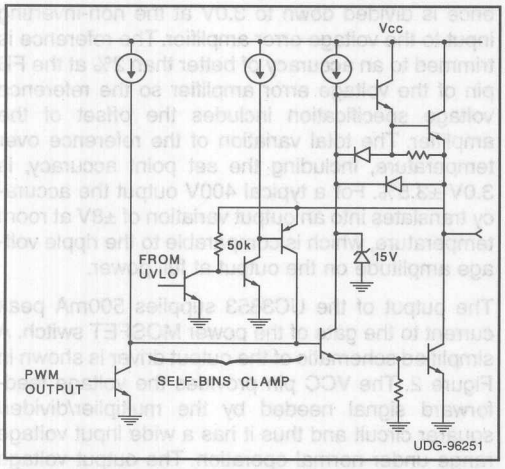


Figure 2. UC3853 Output Driver (Simplified Schematic)

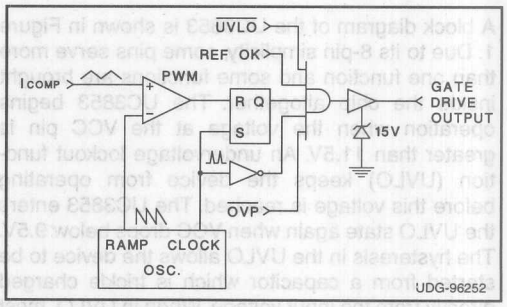


Figure 3. UC3853 PMW Circuit

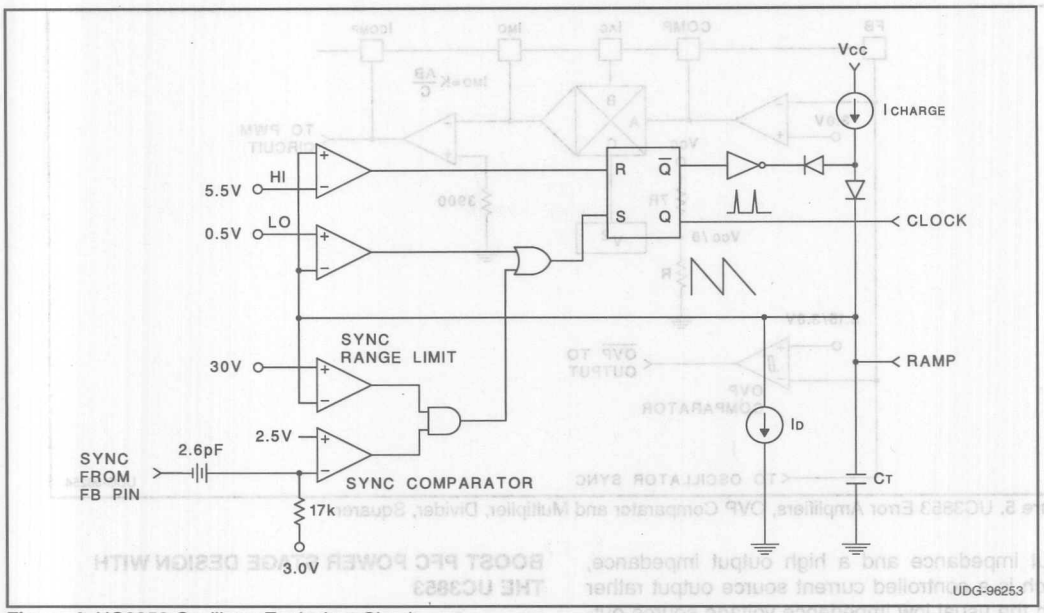


Figure 4. UC3853 Oscillator Equivalent Circuit

ative polarity of the two signals is therefore opposite, which is the correct orientation. This is all internal to the device. The width of the clock output pulse determines the minimum dead time of the output and is less than 1% of the clock period. An equivalent circuit for the oscillator and the sync circuit is shown in Figure 4.

The synchronizing pulse for the oscillator comes from the FB pin. The voltage feedback and the overvoltage protection are also connected to the FB pin. If the synchronizing signal is capacitively coupled into the FB pin it will not upset the DC output voltage value since the bandwidth of the amplifier is very small compared to the switching frequency. The compensation network on the output of the transconductance amplifier will eliminate the synchronizing signal from the output of the amplifier. The guaranteed synchronization frequency range is 95kHz to 115kHz. Circuits for synchronizing the oscillator are described later in this Application Note.

The voltage and current loop amplifiers, the squarer and the multiplier/divider circuits are shown in Figure 5. The current amplifier is a wideband operational amplifier and it has ground referenced inputs. The inverting input of the amplifier is a summing junction where the feedback, the input current signal and the current programming signal from the multiplier output come together. The current signal is negative and the output of the multiplier is positive so the current loop is adjusted to keep the voltage at the inverting input zero since the non-inverting input of the current amplifier is connected to ground through a 3.9kΩ resistor. This resistor provides DC balancing of the amplifier input bias currents. The amplifier has sufficient output drive capability to handle a wide range of feedback networks.

The squarer and multiplier/divider are the heart of the control circuit and are shown in Figure 5. This circuitry makes it possible to operate a boost PFC stage over a 3:1 input voltage range and still get excellent voltage loop bandwidth and fast response to input voltage variations. The multiplier/divider requires three inputs which are traditionally labeled A, B and C. The A input is the output of the voltage error amplifier which controls the average output voltage. The B input is the IAC signal which is a current from the input voltage and it is multiplied by the output of the voltage error amplifier to provide the current shape and amplitude needed to program the current loop. The C input is the divider input and it is the feed forward voltage that comes through the squarer. This input is proportional to the square of the average input voltage and it adjusts the gain of the multiplier to keep the gain of the voltage control loop constant. This is the secret to achieving a wide bandwidth control loop over a wide input voltage range. The squaring circuit takes its input from the VCC pin so the bias voltage for the UC3853 must be proportional to the input voltage for this feature to work properly.

The voltage error amplifier in the UC3853 is a transconductance amplifier and it has both a high

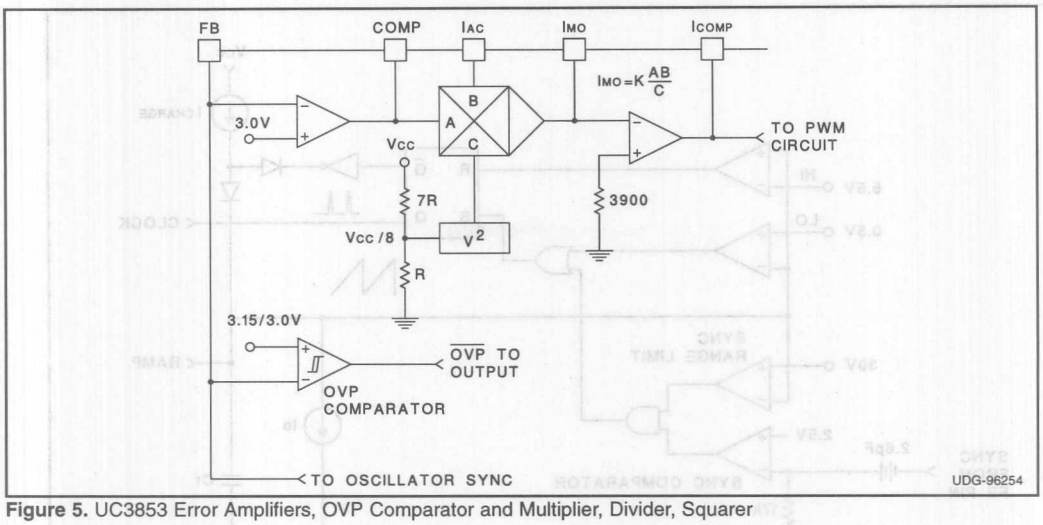


Figure 5. UC3853 Error Amplifiers, OVP Comparator and Multiplier, Divider, Squarer

input impedance and a high output impedance, which is a controlled current source output rather than the usual low impedance voltage source output. The gain of a transconductance amplifier is not given by the ratio of volts out to volts in. Instead it is given by the ratio of amperes out to volts in, which is a transconductance (the inverse of a resistance) and has the units of Siemens. The transconductance is a gain in this case and is often denoted by the symbol G_M. The gain of a transconductance amplifier can be changed into a voltage ratio by multiplying the transconductance gain by the load resistance. Hence, the voltage gain is set by an RC network to ground from the output of the amplifier. This allows the gain and frequency response of the amplifier to be determined by the load impedance without any components connected from the output of the amplifier to the input.

A transconductance amplifier was chosen to allow three functions to be combined on the FB pin. The oscillator sync input and the overvoltage comparator share the same input pin as the error amplifier so if a feedback network were connected around the amplifier the overvoltage comparator would be inaccurate. Since both the transconductance amplifier and the overvoltage comparator require only a simple voltage divider at their inputs for proper operation they can be combined into a single pin. The non-inverting input of the voltage amplifier is connected to a 3.0V DC reference which is the reference for the output voltage. The overvoltage comparator turns the output of the UC3853 off when the voltage at the FB pin exceeds 3.15V. The output turns back on when the voltage at the FB pin comes back to 3.0V.

BOOST PFC POWER STAGE DESIGN WITH THE UC3853

The circuit for a boost PFC is shown in Figure 6. The reference designators for the parts on the schematic match those in U-134 where the functions of the parts are the same. In all cases the reference designators are appropriate for the function of the device. A 100W boost power factor corrector is used as an example of the design process and this is the circuit that is shown in Figure 6. A table is provided at the end of this Application Note that extends the design over the range of 25W to 200W. The control circuits are the same whether at 25W or at 200W. The values of the control circuit components change only if the choices for circuit performance are different from those made here. The following design process allows the design to be modified to suit a wide variety of applications.

The design of a boost PFC begins with the specification for the system performance. The minimum and maximum input line voltages, the maximum output power, and the line frequency range must be specified. For the example circuit the specifications are:

- Maximum power output: 100 Watts
- Input line voltage range: 80-270VAC
- Line frequency range: 47-65Hz

The input line voltage and frequency range are a "universal" input range and allow this power factor corrector to operate from power lines anywhere in the world without switches or other adjustments.

The output voltage needs to be at least 5% higher than the peak voltage of the highest input line voltage. The peak of a 270VAC line will be about 380V

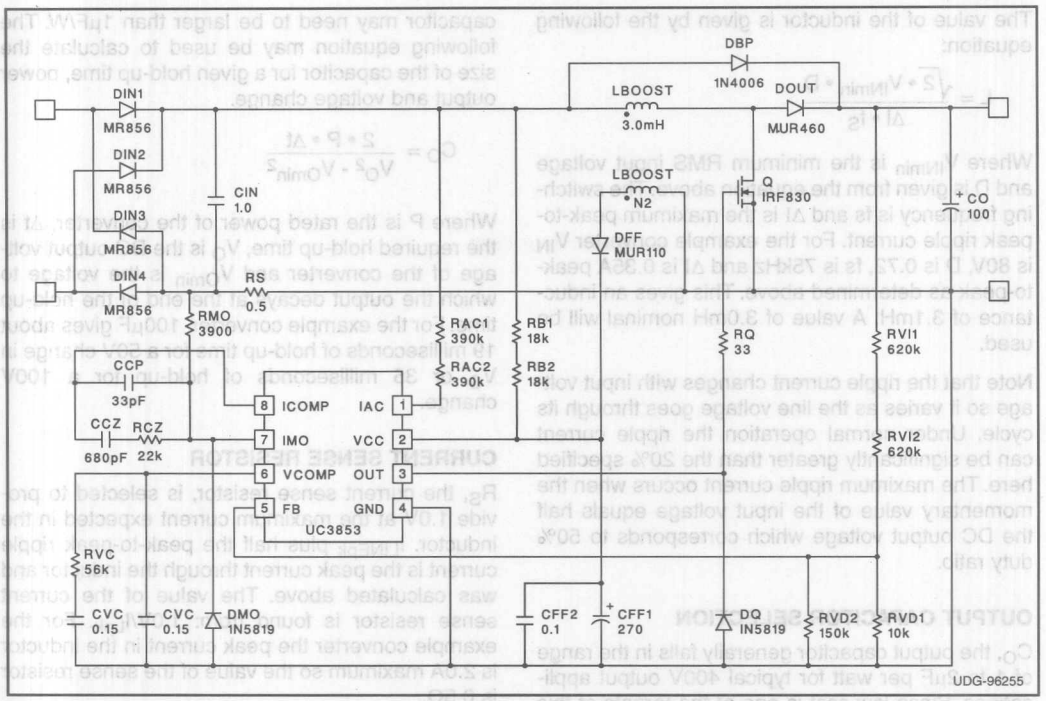


Figure 6. Schematic of a Boost Power Factor Corrector Using the UC3853

so 400V is chosen as the DC output voltage.

The switching frequency is an important consideration in the design process and the switching frequency is internally fixed in the UC3853 at 75kHz nominal and may be synchronized to an external 100kHz oscillator.

INDUCTOR SELECTION

The peak current that the inductor must carry is the peak line current at the lowest input voltage plus the peak high frequency ripple current. The peak line current is given by the following equation:

$$I_{LINEpk} = \frac{\sqrt{2} \bullet P}{V_{INmin}}$$

Where P is the maximum input power to the converter. Generally, using the output power is sufficiently accurate for this calculation since the efficiency of the converter should be greater than 90%. If greater accuracy in the design process is required, the design may be completed, the efficiency calculated and then the design process may be iterated using the calculated value for efficiency. For the example converter, the output power is 100W and V_{INmin} is 80VAC so I_{LINEpk} is 1.77A.

The high frequency ripple current, ΔI, must be kept reasonably small and is usually in the range of 15% to 25% of the peak line current given above. If the ripple current is too high the AC input filters required to filter out this noise become larger. If the ripple current is too low the value of the inductance is too large and the cusp distortion on the leading edge of the waveform will be large and the power factor will be low. For the example converter, the ripple current, ΔI, is chosen to be 20% of the peak line current or about 0.35A peak-to-peak. The peak current in the inductor, I_{Lpk}, is the sum of the peak line current and half of the peak-to-peak ripple current or 1.95A for the example converter.

The value of the inductor is determined by the peak current at low input line voltage, the duty factor, D, at that input voltage and the switching frequency. This value of the duty factor is given by the following equation:

$$D = \frac{V_O - \sqrt{2} \bullet V_{INmin}}{V_O}$$

Where V_{INmin} is the minimum RMS input line voltage and V_O is the DC output voltage. For the example converter V_{INmin} is 80V and V_O is 400V so D is 0.72.

The value of the inductor is given by the following equation:

$$L = \frac{\sqrt{2} \bullet V_{INmin} \bullet D}{\Delta I \bullet f_S}$$

Where V_{INmin} is the minimum RMS input voltage and D is given from the equation above. The switching frequency is fs and ΔI is the maximum peak-to-peak ripple current. For the example converter V_{IN} is 80V, D is 0.72, fs is 75kHz and ΔI is 0.35A peak-to-peak as determined above. This gives an inductance of 3.1mH. A value of 3.0mH nominal will be used.

Note that the ripple current changes with input voltage so it varies as the line voltage goes through its cycle. Under normal operation the ripple current can be significantly greater than the 20% specified here. The maximum ripple current occurs when the momentary value of the input voltage equals half the DC output voltage which corresponds to 50% duty ratio.

OUTPUT CAPACITOR SELECTION

C_O, the output capacitor generally falls in the range of 1 to 2μF per watt for typical 400V output applications. Since low cost is one of the targets of this converter, 1μF/W is chosen and thus a 100μF capacitor will be used for C_O. There are many factors that influence the value of the output capacitor. The output voltage hold-up time, the output ripple voltage, the loop transient response and the input current third harmonic distortion are all dependent to some degree on the value of the output capacitor and, in all cases except cost, a larger value of the output capacitance results in better performance. Nevertheless, a reasonable compromise can be reached with the 1μF/W value.

All power factor correction circuits have a large ripple current on their output at the second harmonic of the line current as highlighted in U-134. As the output capacitor becomes smaller, the output ripple voltage due to the second harmonic ripple current increases and the bandwidth of the voltage loop must be made smaller to keep the same level of distortion in the input current. A 1% second harmonic ripple voltage at the output of the voltage error amplifier becomes 0.5% third harmonic distortion of the input current. The only ways to reduce this source of distortion are to (1) increase the size of the output capacitor and (2) reduce the gain of the error amplifier at the second harmonic frequency by reducing the amplifier bandwidth. Reducing the loop bandwidth slows the transient response and increases its deviation.

The output capacitor may need to be larger for other reasons. If hold-up time is required, the capacitor may need to be larger than 1μF/W. The following equation may be used to calculate the size of the capacitor for a given hold-up time, power output and voltage change.

$$C_O = \frac{2 \bullet P \bullet \Delta t}{V_O^2 - V_{Omin}^2}$$

Where P is the rated power of the converter, Δt is the required hold-up time, V_O is the DC output voltage of the converter and V_{Omin} is the voltage to which the output decays at the end of the hold-up time. For the example converter, 100μF gives about 19 milliseconds of hold-up time for a 50V change in V_O or 35 milliseconds of hold-up for a 100V change.

CURRENT SENSE RESISTOR

R_S, the current sense resistor, is selected to provide 1.0V at the maximum current expected in the inductor. I_{LINEpk} plus half the peak-to-peak ripple current is the peak current through the inductor and was calculated above. The value of the current sense resistor is found from: $1.0V/I_{Lpk}$. For the example converter the peak current in the inductor is 2.0A maximum so the value of the sense resistor is 0.5Ω.

SWITCHES AND DIODES

The power switch must have a low R_{DSon} rating and a peak voltage rating greater than the output voltage of the converter with some margin for transient overshoot, ripple voltage on the output and appropriate levels of derating. A low R_{DSon} of the power switch will result in lower conduction losses but these devices also have high gate capacitances and may therefore have longer turn-on times, resulting in greater overall switch power dissipation. There is an optimum size switch for each application although the optima is rather broad. Suggestions for switches for a variety of power levels are contained in the table at the end of this application note. These are by no means the only possibilities and are simply generic choices. For the example converter an IRF830 was chosen.

The output diode must be rated for the peak output current and must be an incredibly fast diode. A reverse recovery time below 100 nanoseconds is strongly recommended and faster is much better. The reverse recovery time of the diode has a direct effect on the power dissipation in the switch. The switch must conduct full output current at full output voltage from the time it turns on until the diode turns off. For the example converter this will be 400V at 2.0A for a peak power of 800W. If this lasts for 100nsec the average power will be 6.0W at a 75kHz switching frequency. If a 35nsec recovery

diode is used the average power will be 2.1W. There are many diodes available that meet the requirements of this application. The temperature rise of the diode must be kept below maximum for the worst case conditions as well. The reverse recovery time of the diode becomes larger as the temperature increases and this increases the power dissipation of the switching transistor. Heat sinking of the diode may be required to control the maximum temperature. For the example converter either an MUR460 or a BYM26C is used.

INPUT DIODES

The input diodes are not particularly critical. They must have a current rating sufficient for the maximum current at low line and they must be held to a reasonable temperature rise. Fast recovery types generally prove to be a bit less noisy than standard recovery types. Avalanche breakdown types work better with noisy power lines. The exact choice of input diodes depends on many such factors as well as the amount of filtering present on the AC side of the bridge. For the example converter, MR856 or BYW95C diodes are used. Both are fast recovery types.

C_{IN} is part of the input filter even though it is after the input diodes. The value must be chosen in conjunction with the input filter and must be kept reasonably small. This capacitor carries most of the ripple current from the inductor so it needs to be a film type capacitor with a substantial high frequency ripple current capability. At light loads C_{IN} can have a large effect on the distortion of the input current because it is after the input diodes. At these low currents, especially near the input voltage zero crossing, the capacitor stores enough energy to maintain the output current and the input diodes turn off, thus introducing distortion into the input current. For the example converter, a 1.0µF capacitor was chosen to give less than 1V peak-to-peak ripple voltage at the switching frequency with 100W output.

CONTROL CIRCUIT DESIGN WITH THE UC3853

The heart of the UC3853 is the multiplier and it is quite easy to set the parameters for proper operation. The equation for the multiplier is given below and, even though it looks complex, it is quite straight forward.

$$I_{MO} = \frac{I_{AC} \bullet (V_{COMP} - 1.5)}{K_M \bullet \left(\frac{V_{CC}}{8}\right)^2}$$

I_{MO} is the output current from the multiplier. I_{AC} is the programming current that comes from the input through R_{AC} and is proportional to the input voltage. It tells the current loop what to do to maintain an input current which is proportional to the input voltage. V_{COMP} is the output of the voltage error amplifier and is the other input to the multiplier. K_M is the gain constant of the multiplier and is given in the data sheet for the UC3853. V_{CC} is the supply voltage to the UC3853 and it is divided by eight internally and then squared in the squaring circuit. This forms the divider input to the multiplier and is used to keep the gain of the voltage loop constant so that the loop bandwidth may be kept large and thus have a relatively fast transient response.

I_{AC} must be programmed to have a maximum value of 500µA when the AC line voltage is at its peak. The voltage at the IAC pin is 2.0V so it introduces very little error into the current if this voltage is ignored. For the example converter the maximum input voltage is 270VAC and this has a peak value of about 380V. A 760kΩ resistor will give 500µA. Most resistors are only rated to 250V so two resistors will be needed in series. The closest standard value is 390kΩ so this value is chosen for both R_{AC1} and R_{AC2}.

CURRENT LOOP COMPENSATION

The peak value of I_{MO} is about 250µA with the values of R_{AC} given above. If R_{MO} is made 3.9kΩ, the peak value of voltage across R_S will be 1.0V. This value of R_{MO} also matches the 3.9kΩ resistor internal to the UC3853 which is connected to ground from the non-inverting input of the current error amplifier. These two values provide the correct balance for the DC bias currents into the amplifier and give the correct input offset voltage. If the offset voltage is in the wrong direction the current loop could latch at zero output.

The PFC input current must track the current programming signal (I_{MO}) from the multiplier very closely to achieve a low distortion input current. Accurate tracking requires high gain in the current loop to minimize the errors. For the current loop to be stable, the frequency at which the gain of the loop is equal to one must be less than one thirds of the switching frequency and the gain must roll off with a single pole slope. The boost power stage has a single pole due to the main inductor and the current sense resistor. This L/R pole creates a stable loop with a fixed gain, wide bandwidth error amplifier. These two requirements can be accommodated by using pole zero compensation around the error amplifier. Pole zero compensation has high

gain at low frequencies and flat gain at high frequencies so that the input current tracks the programming signal accurately and is also stable at high frequencies. This is the essence of average current mode control and it is necessary for a low distortion PFC.

A block diagram of the current loop is shown in Figure 7. A bit of topological manipulation has been done to put the loop into this form. The switch, output diode and output capacitor have been moved to the other side of the inductor and lumped into the voltage source V_S, which is now a controlled source and is controlled by the duty factor d from the PWM circuit in the UC3853. The reason for showing the circuit model in this form is to highlight the source of the L/R pole in the current loop and to show how the pole zero compensation of the current error amplifier affects the loop.

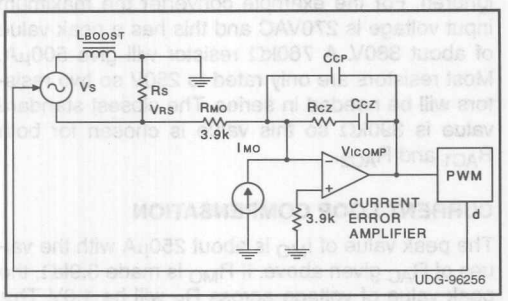


Figure 7. Simplified Block Diagram of a Boost PFC Current Loop

Figure 8 shows the control to output current gain of the current loop and the current amplifier compensation as well as the complete current loop gain. The graph ignores the double pole occurring at the switching frequency and the aliasing effects of the sampling system. The graph is based on a linear model to promote understanding of the loop dynamics and the compensation methods employed. The lower curve is the control to current transfer function of the boost stage and the pulse width modulator (V_{RS}/V_{Icomp}). The gain is moderate at low frequencies and shows the L/R corner frequency and single pole roll off up to half of the switching frequency. The pole zero compensation of the current error amplifier is shown along with the complete current loop response.

The design of the pole-zero compensation for the current loop begins with the equation for the control to output transfer function of the boost power stage. The control variables for this transfer function are the output of the current amplifier, V_{Icomp}, and the voltage across the current sense resistor, V_{RS}. The equation is:

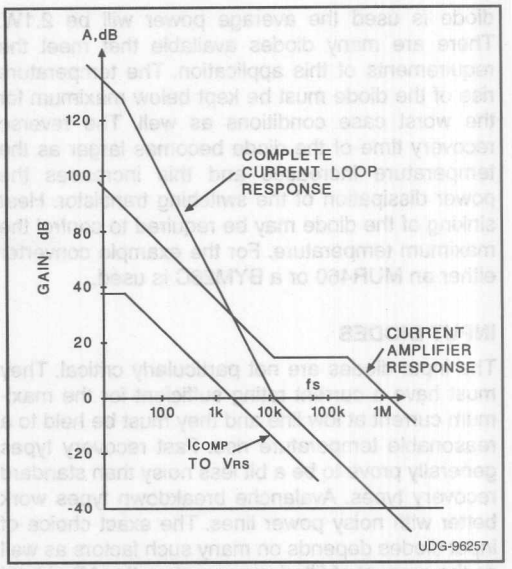


Figure 8. Current Loop Transfer Functions for 100W Example Boost Converter

$$\frac{V_{RS}}{V_{Icomp}} = \frac{V_O \bullet R_S}{V_{OSC} \bullet (R_S + X_L)}$$

Where V_O is the DC output voltage of the converter, R_S is the sense resistor value, V_{OSC} is the peak-to-peak amplitude of the oscillator ramp voltage and X_L is the impedance of the boost inductor ($2 \bullet \pi \bullet f \bullet L$).

The current loop is a very wide bandwidth loop and stability is achieved by adjusting the current amplifier gain so that the natural roll off from the L/R_S pole of the boost stage crosses 0dB gain at the appropriate frequency. Because the bandwidth is large, slope compensation must be added to the loop to compensate for the double pole which occurs at the switching frequency. In average current mode control the slope compensation is provided by the oscillator ramp, which is one of the inputs to the PWM comparator. If the gain of the error amplifier is correct, the amplitude of the oscillator ramp will introduce the correct amount of slope compensation. The procedure is to match the down slope of the inductor current with the slope of the oscillator ramp. That gives the correct value for the loop gain at the switching frequency to maintain stability. A capacitor is then added in series with the resistor for pole-zero compensation which gives the maximum amplifier gain at low frequencies.

The maximum down slope of the inductor current occurs when the input voltage is near zero. The equation for the inductor yields the slope of the current.

$$\frac{dI}{dt} = \frac{V_O}{L}$$

Where dI/dt is the slope of the inductor current in amperes per second, V_O is the DC output voltage of the converter and L is the value of the boost inductance. This current flows through the sense resistor and becomes a voltage so the equation is modified as follows:

$$\frac{dV}{dt} = \frac{V_O}{L} \bullet R_S$$

Where R_S is the sense resistor value. For the example converter the output voltage is 400VDC and the inductance is 3.0mH so the dI/dt is 0.133A/µsec, and R_S is 0.5Ω so dV/dt is 0.066V/µsec.

The oscillator in the UC3853 has a peak-to-peak amplitude of 5.0V and the period is 13.3µsec so the slope is 0.375V/µsec (the slope does not change with synchronization). The gain of the current amplifier at the switching frequency is determined by the ratio of the oscillator voltage slope divided by the current slope. The gain of the current amplifier at the switching frequency is the ratio of R_{CZ} to R_{MO}. For the example converter the current slope is 0.066V/µsec and the oscillator slope is 0.375V/µsec so the gain is 5.625. R_{MO} is 3.9kΩ so R_{CZ} is 22kΩ.

The value of the capacitor C_{CZ}, which introduces a zero into the current error amplifier response, is set by the current loop crossover frequency. The zero must be at or below that frequency to maintain the phase margin of the current loop. The equation for f_{CI} given below is simplified somewhat but is accurate over this frequency range.

$$f_{CI} = \frac{V_O \bullet R_S \bullet R_{CZ}}{2 \bullet \pi \bullet L \bullet R_{MO} \bullet V_{OSC}}$$

Where V_O is the DC output voltage of the converter, R_S is the value of the current sense resistor and R_{CZ} is the current amplifier feedback resistance determined above. V_{OSC} is the peak-to-peak oscillator ramp voltage, L is the value of the boost inductor and R_{MO} is the current amplifier input resistance. For the example converter, V_O is 400VDC, R_S is 0.5Ω, R_{CZ} is 22kΩ, V_{OSC} is 5V, L is 3.0mH and R_{MO} is 3.9kΩ resulting in an f_{CI} of 12kHz.

C_{CZ} must have an impedance equal to or less than R_{CZ} at f_{CI}. This is easily found from:

$$C_{CZ} = \frac{1}{2 \bullet \pi \bullet f_{CI} \bullet R_{CZ}}$$

For the example converter, f_{CI} is 12kHz and R_{CZ} is 22kΩ so C_{CZ} must be greater than 600pF. A 680pF capacitor is chosen to give a bit of extra phase margin.

C_{CP} is included to suppress high frequency noise in the current amplifier and it must have an impedance of at least 2 • R_{CZ} at the switching frequency. Substituting f_S for f_{CI} into the equation above gives C_{CP}.

$$C_{CP} = \frac{1}{2 \bullet \pi \bullet f_S \bullet 2 \bullet R_{CZ}}$$

For the example converter C_{CP} must be less than 50pF. A value of 33pF is chosen to accommodate a 100kHz synchronization frequency.

A hard current limit is not necessary to protect the switch in an average current mode controlled system. The gain of the current amplifier is set so that the maximum change of current in the inductor results in at most a 20% change of the current during one clock period. This makes it impossible for the control circuit to cause the switch to be on long enough to enter an overcurrent condition. The current programming signal is also limited so the inductor current can not exceed this value.

HARMONIC DISTORTION BUDGET

Once the current loop is stable the next two tasks are setting the voltage loop compensation and the feedforward compensation. Both of these are determined by the amount of harmonic distortion each contributes to the input current. The voltage loop contributes 0.5% third harmonic distortion to the input current for each 1% ripple voltage at the output of the error amplifier. The feedforward compensation comes from the voltage supplied to the UC3853 and each 1% ripple on this input contributes 1% third harmonic distortion to the input current.

The choice of input current harmonic distortion limit and the allocation of this distortion to the two major sources is somewhat arbitrary. For the example converter, the THD will be limited to 5% of the input current. The voltage loop is allowed to contribute 2% of the distortion and the feedforward voltage is allowed to contribute 2% of the distortion. The remaining 1% will be allocated to other sources such as cusp distortion and possible multiplier nonlinearity. 5% THD gives a power factor of 0.99875.

VOLTAGE LOOP COMPENSATION

A simplified block diagram of the voltage loop is shown in Figure 9. Average current mode control turns the power stage of the boost converter into a voltage controlled current source driving a capacitor, C_O, in parallel with the load resistance. The cur-

rent loop therefore becomes a transconductance amplifier with a voltage input and current output. The voltage gain of the current loop is given by $G_{CL} \bullet Z_L$ where G_{CL} is the transconductance of the current loop and Z_L is the parallel combination of C_O and R_L, the load resistance. The frequency response of the current loop has a DC gain given by $G_{CL} \bullet R_L$ and a single pole roll off due to C_O and R_L within the frequency range of interest. Theoretically, if the voltage loop is closed around the current loop with a fixed gain error amplifier, the voltage loop will be stable because there is only a single pole from C_O and R_L within the loop. As the gain of the amplifier increases, the bandwidth of the voltage loop also increases. Although this solution is very appealing, it is not feasible with the UC3853 because the limited current capability of the voltage error amplifier. Therefore, the error amplifier compensation will have a zero below and a pole at the crossover frequency of the voltage loop.

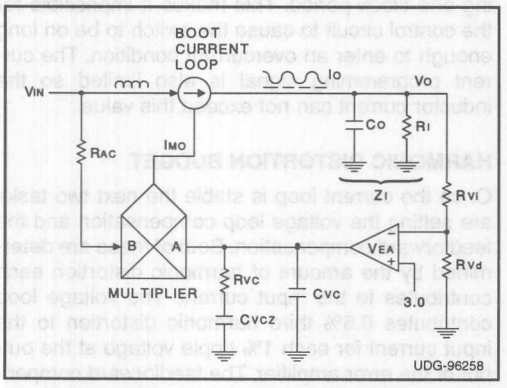


Figure 9. Simplified Block Diagram of a Boost PFC Voltage Loop

The multiplier in the voltage loop adds the current programming signal from the line frequency and it acts like a switching frequency. Therefore the bandwidth of the voltage loop must be kept below $(2 \bullet f_L/\pi)$ to maintain voltage loop stability where f_L is the line frequency. The gain of the error amplifier needs to be high to maintain wide bandwidth in the voltage loop and thus fast transient response but if it is too high the loop will go unstable due to the line frequency introduced by the programming signal in the multiplier. If the gain of the amplifier in the loop is set with a fixed gain to give maximum bandwidth, the DC gain of the loop is reasonable and the output voltage regulation is within a percent or two of the set point.

The relatively wide bandwidth of the loop gives good transient response but also gives little attenuation of the second harmonic ripple voltage on the output capacitor. This voltage modulates the input current so the harmonic distortion of the input current will be too high. Reducing the harmonic distortion requires reducing the gain of the loop at the second harmonic of the power line frequency, which is the ripple voltage frequency on the output capacitor. The bandwidth of the loop must also be kept as high as possible to maintain good transient response. If the loop is closed with an error amplifier having an extra pole just after the unity gain crossover frequency, it is possible to reduce the harmonic distortion and still maintain good loop bandwidth and adequate phase margin.

Figure 10 is a Bode diagram of the resulting loop response. The loop response has a pole at low frequency due to the load resistance and the output capacitance and then rolls off smoothly with a first order slope due to the output capacitor. Just after the gain of the loop crosses 0dB at f_{VI}, a second pole takes the slope to a second order roll off and this reduces the loop gain to the required level at the second harmonic of the line frequency. For greater DC regulation of the output voltage and because of the requirements of the voltage error amplifier on the UC3853, a zero is added to the loop at low frequencies to compensate for the load resistance and output capacitance pole.

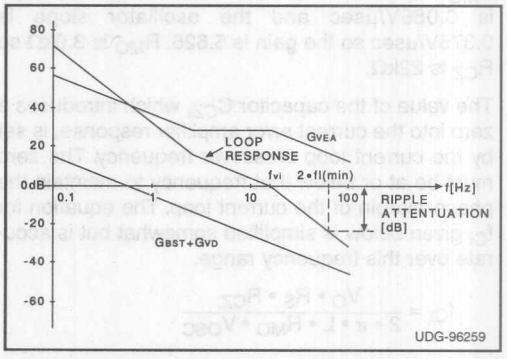


Figure 10. Transfer Functions of Voltage Loop

The design of the voltage loop compensation begins at the output capacitor. The voltage loop compensation reduces the amplitude of the ripple voltage from the output capacitor to a level, at the output of the voltage error amplifier, which is consistent with the harmonic distortion specification. The amount of ripple voltage on the output capacitor, C_O, is given by the following equation.

$$\Delta V_{Opk} = \frac{P}{2 \bullet \pi \bullet 2 \bullet f_{Lmin} \bullet C_O \bullet V_O}$$

Where P is the maximum input power of the converter. Use of the input power in place of the output power is a reasonable compromise since the efficiency of the converter is high. The lowest power

line frequency is f_{Lmin}, the output capacitor value is C_O and V_O is the DC output voltage. For the example converter, P (approximately P_{OUT}) is 100W, f_{Lmin} is 47Hz, C_O is 100µF and V_O is 400VDC. ΔV_{Opk} is therefore 4.2Vpk. Note that this is half the peak-to-peak value. Mathematically, this is the amplitude of the ripple voltage vector. At low line frequencies the ripple voltage is larger as is the gain of the error amplifier because of the loop compensation requirements. If performance is to be maintained over the range of line frequencies, then the lowest frequency must be used for the design.

The gain of the voltage error amplifier and the voltage divider preceding it are determined by the harmonic distortion budget for the voltage loop and the amount of ripple voltage on the output capacitor. The amount of ripple voltage allowed on the output of the voltage error amplifier is equal to twice the percentage of the distortion. Each 1% of second harmonic ripple voltage on the output of the amplifier results in 0.5% third harmonic current on the input. The %ripple on the output of the voltage error must be translated into an absolute voltage to find the gain of the voltage error amplifier and the voltage divider at the second harmonic of the line frequency. The %ripple is multiplied by the range of the output voltage (ΔV_{COMP}) to get the amplitude of the ripple voltage on the output of the amplifier. This is divided by the amplitude of the ripple voltage on the output capacitor to give the combined gain of the voltage error amplifier and the voltage divider. The equation for the gain is:

$$G_V = \frac{\Delta V_{COMP} \bullet \%ripple}{\Delta V_{Opk}}$$

Where G_V is the gain of the voltage divider and the voltage error amplifier, ΔV_{COMP} is the range of the voltage error amplifier output, %ripple is the percentage of ripple voltage allowed in the output of the voltage error amplifier and ΔV_{Opk} is given previously. For the example converter, ΔV_{COMP} is actually the active range of the input to the multiplier rather than the output range of the amplifier. On the UC3853 the active input range of the multiplier is between 1.5V and 6.0V so ΔV_{COMP} is 4.5V. The percent THD of the input current allowed from the voltage loop according to the harmonic distortion budget is 2% which results in 4% ripple voltage at the output of the voltage error amplifier. The numeric value of 0.04 must be used in the equation. The value of ΔV_{Opk} is 4.2V. Therefore:

$$G_V = \frac{4.5 \bullet 0.04}{4.2} = 0.043$$

The voltage divider is composed of R_{VI} and R_{VD} and is determined by the ratio of the DC output voltage to the internal reference voltage in the UC3853, which is 3.0V. The impedance of the voltage divider is somewhat arbitrary. For the example converter the output voltage is over 250V so two resistors are used in series to get the necessary voltage rating. 1.24MΩ is chosen as the divider impedance so two 620kΩ resistors are used for R_{VI}. R_{VD} is determined from the voltage divider equation and the value is just below 10kΩ so a 10kΩ resistor is used with a 150kΩ resistor in parallel. The gain of the voltage divider is given by the following equation:

$$G_{VD} = \frac{R_{VD}}{R_{VD} + R_{VI}}$$

The gain of the voltage divider, G_{VD}, is 0.0075 in the example. The gain of the divider and the voltage amplifier together must be 0.043. The gain of the amplifier at twice the line frequency (low line frequency is 47Hz) must be 5.7 for the example converter.

The gain of a transconductance amplifier is given by $A = G_M \bullet Z_A$. Where A is the voltage gain of the amplifier, G_M is the transconductance of the amplifier and Z_A is the load impedance from the V_{COMP} pin to ground. The transconductance of the amplifier in the UC3853 is 485µmhos. The gain needed for this application is 5.7, so the load impedance is 11.75kΩ. At the second harmonic of the line frequency, the gain of the amplifier is determined by C_{VC}, the voltage compensation capacitor. For the example converter, a capacitor with an impedance of 11.75kΩ at 94Hz has a value of 0.15µF and this is the value used.

The value of R_{VC} is found by extrapolating from the second harmonic frequency back to find the frequency at which the gain of the voltage loop is unity, f_{VI}. R_{VC} is then found by writing the equation for the gain of the loop, setting it to unity and solving the resulting equation for R_{VC}. The loop equation is the product of the gain of the current loop and load impedance, G_{BST}, the gain of the voltage amplifier, G_{VEA}, and the voltage divider, G_{VD}.

The gain of the boost stage is given by the following equation:

$$G_{BST} = \frac{P \bullet X_{CO}}{\Delta V_{COMP} \bullet V_O}$$

Where P is the input power and is here taken to be the output power because of the assumption of high efficiency. X_{CO} is the impedance of the output capacitor and varies with frequency. ΔV_{COMP} is the range of the voltage error amplifier output and is equal to 4.5V on the UC3853. V_O is the DC output voltage. By using the output power ($V_O \bullet I_O$) in the equation, all of the terms that are associated with the multiplier and divider drop out of the equation.

The gain of the voltage divider, G_{VD}, is given above. The gain of the transconductance amplifier and its load are given by the following:

$$G_{VEA} = G_M \bullet X_{CVC}$$

Where G_M is the transconductance of the amplifier and X_{CVC} is the impedance of the compensation capacitor C_{VC}.

Finally, the equation for the loop can be written from these equations as:

$$G_V = \frac{P \bullet X_{CO} \bullet G_M \bullet X_{CVC} \bullet G_{VD}}{\Delta V_{COMP} \bullet V_O}$$

By setting $G_V = 1$ the equation can be solved for frequency since all other variables are known at this point. Note that there are two terms in the equation which vary with frequency, X_{CO} and X_{CVC}. The loop has a second order roll off at this point so the equation is solved for the square of the frequency. The unity gain crossover frequency, f_{VI}, is found from the following equation.

$$f_{VI}^2 = \frac{P \bullet G_M \bullet G_{VD}}{(2 \bullet \pi)^2 \bullet C_O \bullet C_{VC} \bullet \Delta V_{COMP} \bullet V_O}$$

For the example converter f_{VI} is 18.6Hz. The value of R_{VC}, which is what we have been trying to determine all along, is equal to the impedance of C_{VC} at f_{VI}. For the example converter, this is 57kΩ, so a 56kΩ standard value resistor is chosen.

The last step is the addition of a low frequency zero in the feedback loop. It is accomplished by adding C_{VCZ} in series with R_{VC} as shown in the schematic. From an operational standpoint, the effect of C_{VCZ} is to double the peak-to-peak variation of the output voltage during a step load transient. The overvoltage protection circuit built into the UC3853 will prevent the output voltage from exceeding the maximum value by turning the switch off until the output voltage is back within range. The undervoltage transient caused by a step load change will be unaffected.

The value of C_{VCZ} is not especially critical. However, since it adds both a pole and an zero to the loop gain, the zero must be far enough away in frequency from the C_{VC} and R_{VC} pole so that it does not contribute extra phase shift at the unity gain frequency, f_{VI}. This requires that the zero be at least two octaves below f_{VI}. For the example converter, the zero has been placed almost a full decade below f_{VI} and the value of C_{VCZ} is chosen as 1.0μF.

THE FEEDFORWARD VOLTAGE AND STARTUP CIRCUIT

The UC3853 makes use of a divider and squaring circuit to compensate the gain of the voltage loop for changes of the input voltage as shown in Figure 5. The input to the squarer and divider is the supply voltage to the UC3853 and is called V_{FF}. The function of the supply voltage, besides powering the chip, is to feed-forward information about the input voltage to the voltage loop. This means that V_{FF} must be proportional to the average value of the input voltage and must also have low ripple voltage because 1% ripple on this voltage will create 1% harmonic distortion on the input current.

The V_{FF} input is generated by a winding on the boost inductor that operates like a transformer. When the switch is turned on, the voltage across the inductor is equal to the input voltage. This voltage is tapped off by using an additional winding on the inductor to supply the control circuits. The current drain of the control circuits, I_{CC}, is typically about 15mA of which 10mA are allocated to the UC3853 and 5mA are allocated to the MOSFET gate drive current. These currents are constant and do not change appreciably with a change of the supply voltage.

The supply voltage range of the UC3853 is great enough to cover a 3:1 input voltage range. To provide the best utilization of the V_{FF} programming range the supply voltage to the UC3853 should be set to provide 10.5V when the input voltage is at low line. If a narrower range is being used for the input voltage than is used for this example, it may be desirable to set the minimum voltage slightly higher, in the range of 12V to 15V, to provide more voltage for the gate drive at lower line voltages and thus lower R_{DSon}. For the example converter, a turns ratio of 10:1 on the inductor will provide the correct value of V_{FF}. The minimum voltage is about 10.5V, with an input line voltage of 80VAC, after all of the diode drops have been taken into account. The UVLO threshold for turning the UC3853 off is 9.5V so a 10.5V minimum value of V_{FF} leaves some margin in the design for component variation.

The diode D_{FF} must block 80V, carry an average current of 15mA for the example converter and have a very fast recovery time. Small 100V diodes, such as BYD71B or MUR110 are suitable devices for this application.

The amount of harmonic distortion allocated to the V_{FF} input of the UC3853 is 2%, so the ripple voltage must be held to 2% of the minimum value of V_{FF}. For the example converter, the minimum voltage is 10.5V so the allowable ripple voltage is 0.21V. This is not the peak-to-peak value of the ripple but is the peak value of the second harmonic of the line frequency. The peak-to-peak ripple voltage, ΔV_{FF}, is this value multiplied by π. For the example converter, ΔV_{FF} is therefore 0.66V peak-to-peak.

The value of C_{FF} can be found from the equation for a capacitor and the current drain of the control circuits, I_{CC}.

$$C_{FF} = \frac{I_{CC}}{\Delta V_{FF} \bullet 2 \bullet f_{Lmin}}$$

Where C_{FF} is the value of the V_{FF} bypass capacitor, I_{CC} is the current drain of the control circuits, ΔV_{FF} is the peak-to-peak ripple voltage on V_{FF} and f_{Lmin} is the minimum line frequency. For the example converter the value is 240µF. A standard value of 270µF is chosen and it is bypassed with a 0.1µF ceramic capacitor.

This value for C_{FF} also gives sufficient time to start the circuit since one half cycle of the input line frequency is needed to reach full operation. The turn-on threshold of the UC3853 is 11.5V and the turn-off threshold is 9.5V so there is more than sufficient energy stored to begin circuit operation.

$$\Delta t = \frac{C_{FF} \bullet (V_{TN} - V_{TF})}{I_{CC}}$$

Where Δt is the amount of time available for start-up, C_{FF} is the capacitance on V_{FF}, V_{TN} is the turn on threshold of the UC3853 (11.5V), V_{TF} is the turn off threshold (9.5V), and I_{CC} is the current drain of the control circuits. For the example converter Δt is 36 milliseconds.

Startup of the UC3853 is accomplished by charging V_{FF} to 11.5V through R_B. The value of R_B must be small enough to provide a reasonably short turn-on delay after power is applied and yet large enough to keep power dissipation low. The current through R_B at V_{INmin} must also be greater than the UC3853 startup current (500µA). For the example converter a 1 second delay at turn-on requires a bias current of approximately 3mA from the low input line voltage. The equivalent resistance is about 36kΩ. This resistance needs to be split into two equal resistors since the peak input voltage will exceed 250V so two 18kΩ resistors are used. At high line this gives about 6.8mA of bias current to V_{FF}. This is less than the current required by the UC3853 so this value of R_B is acceptable. If the current at high line were too great, V_{FF} would not accurately reflect the input voltage and performance would suffer. A larger value of R_B resulting in a longer turn-on delay is required in that case. At high line each of the 18kΩ resistors dissipates 0.82W. A 2W rating is specified.

The gate drive voltage of the UC3853 is limited to 15V by an internal clamp. This allows V_{FF} to change without causing the gate voltage to exceed the rating of the MOSFET. The UC3853 is designed to drive moderate size MOSFET switches, and the gate drive current is limited to 500mA(pk). This is more than sufficient to obtain the fast rise and fall times needed for high efficiency. R_Q is the resistor in series with the gate of the MOSFET. Its value of 33Ω is chosen to limit the peak gate current to about 350mA under normal operating conditions. In addition, this is the minimum value for which D_Q, the gate drive clamp, is NOT required under most circumstances. In general, if R_Q is made small there will not be sufficient damping of the resonance of the parasitic circuit inductances with the MOSFET gate capacitance, so the output of the UC3853 could be drawn below ground. Keeping R_Q in the range of 30Ω to 60Ω prevents this, eliminates the need for D_Q and at the same time provides ample output current for fast rise and fall times on the drain of the MOSFET. It is wise practice to leave room for D_Q on the circuit board until it can be verified in the laboratory that it is not needed.

OVER CURRENT PROTECTION

The boost converter is inherently unprotected against any overload situation. Because the switch is connected in parallel with the input source, the DC current path through the inductor, diode and the load impedance (parallel combination of C_O and R_L) can not be interrupted. The result is practically unlimited current flowing from the input to the output of the converter when the output voltage falls below the input voltage. This happens every instance when power is being applied to the converter at startup and when the load requires more power than the circuit was originally designed for. Unfortunately, these situations can not be avoided, but there are certain measures which can protect the circuit from a catastrophic failure.

The diode, D_{BP} in Figure 6 provides protection for the boost inductor and for the output rectifier, D_{OUT}. During the initial charging of the output capacitor at startup and in case of an overload, a high surge current flows from the input to the output of the converter. This high peak current would flow through the boost inductor and the very sensitive high speed epitaxial diode used for rectification. This high surge current can saturate the inductor and damage the diode causing a disastrous failure eventually. D_{BP} prevents the high current flowing in the inductor-diode path by providing a lower impedance direct path between the input and the output. The additional benefit of the D_{BP} diode is the protection against input voltage transients. When other high power loads are connected to the same distribution branch of the power line, their turn off generates huge inductive spikes appearing at the input of the power factor corrector power supply. This can cause the input voltage of the boost converter to be higher than its output voltage even under normal operating conditions. The voltage

spikes impose an increased voltage stress on the input rectifier diodes and it might cause the boost inductor to saturate depending on the duration and the amplitude of the line transient. The addition of the D_{BP} diode clamps the input voltage to the output capacitor voltage which will also absorb the transient energies without passing high current through the boost inductor and rectifier diode.

In normal circumstances D_{BP} has no effect on the circuit operation. Note that the diode D_{BP} can not prevent the circuit from developing high currents from the input to the output. It simply provides a safe passage for the high current to pass through the circuit. Once the high current is flowing, it has to go through the current sense resistor, R_S. Higher than nominal currents will develop negative voltage across R_S in excess of the 1V maximum value used in the design. Since the I_{MO} current is limited to 0.5 • I_{AC}, the IMO pin of the UC3853 will be pulled below ground. This could present a problem for the integrated circuit because of reverse biasing the substrate. When the IMO pin is pulled 0.3V below ground (to -0.3V), the OUT pin goes high turning on the main switch of the boost converter. Since the current can not be limited, the only way to avoid the parasitic turn on of the output is to limit the negative voltage on the IMO pin of the IC. It is accomplished by the Schottky diode, D_{MO} connected between the IMO pin of the UC3853 and circuit ground, as shown in Figure 6.

ABOUT SYNCHRONIZATION

Synchronization of the UC3853 oscillator requires a fast falling edge on the FB pin. The minimum requirements for the falling edge of the waveform are that it must have a slope of at least 20V/µsec and an amplitude of at least 1.0V. Faster fall times and greater amplitudes are strongly recommended. The amplitude of the sync signal must be kept below 3.0V so that the FB pin is not driven below ground. The sync signal must be capacitively coupled into the FB pin so that the DC feedback is not disturbed by the synchronization. The capacitor must be large enough so that it does not gain enough voltage during the pulse to trip the overvoltage comparator of the UC3853 on the rising edge of the sync waveform. These requirements are easily met with the circuit of Figure 11 as shown below.

In most applications the UC3853 will be synchronized to another PWM integrated circuit used to control the DC output voltage of the power supply. A few PWM integrated circuits, such as the UC3526A, have inverted pulse sync outputs and these can be interfaced to the UC3853 with just a small capacitor. Other PWM circuits have an output pulse which is positive and has a narrow pulse width. This signal needs to be inverted and conditioned to interface with the UC3853. If the pulse is more than 100nsec wide then the signal must be shortened as well. Some PWM integrated circuits do not have a sync output but these can still be synchronized with a little ingenuity and a few small parts.

A schematic of a generic sync circuit is shown in Figure 11. This circuit accepts a positive input pulse and provides the correct output pulse to the FB pin of the UC3853. The pulse is capacitively coupled to the FB pin through C_{SYNC}. The value of this capacitor is chosen so that the voltage change across it during a 2.5V pulse of 100 nanoseconds duration is about 100mV. This precludes the sync pulse having a significant effect on the UC3853 output voltage. If R_{VD} in Figure 6 is about 10kΩ then C_{SYNC} will be about 220pF. A larger value for C_{SYNC} may be used but the capacitor adds a pole to the feedback loop and the pole must be kept above the switching frequency. The voltage divider R_{SVD1} and R_{SVD2} reduce the effect of the pole by providing a compensating zero so their impedance must be relatively high. A value of 22kΩ was chosen to present a 10k impedance to the feedback network and thus keep the additional pole and zero relatively close together. The 5V source for the voltage divider is supplied from another PWM integrated circuit.

An NPN transistor is shown in Figure 11 to invert the input signal and drive the FB pin of the UC3853. Any fast general purpose small signal transistor will work in this application. The network chosen for the base of the transistor depends on the clock that it is being interfaced to. The base network shown in Figure 11 allows the circuit to work with a wide variety of inputs. C_{ST} and R_{ST} form a 100nsec time constant which will limit the width of the sync pulse output. The resistor R_{SB} and diode D_{SB} provide reset for the sync input time constant. A relatively fast rising edge on the input pulse is required for proper circuit operation.

As an example of synchronization, the sync circuit in Figure 11 may be used with the UC3525B by

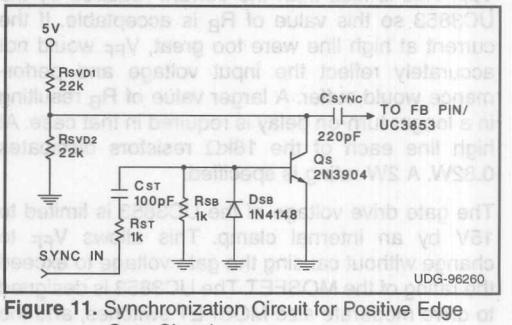


Figure 11. Synchronization Circuit for Positive Edge Sync Signals

connecting the sync circuit input to the CLOCK output. The UC3525B has a positive going clock pulse whose width is equal to the discharge time of the timing capacitor. If the clock pulse width is small, below 100nsec, the input capacitor to the sync circuit, C_{ST}, may be eliminated.

Figure 12 shows a sync circuit for the UCC3802. This circuit may be modified for use with other PWM control circuits that do not have an oscillator sync output. The UCC3802 discharges the timing capacitor C_T with a 1.8mA current. The sync circuit is configured so that when C_T discharges, a negative voltage appears across R_{ST}. The emitter of Q_S is connected here and when the C_T is being discharged most of the current flows through Q_S and takes it into saturation. The collector of Q_S is connected to the FB pin of the UC3853 through the same network described above. The base of Q_S is biased above ground because the timing capacitor C_T will not discharge completely in this circuit due to the voltage offset of the emitter base junction of Q_S. This offset voltage changes the amplitude of the oscillator voltage and its frequency. By raising the base of Q_S above ground, the offset voltage is minimized. The offset voltage also has a temperature coefficient and D_S compensates for this so that the oscillator frequency drift over temperature will be reduced. All of the base components are optional but they do improve the performance of the sync circuit.

Further information about synchronization in general may be found in Unitrode Application Note U-111. Several of the circuits there may be adapted to the UC3853 synchronization circuits shown here.

LAYOUT CONSIDERATIONS

The UC3853 is a high speed circuit generally operating in a high noise environment. It requires careful layout and grounding to operate correctly. A ground plane extending at least 1 inch on each side of the device is recommended to control noise pickup. Do not let power currents in the ground plane run beneath the device. A split in the ground plane is acceptable to control the flow of current and divert it around the device if necessary. It is worthwhile to keep low level signals as far away from high noise signals, such as the output gate drive, as possible. Good bypassing of the VCC pin is essential. A 0.1μF ceramic capacitor connected between VCC and GND should be located within 0.5 inch of the UC3853 and connected with short, direct connections. The IMO pin and the FB pin are especially sensitive to noise because they are high impedance nodes. Keep the amount of printed circuit board trace connected to these pins as short as possible. The total length should be kept less than 1 inch. The general rule of thumb for printed circuit board layout is to place the UC3853 in the desired position and then to place the ceramic bypass capacitor as close to the VCC pin as possible. Then, and only then, proceed with placing the other components.

DISCONTINUOUS CONDUCTION MODE AND LIGHT LOAD OPERATION

The boost converter described in this Application Note normally runs in continuous inductor current mode but enters discontinuous conduction mode when the input voltage is low and when the load current is light. In discontinuous conduction mode the gain of the boost power stage is reduced which can lead to reduced performance. The UC3853 uses an average current control technique where the boost power stage is embedded in a feedback loop that includes a high gain opamp which compensates for the changes in gain. The average current control loop regulates the input current in the converter and maintains the correct input current

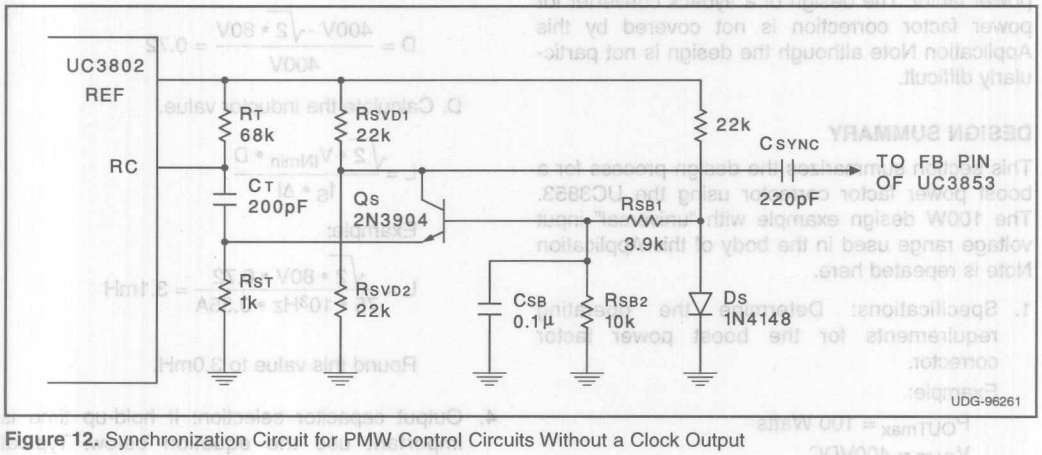


Figure 12. Synchronization Circuit for PMW Control Circuits Without a Clock Output

wave shape even though the current through the inductor is not continuous.

During operation of the converter at light loads, the input filters can contribute phase shift to the input current that reduces the power factor. Careful design is required to maintain high power factor at light loads. A capacitor, generally included after the input diodes as part of the input filter, is necessary to keep the high frequency ripple current from the boost converter out of the power lines. At light loads this capacitor holds charge as the input voltage goes through zero volts and turns the diode bridge off, introducing distortion into the input current. This is why the input capacitor value must be carefully selected.

It is possible to design a power factor corrector using the UC3853 which operates only in discontinuous inductor current mode. Such a converter will have good power factor and low distortion input current but it will also have high input ripple current which must be filtered out to pass EMI requirements. The design of a discontinuous conduction mode boost power factor corrector is not covered in this Application Note.

Another application of the UC3853 is with a flyback converter to produce a power factor corrected input current and a regulated and, optionally, isolated output voltage. Any power factor corrected converter produces a sinusoidal output current at the second harmonic of the input line frequency so a large amount of filtering or secondary regulation may be necessary to provide a useful output in most applications. The flyback converter may be operated in either continuous or discontinuous conduction modes. Both modes have large amounts of high frequency input current that must be filtered out to meet EMI requirements and the filter produces phase shift of the input current and reduces the power factor. The design of a flyback converter for power factor correction is not covered by this Application Note although the design is not particularly difficult.

DESIGN SUMMARY

This section summarizes the design process for a boost power factor corrector using the UC3853. The 100W design example with "universal" input voltage range used in the body of this Application Note is repeated here.

1. Specifications: Determine the operating requirements for the boost power factor corrector.

   Example:

   P_{OUTmax} = 100 Watts
   V_{OUT} = 400VDC
   Line voltage range = 80 to 270VAC
   Line frequency range = 47 to 65Hz
   Maximum THD = 5%
   Power Factor = 0.99

2. Switching frequency: The switching frequency is fixed at 75kHz but may be synchronized in the range of 95kHz to 115kHz. See the text for further information on synchronization.

3. Inductor selection:

   A. Find the maximum peak line current. Assume $P_{IN} = P_{OUT}$ and use P for the power rating.

   $$Ipk = \frac{\sqrt{2} \bullet P}{V_{INmin}}$$

   Example:

   $$Ipk = \frac{\sqrt{2} \bullet 100W}{80V} = 1.77Apk$$

   B. Find ΔI, the peak-to-peak high frequency ripple current. See the text for information on the selection of the ripple current. The typical range is 15 to 25% of Ipk.

   $$\Delta I = 0.2 \bullet Ipk$$

   Example:

   $$\Delta I = 0.2 \bullet 1.77Apk = 0.35Apk\text{-}pk$$

   C. Find the minimum duty factor, D, at $V_{INmin(pk)}$. This occurs at Ipk.

   $$D = \frac{V_O - \sqrt{2} \bullet V_{INmin}}{V_O}$$

   Example:

   $$D = \frac{400V - \sqrt{2} \bullet 80V}{400V} = 0.72$$

   D. Calculate the inductor value.

   $$L = \frac{\sqrt{2} \bullet V_{INmin} \bullet D}{f_S \bullet \Delta I}$$

   Example:

   $$L = \frac{\sqrt{2} \bullet 80V \bullet 0.72}{75 \bullet 10^3 Hz \bullet 0.35A} = 3.1mH$$

   Round this value to 3.0mH.

4. Output capacitor selection: If hold-up time is important use the equation below. Typical

values for a 400V output are 1μF to 2μF per Watt. If hold-up is not required, use the second harmonic ripple voltage and capacitor power dissipation to determine the minimum size of the capacitor. Δt is the hold-up time in seconds and V_{Omin} is the voltage to which the output decays at the end of the hold-up time.

$$C_O = \frac{2 \bullet P \bullet \Delta t}{V_O^2 - V_{Omin}^2}$$

Example: V_{Omin} is 350V and Δt is 19msec.

$$C_O = \frac{2 \bullet 100W \bullet 19 \bullet 10^{-3}sec}{(400V)^2 - (350V)^2} = 100\mu F$$

5. Current sense resistor selection: Select the current sense resistor to give 1.0V at the maximum peak input current.

$$R_S = \frac{1V}{Ipk + \frac{\Delta I}{2}}$$

Example:

$$R_S = \frac{1V}{1.77A + 0.5 \bullet 0.35A} = 0.5\Omega$$

6. Switch and diode selection: The switches and diodes may be selected from the table which follows this section or may be chosen by any other standard design criteria. The text discusses selection criteria.

   The output drive of the UC3853 provides about 500mA peak current. Choose R_Q to limit the current under normal operating conditions. A value of 33Ω or more will provide adequate control of the gate charge current, give good rise and fall times for small switches and eliminates the need for D_Q. If a lower value of R_Q is chosen, then D_Q is required.

7. Input diode and capacitor selection: Fast recovery rectifiers are recommended for D_{IN}. The faster the diode reverse recovery the lower the input current distortion will be. Choose a diode type rated for the maximum voltage at high line and for the maximum current at low line. It must also have adequate power dissipation capability.

   The choice of C_{IN} is a compromise between power factor and EMI performance. The value may not be too large or input distortion increases. The value may not be too small or EMI increases. Choose a device which will handle the full high frequency ripple current from the boost converter. A film or ceramic type is generally recommended. See the text for further selection information.

8. Multiplier set up: I_{AC} is 500μA maximum. R_{AC} is determined by Ohm's law.

$$R_{AC} = \frac{\sqrt{2} \bullet V_{INmax}}{0.5 \bullet 10^{-3}A}$$

   Example:

$$R_{AC} = \frac{\sqrt{2} \bullet 270V}{0.5 \bullet 10^{-3}A} = 764k\Omega$$

   Choose two standard value 390kΩ resistors in series to allow for voltage stress ratings.

9. Current amplifier gain at the switching frequency:

   A. Calculate ΔV_{RS}, the voltage change across the sense resistor due to the down slope of the inductor current if V_{IN} = 0 (at the zero crossing).

$$\Delta V_{RS} = \frac{V_O \bullet R_S}{L \bullet f_S}$$

   Example:

$$\Delta V_{RS} = \frac{400V \bullet 0.5\Omega}{3 \bullet 10^{-3}H \bullet 75 \bullet 10^3Hz} = 0.89V$$

   B. The gain of the current amplifier at the switching frequency is the ratio of the oscillator voltage and ΔV_{RS}. The oscillator voltage in the UC3853 is 5.0Vpk-pk.

$$G_{CA} = \frac{V_{OSC}}{\Delta V_{RS}}$$

   Example:

$$G_{CA} = \frac{5V}{0.89V} = 5.625\ (15.0dB)$$

10. Current amplifier compensation:

    A. R_{MO} selection: R_{MO} = 3.9kΩ

    B. R_{CZ} selection: R_{CZ} sets the gain of the amplifier at the switching frequency.

    $R_{CZ} = G_{CA} \bullet R_{MO}$

    Example:

    $R_{CZ} = 5.625 \bullet 3.9k\Omega = 22k\Omega$

    C. C_{CZ} selection: Calculate the unity gain crossover frequency of the current loop if C_{CZ} were not present.

$$f_{CI} = \frac{V_O \bullet R_S \bullet R_{CZ}}{V_{OSC} \bullet 2 \bullet \pi \bullet L \bullet R_{MO}}$$

Example:

$$f_{CI} = \frac{400V \bullet 0.5\Omega \bullet 22 \bullet 10^3\Omega}{5V \bullet 2 \bullet \pi \bullet 3 \bullet 10^{-3}H \bullet 3.9 \bullet 10^3\Omega}$$

$$= 12 \bullet 10^3 Hz$$

Choose the value of C_{CZ} to have an impedance equal to or less than R_{CZ} at f_{CI}.

$$C_{CZmin} = \frac{1}{2 \bullet \pi \bullet f_{CI} \bullet R_{CZ}}$$

Example:

$$C_{CZmin} = \frac{1}{2 \bullet \pi \bullet 12 \bullet 10^3 Hz \bullet 22 \bullet 10^3\Omega}$$

$$= 600 \bullet 10^{-12}F$$

Choose a larger value of capacitance to increase the phase margin. C_{CZ} = 680pF.

D. C_{CP} selection: The C_{CP} and R_{CZ} pole must be greater than the switching frequency.

$$C_{CPmax} = \frac{1}{2 \bullet \pi \bullet f_S \bullet R_{CZ}}$$

Example:

$$C_{CPmax} = \frac{1}{2 \bullet \pi \bullet 75 \bullet 10^3 Hz \bullet 22 \bullet 10^3\Omega}$$

$$= 100 \bullet 10^{-12}F$$

Choose a smaller value of capacitance.

C_{CP} = 68pF

11. Harmonic Distortion Budget: The allocation of the allowed THD among the main error sources is somewhat arbitrary. The feedforward voltage contributes 1% third harmonic distortion for each 1% second harmonic on the bias supply to the UC3853. The voltage loop contributes 0.5% third harmonic distortion for each 1% second harmonic voltage on the output.

    Example: The specification is for 5% THD maximum. 2% is allocated to the feedforward voltage, 2% is allocated to the voltage control loop and 1% to miscellaneous sources.

12. Voltage amplifier: The voltage loop amplifier is a transconductance amplifier so its compensation is a bit different from other types of amplifiers.

    A. Voltage Divider: R_{VI} and R_{VD}. This voltage divider sets the DC output voltage. The UC3853 reference voltage is 3.0V. Choose a value for R_{VD} and calculate the value for R_{VI} from the equation.

$$R_{VI} = R_{VD} \bullet \left(\frac{V_O}{V_{FB}} - 1\right)$$

Example:

Choose $R_{VD} = 10k\Omega$.

$$R_{VI} = 10 \bullet 10^3\Omega \bullet \left(\frac{400V}{3V} - 1\right) = 1.3 \bullet 10^6\Omega$$

Choose two standard value 620kΩ resistors in series for R_{VI} to allow for the resistor voltage rating.

Solve for a parallel resistance to R_{VD} to get correct output voltage.

$$R_{VD} = \frac{R_{VI} \bullet V_{FB}}{V_O - V_{FB}}$$

Example:

$$R_{VD} = \frac{1.24 \bullet 10^6\Omega \bullet 3V}{400V - 3V} = 9.37 \bullet 10^3\Omega$$

This is 10kΩ in parallel with 150kΩ.

B. Voltage divider gain: The gain of the voltage divider is given from the following equation:

$$G_{VD} = \frac{V_{FB}}{V_O}$$

Example:

$$G_{VD} = \frac{3V}{400V} = 0.0075 \ (-42.5dB)$$

C. Output ripple voltage: Output ripple voltage is given by the following equation where f_{Lmin} is the minimum line frequency. Low line frequency will give the greatest value of V_{Opk}.

$$V_{Opk} = \frac{P}{2 \bullet \pi \bullet 2 \bullet f_{Lmin} \bullet C_O \bullet V_O}$$

Example:

$$V_{Opk} = \frac{100W}{2 \bullet \pi \bullet 2 \bullet 47Hz \bullet 100 \bullet 10^{-6}F \bullet 400V}$$

$$= 4.2V$$

D. Amplifier Gain: This gain calculation includes the gain of the voltage divider. The

input range to the multiplier is the active range of the amplifier output voltage on the UC3853. ΔV_{COMP} is 4.5V on the UC3853. The %ripple used in the equation below is the amplitude of the ripple at the output of the voltage amplifier as a percentage of ΔV_{COMP} and the percentage is twice that specified for second harmonic voltage since the ripple is reduced by half in the power circuits. The equation uses %ripple in its numeric form.

$$G_V = \frac{\Delta V_{COMP} \bullet \%ripple}{V_{Opk}}$$

Example:

$$G_V = \frac{4.5V \bullet 0.04}{4.2V} = 0.043\ (-27.3dB)$$

The gain of the voltage error amplifier alone is G_V divided by the gain of the voltage divider.

$$G_{VEA} = \frac{G_V}{G_{VD}}$$

Example:

$$G_{VEA} = \frac{0.043}{0.0075} = 5.73\ (15.2dB)$$

E. Amplifier Compensation: A network connected from the output of a transconductance amplifier to ground determines its gain and frequency response. The gain of the amplifier is set for loop stability without regard to DC gain or THD. Those considerations come next. The gain of the amplifier is:.

$$G_{VEA} = G_M \bullet X_{CVC}$$

Where G_M is the transconductance of the UC3853 voltage amplifier as specified in the data sheet as 485µS. X_{CVC} is the impedance of C_{VC} at the second harmonic of the line frequency ($2 \bullet f_{Lmin}$). Solve the equation for X_{CVC} then convert the impedance to a capacitance value.

$$C_{VC} = \frac{G_M}{2 \bullet \pi \bullet 2 \bullet f_{Lmin} \bullet G_{VEA}}$$

Example:

$$C_{VC} = \frac{485 \bullet 10^{-6}S}{2 \bullet \pi \bullet 2 \bullet 47Hz \bullet 5.73} = 0.15 \bullet 10^{-6}F$$

F. Unity Gain Voltage Loop Crossover Frequency: The unity gain frequency of the now completed voltage control loop is found next. The following equation gives the frequency at which the loop gain is equal to one. Solve for f_{VI}.

$$f_{VI}^2 = \frac{P \bullet G_M \bullet G_{VD}}{(2 \bullet \pi)^2 \bullet C_O \bullet C_{VC} \bullet \Delta V_{COMP} \bullet V_O}$$

Example:

$$f_{VI} = \frac{1}{2 \bullet \pi} \bullet \sqrt{\frac{100W \bullet 485 \bullet 10^{-6}S \bullet 0.0075}{100 \bullet 10^{-6}F \bullet 0.15 \bullet 10^{-6}F \bullet 4.5V \bullet 400V}}$$

$$= 18.6Hz$$

G. R_{VC}: R_{VC} is added to the loop compensation to give a pole at f_{VI}. The value of R_{VC} is the resistance equal to the impedance of C_{VC} at f_{VI}. This gives approximately 45° of phase margin. A smaller value of R_{VC} will increase the phase margin at the expense of loop bandwidth.

$$R_{VC} = \frac{1}{2 \bullet \pi \bullet f_{VI} \bullet C_{VC}}$$

Example

$$R_{VC} = \frac{1}{2 \bullet \pi \bullet 18.6Hz \bullet 0.15 \bullet 10^{-6}F}$$

$$= 57 \bullet 10^3\Omega$$

The closest standard value is 56kΩ.

H. C_{VCZ}: C_{VCZ} is added in series to R_{VC} to break the DC current path from the output of the voltage error amplifier to ground because the limited current capability of the transconductance amplifier stage. The zero added to the loop compensation increases the DC regulation of the output at the expense of increased peak-to-peak voltage excursions during transients. This zero introduced by C_{VCZ} must be set at least two octaves below f_{CI} to maintain a reasonable phase margin. The value of C_{VCZ} must therefore be at least four times the value of C_{VC}.

$$C_{VCZ} = 4 \bullet C_{VC}$$

Example:

$$C_{VCZmin} = 4 \bullet 0.15\mu F = 0.6\mu F$$

Choose C_{VCZ} = 1.0µF to give increased phase margin.

13. Voltage Feedforward: The feedforward voltage comes from the bias supply V_{FF}, which is supplied by a winding on the inductor. For the example converter, the turns ratio is set to give 10.5VDC with minimum input voltage after all parasitic losses are taken into account. The second harmonic ripple voltage must be held to 2% peak of V_{FFmin} according to the THD budget in step #10 above. The numeric value of THD is used in the equation. See the text for further information. The peak-to-peak ripple voltage is given by:

$$V_R = \pi \bullet V_{FF} \bullet THD$$

Example:

$$V_R = \pi \bullet 10.5V \bullet 0.02 = 0.66Vpk\text{-}pk$$

The current drawn by the control circuits is about 15mA. The value of C_{FF} is given by:

$$C_{FF} = \frac{I_{FF}}{V_R \bullet 2 \bullet f_{Lmin}}$$

Example:

$$C_{FF} = \frac{0.015A}{0.66V \bullet 2 \bullet 47Hz} = 242 \bullet 10^{-6}F$$

Choose a standard value of 270µF.

14. Starting Resistors: C_{FF} must be charged to 11.5V to start the UC3853 and it is trickle charged from V_{IN} by the current through R_B. The current through R_B at high line must not exceed the bias current of the UC3853 or V_{FF} will not track the input voltage and feedforward will be lost. The value of R_B may not be too large or the delay between the application of power and the start of the circuit will be too long. If the current through R_B is less than 500µA at low line the circuit will never start. A 1sec delay at low line is chosen as the maximum value. This is an arbitrary decision within the guidelines given.

$$R_B = \frac{t_{DELAY} \bullet \sqrt{2} \bullet V_{INmin}}{V_{FF} \bullet C_{FF}}$$

Example:

$$R_B = \frac{1sec \bullet \sqrt{2} \bullet 80V}{11.5V \bullet 270 \bullet 10^{-6}F} = 36 \bullet 10^{3}\Omega$$

Split this into two 18kΩ resistors because the voltage at high line is greater than 250V peak. At high line this gives 6.8mA of bias current which is less than I_{FF} (15mA) so this value is acceptable.

15. This completes the design of the boost power factor corrector.

INDUCTOR DESIGN

The 3.0mH inductor may be built as follows:

Core: Micrometals T157-8/90 — OD = 1.57in.
ID = 0.95in. Ht = 0.57in. m = 35
Main winding: 250 turns #20AWG
Auxiliary winding: 25 turns #28AWG

DESIGN TABLE FOR "UNIVERSAL" INPUT VOLTAGE RANGE

P_{OUT}	25	50	75	100	125	150	200	(Watts)
L	12	6.0	4.0	3.0	2.5	2.0	1.5	(mH)
C_O	25	50	75	100	125	150	200	(µF)
R_S	2.0	1.0	0.68	0.5	0.39	0.33	0.25	(Ω)
C_{IN}	0.22	0.5	0.68	1.0	1.0	1.0	1.0	(µF)
Q	IRF820 ---------->		I RF830 ---------->					
D_{OUT}	MUR160 -------->I		MUR460 ----->I		MUR860 ---------->I			
	BYV26C -------->I		BYM26C ------>I					
D_{IN}	1N4005 --------->I MR856 ---------->I							
	1N4937 --------->I BYW95C ---------->I							

Note: The values of the control circuit components remain the same and do not change with power output as long as the main component values are selected from the table. The control circuit components do change value under several circumstances: 1) The main component values are different from those given in the table. 2) The input voltage range or frequency range is different from that specified for the example converter. 3) The THD budget is different. 4) The output voltage is different.

The core is an iron powder toroid. The two windings must be phased properly for correct operation of the converter. The main winding is best wound with bank or progressive winding rather than layer winding. Progressive or bank winding starts at one point on the core and winds progressively around the core until all the turns are in place. A small amount of backing up is required to get the wires to lay evenly on the core. The object is to get the turn-to-turn voltage to be as low as possible. This reduces the effective capacitance of the winding and increases the resonant frequency as well as eliminating the possibility of corona in the winding. The auxiliary winding needs to be insulated from the main winding and is wound outside the main winding.

HEAT SINK

The switch in the example converter dissipates approximately 8W at low line input. The heat sink is an Aavid 529802 and has a thermal resistance of 5°C/W.

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APPENDIX A: WHAT IS POWER FACTOR?

If a resistor is connected to a sinusoidal AC power line, the current will be sinusoidal and it will be in phase with the voltage. Any deviation from this ideal results in distortion of the current waveform. The apparent power delivered to the load is the sum of the real power and the distortion. The ratio of the apparent power delivered to the load and the real power delivered is the power factor and has a value between zero and one. The current through a purely resistive load has no phase shift and no harmonic distortion and so has a power factor of 1.0. Power factor is given by the following equation:

$$PF = \frac{\text{Real Power}}{V_{RMS} \bullet I_{RMS}}$$

The distortion of the input current has two components, a linear component which is the phase shift between the voltage and current and a non-linear component which is the harmonic distortion of the current waveform. The above equation for power factor may be solved for the phase distortion and the result becomes:

$$PF = \cos(\Theta)$$

Where Θ is the angle between the voltage sinusoid and the current sinusoid. This is the classic definition of power factor as used by electric utilities and it is the major form of distortion created by linear circuits such as motors.

The equation for power factor may also be solved for the harmonic distortion and the equation becomes:

$$PF = \frac{1}{\sqrt{1 + (THD)^2}}$$

Where THD is the Total Harmonic Distortion of the current. This equation is the one with which we are most concerned in power electronics.

In a typical power electronics application the sinusoidal voltage from the power line is rectified and filtered to produce a high DC voltage which is then changed by a DC/DC converter to some other voltage which is useful to the system. The current from the rectifier and input filter generally has little phase shift but has much distortion. A choke input filter will produce a square wave input current with a power factor of about 0.9 and a THD near 50%. A capacitor input filter will produce a train of sharp current spikes with a power factor near 0.5 and THD over 100%. A power factor corrected input will produce a sinusoidal current which has a power factor of greater than 0.99 and harmonic distortion well below 5% at nominal load.

Power factor correction is required in much of the European Community for many electronic products. Power factor correction simplifies the distribution of electric power and thus reduces the cost to the consumer. It is expected that the requirement for power factor correction will grow in the future.

The boost power factor corrector is a boost converter whose control circuit programs the input current to be proportional to the input voltage and thus the input impedance appears resistive. It is the most common type because the boost converter has continuous input current and thus requires the least amount of filtering for the switching frequency ripple current.

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Simple Circuit Modifications Enhance Optocoupler Performance

by Philip Cooke

The optocoupler is often used in pulse-width-modulated power converters to transmit an error signal across an isolation boundary. This error signal is used on the primary side to close the control loop. A phototransistor within this optocoupler has a large collector to base area in order to efficiently detect the photons of light emitted from the photodiode. This large area makes a good detector but it increases the collector to base capacitance. Larger capacitance adversely effects the bandwidth of the optocoupler by introducing a phase lag, even at low frequencies, in the small signal model of the compensation circuit. Figure 1 shows a typical optocoupler feedback scheme using a Texas Instruments TL431 Adjustable Shunt Regulator and a Siemens optoelectronics IL207 optocoupler. As the output voltage (V_O) drops below its nominal value, due to a sudden increase in load, the photodiode current decreases. This decrease causes the emitter voltage on the phototransistor to decrease which increases the duty cycle of the modulator. The higher duty cycle restores the output voltage to its nominal value. The type of compensation (I, PI, etc) on the error amplifier is dependent on the PWM control method (i.e., voltage mode or current mode) and the power circuit topology. In all cases the bandwidth and phase of the phototransistor can effect the stability of the power supply. It is the intent of this application note to present test data on circuit configurations which show improvements in the bandwidth performance of a common optocoupler.

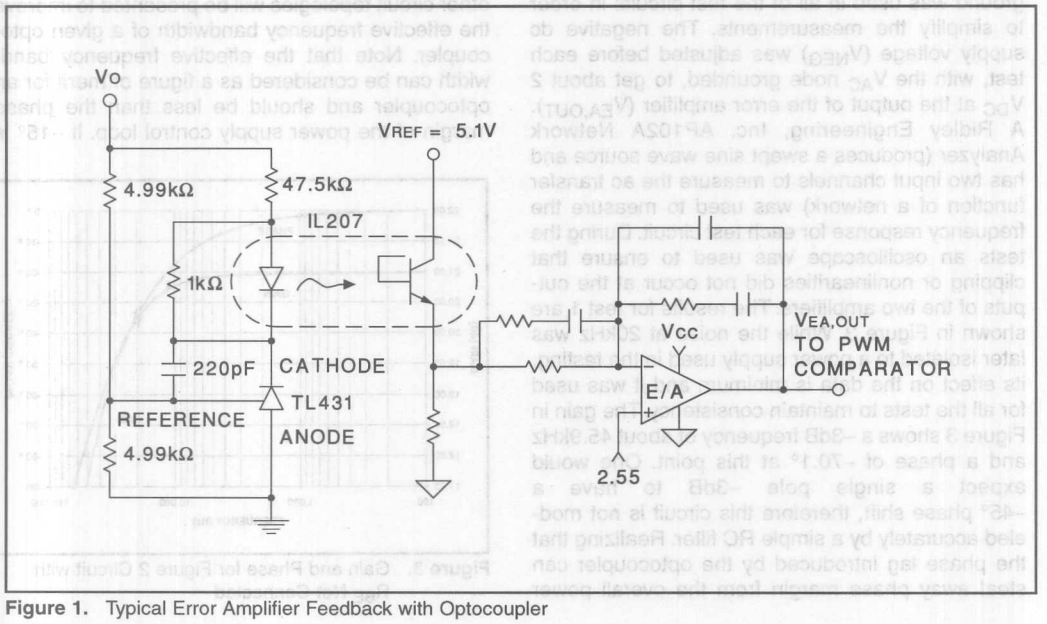


Figure 1. Typical Error Amplifier Feedback with Optocoupler

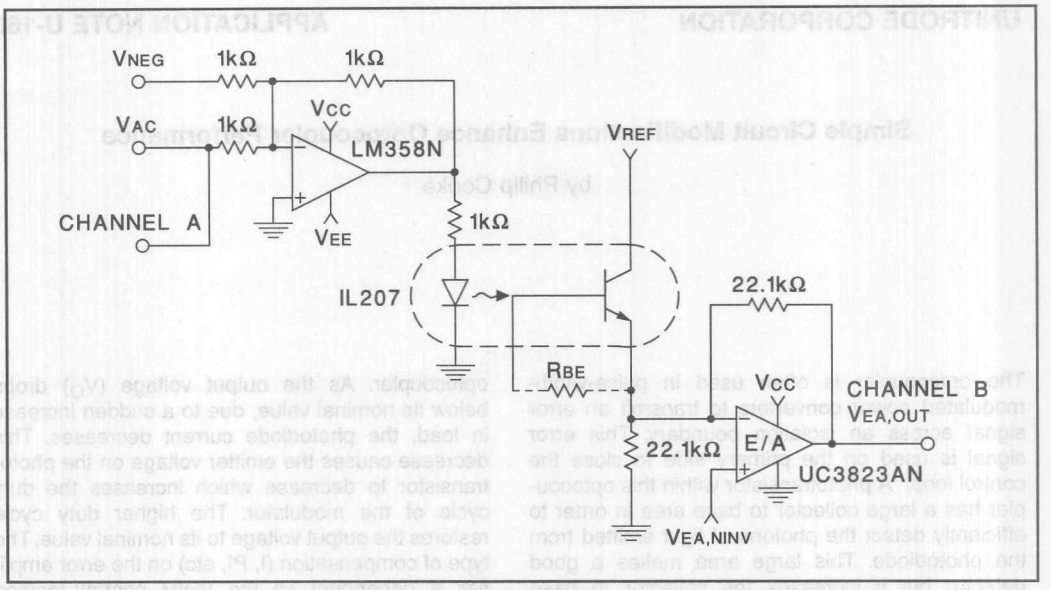


Figure 2. Data Collected for Test 1 with R_{BE} Connected, Data Collected for Test 2 with R_{BE} Not Connected

A test circuit, shown in Figure 2, was used to measure the gain and phase of an IL207 optocoupler along with the error amplifier of a UC3823AN PWM controller. The integrators in the compensation circuit of Figure 1 were left out and a common ground was used in all of the test circuits in order to simplify the measurements. The negative dc supply voltage (V_{NEG}) was adjusted before each test, with the V_{AC} node grounded, to get about 2 V_{DC} at the output of the error amplifier ($V_{EA,OUT}$). A Ridley Engineering, Inc. AP102A Network Analyzer (produces a swept sine wave source and has two input channels to measure the ac transfer function of a network) was used to measure the frequency response for each test circuit. During the tests an oscilloscope was used to ensure that clipping or nonlinearities did not occur at the outputs of the two amplifiers. The results for test 1 are shown in Figure 3. While the noise at 20kHz was later isolated to a power supply used in the testing, its effect on the data is minimum and it was used for all the tests to maintain consistency. The gain in Figure 3 shows a –3dB frequency of about 45.9kHz and a phase of –70.1° at this point. One would expect a single pole –3dB to have a –45° phase shift, therefore this circuit is not modeled accurately by a simple RC filter. Realizing that the phase lag introduced by the optocoupler can steal away phase margin from the overall power supply control loop, it is clear that the optocoupler is phase limited with respect to bandwidth. A goal of this application note is to illustrate the importance of the phase limitations that optocouplers have in power supply feedback loops. To this end other circuit topologies will be presented to improve the effective frequency bandwidth of a given optocoupler. Note that the effective frequency bandwidth can be considered as a figure of merit for an optocoupler and should be less than the phase margin of the power supply control loop. If –15° is

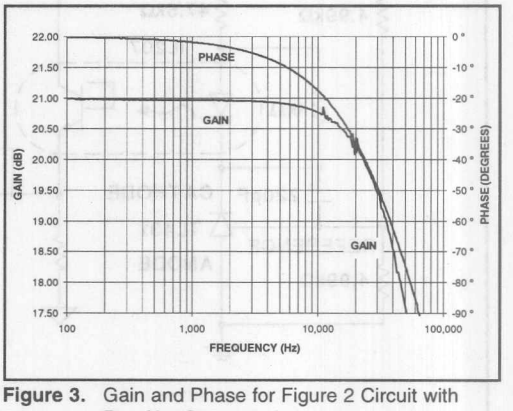


Figure 3. Gain and Phase for Figure 2 Circuit with R_{BE} Not Connected

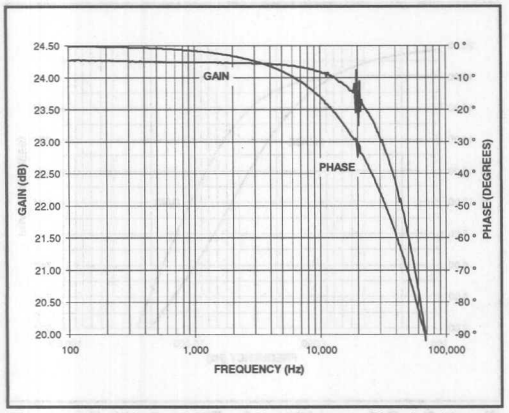


Figure 4. Gain and Phase for Figure 2 Circuit with R_{BE} = 300kΩ

arbitrarily selected as this phase it is obvious that the –3dB point on the optocoupler transfer gain curve (Figure 3) will be at a higher frequency.

As mentioned above the designer should keep the control loop crossover frequency below the effective opto bandwidth to ensure enough phase margin and thus power supply stability. For the case of the data shown in Figure 3 the –15° phase point reveals an effective opto bandwidth of 8.56kHz. In contrast the –3dB point yields a much higher frequency value of 45.9kHz. The 8.56kHz frequency may be fine for some designs but others may need up to 30kHz or more of effective opto bandwidth to support a higher crossover frequency. Techniques to improve this effective bandwidth will be introduced shortly.

By adding a 300kΩ base-to-emitter resistor in the circuit of Figure 2, test 2 results where obtained and are shown in Figure 4. The added base-to-emitter resistor is often used to reduce noise, typical in optocouplers that have the optotransistor base connection brought out to an IC pin. From the data graphed in Figure 4 it is clear that the R_{BE} resistor also increases the effective bandwidth by about 9% relative to test 1.

The circuit shown in Figure 5 was used to collect data for tests 3 and 4. Graphs of the responses are shown in Figures 6 and 7 respectively. These tests have the inverting input of the error amplifier (E/A) disconnected from the emitter terminal of the phototransistor and a resistor added between these points. The goal is to observe the effects of using the error amplifier in a topology which allows dc gain (however, unity gain was used in the test results presented here). With this configuration the effective opto bandwidth for tests 3 and 4 actually decreased from tests 1 and 2 by a factor of approximately 8, thus implying that the virtual ground at the emitter of the phototransistor was useful in increasing the bandwidth of the system. Note that for isolated power supplies the compensation gain could be realized on the TL431 side (secondary side). Therefore, setting up the error amplifier (on the primary side) for nearly unity gain or less is not a problem. In fact, all of the compensation could be

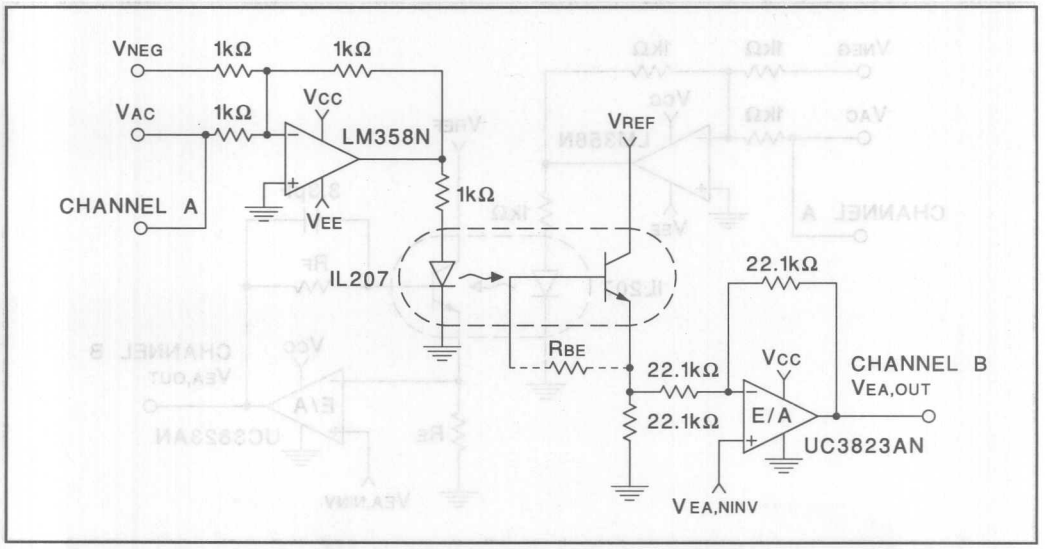


Figure 5. Data Collected for Test 3 with R_{BE} Not Connected, Data Collected for Test 4 with R_{BE} Connected

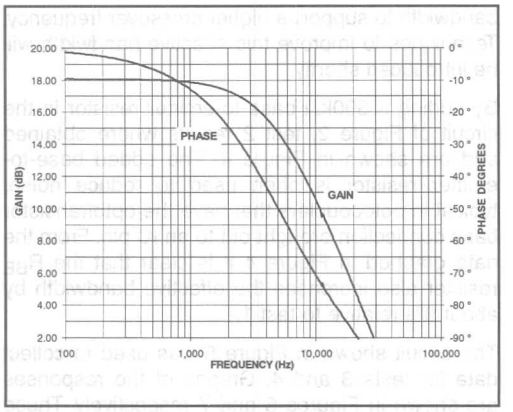


Figure 6. Gain and Phase for Figure 5 with R_{BE} = 300kΩ

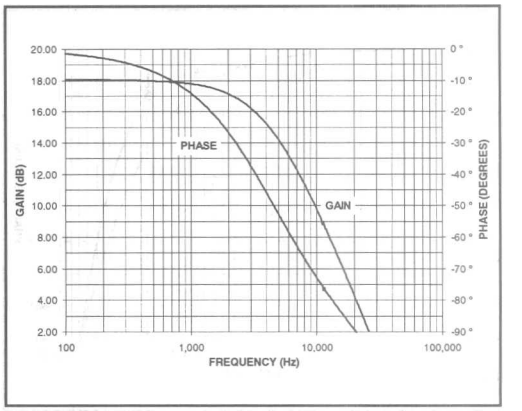


Figure 7. Gain and Phase for Figure 5 with R_{BE} Not Connected

done at the adjustable shunt regulator. For the final test circuit the error amplifier is used with the optotransistor to realize the widest bandwidth from the optocoupler device.

The circuit shown in Figure 8 was used for tests 5 through 9. The base of the phototransistor is connected to the feedback resistor, R_F. An increase in the effective opto bandwidth and the –3dB bandwidth is seen in this optocoupler circuit. The phototransistor has a component of base current provided by the photodiode and another component of current by the base connection to the feedback resistor. For small signal conditions the base to emitter junction is forward biased. Large signal characteristics, as would be seen under power supply start up or current limit conditions, were not investigated. In tests 5 through 9 different dc gains were achieved by varying the values of R_F and R_E, the feedback and optotransistor emitter resistors. In some cases a 3.3pF capacitor had to be put in parallel with the R_F resistor to prevent oscillation. Depending upon a given power supply design a capacitor of approximately 220 pF could be used in parallel with R_F to prevent oscillations.

Test results indicate that the maximum practical

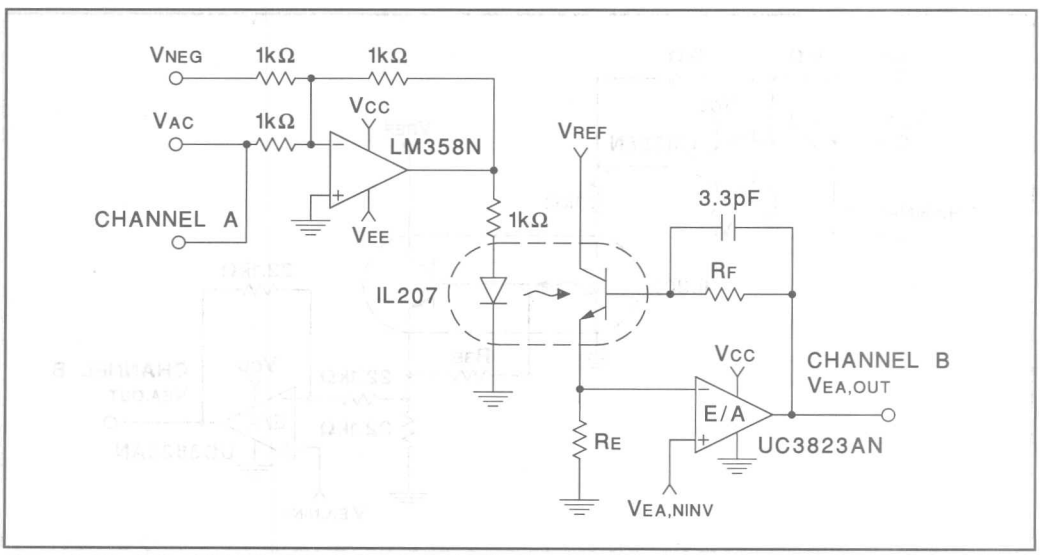


Figure 8. Circuit Used in Tests 5 Through 9, Data Results Shown in Figures 9 through 13

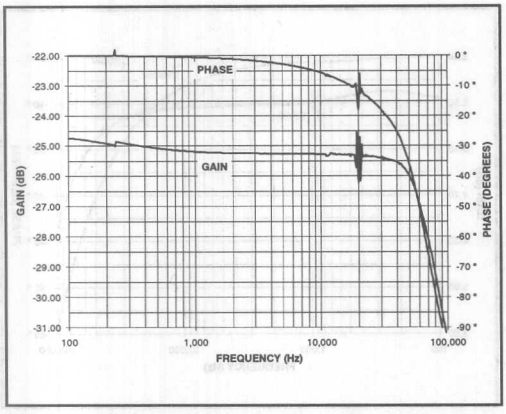


Figure 9. Gain and Phase for Figure 8, $R_F = 22.1k\Omega$ and $R_E = 22.1k\Omega$

overall dc gain of the error amplifier is about 7dB (test 9). As mentioned above, the dc gain required in the compensation network for the power supply can be realized with the TL431 so the 7dB limit does not present a system limitation. The maximum measured effective opto bandwidth of 25.5kHz was achieved for the values of $R_F = 22.1k\Omega$ and $R_E = 22.1k\Omega$, as graphically depicted in Figure 9. This is a frequency improvement of about three to one relative to test 1 using the same optocoupler device. All the test results are summarized in Table 1 below.

SUMMARY

The often unknown effective opto bandwidth for a power supply design may cause stability problems. Potential variation in optocoupler parameters from manufacturer to manufacturer in addition to part-to-part variations should be of concern to the designer in terms of closing the loop. The compensation circuit reviewed in this application note can reduce the phase lag effects introduced by the optocoupler by shifting the effective opto bandwidth higher in frequency by a factor of about three. This circuit can be used to help ensure that the variations in optocoupler parameters from lot-to-lot will have less impact on the power supply closed loop performance.

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[1] Mammano, Bob, "Isolating the Control Loop", Unitrode SEM-800, 1991.

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[3] Krause, Bob, "Optoelectronic Feedback Control Techniques for Linear and Switch Mode Power Supplies", PCIM, Power Quality, 1993.

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Test Number	V_{NEG} =V_{EE} (V)	V_{AC} (mV rms)	–15° Phase Frequency (kHz)	–3dB Frequency (kHz)	R_{BE} (kΩ)	Phase at –3dB point (°)	"dc Gain" (dB, at 100Hz)	Graph Figure Number	Circuit Figure Number	R_F (kΩ)	R_E (kΩ)
1	–1.44	49.8	8.50	45.9	NC	–70.1	21.0	3	2		
2	–2.28	49.8	9.33	53.6	300	–75.3	24.3	4	2		
3	–2.31	49.8	1.18	4.59	300	–47.3	18.1	6	5		
4	–1.49	49.8	1.07	4.14	NC	–47.0	18.1	7	5		
5	–2.31	994	25.5	64.9	NC	–58.2	–24.7	9	8	22.1*	22.1
6	–2.32	49.8	17.9	>100	NC	<–79.4	–4.39	10	8	221*	22.1
7	–4.07	198	18.5	>100	NC	<–78.3	–2.13	11	8	221*	2.25
8	–2.06	198	24.3	>100	NC	<–59.1	5.54	12	8	750	22.1
9	–1.95	198	21.0	>100	NC	<–68.1	7.56	13	8	1000	22.1

Notes: $V_{EA, NINV} = 2.49V$ and $V_{CC} = 15.0V$ for all tests.
NC = Not Connected.
* means R_F with 3.3pF in parallel.

Table 1. Summary of Test Data

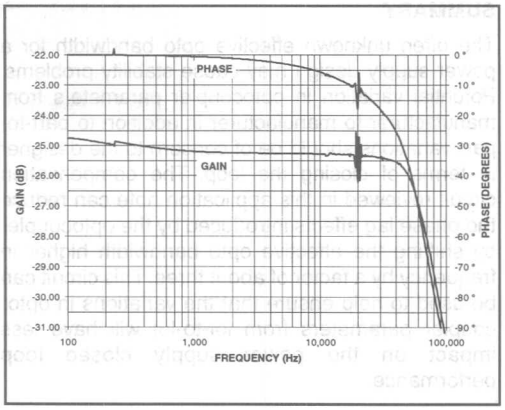


Figure 10. Gain and Phase for Figure 8, R_F = 221kΩ and R_E = 22.1kΩ

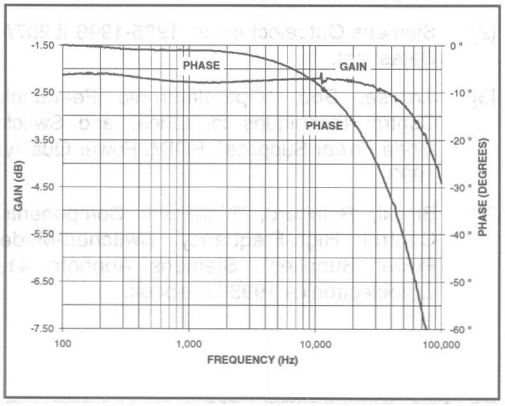


Figure 11. Gain and Phase for Figure 8, R_F = 221kΩ and R_E = 2.25kΩ

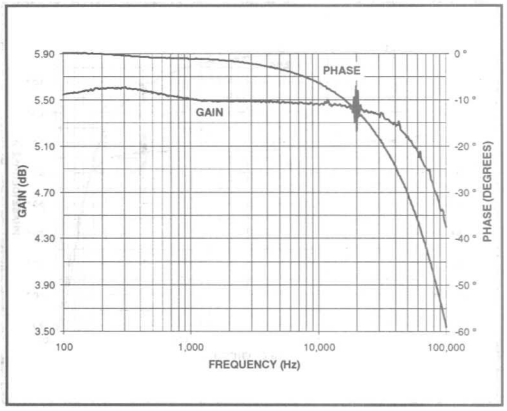


Figure 12. Gain and Phase for Figure 8, R_F = 750kΩ and R_E = 22.1kΩ

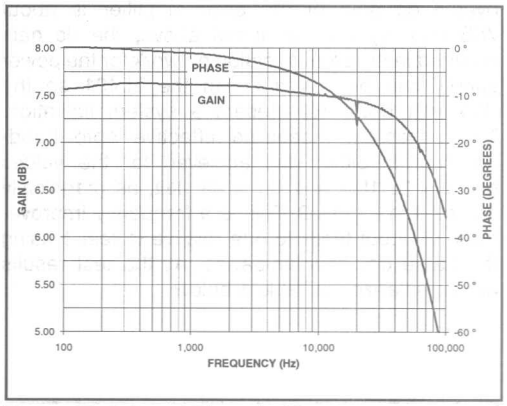


Figure 13. Gain and Phase for Figure 8, R_F = 1MΩ and R_E = 22.1kΩ

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POWERING A 35W DC METAL HALIDE HIGH INTENSITY DISCHARGE (HID) LAMP USING THE UCC3305 HID LAMP CONTROLLER

by Ron Fiorello

Unitrode Corporation

ABSTRACT

High Intensity Discharge (HID) metal halide lamps are being used in more and more applications where lamp color, long life and efficiency are important. From automotive and industrial lighting to theatrical and stage lighting, HID promises to be the light of the future. HID lamps offer many advantages over many other types of discharge lamps because of their luminous efficiency (their ability to convert electrical power to visible light) and the color of the light output is closer to an ideal source (the sun) then other types of discharge lamps i.e.; low pressure sodium, high pressure sodium etc.

The purpose of this application note is to demonstrate the use of the UCC3305 HID lamp controller IC. Information is presented on a design example to help the user better understand all of the controllers many features.

INTRODUCTION

The following section specifies typical design requirements necessary of an HID ballast which would be powering a DC headlamp in an automotive application. The headlamp used in this application is a 35W DC metal halide lamp manufactured by OSRAM/SYLVANIA.

Input Voltage Requirements - 9 to 16VDC

Startup Requirements - Must run/startup down to 6VDC

Protection/Fault Monitor- Protection against input overvoltage, output open circuit and output short circuit.

Power Regulation - Regulate power to the lamp within +5% over a lamp voltage variation of 60 to 100VDC.

Lamp Ignition Voltage - Provide an open circuit voltage of greater then 500VDC at start-up in order to ignite the lamp.

Efficiency - greater than 85%.

Cold Start - The light output on initial start-up must be within a window as specified by SAE J2009.

Hot Restrike - The ballast must be able to properly light the lamp when hot without a cool down period.

The load presented to the ballast by the lamp is non-linear. Before ignition occurs, the lamp draws very little current from the ballast. The ballast sees essentially an open circuit on its output at start-up. The open circuit voltage feeds an ignitor circuit (internal to the lamp) which steps-up the voltage in order to provide the approximately 20kV ignition voltage necessary for the lamp. Upon ignition, metals and gases inside the lamp are ionized causing the lamp voltage to collapse. During ionization, the lamp will require significant current from the ballast to properly establish and maintain the arc discharge. During this time, the current into the lamp must also be controlled to protect the lamp electrodes [1].

The initial start-up power into the lamp is higher then its steady state value. This is necessary in order to get the light output up to 75% of its steady-state value within 2 seconds, which is a requirement for an automotive application as specified under SAE J2009. The lamp voltage right after the glow to arc transition varies from lamp to lamp but is usually between 20 and 40VDC. As the lamp warms up and the internal pressure inside the arc tube increases, the voltage begins to rise and will gradually reach a steady-state value of between 60 and 110VDC after 150 seconds. This depends on the age of the lamp. A typical steady-state voltage of this type of lamp is between 75 and 90VDC.

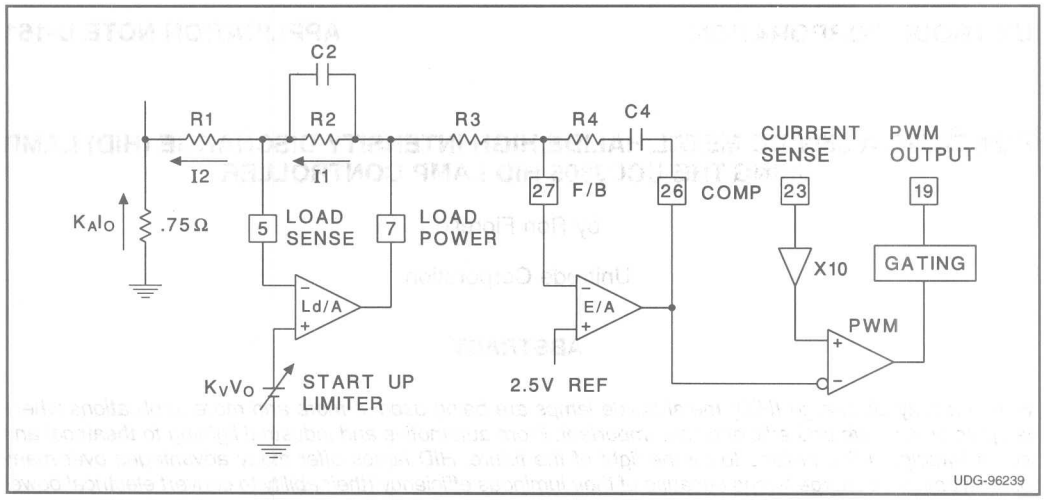


Figure 1. Power Regulation Loop

Optimal converter topology

The optimal converter topology for this application would meet the following requirements;

1) Output voltage that is capable of being higher then input voltage.
2) Low input current ripple for reduced input filter requirements
3) High efficiency
4) Minimal number of magnetic components
5) Minimal number of power semiconductors

There are a few candidate topologies which meet some of the above requirements. The best choice for this particular application is the SEPIC converter which meets all of the above requirements for a 35W lamp. The schematic of this circuit is shown in Figure 2 [2].

The UCC3305 HID controller

The features of the UCC3305 HID controller are outlined below:

- OV input protection
- Output fault protection/timing
- Power regulation vs. lamp voltage
- Lamp start-up/cool down simulation
- Current-mode control
- Fixed frequency operation
- DC or AC lamp drive capability
- High current drive capability
- On board charge pump to provide gate drive down to 6VDC
- Adjustable start-up to steady-state current ratio

Below is a summation of the different functional blocks of the UCC3305 and their major electrical characteristics;

VCC/OV Protection/VREF/VBOOST Block

VCC Maximum Voltage - 8 Volts
Must bypass with 0.1μF to 1.0μF Ceramic Monolithic Capacitor as close to the IC as possible

OV Threshold - Internal Comparator with reference voltage tied to internal 5V. OV threshold adjustable with external resistor divider

VREF:
5.0V Trimmed Bandgap Reference
Must bypass with 0.1μF Low ESR Capacitor as close to the IC as possible

VBOOST Max Voltage - 12 Volts
Supplies drive for output drive stage
Must bypass with 0.1μF to 1μF Ceramic Monolithic Capacitor as close to IC as possible

Output Drive Stage:

PWMOUT:
1.0A Peak current drive capability

Q and Q not outputs
Outputs to drive external bridge via external MOSFET drivers Output frequency is fs/512
At lamp start, outputs are disabled via RC from NOT-ON and DIV. PAUSE

Oscillator:

OSC:
Sawtooth Oscillator with Programmable Frequency D_{MAX} from 0% to 100% possible
With R_{SET} = 150k, Fs ~ 22xe-6/C_{OSC}
Maximum operating frequency is 300kHz

Load Power and Main Error Amplifiers:

LOADSENSE, LPOWER, COMP AND FB

The LOADSENSE amplifier, the main error amplifier and its external associated resistors and capacitors will determine where the peak of the power curve occurs as well as the shape of the frequency response of the ballast. Below is an analysis of this operational block based on the 35W DC lamp in an attempt to show how the power curve of the ballast is determined for this particular application.

From the simplified schematic of this loop shown in Figure 2 below, the power curve equation is determined as follows;

Power curve equation

From the simplified schematic of the power regulation loop, shown in Figure1, the currents I_1 and I_2 can be found as follows;

$$I_1 = \frac{V_{REF} - K_V \bullet V_O}{R2}$$

$$I_2 = \frac{K_V \bullet V_O + K_I \bullet I_O}{R1}$$

where K_V and K_I are the proportionality constants for voltage and current respectively; since

$$I_1 = I_2$$

$$\frac{V_{REF} - K_V \bullet V_O}{R2} = \frac{K_V \bullet V_O + K_I \bullet I_O}{R1}$$

rearranging the above equation and solving for I_O,

$$K_I \bullet I_O = (V_{REF} - K_V \bullet V_O) \bullet \frac{R1}{R2} - K_V \bullet V_O$$

$$I_O = \left[(V_{REF} - K_V \bullet V_O) \bullet \frac{R1}{R2} - KV \bullet Vo\right] \bullet \frac{1}{K_I}$$

since

$$P_O = V_O \bullet I_O$$

substituting the expression found for I_O into the power equation,

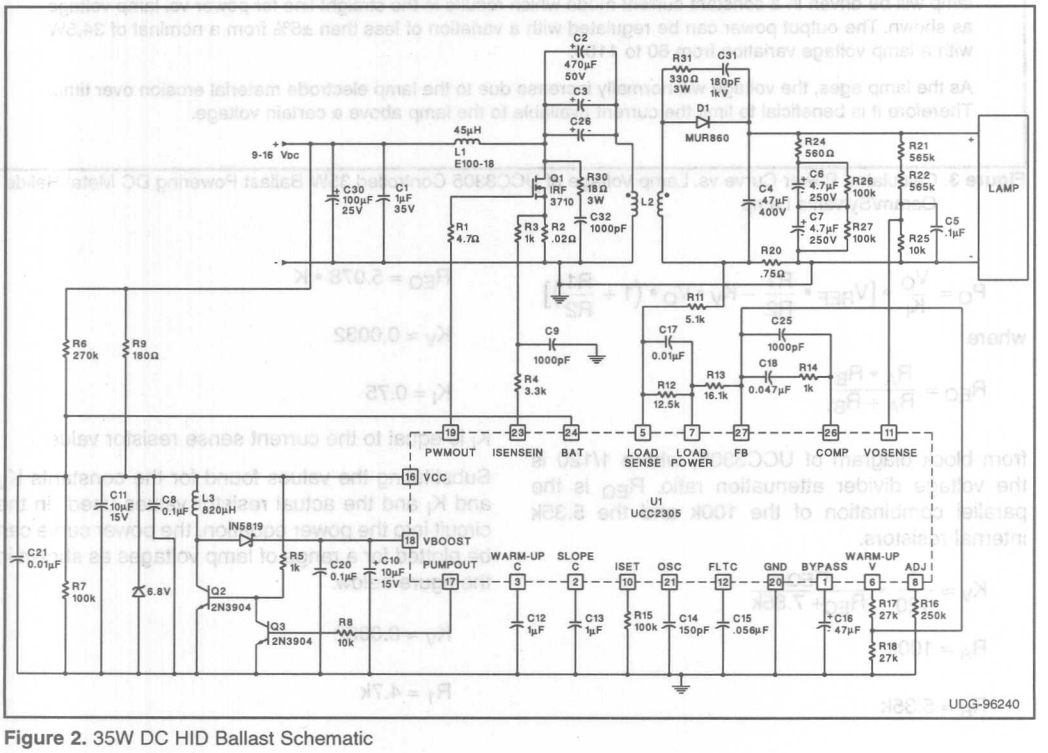
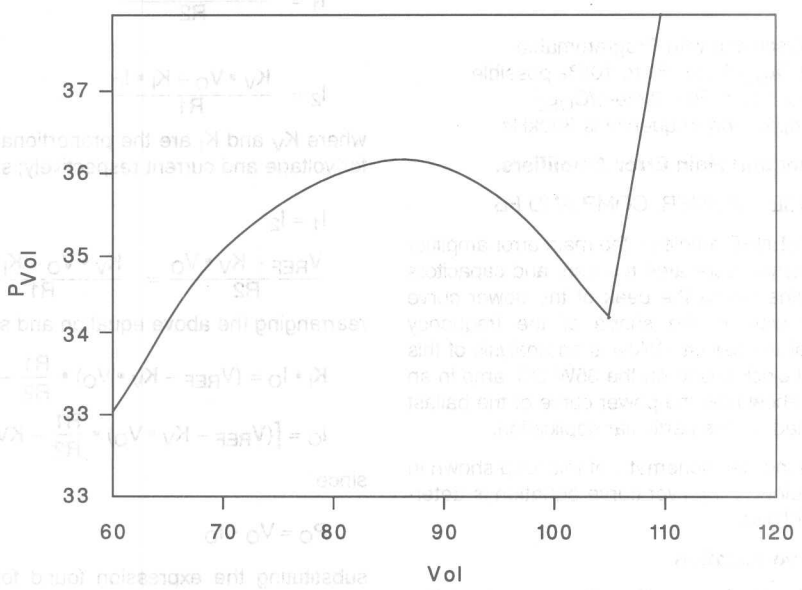


Figure 2. 35W DC HID Ballast Schematic



The expression for P_{O1} is valid for lamp voltages from 60 to 105V. The expression for P_{O2} is valid for lamp voltages above 105V (This is due to the limiter block inside the UCC3305). Above approximately 105V, the lamp will be driven in a constant current mode which results in the straight line for power vs. lamp voltage as shown. The output power can be regulated with a variation of less than ±5% from a nominal of 34.5W with a lamp voltage variation from 60 to 110V.

As the lamp ages, the voltage will normally increase due to the lamp electrode material erosion over time. Therefore it is beneficial to limit the current available to the lamp above a certain voltage.

Figure 3. Calculated Power Curve vs. Lamp Voltage of UCC3305 Controlled 35W Ballast Powering DC Metal Halide Osram/Sylvania Lamp

$$P_O = \frac{V_O}{K_I} \bullet \left[V_{REF} \bullet \frac{R1}{R2} - K_V \bullet V_O \bullet \left(1 + \frac{R1}{R2}\right)\right]$$

where

$$R_{EQ} = \frac{R_A \bullet R_B}{R_A + R_B}$$

from block diagram of UCC3305, where 1/120 is the voltage divider attenuation ratio. R_{EQ} is the parallel combination of the 100k and the 5.35k internal resistors.

$$K_V \approx \frac{1}{120} \bullet \frac{R_{EQ}}{R_{EQ} + 7.85k}$$

$R_A = 100k$

$R_B = 5.35k$

$R_{EQ} = 5.078 \bullet K$

$K_V \approx 0.0032$

$K_I = 0.75$

K_I is equal to the current sense resistor value

Substituting the values found for the constants K_V and K_I and the actual resistor values used in the circuit into the power equation, the power curve can be plotted for a range of lamp voltages as shown in the figure below.

$K_V \approx 0.0032$

$R_1 = 4.7k$

$K_I = 0.75$

$R2 = 16k$

$V_{O1} = 60, 65..110$

$V_{REF} = 2.5$

$V_{O2} = 110, 115..120$

$$P_{Vo(1)} = \frac{V_{O1}}{K_I} \bullet [(\frac{R1}{R2}) \bullet V_{REF} - K_V \bullet V_{O1} \bullet (\frac{R1}{R2} + 1)],$$

$$P_{Vo(2)} = \frac{V_{O2}}{K_I} \bullet [(\frac{R1}{R2}) \bullet V_{REF} - 0.322 \bullet (\frac{R1}{R2} + 1)]$$

Current sense comparators/amplifiers

The INPUT ISENSE comparitor/amplifier inside the UCC3305 provides cycle by cycle current control as in a typical peak current-mode controller. An added feature allows the user to program the start-up to steady-state current ratio of this current. This allows the ballast to provide increased power to the lamp at start-up in order to get the lamp light output up to its steady-state level as quick as possible. The simplified schematic of this section is shown in Figure 4 below.

By the addition of an external resistor from the ADJ. pin to ground, this ratio can be programmed. At the instant of start-up, the output of the limiter is at zero volts since the WARMUPC capacitor has not charged. Because of this, the inverting input to amplifier A1 is at ground with $20\mu A \bullet R_{ADJ}$ volts on its non-inverting input. As an example, if $R_{ADJ} = 150k$, then the voltage at the non-inverting input is 3V.

$$V_{O(-)} = -(\frac{V_{(-)}}{83k}) \bullet 10k$$

$$V_{O(-)} = -(\frac{V_{(-)}}{83k}) \bullet 10k + V_{(+)}$$

where

$V_{O(+)}$ = the contribution of the non-inverting input to V_O of A1

$V_{O(-)}$ = the contribution of the inverting input to V_O of A1

$V_{(+)}$ = the voltage at the non-inverting input of A1

$$V_O = V_{(+)} \bullet (\frac{10k}{83k} + 1) - V_{(-)} \bullet (\frac{10k}{83k})$$

on start-up,

$V_{(-)} = 0$

so;

$V_O = 3.36$ Volts

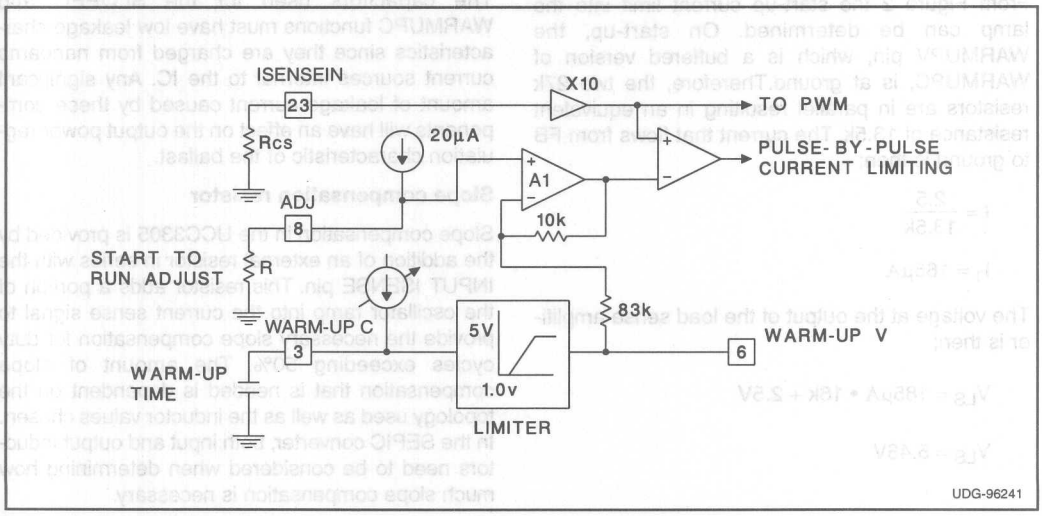


Figure 4. Current Sense / Limit Block

The current sense threshold is then;

$$V_S = \frac{3.36}{10}$$

$$V_S = 0.336 \text{ Volts}$$

This translates to a peak switch current at start-up of;

$$I_P = \frac{3.36}{0.02}$$

$$I_P = 16.8 \text{ Amps}$$

This current threshold will gradually decrease as the WARMUPC capacitor charges up to 10V.

The limiter limits the inverting input of A1 at steady-state to 5V. The current limit at this point is then;

$$V_O = 3.36 - 0.6$$

$$V_O = 2.76 \text{ Volts}$$

$$I_P = \frac{0.276}{0.02}$$

$$I_P = 13.8 \text{ Amps}$$

The switch current in the SEPIC converter is a combination of the input inductor current plus the reflected load current. At steady-state, 9 V_{IN}, the peak-to-peak current thru the output rectifier is approximately 1A. This reflects back to the primary as 6A into the switch plus 3.1 Amps from the inductor. The total current thru Q1 is then 9.1 Amps.

Output current limit on start-up

From Figure 2 the start-up current limit into the lamp can be determined. On start-up, the WARMUPV pin, which is a buffered version of WARMUPC, is at ground.Therefore, the two 27k resistors are in parallel resulting in an equivalent resistance of 13.5k. The current that flows from FB to ground is then;

$$I = \frac{2.5}{13.5k}$$

$$I_1 = 185\mu A$$

The voltage at the output of the load sense amplifier is then;

$$V_{LS} = 185\mu A \bullet 16k + 2.5V$$

$$V_{LS} = 5.46V$$

The current which flows thru the feedback resistor of the load sense amplifier is;

$$I_{LS} = \frac{5.46 - 0.30}{12k}$$

$$I_{LS} = 430\mu A$$

Assuming that the current which flows thru the feedback resistor also flows thru the inverting input resistor, the voltage across the output current sense resistor is;

$$V_{CS} = 0.30 - (430\mu A \bullet 5.1k)$$

$$V_{CS} = 1.89V$$

(the negative sign of the voltage is ignored since this is defined as positive current)

$$I_L = \frac{1.89}{0.83}$$

$$I_L = 2.3 \text{ Amps}$$

This defines the maximum startup current which flows into the lamp at ignition. The current into the lamp will decay exponentially due to the voltage charging characteristic of the WARMUPC and SLOPEC capacitors. The current will decay to a steady-state value of approximately 450mA after a period of time given by the time constant of the internal 50 Meg resistor and the capacitor placed from the SLOPEC pin to ground. In this example, the time to steady-state is 150 seconds from:

$$t = 50 \exp(6) \bullet C_{SLOPEC}$$

The capacitors used for the SLOPEC and WARMUPC functions must have low leakage characteristics since they are charged from nanoamp current sources internal to the IC. Any significant amount of leakage current caused by these components will have an effect on the output power regulation characteristic of the ballast.

Slope compensation resistor

Slope compensation in the UCC3305 is provided by the addition of an external resistor in series with the INPUT ISENSE pin. This resistor adds a portion of the oscillator ramp into the current sense signal to provide the necessary slope compensation for duty cycles exceeding 50%. The amount of slope compensation that is needed is dependent on the topology used as well as the inductor values chosen. In the SEPIC converter, both input and output inductors need to be considered when determining how much slope compensation is necessary.

The current sense comparator compares the current sense signal to the output of the error amplifier to determine the duty cycle of the power switch [3]. V_I, the voltage at the current sense resistor can be determined as follows

$$V_I = R_I \bullet \left(\frac{N_S}{N_P}\right) \bullet (I_{OAV} + M2 \bullet t) + R_I \left(I_{IN} + \frac{M_1}{2} \bullet t_{OFF}\right)$$

where;

N_S = number of turns of secondary winding of L2

N_P = number of turns of primary windings of L2

R_I = current sense resistor

L_{OAV} = secondary average output current

M_2 = down slope of secondary current thru L2

M_1 = down slope of primary current thru L1

I_{IN} = average input current

t_{OFF} = off time of switch

The above equation can be rewritten as follows;

$$V_I = R_I \bullet \left(\frac{N_S}{N_P}\right) \bullet \left(L_{OAV} + M2 \bullet (T - t_{ON})\right) + R_I \left[I_{IN} + \frac{M_1}{2} \bullet (T - t_{ON})\right]$$

The first term is the contribution of the output current thru L2 (output inductor) to the current sense resistor. The second term is the contribution of the input current thru L1 (input inductor) to the current sense resistor

This signal is set equal to the voltage at the output of the error amplifier. This results in the following equation after rearranging terms;

$$R_I \left(\frac{N_S}{N_P}\right) \bullet L_{OAV} = V_{EA} + t_{ON} \bullet \left(\frac{M_1}{2} \bullet R_I + R_I \frac{N_S}{N_P} \bullet M_2 - m\right) - I_{IN} - \frac{M_1}{2} \bullet T \bullet R_I - M_2 \bullet T$$

In order to eliminate the possibility of subharmonic oscillations, the term which multiplies t_{ON} should be set equal to zero eliminating any dependency on duty cycle.

$$\frac{M_1}{2} \bullet R_I + R_I \bullet \frac{N_S}{N_P} \bullet M_2 = M$$

From the simplified schematic of the current sense circuit;

$$S = \frac{2}{10 \bullet \exp(-6)}$$

where S is defined as the slope of the oscillator ramp. Substituting the following values into the equation for R_P will allow us to determine the value of the slope compensation resistor.

$M_2 = 178571$

$N_S = 60$

$M_1 = 178571$

$N_P = 10$

$R_I = 0.01$

$S = 181818$

$$R_P = \frac{\frac{M_1}{2} \bullet R_I + \frac{N_S}{N_P} \bullet R_I \bullet M_2}{2}$$

$R_P = 0.064$

$R4 = 50k$

R3 is the slope compensation resistor and R4 is the internal 50kΩ resistor;

$$R_P = \frac{R3}{R3 + R4}$$

Solving for R3;

$$R3 = 0.064 \bullet \frac{R4}{1 - 0.064}$$

$R3 = 3.419k$

Therefore, the slope compensation resistor chosen must be greater than 3.42k in order for stable converter operation at duty cycles which exceed 50%.

Frequency response of the power regulation loop

The frequency response of the ballast is determined by analysis of the power regulation loop. Since it is really the output current that is being regulated and not the output voltage (any change in output voltage is attenuated by 1/120), the analysis can be simplified by modeling the power stage as a voltage controlled current source with some transconductance gain G_M. This assumption is valid for a loop cross over frequency below resonance of the power stage which is approximately 10kHz.

The transconductance gain, G_M, can be found as follows;

$$G_M = \frac{\Delta I_O}{\Delta V_E}$$

The output current is converted to a voltage by the output current sense resistor. The gain of the power stage is then;

$$G_P = R_{ls} \frac{\Delta I_O}{\Delta V_E}$$

or;

$$G_P = R_{ls}\, G_M$$

where; R_{ls} = the load sense resistance (0.75Ω)

ΔI_O = load current change (500mA)

ΔV_E = error amp voltage change (5V)

G_P = –22.5dB

The loop response must now be tailored for good power regulation (high DC gain) and adequate phase and gain margin at the loop crossover frequency. The gain of the LOAD SENSE amplifier is restricted due to the fact that gain of this stage effects the power curve characteristic as shown in above analysis of the power curve equation.

The LOADSENSE amplifier should be set up as an integrator so that it can filter out switching frequency noise from the control loop. The pole frequency was chosen to be at 1kHz to give good rejection of the switching frequency noise. This results in a capacitor value of 0.01μF. The low frequency gain of this amplifier is set to 7.5dB. The combination of this gain and the power stage gain results in –15dB of low frequency gain with a pole at 1kHz.

The response can now be tailored with the main error amplifier. A zero must be added in the amplifier response at some mid-band frequency so that the DC gain for the overall loop is as high as possible. The high frequency gain of this amplifier must be well below 0dB to ensure adequate gain and phase margin for the open loop gain. Since the 16kΩ, resistor has been determined from the power curve characteristic desired, only the feedback resistor value can be chosen. If this resistor is chosen so that the high frequency gain is to be less then –20dB for good gain margin, or the feedback resistor value of 1kΩ, the capacitor value can then be determined. If a zero frequency of 3.4kHz this assumed, this will give an adequate low frequency gain boost. From this, the value of the capacitor can now be determined to be 0.047μF. The gain and phase margin with these component values is greater than 20dB and 60 degrees, respectively.

CIRCUIT EXAMPLE:

A 9 to 16VDC input SEPIC converter powering a 35W OSRAM/SYLVANIA DC lamp was built and tested. Data on efficiency, power curve and various oscillagrams of current and voltages in the power/control circuit were taken and are discussed.

Magnetics Design

L1

The input inductor L1, is designed based on the same criteria as a boost inductor. Energy is stored in L1 during the on time of Q1 and transferred during the off time. L1 is designed to operate in the continuous mode with low current ripple. At 9 V_{IN} with 36W of output power and a converter efficiency of 85%, the average input current is 4.7 Amps. If a total peak-to-peak ripple current of 2 Amps is assumed the inductance of L1 can be found. But before we can calculate the inductance required, the minimum and maximum duty cycle must be found so that the maximum and minimum on time of Q1 can be determined. The SEPIC converter has a DC transfer function of;

$$V_O = V_{IN} \bullet n \frac{D}{1 - D};$$

The turns ratio, n can be found from the maximum acceptable voltage stress on Q1. The stress on Q1 is the sum of the capacitor voltage plus the reflected secondary voltage. The capacitor voltage is essentially equal to V_{IN}, so;

$$V_{DS} = V_{IN} + \frac{V_O}{n};$$

The worst case output voltage on startup of the lamp is restricted to 500V, since this voltage will be reflected back to the drain of Q1. The turns ratio must be chosen so that the drain voltage never exceeds its maximum rating. A IRF1310 was chosen for this application in part because of its 45mΩ on resistance and V_{DS} = 100V. Calculating the turns ratio at V_{IN} = 16V; n is then found to be 5.8. A turns ratio of 6 is used.

The maximum duty cycle can now be determined from the DC transfer function. To find the maximum duty cycle, the worst case steady-state lamp voltage is used of 110VDC at V_{IN} = 9V. Lamp voltages between 60 and 110V will be within the power regulation range of the ballast. Lamp voltages outside of this range will be operated in the constant current mode. Therefore;

$V_{IN} = 10V$.

$D_{MIN} = 0.38$

For a switching frequency of 100kHz, $t_{ON\ MAX}$ = 6.7μS, $t_{ON\ MIN}$ = 3.8μS

The inductance based on $t_{ON\ MAX}$ at $V_{IN\ MIN}$ can be calculated;

$$L1 = \frac{9 \bullet 6.7\mu S}{2} = 30\mu H.$$

L1 consists of 30T of 19AWG wound on a Micrometals E100 –18 core.

L2

The voltage across the primary winding of L2 when Q1 is on, is for all practical purposes, equal to the input voltage (neglecting voltage ripple on the capacitor) since the series capacitor is switched across the primary. The inductance of the primary winding is chosen based on the peak current desired (it is desired that the inductor current is continuous). The peak current chosen is based on a tradeoff between the voltage stress on Q1 and minimal number of turns to minimize the leakage inductance which in turn means reducing the number of layers of windings. If the peak current thru L2 is restricted to 3.0A, the primary inductance can then calculated as;

$$L2 = \frac{9 \bullet 6.7\mu S}{3} = 20\mu H.$$

The inductance of L1 and L2 could have been set equal to each other. This would have made both inductors "easy" to integrate on the same core. This was not attempted here because of leakage inductance concerns between the primary and secondary windings of L2.

The number of turns for L2 can now be determined based on the particular core geometry chosen. The area product (AP) required is found from;

$$AP = \frac{L \bullet I_P \bullet I_{RMS}}{K_F \bullet J \bullet B_M} = 0.362\ cm^2$$

This is based on the following parameters;

B = 0.1T	L = 20μH	I_P = 4.7A
J = 450A/cm	K = 0.4	I_{RMS} = 5.2A

$A_E \bullet B \quad 89 \bullet e\text{-}6 \bullet 0.11$

(10T is used since this will easily fit in one layer with the desired core and wire gauge chosen)

This ferrite core must be gapped since it stores energy. It is desired that the total gap be placed in the center leg. The gap is calculated from;

$$L_P = \frac{u_O \bullet u_R \bullet N_P^2 \bullet A_E}{L} = 12.56 \bullet 10^{-7}$$

$$\frac{0.89 \bullet 100}{0.020mH} = 0.56mm = 0.02\ in$$

The secondary turns can be calculated from the turns ratio as 60T. The core used for L2 has a center leg gap of 0.022 in. Multifilar wire is used for both the primary and secondary turns to minimize the copper losses. The winding sequence used was; primary-secondary-primary-secondary-primary.

Performance data

Performance data on the ballast is presented in the following curves showing efficiency and the measured power curve. Oscillograms of Q1 voltage and current are also given as well as startup characteristics of the lamp voltage and current. The maximum efficiency achieved was 86.2% at a lamp voltage of 100V. The efficiency decrease after this point is due to an increase in output power which occurs at lamp voltages above 100 to 105V. The lamp cold start voltage and current waveforms are shown with a time base of 50mS and 1Sec. As can be seen, the ballast output voltage is 600V before lamp ignition. Once the lamp ignites, the voltage collapses and the lamp current increases to 2A. Eventually, the lamp voltage begins to increase and the current decreases. They will arrive to their steady-state values of 80 to 90VDC and 450mA respectively after approximately 150 seconds.

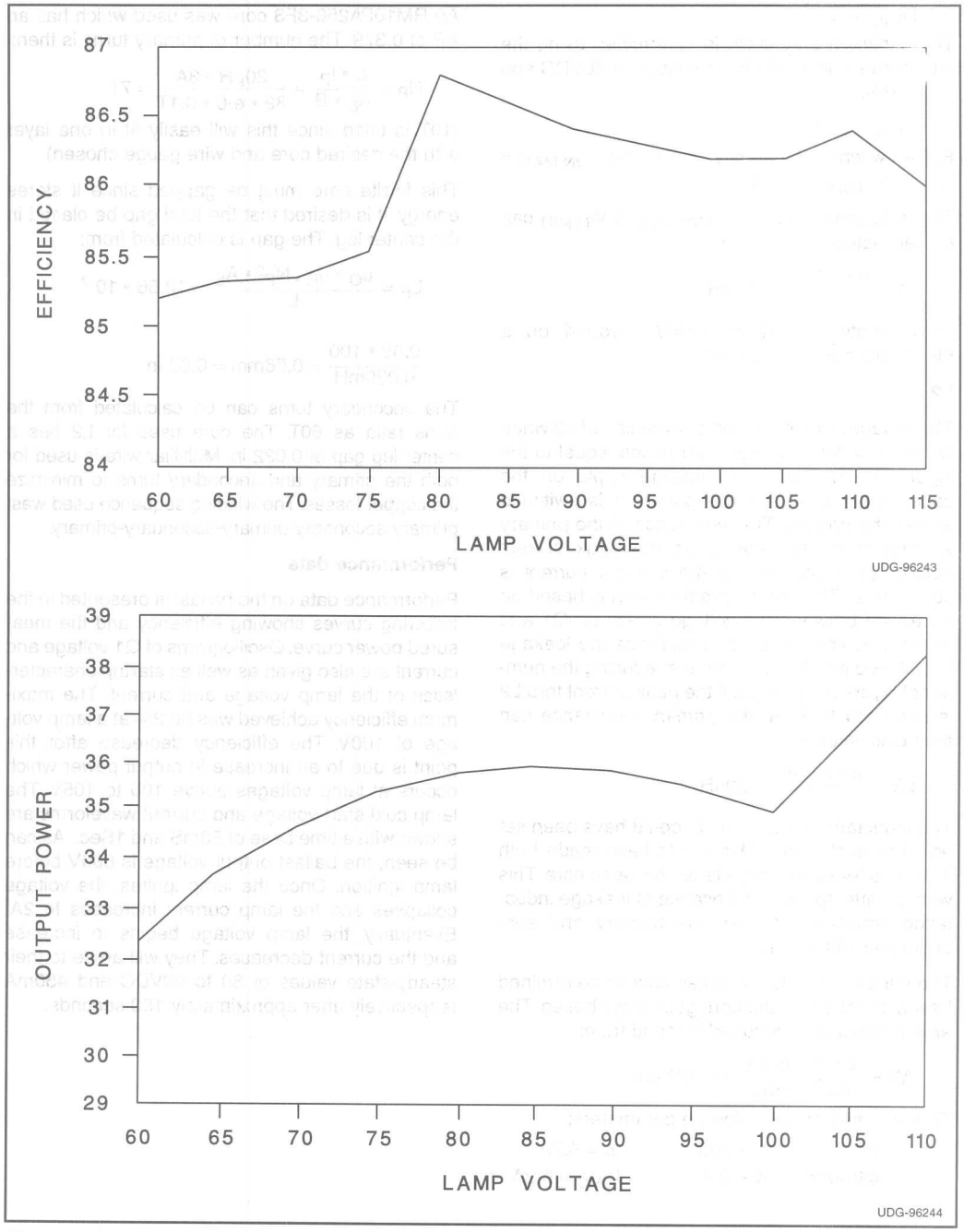


Figure 5. Efficiency and Power Curve of 35W HID Ballast

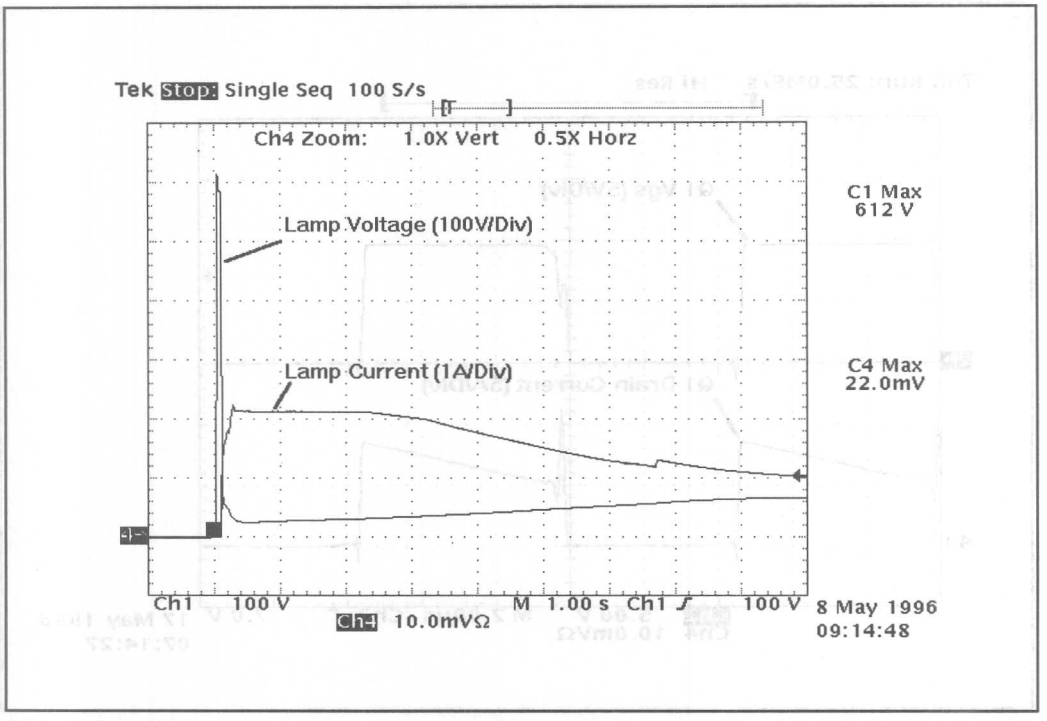


Figure 6. Ballast Output Voltage and Current

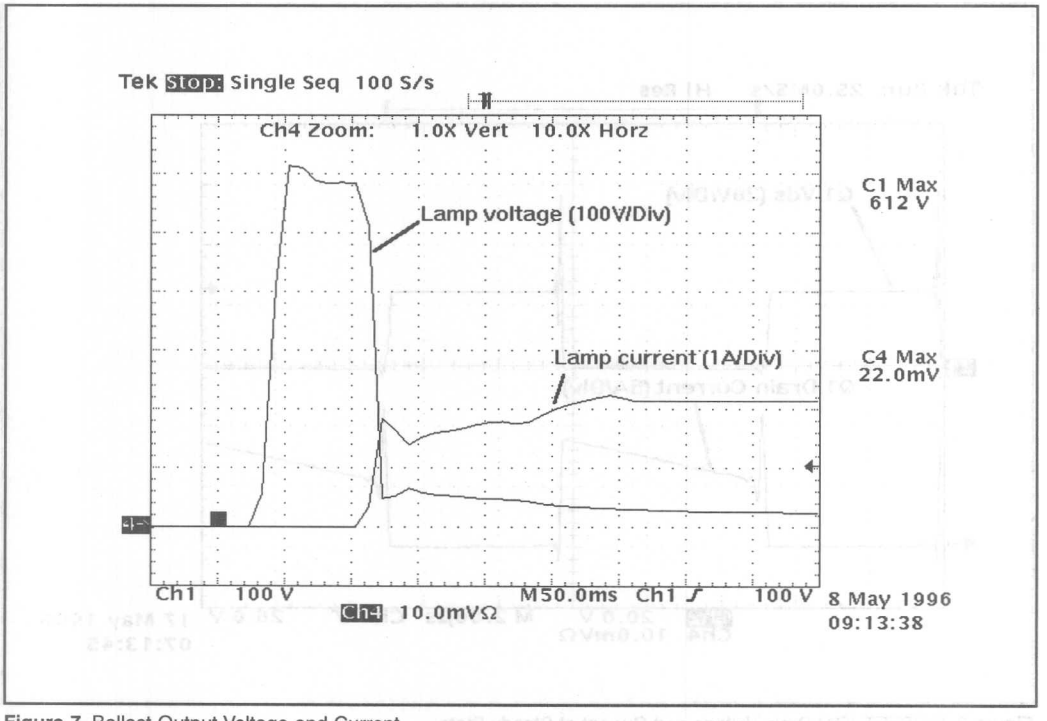


Figure 7. Ballast Output Voltage and Current

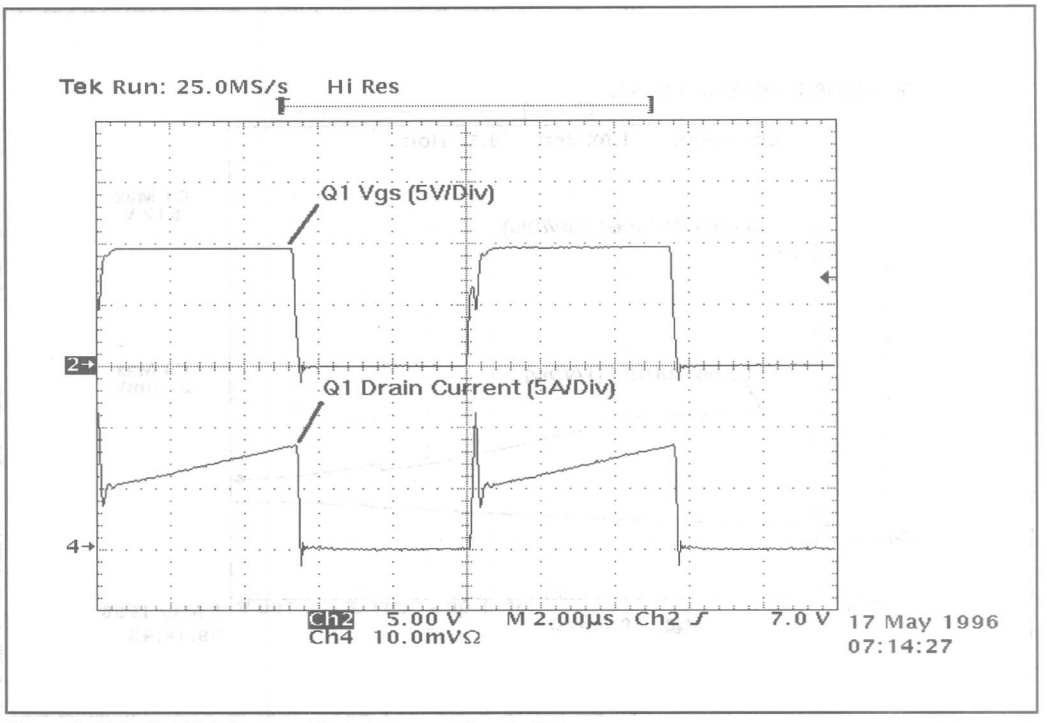


Figure 8. MOSFET (Q1) Gate and Drain Voltage at Steady State

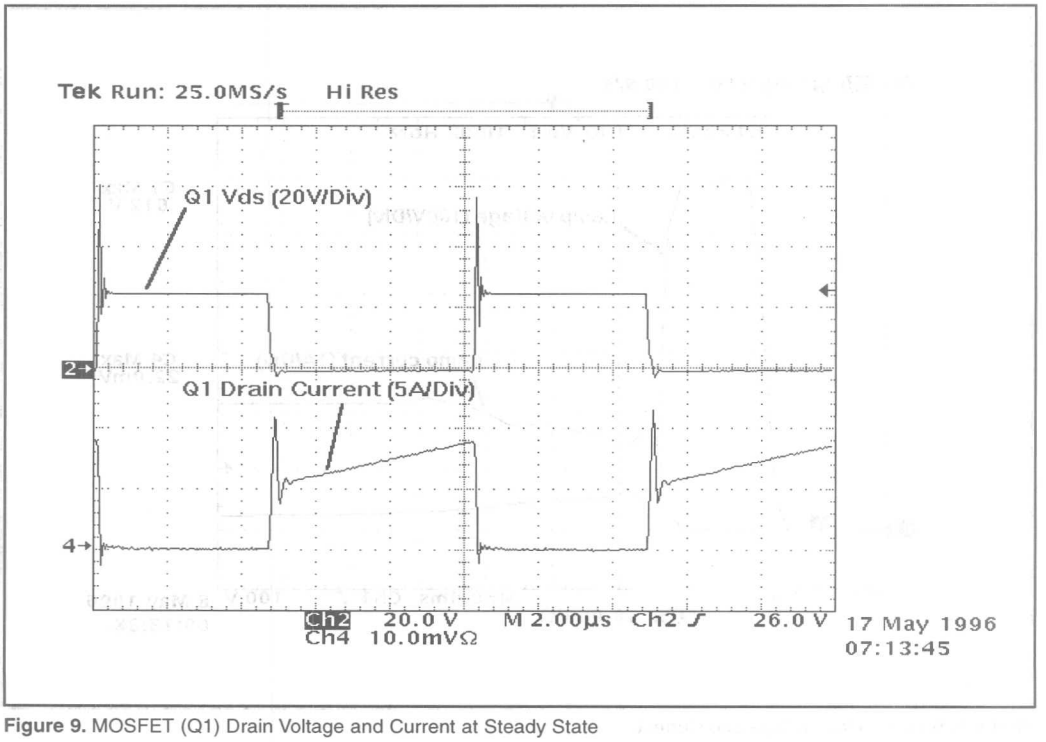


Figure 9. MOSFET (Q1) Drain Voltage and Current at Steady State

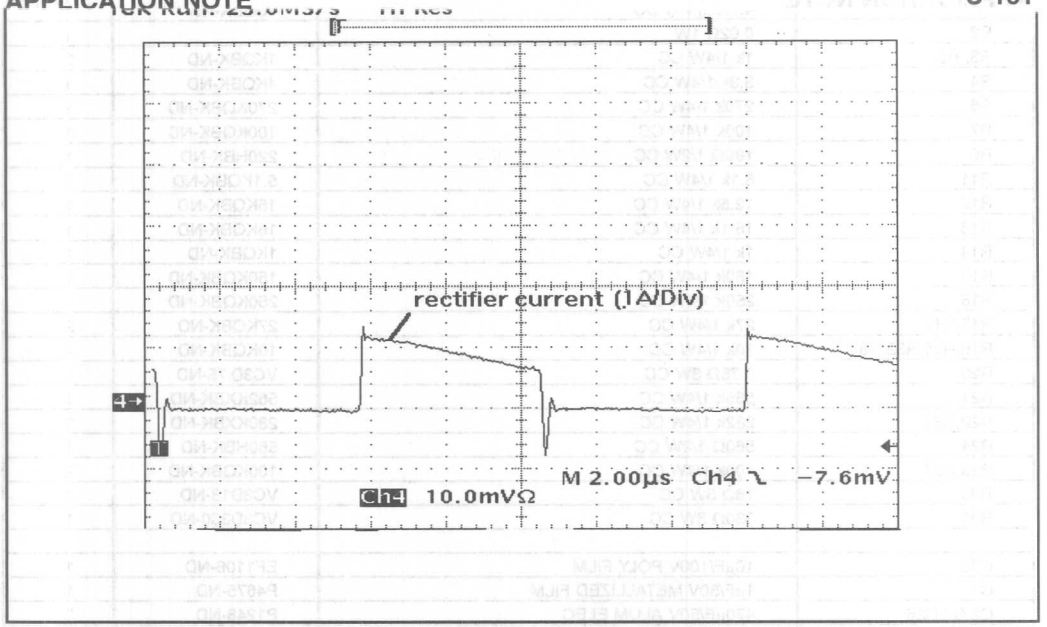


Figure 10. Output Rectifier (D1) Current at Steady State

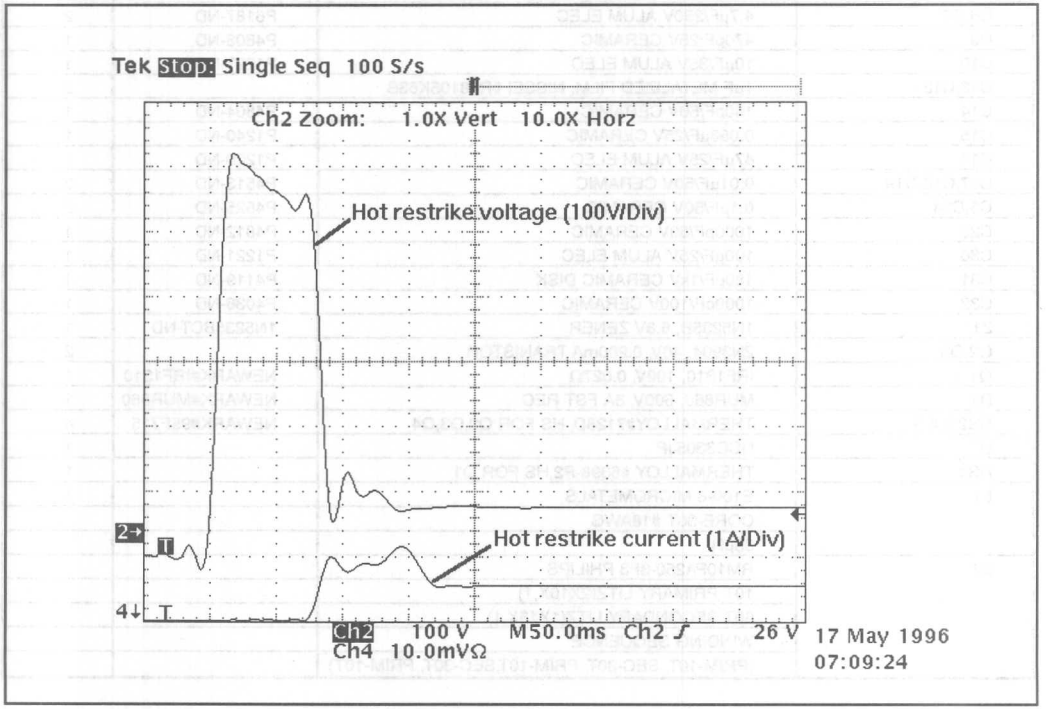


Figure 11. Ballast Hot Restrike Voltage and Current

35W HID BALLAST PARTS LIST

REF DES	PART DESCRIPTION	DIGIKEY NUMBER	QTYPER
RI	4.7Ω 1/4 W CC	10QBK-ND	1
R2	0.02Ω 1W		1
R3, R5	1k 1/4W CC	1KQBK-ND	2
R4	3.3k 1/4W CC	4KQBK-ND	1
R6	270k 1/4W CC	270KQBK-ND	1
R7	100k 1/4W CC	100KQBK-ND	1
R9	180Ω 1/2W CC	220HBK-ND	1
R11	5.1k 1/4W CC	5.1KQBK-ND	1
R12	12.5k 1/4W CC	15KQBK-ND	1
R13	16.1k 1/4W CC	16KQBK-ND	1
R14	1k 1/4W CC	1KQBK-ND	1
R15	150k 1/4W CC	150KQBK-ND	1
R16	250k 1/4W CC	250KQBK-ND	1
R17,R18	27k 1/4W CC	27KQBK-ND	2
R19,R25,R32,R8	10k 1/4W CC	10KQBK-ND	4
R20	0.75Ω 3W CC	VC3D.75-ND	1
R21	565k 1/4W CC	562KXBK-ND	1
R22,R23	282k 1/4W CC	280KXBK-ND	2
R24	560Ω 1/2W CC	560HBK-ND	1
R26,R27	100k 1/4W CC	100KQBK-ND	2
R30	18Ω 3W CC	VC3D18-ND	1
R31	330Ω 3W CC	VC3D330-ND	1
C33	10μF/100V POLY FILM	EF1106-ND	1
C1	1μF/50V METALLIZED FILM	P4675-ND	1
C2,C3,C26	470μF/50V ALUM ELEC	P1248-ND	3
C4	0.47μF/630V POLY FILM	EF4225-ND	1
C8,C11	0.47μF/50V CERAMIC	P4671-ND	2
C6,C7	4.7μF/250V ALUM ELEC	P6187-ND	2
C9	470pF/25V CERAMIC	P4808-ND	1
C10	10μF/35V ALUM ELEC	P1227-ND	1
C12,C13	1μF METALIZED FILM, NISSEI #R68105K63B		2
C14	150pF/50V CERAMIC	P4804-ND	1
C15	0.056μF/25V CERAMIC	P1240-ND	1
C16	47μF/25V ALUM ELEC	P1220-ND	1
C17,C18,C19	0.01μF/50V CERAMIC	P4513-ND	3
C5,C24	0.1μF/50V CERAMIC	P4525-ND	2
C25	1000pF/50V CERAMIC	P4812-ND	1
C30	100μF/25V ALUM ELEC	P1221-ND	1
C31	180pF/1kV CERAMIC DISK	P4119-ND	1
C32	1000pF/100V CERAMIC	P4036-ND	1
Z1	1N5235B, 6.8V ZENER	1N5235BCT-ND	1
Q2,Q3	2N3904, 40V, 0.200mA TRANISTOR		2
Q1	IRF1310, 100V, 0.027Ω	NEWARK#IRF1310	1
D1	MUR860, 600V, 8A FST REC	NEWARK#MUR860	1
HS2,3,4,5	THERMALLOY#7128D, HS FOR Q2,Q3,Q4	NEWARK#95F715	4
U1	UCC3305JP		1
HS1	THERMALLOY #6398-P2,HS FOR Q1		1
L1	E100-8 MICROMETALS		1
	CORE-30T #18AWG		
	35μH		
L2	RM10PA250-3F3 PHILIPS		
	10T PRIMARY LITZ(2X10X,1)		
	60T SECONDARY LITZ(1X15X,1)		
	WINDING SEQUENCE		
	(PRIM-10T, SEC-30T, PRIM-10T,SEC-30T, PRIM-10T)		

CONCLUSION

The performance data presented of a typical UCC3305 HID lamp controller application, demonstrated it to be a excellent means of controlling a 35W DC metal halide HID lamp. The power regulation and efficiency achieved using the SEPIC converter topology proved it to be a good alternative to other conventional circuit topologies for an automotive lighting application. The many protection and control features of the UCC3305 simplify the task of the ballast designer considerably, making it an economically feasable choice for AC as well as DC HID lamp applications.

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THE UC3902 LOAD SHARE CONTROLLER AND ITS PERFORMANCE IN DISTRIBUTED POWER SYSTEMS

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Unitrode Corporation

UC3902 APPLICATIONS

The current demanded by large electronic systems continuously rises due to higher performance and increased functionality. At the same time, supply voltages, especially in digital circuits, are falling to previously unprecedented low levels. The combination of higher load currents and low supply voltages impose difficult requirements on the power distribution and in most cases, forces a higher voltage distribution bus with local voltage conversion.

Users of distributed power systems are seeking reliable and economic solutions to supply their loads. A modular approach, where stand alone power supplies are utilized for local power conversion, is widely accepted in these applications. The power rating of the individual converters are usually limited by the available height, board space and by the limitation on volumetric heat dissipation. High current loads are supplied by several parallel connected power supplies. In addition to higher currents, the parallel modules can also offer redundancy, an important factor to achieve reliable, uninterrupted operation and extended life expectancy in these systems.

Parallel connected power supplies require a dedicated control mechanism, called load share circuitry to assure full utilization of the system. The purpose of a load share controller, like Unitrode's UC3902, is to provide for equal distribution of the load current among the parallel connected power supplies. By equalizing the output currents, uniform thermal stress of the individual modules is also ensured which has the utmost importance for long term reliability of electronic components.

For the UC3902 to work properly, the modular power system has to consist of power supplies which possess their own feedback circuits. Furthermore, the stand alone modules have to be equipped with true remote sense capability or with an output voltage adjustment terminal. Each module must have its own load share controller. The operating principle of a load share mechanism is to measure the output current of each individual module and to be able to modify the output voltage of the units until all participating power supplies deliver equal output currents. It is accomplished by the UC3902 integrated circuits which are connected to the common load share bus and adjust the positive sense voltage (or the voltage of the output voltage adjust pin) of their respective modules to provide equal load current sharing.

UC3902 BLOCK DIAGRAM

The UC3902 is an 8-pin integrated circuit. Its sole purpose is to provide the load sharing function for existing power supplies. The chip incorporates only the building blocks required for load sharing. Tight regulation of the converters' output voltage is not anticipated with this circuit. In fact, the UC3902 performs just the opposite task by finely adjusting the regulated output voltage of the converters to match all output currents evenly.

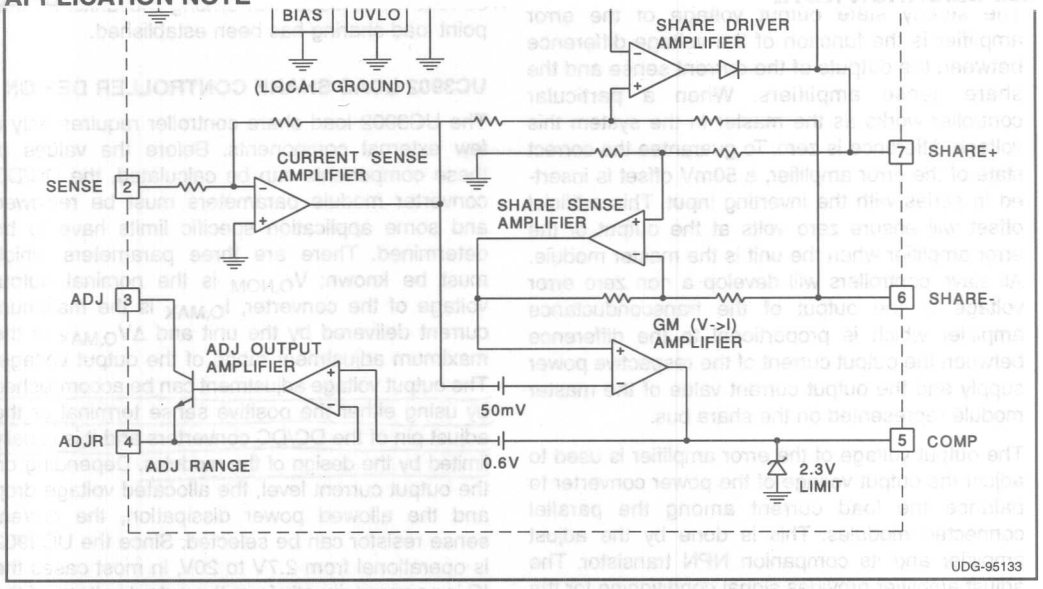


Figure 1. UC3902 Block Diagram

A unique advantage of the UC3902 is its differential load share bus. This architecture greatly enhances the noise immunity of the system. Figure 1 shows the block diagram of the load share controller.

The IC consists of a current sense amplifier, a share bus driver and sense amplifier pair, an error amplifier, a buffer stage called adjust amplifier, and housekeeping circuit which provides internal bias and the on-chip reference for the circuit.

The UC3902 has an inverting current sense amplifier with the gain of 40. The output of the current sense amplifier is proportional to the output current of the power supply it is connected to. It provides the input signals to the load share bus driver amplifier and to the inverting input of the error amplifier. Because the share driver amplifier is configured for unity gain, the voltage on the output of the share driver amplifier also equals the output voltage of the current sense amplifier. When this voltage is the highest potential among the parallel connected load share controllers, i.e. the unit delivers the highest output current, the module acts as the master unit. The output of the share driver amplifier of the master also determines the voltage on the share bus. In the case, where this voltage is lower then the share bus voltage, i.e. the module supplies less current than any one of the other units in the system, the share controller will behave as a slave. The output of the share driver amplifier of the slave controllers is disconnected from the share bus by the diodes in series with their respective outputs.

The share sense amplifier measures the voltage on the differential share bus and provides the signal for the noninverting input of the error amplifier. Similar to the share driver amplifier, this circuit has a gain of 1 which is fixed internally. Consequently, the output voltage of the share sense amplifier always corresponds to the highest output current level, delivered by the master unit in the system.

A transconductance amplifier is utilized for the error amplifier function in the UC3902. If a feedback network were connected between the output and the inverting input of the error amplifier, the output current representation would be inaccurate. The transconductance amplifier allows the feedback network to be connected from the amplifier output to the ground which preserves the authenticity of the current signal at the inverting input of the error amplifier. Also note that this type of amplifier requires a voltage difference between its inverting and noninverting inputs. Furthermore, the transconductance amplifier has high input and output impedances. Instead of the usual low impedance voltage source output of operational amplifiers, this circuit has a high impedance current source output. Accordingly, the gain is defined as transconductance (A/V) but it can be converted back to the general V/V gain term by

multiplying the transconductance of the amplifier (Gm) with the impedance of the compensation network (X_{COMP}).

The steady state output voltage of the error amplifier is the function of the voltage difference between the outputs of the current sense and the share sense amplifiers. When a particular controller works as the master in the system this voltage difference is zero. To guarantee the correct state of the error amplifier, a 50mV offset is inserted in series with the inverting input. This artificial offset will ensure zero volts at the output of the error amplifier when the unit is the master module. All slave controllers will develop a non zero error voltage at the output of the transconductance amplifier which is proportional to the difference between the output current of the respective power supply and the output current value of the master module represented on the share bus.

The output voltage of the error amplifier is used to adjust the output voltage of the power converter to balance the load current among the parallel connected modules. This is done by the adjust amplifier and its companion NPN transistor. The adjust amplifier provides signal conditioning for the error signal and its output drives a NPN transistor which is configured as a programmable current source. A resistor from its emitter to ground and the error voltage defines the current, I_{ADJ}, which flows through a resistor connected between the ADJ pin of the load-share controller and the positive output terminal. The I_{ADJ} current causes a voltage drop across the resistor which requires the power supply to increase its output voltage. The resulting higher power supply output voltage increases the output current of that particular module until the output current levels equal out among the units. At that point load sharing has been established.

UC3902 LOAD SHARE CONTROLLER DESIGN

The UC3902 load share controller requires only a few external components. Before the values of these components can be calculated, the DC/DC converter module parameters must be reviewed and some application specific limits have to be determined. There are three parameters which must be known; $V_{O,NOM}$ is the nominal output voltage of the converter, $I_{O,MAX}$ is the maximum current delivered by the unit and $\Delta V_{O,MAX}$ is the maximum adjustment range of the output voltage. The output voltage adjustment can be accomplished by using either the positive sense terminal or the adjust pin of the DC/DC converters and it is usually limited by the design of the modules. Depending on the output current level, the allocated voltage drop and the allowed power dissipation, the current sense resistor can be selected. Since the UC3902 is operational from 2.7V to 20V, in most cases the IC is powered directly from the output voltage of the system. If that is not possible because of an inappropriate value of the output voltage, the supply voltage, V_{CC}, has to be determined as well.

SETTING UP THE DC OPERATING POINT

Figure 2 shows a typical application of the UC3902 load share controller. This circuit must be repeated

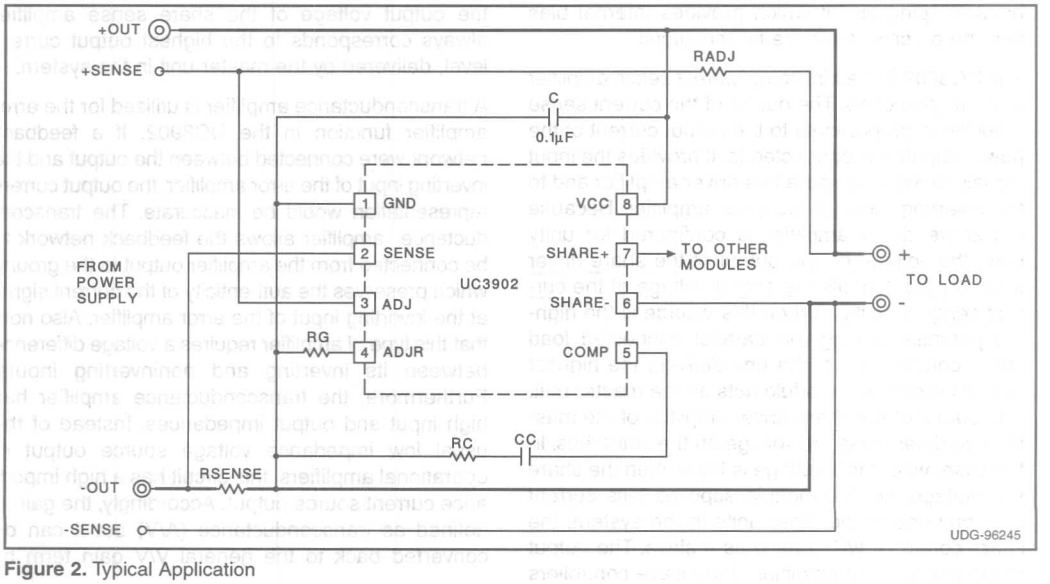


Figure 2. Typical Application

for each power supply sharing the current for a common load in the system. The design process starts with calculating the component values for setting up the basic operating conditions for the IC.

In order to precisely share the load current among parallel connected modules, the output current of each individual power supply has to be measured. A current sense resistor, R_{SENSE} is placed in the negative return path of the units. Choosing R_{SENSE} is based on two factors; the maximum power dissipation and the maximum voltage drop across the sense resistor. While the power dissipation is only limited by practical considerations like efficiency and component ratings, the maximum voltage drop has to comply with internal signal level limits of the integrated circuit. Most important is to prevent the output of the current sense amplifier from saturation. The highest voltage of the amplifier output, V_{CSAO} is a function of V_{CC}: It equals either 10V or V_{CC} - 1.5V, whichever is lower. Consequently,

$$V_{SENSE,\,MAX} = \frac{V_{CSAO}}{A_{CSA}}$$

where $V_{SENSE,MAX}$ is the maximum voltage drop across the current sense resistor, V_{CSAO} is the maximum voltage of the current sense amplifier output and A_{CSA} is 40, the gain of the current sense amplifier.

Once $V_{SENSE,MAX}$ is determined, the current sense resistor value can be calculated by the following formula:

$$R_{SENSE} = \frac{V_{SENSE,MAX}}{I_{O,MAX}}$$

$I_{ADJ,MAX}$, the maximum current of the adjust amplifier is 10mA as specified in the datasheet. It is a good practice to keep the highest current of the adjust amplifier in the 5mA to 10mA range as lower values might increase the noise sensitivity of the system. This current is determined by the highest possible voltage on the ADJR pin which is 2.6V and by the resistor, R_G, between the ADJR pin and ground. Thus the resistor value can be calculated as:

$$R_G = \frac{2.6V}{I_{ADJ,MAX}}$$

R_{ADJ} is the impedance inserted in the positive sense line of the power supply. Its value is the function of the maximum adjustment range of the output voltage, $\Delta V_{O,MAX}$ and the previously selected $I_{ADJ,MAX}$ current value. Since the voltage drop across the current sense resistor reduces the range available for output voltage adjustment, that factor has to be accounted for as shown in the equation for R_{ADJ} below:

$$R_{ADJ} = \frac{\Delta V_{O,MAX} - I_{O,MAX} \bullet R_{SENSE}}{I_{ADJ,MAX}}$$

This relationship points out an important design constraint for the system. The sum of the voltage drops across the wiring impedances and the voltage drop across the current sense resistor must be significantly lower than $\Delta V_{O,MAX}$ or the load share mechanism has no headroom to adjust the output voltage of the modules to achieve proper distribution of the load current.

CLOSING THE SHARE LOOP

Balanced distribution of the load currents among the parallel connected units is accomplished by an additional control loop provided only for the load share function. Similarly to other control loops inside the power supplies, the current share loop is based on negative feedback. Such control loops must obey certain stability criteria in order to work properly. Although this Application Note does not cover the theoretical background of loop stability, some of the most critical conditions for successfully closing the load share loop will be pointed out.

Since the load share loop is added to existing power supplies, interaction between the existing voltage control loop and the share loop must be avoided. For that reason the crossover frequencies of the two loops must be well separated.

The voltage loop crossover frequency, $f_{0,V}$ is greatly dictated by the required transient response of the converter. In order to maintain the stability of the voltage control loop, the share loop has to be set up not to cause any excess phase shift at $f_{0,V}$. This is usually achieved by placing the crossover frequency of the share loop ($f_{0,S}$) at least one, but preferably two decades lower than the crossover frequency of the voltage loop. Also a zero should be placed in the transfer function at $f_{0,S}$. This way, the effect of the share loop is minimized at the crossover frequency of the voltage loop.

Closing the load share loop at low crossover frequency is acceptable, if the purpose of load sharing is clarified. The primary concern for load sharing is to extend the life expectancy of the system and to increase reliability. It is achieved in the system by paralleling several modules and

assuring that their thermal stresses are balanced during the life of the product. Another advantage in such systems is the possibility for redundancy. These goals can be completely fulfilled by slow acting corrective measures which allow $f_{0,S}$ to be significantly lower than $f_{0,V}$.

The first step is to determine the transfer functions of the individual building blocks for the frequency range from 0.1Hz to approximately 1kHz. The unity gain crossover frequency of the load share control loop is expected to be within these frequency limits. If off-the-shelf power supplies are being used, then a network analyzer should be used to measure the transfer function. This is also a good practice to confirm actual versus calculated performance as well.

The valid transfer functions for the range of our interest are:

- $A_{PWR}(s)$: the transfer function of the power supply, measured by injecting an AC signal between V_{SENSE+} and V_{OUT+} terminals.
- $A_{Vo\rightarrow Vis}$: this gain term describes the relationship between the output voltage and the voltage across the current sense resistor. It varies with the load impedance according to

$$A_{Vo\rightarrow Vis} = \frac{R_{SENSE}}{R_{LOAD}}$$

- A_{CSA}: the gain of the current sense amplifier. This term is a constant and equals 40.
- A_{SHA}: both amplifiers driving and sensing the signal on the differential share bus are configured for unity gain. ($A_{SHA} = 1$)
- $A_{EA}(s)$: the gain of the error amplifier defined as: $A_{EA}(s) = Gm \bullet X_{COMP}(s)$ where Gm is the transconductance of the error amplifier and $X_{COMP}(s)$ is the impedance of the compensation components as a function of complex frequency.
- A_{ADJ}: the adjust circuit gain depends only on the R_G and R_{ADJ} resistors because the adjust amplifier is configured as a unity gain buffer stage. Consequently,

$$A_{ADJ} = \frac{R_{ADJ}}{R_G}$$

The overall share loop characteristic is established by multiplying the gain terms of the individual blocks:

$$A_{SHARE-LOOP}(s) = A_{PWR}(s) \bullet A_{VO\rightarrow VIS} \bullet$$
$$\bullet A_{CS} \bullet A_{SHA} \bullet A_{EA}(s) \bullet A_{ADJ}$$

DESIGN EXAMPLE

Users experimenting with the UC3902 load share controller can utilize a demonstration board featured in Figure 3. This circuit provides a solution for paralleling three power supply modules. The performance of the system was measured using three off-the-shelf DC/DC converter modules, each rated for 100W delivering 8.4A to the load at 12V nominal output voltage.

The design process starts by measuring the transfer function of the power supplies between their positive voltage sense and power output terminals. The resulting Bode plot shown in Figure 4 reveals a 40Hz crossover frequency which will require a crossover frequency of 4Hz for the load share loop. The power stage has 10dB gain at this frequency.

In the demonstration board, the UC3902 is powered from the output voltage of the system. Note the 0.1µF local bypass capacitor connected to the VCC pin of the IC. Using 12V as VCC, the maximum output voltage of the internal amplifiers are approximately 10V. This voltage denotes the highest possible full scale voltage between SHARE+ and SHARE-, but the actual voltage on the load share bus at full load is determined by the designer. Noise sensitivity, accuracy and the number of units in parallel have to be taken into consideration when choosing the full scale bus voltage. The load share bus is driven by the master controller only and each slave module represents a 10kΩ load on the bus. This means that every unit will increase the supply current of the master module by 100µA/V on the load share bus.

The power supply's 8.4A output current rating allows the use of a higher shunt resistor value in favor of better load share accuracy with only a slight decrease in overall efficiency. The full scale bus voltage, V_{CSAO} is selected to be 6V. Accordingly,

$$R_{SENSE} = \frac{6V}{8.4A \bullet 40} = 0.0178\Omega$$

and a 20mΩ standard value had been selected.

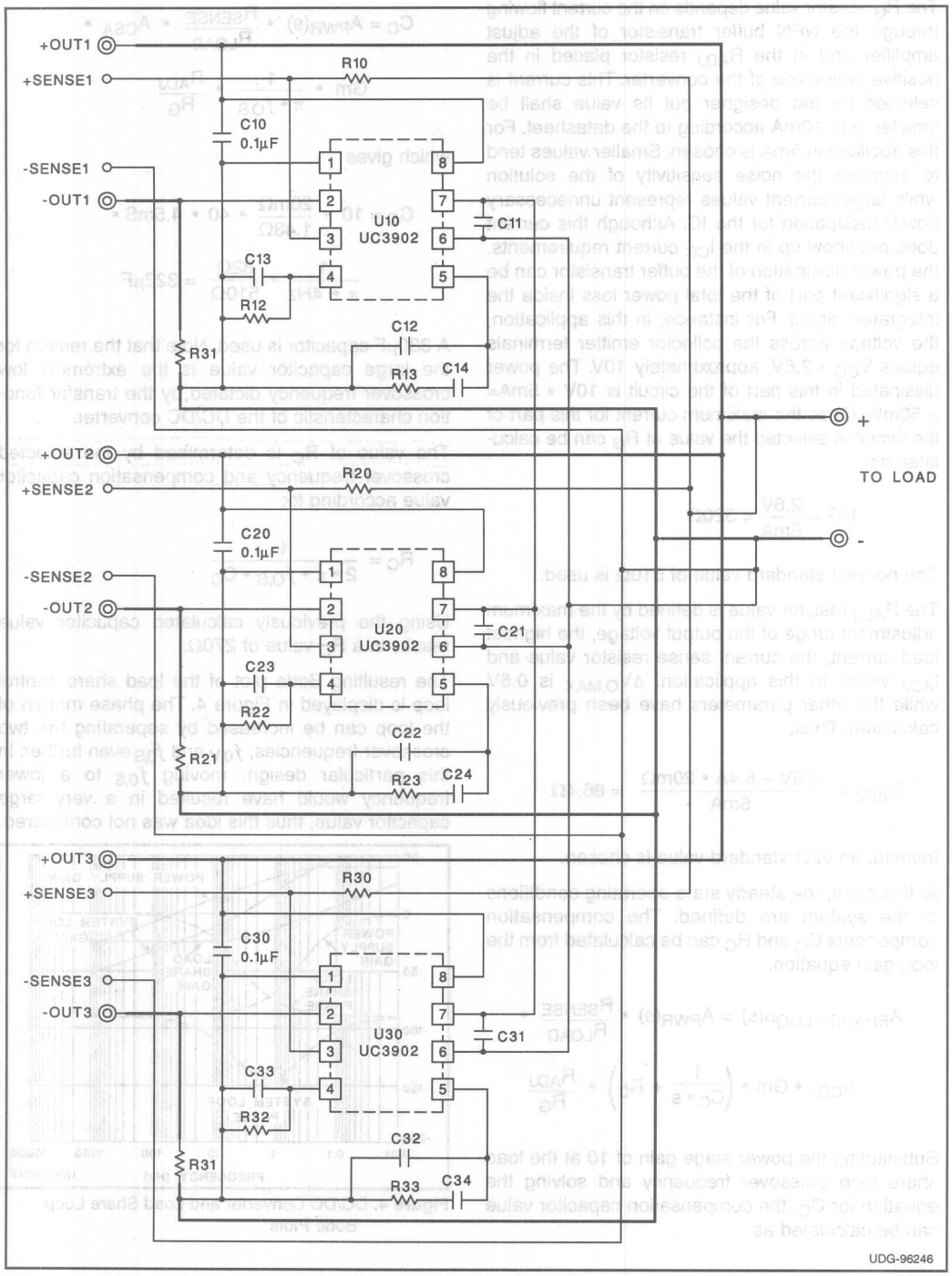


Figure 3. Demonstration Board Schematic

The R_G resistor value depends on the current flowing through the NPN buffer transistor of the adjust amplifier and in the R_{ADJ} resistor placed in the positive sense line of the converter. This current is selected by the designer but its value shall be smaller than 10mA according to the datasheet. For this application 5mA is chosen. Smaller values tend to increase the noise sensitivity of the solution while larger current values represent unnecessary power dissipation for the IC. Although this current does not show up in the I_{CC} current requirements, the power dissipation of the buffer transistor can be a significant part of the total power loss inside the integrated circuit. For instance, in this application, the voltage across the collector emitter terminals equals V_{CC} - 2.6V, approximately 10V. The power dissipated in this part of the circuit is 10V • 5mA= = 50mW. Once the maximum current for this part of the circuit is selected the value of R_G can be calculated as:

$$RG = \frac{2.6V}{5mA} = 520\Omega$$

The nearest standard value of 510Ω is used.

The R_{ADJ} resistor value is defined by the maximum adjustment range of the output voltage, the highest load current, the current sense resistor value and I_{ADJ} value. In this application, $\Delta V_{O,MAX}$ is 0.6V while the other parameters have been previously calculated. Thus,

$$R_{ADJ} = \frac{0.6V - 8.4A \bullet 20m\Omega}{5mA} = 86.4\Omega$$

Instead, an 82Ω standard value is chosen.

At this point, the steady state operating conditions of the system are defined. The compensation components C_C and R_C can be calculated from the loop gain equation.

$$A_{SHARE-LOOP}(s) = A_{PWR}(s) \bullet \frac{R_{SENSE}}{R_{LOAD}} \bullet$$

$$A_{CSA} \bullet Gm \bullet \left(\frac{1}{C_C \bullet s} + R_C\right) \bullet \frac{R_{ADJ}}{R_G}$$

Substituting the power stage gain of 10 at the load share loop crossover frequency and solving the equation for C_C, the compensation capacitor value can be calculated as:

$$C_C = A_{PWR}(s) \bullet \frac{R_{SENSE}}{R_{LOAD}} \bullet A_{CSA} \bullet$$

$$Gm \bullet \frac{1}{\pi \bullet f_{O,S}} \bullet \frac{R_{ADJ}}{R_G}$$

which gives

$$C_C = 10 \bullet \frac{20m\Omega}{1.43\Omega} \bullet 40 \bullet 4.5mS \bullet$$

$$\frac{1}{\pi \bullet 4Hz} \bullet \frac{82\Omega}{510\Omega} = 322\mu F$$

A 330µF capacitor is used. Note that the reason for the large capacitor value is the extremely low crossover frequency dictated by the transfer function characteristic of the DC/DC converter.

The value of R_C is determined by the selected crossover frequency and compensation capacitor value according to:

$$R_C = \frac{1}{2 \bullet \pi \bullet f_{O,S} \bullet C_C}$$

Using the previously calculated capacitor value results in a R_C value of 270Ω.

The resulting Bode plot of the load share control loop is displayed in Figure 4. The phase margin of the loop can be increased by separating the two crossover frequencies, $f_{0,V}$ and $f_{0,S}$ even further. In this particular design, moving $f_{0,S}$ to a lower frequency would have resulted in a very large capacitor value, thus this idea was not considered.

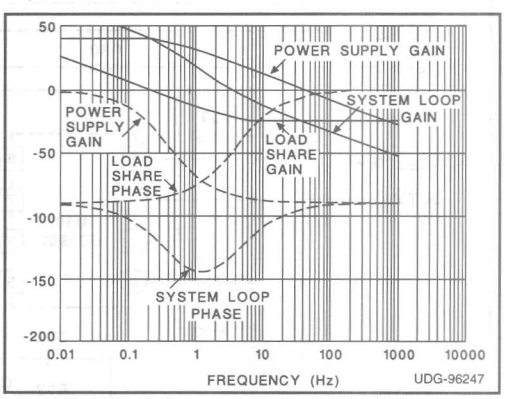


Figure 4. DC/DC Converter and Load Share Loop Bode Plots

PARTS LIST:

C = C10 = C20 = C30 = 0.1µF
C11 = C21 = C31 = 0.01µF
C12 = C22 = C32 = not used
C13 = C23 = C33 = not used
C_C = C14 = C24 = C34 = 330µF
R_{ADJ} = R10 = R20 = R30 = 82Ω
R_{SENSE} = R11 = R21 = R31 = 0.02Ω
R_G = R12 = R22 = R32 = 510Ω
R_C = R13 = R23 = R33 = 270Ω

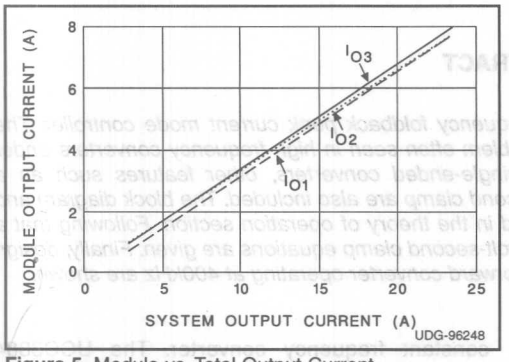


Figure 5. Module vs. Total Output Current

EXPERIMENTAL RESULTS

The performance of the demonstration circuit was measured using the calculated component values and running three DC/DC converters in parallel. Figure 5 shows the output currents of the individual modules as a function of the total load current.

In Figure 6, the percentage of deviation from the calculated average module current is depicted. The current distribution error is the largest at light load, as expected, because of the effects of internal offset voltages and the small current measurement signal level. At full load, where load sharing has the most impact, the three modules shared the load current evenly, within 1% of the ideal load current values.

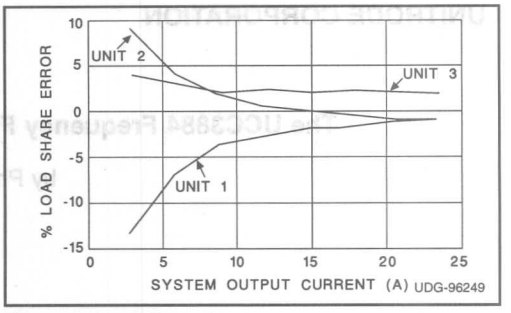


Figure 6. Load Share Accuracy

Results similar to this can be obtained in other applications with the formulas contained within this Application Note.

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[2] M. Jordan, *"UC3907 Load Share IC Simplifies Parallel Power Supply Design"*, U-129 Application Note, Unitrode Corporation

[3] J. Rajagopalan, et al, *"Modeling and Dynamic Analysis of Paralleled DC/DC Converters with Master-Slave Current Sharing Control"*, APEC '96 Proceedings, pp. 678-684

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The UCC3884 Frequency Foldback Pulse Width Modulator

by Philip Cooke

ABSTRACT

This application note focuses on the UCC3884 frequency foldback peak current mode controller. The UCC3884 provides a solution to the current tail problem often seen in high frequency converters under overload fault conditions. Intended primarily for single-ended converters, other features such as a maximum duty-cycle clamp and an accurate volt-second clamp are also included. The block diagram and the main features of the UCC3884 will be presented in the theory of operation section. Following that a derivation of the oscillator, frequency foldback, and volt-second clamp equations are given. Finally, design details and test results for an example RCD clamp forward converter operating at 400kHz are shown.

INTRODUCTION

The output VI characteristic of high frequency, buck-derived, peak current mode converters can exhibit a current tail during current overload conditions. This overload may be caused by a short circuit condition or a low impedance at the power stage output. The current tail is actually a gradual increase in the average output current as the average output voltage decreases toward zero. The peak current limit in a PWM controller commands the power stage switch off during overcurrent conditions which should limit the maximum average output current. However, the propagation delay inherent in the controller and in the power switch during turn-off limits the minimum attainable duty cycle [1]. This minimum duty cycle limit can produce a current tail during overloads. Upon close inspection one finds that this propagation delay exists collectively between the current sense (CS pin) and the output (OUT pin) of the integrated circuit (IC) and the turn-off delay of the power stage switch. The reduction of the propagation delays for a given IC and power stage design can help, but tends to increase system cost. An alternate method is needed to reduce the delays and thus the excessive currents during a fault. One possible technique is implemented in the oscillator section of the UCC3884. During a fault condition as the output voltage approaches zero the operating frequency also decreases. By reducing the frequency during overload conditions the duty-cycle is permitted to decrease below the value previously limited by propagation delay in the constant frequency converter. The UCC3884 reduces the frequency smoothly as the load impedance approaches a short circuit, thus preventing possible latch-up with nonlinear loads [1]. This effectively diminishes the current tail in the output VI characteristic.

The UCC3884 is intended for high performance, peak current mode, single-ended applications that can benefit from frequency foldback. This frequency reduction only operates when the output voltage is below a user programmable value. More specifically, the oscillator runs at constant frequency and only folds back when the output voltage drops below a given value (e.g., 4.2V for a 5V output). A volt-second clamp circuit is also included that allows accurate duty-cycle clamping under transient line and load conditions providing an extra level of circuit protection from transformer saturation. For example, if a sudden increase in load power occurs while the input voltage increases, the applied volt-seconds could be enough to saturate the transformer, which could cause the power switch to fail. In this case, the volt-second clamp circuit could be used to prevent the failure of the power switch by overriding the control loop and limiting the applied volt-seconds. This controller also features a depletion-mode n-channel MOSFET gate drive intended to be used in the bias supply during start up. A reduction in both the size of the start up storage capacitor and turn-on time can be achieved by using an external depletion-mode device.

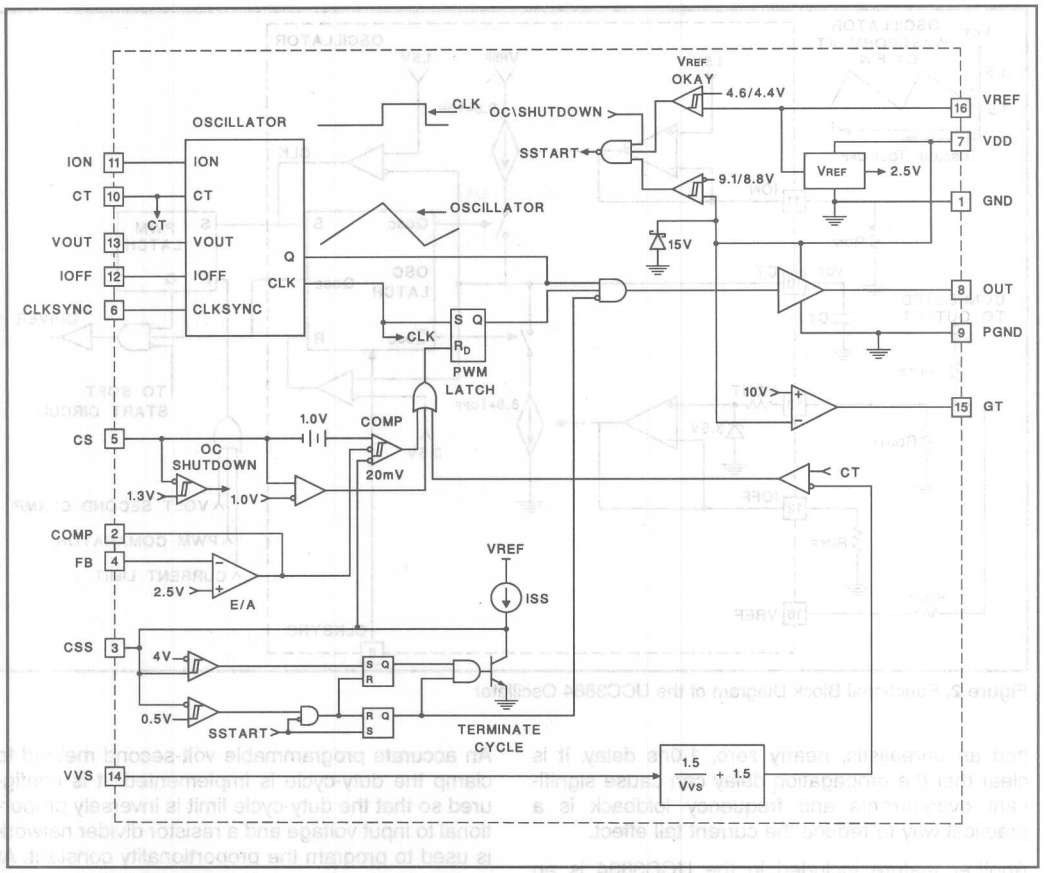


Figure 1. UCC3884 Block Diagram

THEORY OF OPERATION

The UCC3884 current mode controller, shown in Figure 1, contains a programmable oscillator section which includes the ability to synchronize multiply PWMs. The positive and negative sloped portions of the oscillator waveform (measured at CT, the connection point for the timing capacitor) have time intervals that are set by external resistors at ION and IOFF as shown in Figure 2. The nominal operating frequency is determined by the timing capacitor during non-frequency foldback conditions, that is, with the output voltage at its regulated value. The positive sloped portion of the oscillator waveform has a fixed time duration and is set by a resistor connected to ION. In a similar fashion the off-time is set by a resistor at IOFF. However, the negative sloped portion of the oscillator waveform is extended in time as the measured output voltage decreases providing protection during output faults. When the voltage at VOUT decreases below 3.5V, due to an output short circuit, the operating period increases and the IC is in frequency foldback operation. It should be emphasized that normal converter operation, except during start up, is at a fixed frequency.

The power supply output voltage and the voltage from VREF can be fed back into VOUT with summing resistors. This ensures a minimum frequency at startup and during short circuit conditions when the output voltage is zero. Figure 3 shows computer simulated VI curves for a 417kHz forward converter, one with frequency foldback and one without frequency foldback. The total propagation delay was set to 150ns in this computer model of a forward converter with 48V input (8:2 turns ratio). Power stage component values were L = 1.3μH with a DCR of 0.01Ω and C = 10000μF with an ESR of 70mΩ [1]. It can be seen that the current tail is reduced with frequency foldback. Figure 4 further details the effect of the propagation delay. Two simulations were done at the same operating frequency both without frequency foldback. The simulation with the current tail approaching 22A had a 150ns delay and the other

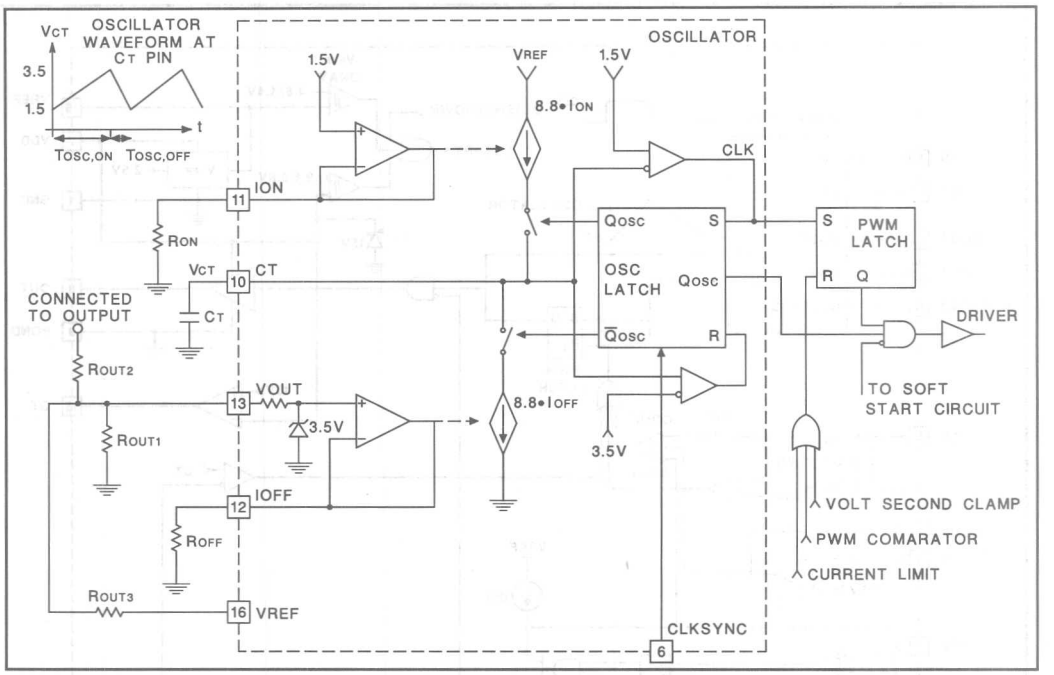


Figure 2. Functional Block Diagram of the UCC3884 Oscillator

had an unrealistic, nearly zero, 1.0ns delay. It is clear that the propagation delay can cause significant overcurrents and frequency foldback is a practical way to reduce the current tail effect.

Another feature included in the UCC3884 is an interface to drive an external depletion-mode MOSFET during power supply startup until the bootstrap winding exceeds a 10V threshold. At which time the depletion-mode MOSFET is turned-off. The internal amplifier controlling this MOSFET has 300mV of hysteresis to avoid oscillation during power-up.

An accurate programmable volt-second method to clamp the duty-cycle is implemented. It is configured so that the duty-cycle limit is inversely proportional to input voltage and a resistor divider network is used to program the proportionality constant. At a given input voltage and constant load, assuming regulation, the operating duty-cycle is a fixed value. The volt-second clamp duty-cycle may then be set somewhat higher than this operating duty-cycle. Since the volt-second duty-cycle limit is inversely proportional to V_{IN} at any other constant input voltage level, the volt-second clamp will still exceed

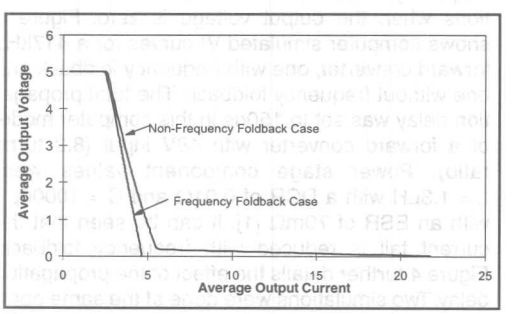


Figure 3. Frequency and Non-Frequency Foldback Comparision

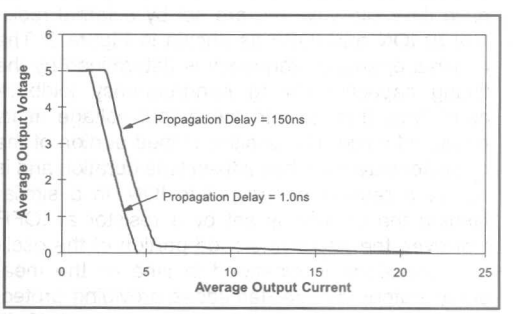


Figure 4. Non-Frequency Foldback with 1.0ns and 150ns Propagation Delays

the steady state operating duty-cycle as shown in Figure 5. This allows normal current-programmed closed-loop operation of the converter without the volt-second duty-cycle limit interfering with the control. For example, during a load transient and possibly an input voltage transient the volt-second clamp can accurately limit the maximum applied volt-seconds by limiting the duty-cycle. This ensures that the transformer does not saturate during a fault which could otherwise fail the power supply. After the fault passes the converter will go back into regulation.

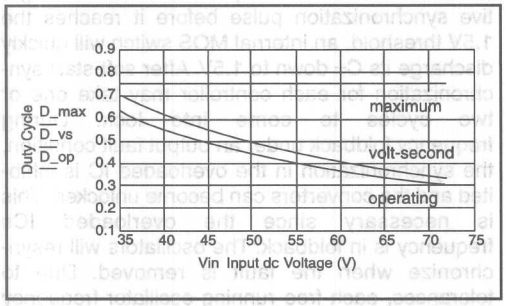


Figure 5. Various Duty Cycles

An external capacitor may be connected to CSS which provides for a soft-start and also allows the IC to be disabled with an external transistor. The frequency foldback and the soft-start functions will both be in effect during power-up since the output voltage fed back to the VOUT pin is less than 3.5V and the voltage on CSS is less than 4V. The increasing on-time at the OUT pin during soft-start is controlled by C_{SS} and the period is controlled by the frequency foldback circuitry. When an overload or short circuit occurs the frequency foldback circuit and possibly the volt-second clamp circuit is activated (assuming the overcurrent is not triggered). In each design the steady state VI characteristic produced by the frequency foldback circuit should be compared to the load VI curve to be certain that the converter will start under load.

The current sense feedback pin has an over current protection feature which forces a soft-start cycle only if the IC is not currently in a soft-start cycle. A voltage bias of 1.0V is added to the voltage sensed on the CS pin in order to facilitate zero duty-cycle when the error amplifier's output is less than 1.0V. The PWM latch is reset dominant so that if the error amplifier output is below 1.0V the output of the latch is not driven high.

The error amplifier is unity gain stable and has a wide gain-bandwidth product for accuracy. Its non-inverting input is internally set to 2.5V.

DETAILED DESCRIPTION AND DESIGN EQUATIONS

A description of the UCC3884 BiCMOS pulse width modulator and design equations will be presented followed by an example RCD Clamped Forward Converter design using the UCC3884 peak current mode controller [2,3,4].

Oscillator and Frequency Foldback Section:

The oscillator section has an independently programmable frequency and a maximum duty-cycle clamp. A single resistor sets the timing capacitor (CT) charge current which creates the positive slope portion of the oscillator waveform. A second resistor sets the timing capacitor discharge time. With reference to Figure 2 the oscillator waveform increases linearly from 1.5V to 3.5V and decreases linearly back to 1.5V completing one cycle. If T_{OSCon} represents the charge time and T_{OSCoff} is the discharge time then the frequency of the converter is given by

$$f = \frac{1}{T_{OSCon} + T_{OSCoff}} . \quad (1)$$

The output of the modulator can only be asserted during the positive slope portion of the oscillator waveform. With this limitation the maximum duty-cycle is given by the ratio of T_{OSCon} to $T_{OSCon} + T_{OSCoff}$;

$$D_{MAX} = \frac{T_{OSCon}}{T_{OSCon} + T_{OSCoff}} . \quad (2)$$

The oscillator off-time is a function of the main output voltage only if the VOUT pin drops below 3.5V. The VOUT pin may exceed 3.5V in which case the off-time is calculated using 3.5V. Note that the IC does not internally clamp this voltage to 3.5V. If the output is short circuited or a low impedance load is applied the feedback voltage to the VOUT pin decreases which causes T_{OSCoff} to increase. This will increase the period and therefore decrease the frequency.

Recall that the oscillator on-time (T_{OSCon}) is constant and does not vary with output voltage. Under nominal operating conditions the frequency is constant and equation 1 can be expanded to

$$f = \frac{1}{\frac{C_T \bullet (3.5 - 1.5)}{8.8 \bullet I_{ON}} + \frac{C_T \bullet (3.5 - 1.5)}{8.8 \bullet I_{OFF}}} = \quad (3)$$

$$\frac{1}{0.227 \bullet C_T \bullet \left(\frac{1}{I_{ON}} + \frac{1}{I_{OFF}}\right)} =$$

$$\frac{4.4}{C_T \bullet \left(\frac{R_{ON}}{1.5} + \frac{R_{OFF}}{3.5}\right)}$$

where C_T is the timing capacitor, R_{ON} sets the value of the C_T charging current, (8.8 • I_{ON}), and R_{OFF} sets the value of the C_T discharging current, (8.8 • I_{OFF}). The maximum current sourced from the ION and IOFF pins is limited to approximately 800µA.

To avoid start up problems, a resistor can be added from VREF to VOUT which provides a voltage bias to VOUT even when the output voltage is zero. The choice of value also sets the minimum operating frequency during frequency foldback, as will be reviewed in the example design section below.

Designs using an isolation transformer can derive a dc voltage level proportional to the output by using a peak detector circuit off of the bootstrap winding of the power transformer (Figure 8). This bias supply is normally required for isolated converters and therefore requires only a minimum of components.

Figure 6 shows the oscillator and frequency foldback portions of the UCC3884, where V_X is found by assuming no limiting action within the VOUT pin (see also Figure 2). V_X is given as

$$V_X = \frac{R_{OUT1} \| R_{OUT2}}{R_{OUT1} \| R_{OUT2} + R_{OUT3}} \bullet V_{REF} + \frac{R_{OUT1} \| R_{OUT3}}{R_{OUT1} \| R_{OUT3} + R_{OUT2}} \bullet V_O \quad (4)$$

where V_{REF} = 5V, V_O is the output voltage, and || represents parallel resistors. If equation 4 yields a V_X greater than 3.5V it would then be replaced with 3.5V. One possible design approach would be to ignore the loading of R_{OUT3} and set V_X slightly below the output voltage minus one-half of the maximum ripple voltage. With R_{OUT1} and R_{OUT2} known, set V_O = 0 and R_{OUT3} may be calculated based upon the minimum operating frequency desired.

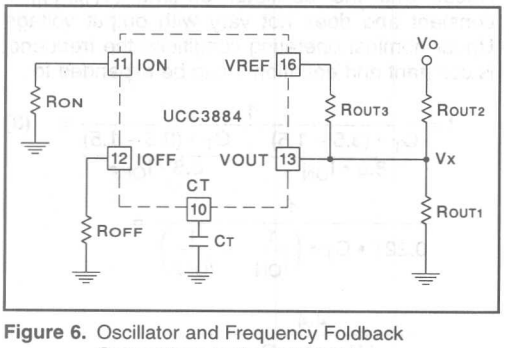


Figure 6. Oscillator and Frequency Foldback Connections to the UCC3884

Synchronization of Multiple ICs:

A CLKSYNC pin is provided which is used to synchronize two or more UCC3884 ICs. Multiple ICs are synchronized in frequency by connecting their CLKSYNC pins with capacitors to the CLKSYNC bus as shown in Figure 7. Each free running oscillator is designed with the same base frequency and the same maximum duty-cycle and is connected to the CLKSYNC bus with a capacitor and a pull-down resistor. A negative edged pulse from any IC will initialize all the ICs to start the upslope of their oscillator waveforms. For a given oscillator on the down-slope, if it receives a negative synchronization pulse before it reaches the 1.5V threshold, an internal MOS switch will quickly discharge its C_T down to 1.5V. After soft-start synchronization for each controller may take one or two cycles to come into lock. During frequency foldback under an output fault condition, the synchronization in the overloaded IC is inhibited and the converters can become unlocked. This is necessary since the overloaded ICs frequency is in foldback. The oscillators will resynchronize when the fault is removed. Due to tolerances, each free running oscillator frequency may be slightly different; therefore the CLKSYNC bus synchronizes to the highest frequency. For multiple PWM converters, synchronization to other controllers is only possible when the VOUT pin is greater than 3V.

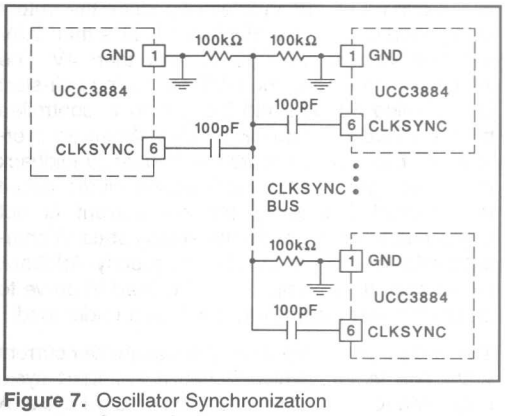


Figure 7. Oscillator Synchronization Connection Diagram

Volt-Second Clamp:

The volt-second duty-cycle clamp operates by taking the reciprocal of the voltage on VVS (see Figure 1) which is directly proportional to the input voltage and uses this signal to limit the duty-cycle. As V_{IN} increases, to maintain constant operating volt-seconds for a forward converter, the duty-cycle

decreases based upon

$$D_{OP} = \frac{V_O + V_D}{(V_{IN} - V_{DSon}) \bullet \frac{N_S}{N_P}}; \quad (5)$$

where D_{OP} is the operating duty-cycle, V_{DSon} is the on-state drain-to-source primary switch voltage, N_S is the secondary turns, N_P is the primary turns, and V_D is the voltage drop of the secondary rectifier diode [5]. In a similar fashion, the maximum duty-cycle clamp due to this volt-second function will also decrease and is given by

$$D_{VS} = \frac{K}{V_{VS}} \bullet \frac{T_{OSCon}}{T_{OSCon} + T_{OSCoff}} \quad (6)$$

$$= 1.1 \bullet \frac{D_{MAX}}{V_{VS}}$$

where D_{VS} is the duty-cycle clamp based upon applied volt-seconds to the transformer, V_{VS} is the voltage on the VVS pin, and K was calculated from

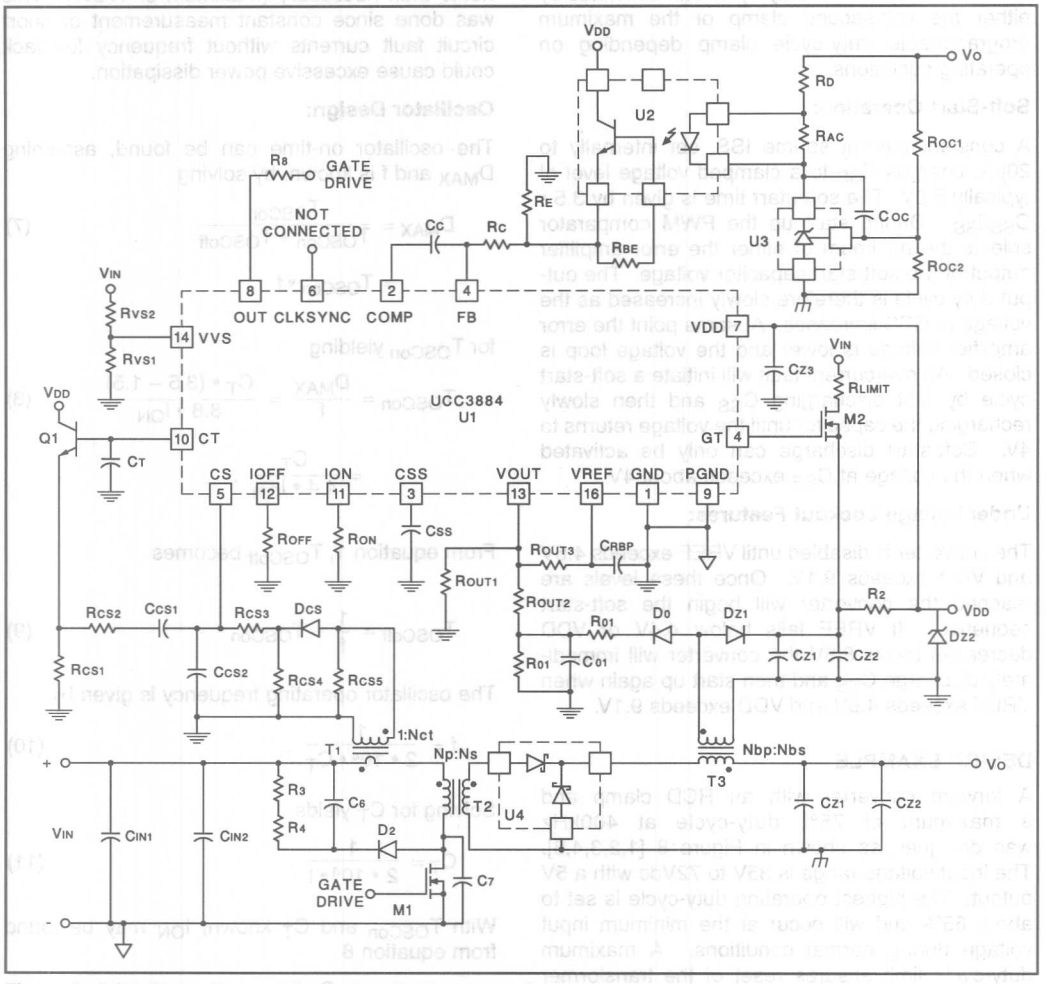


Figure 8. RCD Clamp Forward Converter with Frequency Foldback

the UCC3884 data sheet. The volt-second clamp is set by an external resistor divider network from the input voltage to the VVS pin. Normally, D_{VS} is chosen to exceed D_{OP} by some fixed percentage, say 10%. It may be necessary to put a small ceramic capacitor at the VVS pin to filter switching noise.

This feature allows for an accurate volt-second clamp within the input voltage range under load transient conditions. It is accurate since the timing capacitor tolerance does not effect equation 6. The voltage at VVS can be provided by 1% resistors and the internal accuracy is maintained to 3% (for the 0°C to 70°C temperature range). To limit the on-time at the minimum input voltage the maximum possible duty-cycle is clamped by D_{MAX}. The converters' actual duty-cycle can be limited by either the volt-second clamp or the maximum programmable duty-cycle clamp depending on operating conditions.

Soft-Start Operation:

A constant current source ISS, set internally to 20μA, charges C_{SS} to a clamped voltage level of typically 5.0V. The soft-start time is given by $3.5 \bullet C_{SS}/I_{SS}$. During start up the PWM comparator selects the minimum of either the error amplifier output or the soft-start capacitor voltage. The output duty-cycle is therefore slowly increased as the voltage at CSS increases. At some point the error amplifier voltage is lower and the voltage loop is closed. An overcurrent fault will initiate a soft-start cycle by first discharging C_{SS} and then slowly recharging the capacitor until the voltage returns to 4V. Soft-start discharge can only be activated when the voltage at C_{SS} exceeds about 4V.

Under Voltage Lockout Features:

The converter is disabled until VREF exceeds 4.6V and VDD exceeds 9.1V. Once these levels are reached the converter will begin the soft-start sequence. If VREF falls below 4.4V or VDD decreases below 8.8V the converter will immediately discharge C_{SS} and then start up again when VREF exceeds 4.6V and VDD exceeds 9.1V.

DESIGN EXAMPLE

A forward converter with an RCD clamp and a maximum of 75% duty-cycle at 400kHz was designed as shown in Figure 8 [1,2,3,4,6]. The input voltage range is 35V to 72Vdc with a 5V output. The highest operating duty-cycle is set to about 65% and will occur at the minimum input voltage during normal conditions. A maximum duty-cycle limit ensures reset of the transformer at low line.

Power Circuit Design:

A high frequency forward converter topology is often used in telecommunications applications requiring battery input from 35V to 72V DC with 48V nominal. A common output voltage is 5V and in this design a large capacitor, 10000μF, will be used to smooth the low frequency ripple components in order to more accurately measure average load currents during overload conditions. The output inductor was selected to be 1.3μH with a coupled winding for the bootstrap circuit (5:2 turns ratio). The transformer primary to secondary turns ratio is 8:2 and a RCD clamp is used to reset the transformer during the switch off-time. The laboratory prototype was built using higher rated components than necessary (maximum of 178W). This was done since constant measurement of short circuit fault currents without frequency foldback could cause excessive power dissipation.

Oscillator Design:

The oscillator on-time can be found, assuming D_{MAX} and f is known, by solving

$$D_{MAX} = \frac{T_{OSCon}}{T_{OSCon} + T_{OSCoff}} = T_{OSCon} \bullet f \quad (7)$$

for T_{OSCon} yielding

$$T_{OSCon} = \frac{D_{MAX}}{f} = \frac{C_T \bullet (3.5 - 1.5)}{8.8 \bullet I_{ON}} = \frac{C_T}{4.4 \bullet I_{ON}} . \quad (8)$$

From equation 1, T_{OSCoff} becomes

$$T_{OSCoff} = \frac{1}{f} - T_{OSCon} \quad (9)$$

The oscillator operating frequency is given by

$$f = \frac{1}{2 \bullet 10^4 \bullet C_T} . \quad (10)$$

Solving for C_T yields

$$C_T = \frac{1}{2 \bullet 10^4 \bullet f} . \quad (11)$$

With T_{OSCon} and C_T known, I_{ON} may be found from equation 8

$$I_{ON} = \frac{C_T}{4.4 \bullet T_{OSCon}} . \quad (12)$$

Now R_{ON} is given by

$$R_{ON} = \frac{1.5}{I_{ON}} . \quad (13)$$

The next step is to calculate the maximum value of I_{OFF} which occurs during non-frequency foldback conditions. A portion of equation 3, repeated below,

$$f = \frac{1}{0.227 \bullet C_T \bullet \left(\frac{1}{I_{ON}} + \frac{1}{I_{OFF}}\right)} \quad (14)$$

may be solved for I_{OFF} yielding

$$I_{OFF} = \frac{0.227 \bullet C_T \bullet f \bullet I_{ON}}{I_{ON} - 0.227 \bullet C_T \bullet f} . \quad (15)$$

Finally, the R_{OFF} resistor value is

$$R_{OFF} = \frac{3.5}{I_{OFF}} \quad (16)$$

These equations are used in a Mathcad spreadsheet listed in Appendix I [7].

Frequency Foldback Design:

The three resistors associated with frequency foldback may now be calculated. A useful approach is to first ignore the loading from the VOUT pin and ignore the R_{OUT3} connection. To allow for a small decrease in the output voltage before frequency foldback kicks in (this is not a requirement, but can be used to guarantee constant frequency operation under the expected output voltage ripple) set V_X = 4V and from Figure 6 one can write

$$V_X = 4 \approx \frac{R_{OUT1}}{R_{OUT1} + R_{OUT2}} \bullet V_O \quad (17)$$

where V_O is the actual output voltage. By arbitrarily selecting R_{OUT1}, the value of R_{OUT2} can be determined. Now, the selection of R_{OUT3} determines the minimum frequency of operation. Rewriting equation 16 for the general case (when the VOUT pin is less than 3.5V)

$$V_X = R_{OFF} \bullet I_{OFF} . \quad (18)$$

Setting V_O equal zero in equation 4 one solves

$$V_X = \frac{R_{OUT1} \| R_{OUT2}}{R_{OUT1} \| R_{OUT2} + R_{OUT3}} \bullet V_{REF} \quad (19)$$

for R_{OUT3}. With R_{OUT1}, R_{OUT2}, and R_{OUT3} known, equation 4 can be used in a Mathcad spreadsheet to plot operating frequency of the converter as a function of the output voltage. Listed in Appendix I is an example of the spreadsheet which includes the calculations and graphs of the steady state volt-second clamp and frequency foldback characteristics.

Volt-Second Clamp Design:

The voltage at the VVS pin is given by

$$V_{VS} = \frac{R_{VS1}}{R_{VS1} + R_{VS2}} \bullet V_{IN} \quad (20)$$

once R_{VS1} is selected R_{VS2} can be solved for after D_{VS} is chosen. From equation 6

$$V_{VS} = K \bullet \frac{D_{MAX}}{D_{VS}} \quad (21)$$

as an example D_{VS} may be set to 110% of D_{OP}. For this case, after solving for R_{VS2} in equation 20 with V_{VS} replaced using equation 21, one finds

$$R_{VS2} = R_{VS1} \bullet \left(V_{IN} \bullet \frac{D_{OP}}{D_{MAX}} - 1\right) . \quad (22)$$

Control Loop Component Calculations:

The concentration of this application note is to show the characteristics of the frequency foldback and volt-second clamp features of the UCC3884. Details of the small-signal modeling of the modulator and power circuit can be found in [8] and [9]. Integral compensation was used to set the crossover frequency to 9kHz with a gain of about 7dB needed at this frequency.

EXPERIMENTAL RESULTS

The RCD clamp forward converter was prototyped in the laboratory and relevant results are presented in the following section.

Frequency Foldback Data:

The primary current sense resistor in Figure 8 was increased to 32Ω from 16Ω (16Ω was used in the computer model that generated Figures 3 and 4) in order to limit the average load currents to reasonable values for easy measurement. The previous simulation results showed the basic phenomena of the current tail with and without frequency foldback. Due to effects not included in the computer model the experimental data differs from the simulated data. The computer model is a powerful tool to gain a fundamental understanding of the large signal VI characteristics as shown in Figures 3 and 4. It may be possible to take into account ignored complications so that the simulated results match

more closely the experimental data. It is thought that some of these effects could be the saturation of the magnetics (output inductor), errors in estimating the finite turn-off time of the MOSFET power stage switch and possible saturation of the primary current sense transformer. Despite these measurement inaccuracies the frequency foldback operation does reduce the current tail as compared to non-frequency foldback operation and this can be seen in the simulation results and the actual circuit measurement data.

Figure 9 shows normal operation at constant frequency with about a 4A average load current. The top waveform is the output voltage (5V, channel 3) followed by the oscillator waveform measured at

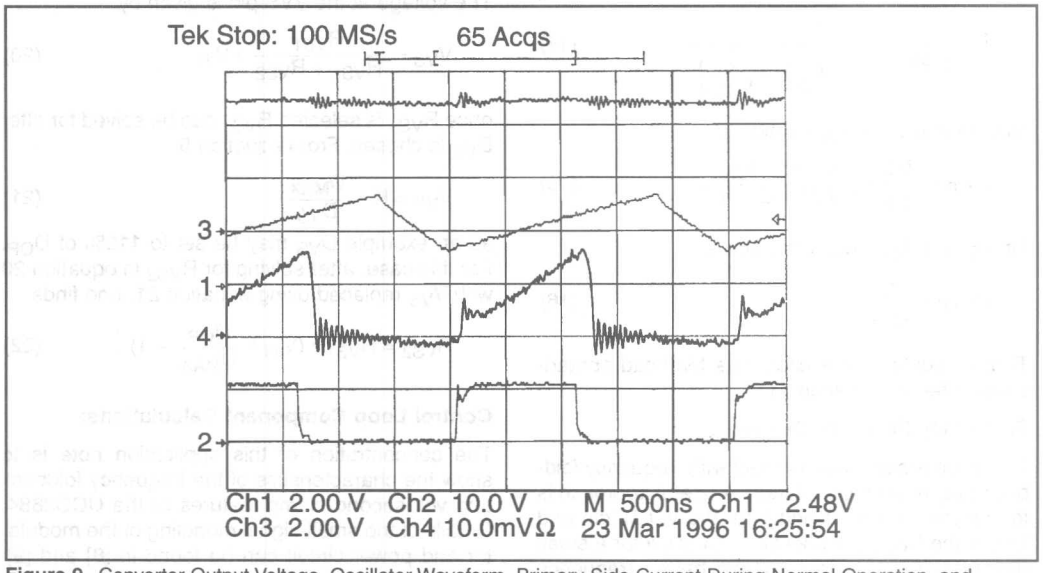


Figure 9. Converter Output Voltage, Oscillator Waveform, Primary Side Current During Normal Operation, and MOSFET Gate Voltage

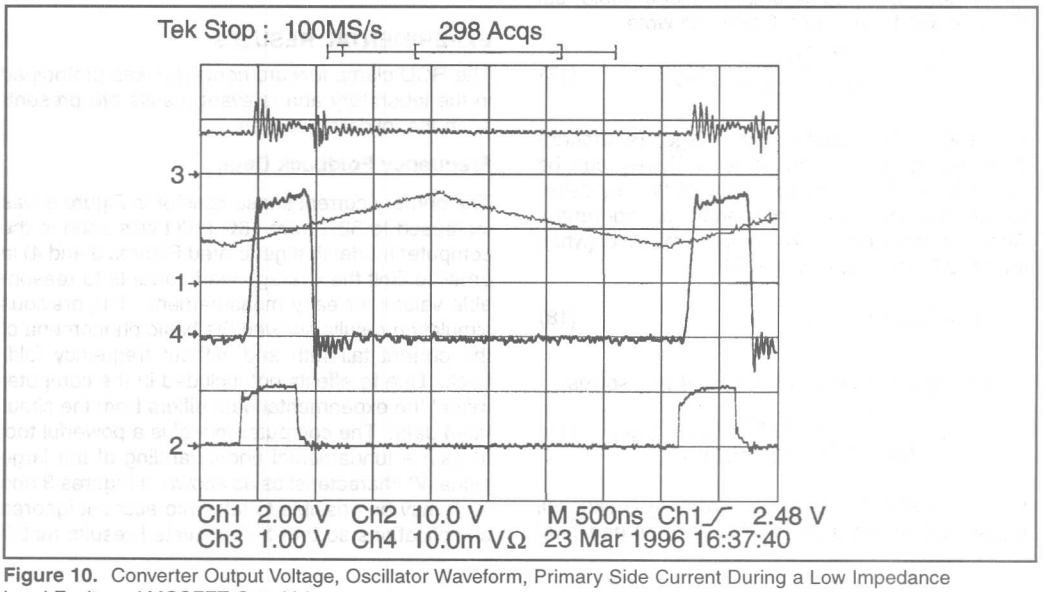


Figure 10. Converter Output Voltage, Oscillator Waveform, Primary Side Current During a Low Impedance Load Fault, and MOSFET Gate Voltage

pin 10 (CT, channel 1). Note that for small values of C_T the scope probe capacitance on pin 10 can decrease the frequency. The third from the top is the primary side current at 1A/div (channel 4). Note that there is a 470pF capacitor in parallel with the MOSFET primary switch to reduce clamp loss [2]. The bottom trace is the gate voltage at pin 8 (OUT, channel 2) which drives an IRF630 through a 13Ω resistor.

A low impedance load was applied and the resulting converter waveforms are shown in Figure 10 with the same scales as used in Figure 9 except the output voltage scale was decreased and the primary current scale on the AM503B was increased from 1A/div to 2A/div (channel 4). The average load current was 17.4A and the frequency was reduced from 403kHz to 267kHz. The output voltage decreased from 5.016V to 0.880V.

A toggle switch was used to change from frequency foldback to non-frequency foldback operation. This allowed direct comparison between frequency foldback and non-frequency foldback operation as the load resistance decreased. Figure 11 shows the data taken under the same conditions with and without frequency foldback. It was found that a fan was helpful in keeping the sense resistors cool in order to avoid drift during current measurement. The shape of the curves in Figure 11 differ from Figure 3, obviously the computer model has not taken into account all of the parasitic and saturation effects. The value of R_{OUT3} calculated in Appendix I was increased to 33.1k to generate the frequency foldback curve shown in Figure 11. The actual measured frequency versus output voltage is shown in Figure 12.

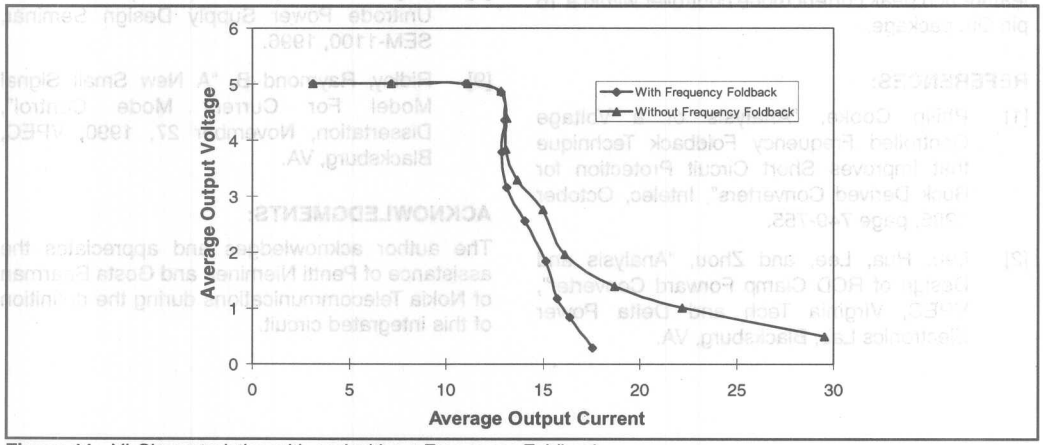


Figure 11. VI Characteristics with and without Frequency Foldback

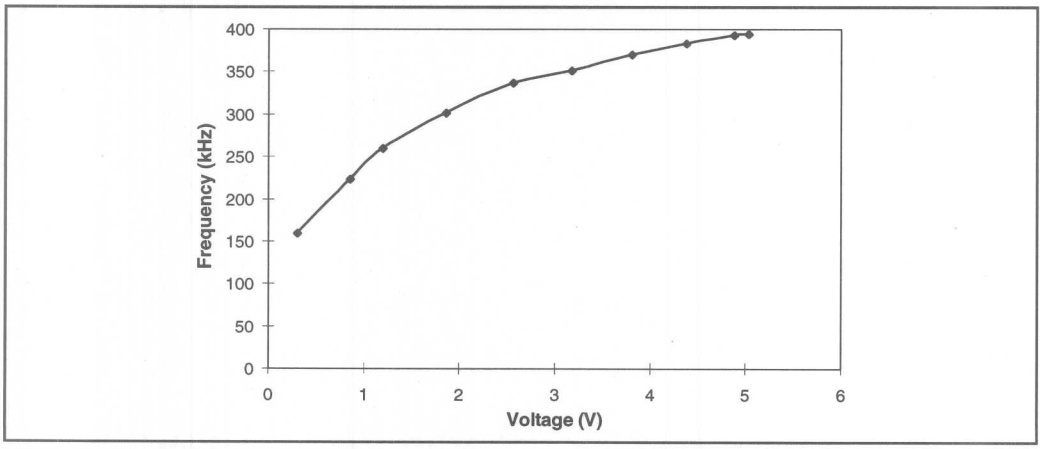


Figure 12. Measured Frequency versus Measured Output Voltage

SUMMARY

The UCC3884 peak current mode controller provides the designer a frequency foldback scheme to reduce the current tail often seen in high frequency buck derived converters. A possible practical design approach in the prototype circuit is to set the minimum frequency to about 1/3 of the nominal frequency and to use the simplified analysis outlined above to give first pass circuit values for the frequency foldback resistors R_{OUT1}, R_{OUT2}, and R_{OUT3}. During testing of the power converter low impedance loads can be applied for final adjustment of the frequency foldback resistors and to verify desired operation. The maximum duty-cycle clamp and volt-second clamp may be used to enhance performance and reliability of the power converter system. The undervoltage lockout, clock synchronization, depletion-mode MOSFET driver, and soft-start functions are all provided to complete a feature rich peak current mode controller within a 16 pin DIL package.

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[9] Ridley, Raymond B, "A New Small Signal Model For Current Mode Control", Dissertation, November 27, 1990, VPEC, Blacksburg, VA.

ACKNOWLEDGMENTS:

The author acknowledges and appreciates the assistance of Pentti Nieminen and Gosta Baarman of Nokia Telecommunications during the definition of this integrated circuit.

Appendix I: Oscillator and Volt-Second Calculations

High Performance UCC3884 PWM with Frequency Foldback and Volt-Second Clamp
Mathcad design worksheet. by Philip Cooke

Specifications:

Input Votage	35V<Vin<72V
Output voltage	5V dc
Operating frequency	400 kHz

$f := 400 \cdot 10^3$ Estimated operating frequency (for non-frequency foldback conditions).

$D_max := 0.75$ Maximum duty-cycle.

$N := \frac{8}{2}$ Primary transformer turns ratio.

$Vt := 3.5$ Peak oscillator voltage.

$Vb := 1.5$ Minimum oscillator voltage.

$Vd := 0.5$ Estimated voltage drop on secondary forward diode.

$Kon := 8.8$ Ion multiplier to charge Ct.

$Koff := 8.8$ Ioff multiplier to discharge Ct.

$K := 1.1$ Volt-second constant.

$Vds_on := 0.15$ Approximate voltage drop of primary switch.

$Vout := 5$ Output dc voltage.

$Vref := 5$ Output of on-board UCC3884 regulator.

$Vin_min := 35$ Minimum input voltage.

$Vin_max := 72$ Maximum input voltage.

Oscillator Calculations:

Calculate the timing capacitor from the frequency:

$Ct := \frac{1}{2 \cdot 10^4 \cdot f}$ which gives $Ct = 1.25 \cdot 10^{-10}$ select $Ct := 120 \cdot 10^{-12}$

Recalculate operating frequency, $f := \frac{1}{2 \cdot 10^4 \cdot Ct}$ so that $f = 4.167 \cdot 10^5$

The oscillator on time is given by equation 8 $Tosc_on := \frac{D_max}{f}$ $Tosc_on = 1.8 \cdot 10^{-6}$

Now from equation 12, calculate Ion

$Ion := \frac{Ct}{4.4 \cdot Tosc_on}$ so that $Ron := \frac{Vb}{Ion}$ $Ron = 9.9 \cdot 10^{4}$

Ioff is found from equation 15 $Ioff := \frac{0.2273 \cdot Ct \cdot f \cdot Ion}{Ion - 0.2273 \cdot Ct \cdot f}$ $Ioff = 4.548 \cdot 10^{-5}$

Finally, Roff is $Roff := \frac{Vt}{Ioff}$ $Roff = 7.696 \cdot 10^{4}$

Checking the Kon*Ion and Koff*Ioff values to be sure they don't exceed 800 mA: $Kon \cdot Ion = 1.333 \cdot 10^{-4}$ $Koff \cdot Ioff = 4.002 \cdot 10^{-4}$

Frequency Foldback Calculations:

Set Rout1 to 4.99 kW. $Rout1 := 4.99 \cdot 10^{3}$

Rearranging equation 17 to solve for Rout2: $Rout2 := \frac{Rout1}{4} \cdot Vout - Rout1$ $Rout2 = 1.248 \cdot 10^{3}$

The minimum frequency is selected to be 1/3.3 of the nominal frequency; now Ioff minimum can be calculated from equation 15:

$$Ioff := \frac{0.2273 \cdot Ct \cdot \frac{f}{3.3} \cdot Ion}{Ion - 0.2273 \cdot Ct \cdot \frac{f}{3.3}} \qquad Ioff = 4.457 \cdot 10^{-6}$$

With Ioff equation 18 is used to find the minium value of Vx

$$Vx := Roff \cdot Ioff$$

With $Vx = 0.343$ V Rout3 is given by (equation 19):

$$Rout3 := \frac{Rout1 \cdot Rout2}{Rout1 + Rout2} \cdot \left(\frac{Vref}{Vx} - 1 \right) \qquad Rout3 = 1.355 \cdot 10^{4}$$

Volt-Second Calculations:

Choose 10 kW for Rvs1 and set D_vs = 1.467*D_max; $Rvs1 := 10 \cdot 10^3$

Calculate the operating duty-cycle at Vin_min. $Dop := \frac{Vout + Vd}{(Vin_min - Vds_on) \cdot \frac{1}{N}}$

From equation 22 $Rvs2 := Rvs1 \cdot \left(\frac{Vin_min \cdot Dop}{D_max} - 1 \right)$ $Rvs2 = 2.846 \cdot 10^5$

Final Selection of Components:

$Rout1 := 4.99 \cdot 10^3$ $Rout2 := 2.00 \cdot 10^3$ $Ron := 100 \cdot 10^3$ $Roff := 76.8 \cdot 10^3$

$Rout3 := 13.7 \cdot 10^3$ $Ct := 120 \cdot 10^{-12}$ $Rvs1 := 10 \cdot 10^3$ $Rvs2 := 287 \cdot 10^3$

Recalculate Ion, Ioff, f, Tosc_on, and Tosc_off:

$Ion := \frac{Vb}{Ron}$ $Ion = 1.5 \cdot 10^{-5}$ $Kon \cdot Ion = 1.32 \cdot 10^{-4}$

$Ioff := \frac{Vt}{Roff}$ $Ioff = 4.557 \cdot 10^{-5}$ $Koff \cdot Ioff = 4.01 \cdot 10^{-4}$

$f := \frac{1}{2 \cdot 10^4 \cdot Ct}$ $f = 4.167 \cdot 10^5$

$Tosc_on := \frac{Ct}{4.4 \cdot Ion}$ $Tosc_on = 1.818 \cdot 10^{-6}$

$Tosc_off := \frac{1}{f} - Tosc_on$ $Tosc_off = 5.818 \cdot 10^{-7}$

Derive Equations to Plot:

$i := 0, 1 .. 100$ Set up a range variable.

$Vin_i := Vin_min + \left(\frac{Vin_max - Vin_min}{100} \right) \cdot i$ Use i as a parameter to vary Vin.

$$Vo_i := Vout \cdot \left(1 - \frac{i}{100}\right)$$

Vary Vo parametry with i.

$$D_op_i := \frac{Vout + Vd}{\left(Vin_i - Vds_on\right) \cdot \frac{1}{N}}$$

Calculate the steady state operating duty-cycle as a function of input voltage.

The Vx voltage is calculated assuming no clamp or load of the VOUT pin:

$$Vx_i := \frac{\frac{Rout1 \cdot Rout3}{Rout1 + Rout3}}{\left(\frac{Rout1 \cdot Rout3}{Rout1 + Rout3} + Rout2\right)} \cdot Vo_i + \frac{\frac{Rout1 \cdot Rout2}{Rout1 + Rout2}}{\left(\frac{Rout1 \cdot Rout2}{Rout1 + Rout2} + Rout3\right)} \cdot Vref$$

Next, the 3.5V limit is taking care of by the Mathcad conditional if statement:

$$Vout_i := if\left(Vx_i > 3.5, 3.5, Vx_i\right)$$

Now the Ct discharge current, Tosc_off, and f can be found as a function of Vout;

$$Ioff_i := \frac{Vout_i}{Roff} \qquad Tosc_off_i := \frac{(Vt - Vb) \cdot Ct}{Koff \cdot Ioff_i} \qquad f_i := \frac{1}{Tosc_on + Tosc_off_i}$$

A temporary variable is used to calculate the voltage at the VVS pin as the input voltage varies. Stop gaps of 0.6V and 4.5V are assumed.

$$Vtemp_i := \frac{Rvs1}{Rvs1 + Rvs2} \cdot Vin_i$$

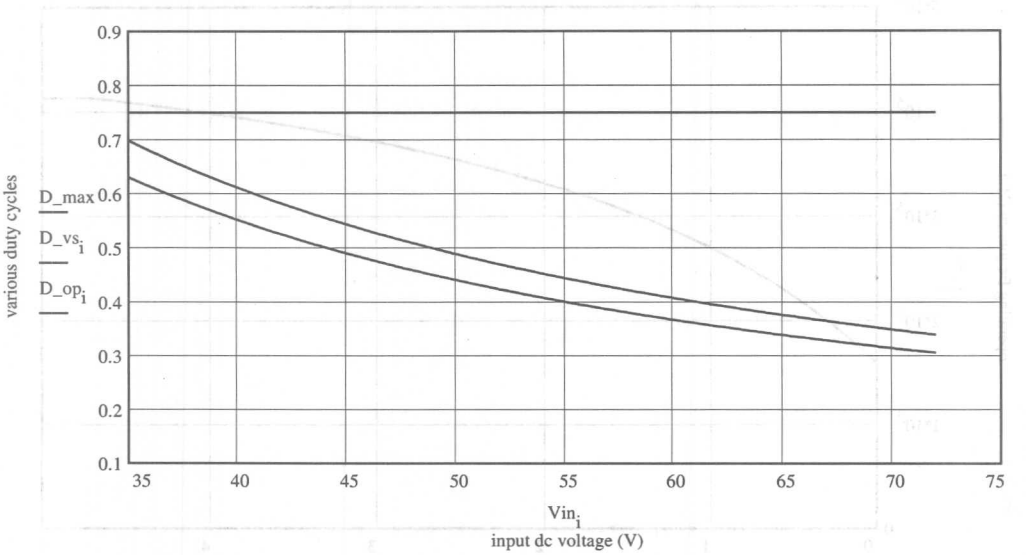
$$Vvs_i := if\left(Vtemp_i < 0.6, 0.6, if\left(Vtemp_i > 4.5, 4.5, Vtemp_i\right)\right)$$

Finally, the effective volt-second duty-cycle clamp is calculated;

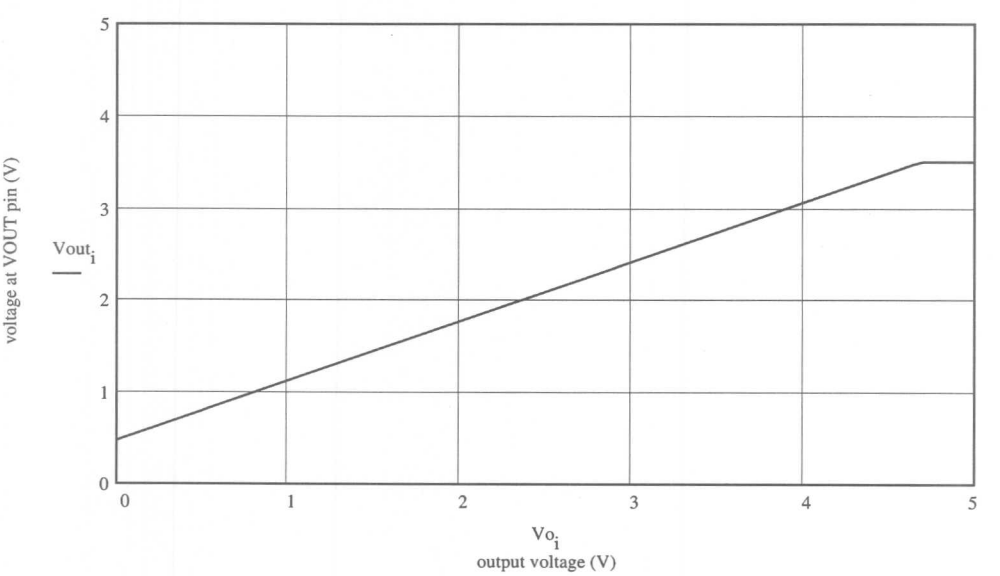
$$D_vs_i := K \cdot \frac{D_max}{Vvs_i}$$

Plot Expected Results:

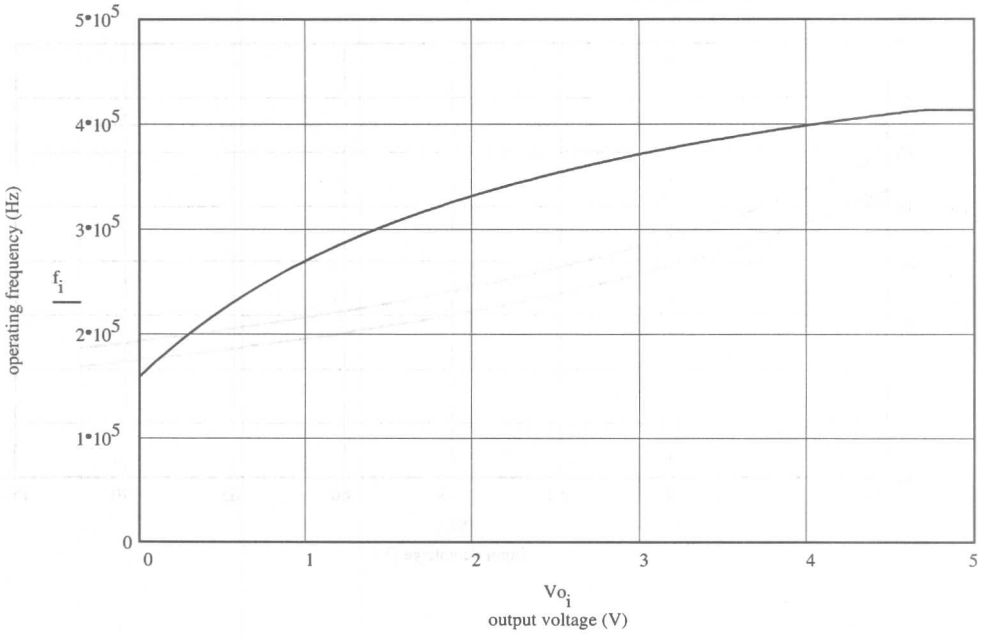
Waveforms from top to bottom; maximum duty cycle, volt-second clamp, and operating duty cycle

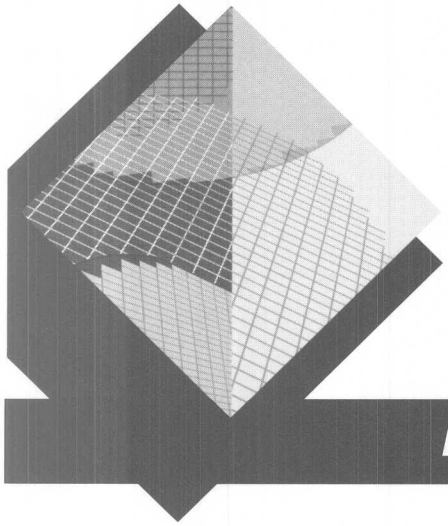


Voltage at the VOUT pin as the actual output voltage varies.



Frequency foldback characteristics: as the output voltage decreases the converters operating frequency decreases.





Please see Unitrode Databook (IC-1050) for complete datasheets.

Please note Hot Swap Power Managers were formerly known as "Electronic Circuit Breakers".

Design Notes

4


UNITRODE

A SIMPLE ISOLATION AMPLIFIER USING THE UC1901

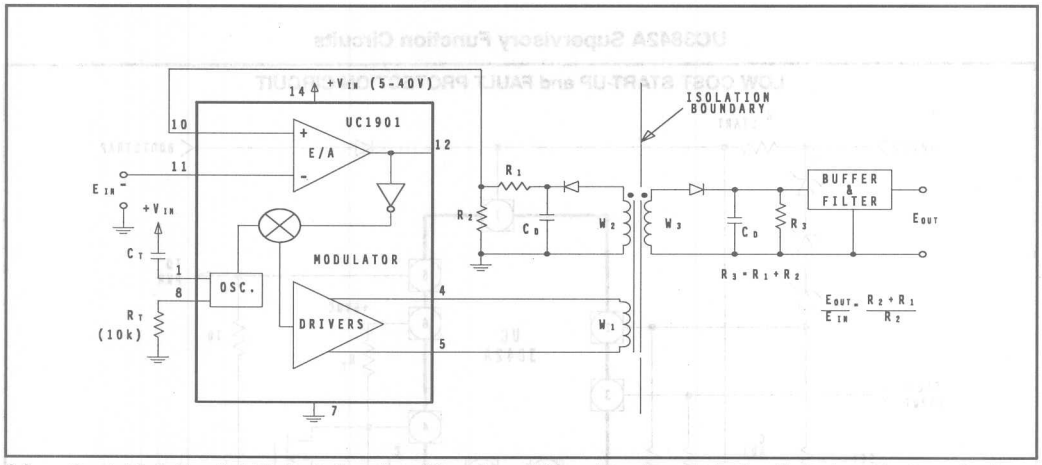
The UC1901 Isolated Feedback Generator has other applications besides providing isolated feedback in switching power supplies. This IC's amplitude modulation system and error amplifier can be used to implement a very low cost, high bandwidth, isolation amplifier. Isolation amplifiers of this type find use in switching power supplies, motor controls, instrumentation, industrial controls and medical systems.

The UC1901 generates a programmable high frequency carrier signal (up to 5MHz) with an amplitude that is controlled by a high gain error amplifier. In a typical feedback application, this amplifier and modulator are used, in conjunction with the UC1901's 1.5V reference and a small signal coupling transformer, to provide precision regulation for an isolated switching power supply. Capacitively coupled feedback around the UC1901 error amplifier determines the device's small signal AC response, but the DC operating point is determined by the requirements of the overall power supply loop. By adding an additional winding on the coupling transformer and a demodulator circuit for this winding, local DC feedback can be provided to the UC1901's error amplifier. In this mode very accurate DC, as well as small signal, AC, transfer functions can be established across the isolation boundary.

The configuration of an isolation amplifier using the UC1901 is shown in the figure below. The drivers on the UC1901 couple an amplitude modulated carrier to two matched windings (W2 and W3) on a small signal transformer. The demodulated signal from winding W2 is used to provide feedback to the UC1901's error amplifier while the demodulated signal from W3 is the isolated output signal. The use of the feedback winding linearizes the transfer function of the overall amplifier and allows DC signals to be accurately transferred. Matching of the two demodulator windings and demodulator circuits is important to maximize linearity and minimize DC offsets. An optional output buffer and filter will reduce residual carrier ripple and isolate the output demodulator from its load. The internal gain compensation on the UC1901 is sufficient for stable operation with overall gains down to 12dB. This circuit requires a supply voltage to the UC1901 that, if not available in the system already, can be generated using a second similar circuit operating in the reverse direction.

The primary features of this circuit are:

1. Good Signal Linearity
2. Wide Bandwidth (3dB Bandwidths > 500kHz)
3. High Isolation Capability
4. Low Cost



A Low Cost, High Bandwidth, Isolation Amplifier: An additional feedback winding linearizes the transfer function of the amplifier by matching the coupling characteristics to the isolated output.

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UC3842A
LOW COST START-UP AND FAULT PROTECTION CIRCUIT

This circuit optimizes control circuit performance to include:

- **Low Start-up Current, Less Than 0.5 ma**
- **MOSFET Compatible Undervoltage Lockout Thresholds 16V Turn-on, 10V Turn-off**
- **Programmable Restart Delay HICCUP Fault Protection**
- **Auxiliary 5V Precision Reference**
- **Overvoltage/Overtemperature Protection**

CIRCUIT DESCRIPTION AND OPERATION:

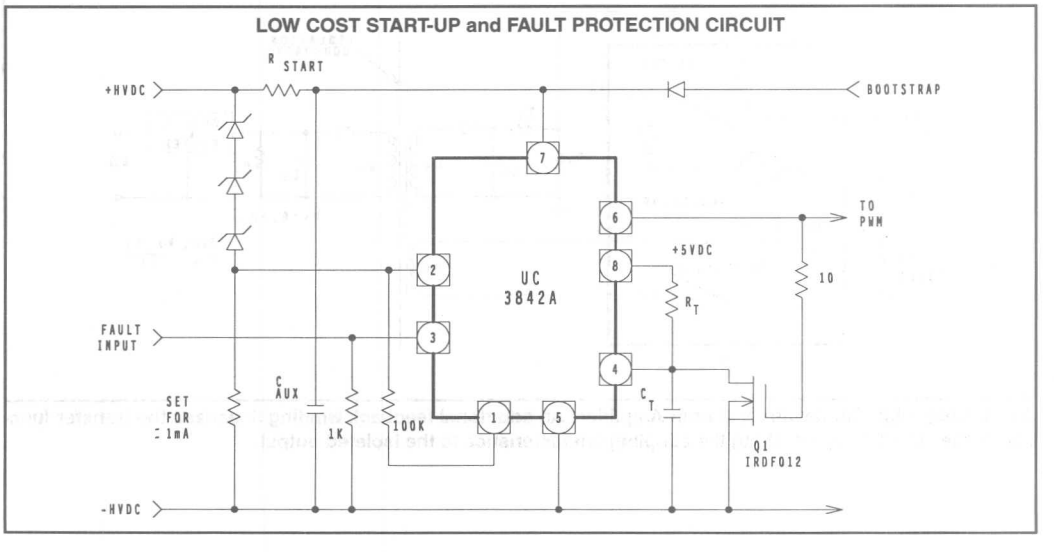
The UC3842A Controller is featured in this design ***NOT*** as the power supply control IC, but in a supervisory function to assist the principal PWM. It will be utilized to facilitate a low current start-up of less than 0.5 milliamp from the high voltage bulk supply. Additionally, the UC3842A features 16 volt turn-on and 10 volt turn-off thresholds, ideally suited for power mosfet gate drive circuits. The 1 amp output of the UC3842A is used to switch the auxiliary supply voltage to the principal PWM controller, a UC3825 or UC3846 for example.

The oscillator of the UC3842A is configured to generate a constant off time, corresponding to the desired restart delay interval. At the beginning of its operation, the UV initiates a clock cycle and the PWM output at pin 6 goes high. This is fed to transistor Q_1 which pulls the R_t/C_t input at pin 4 low, thus "freezing" the oscillator, while keeping the PWM output high. Once a valid fault (greater than 1 volt) is received at the current sense input (pin 3), the output at pin 6 will go low. Transistor Q_1 is then turned off, and the oscillator generates an off period, or delay as programmed by the R_t/C_t components. This procedure will repeat as often as dictated by the fault conditions, but significantly reduces the average short circuit currents and power dissipation.

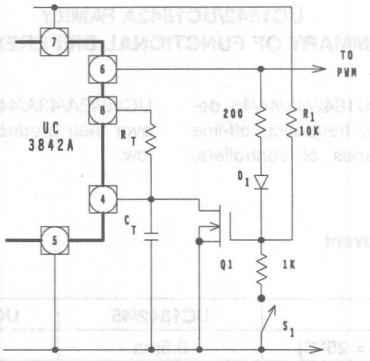
The UC3842A's current sense node is used as the fault input, and can be configured to provide numerous safeguards. Primary overvoltage protection is accomplished by using a simple resistor divider network or series string of zener diodes to the high voltage rail. Overtemperature protection is possible by including the UC3730 Precision Thermal Monitor IC, or a variable impedance thermistor. In a simple configuration, the fault circuit is designed to deliver a 1 volt input to pin 3 of the UC3842A when a fault response is necessary. The error amplifier can also be biased to accept lower amplitudes of valid fault inputs at the current sense input. A precision five volt auxiliary supply is made available at the IC's reference output, pin 8 and can supply 20 milliamps maximum.

UC3842A Supervisory Function Circuits

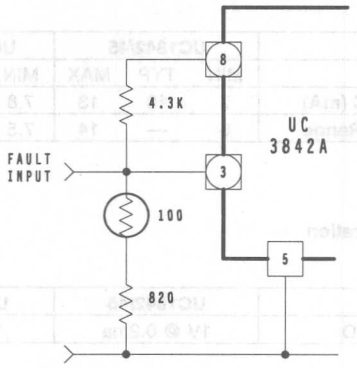
LOW COST START-UP and FAULT PROTECTION CIRCUIT



COMBINED LATCH/RESET/HICCUP FUNCTIONS
General Circuit



OVER-TEMPERATURE PROTECTION
using 50 to 100Ω thermocouples



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UC1842/UC1842A FAMILY
SUMMARY OF FUNCTIONAL DIFFERENCES

The industry standard series of UC1842/43/44/45 devices has been improved for higher frequency, off-line power supplies. This new "A" series of controllers, UC1842A/43A/44A/45A, feature three major advantages over their predecessors as shown in the summary below.

Start Up Current

	UC1842/45	UC1842A/45A
Typical (T_J = 25°C)	0.5ma	0.3ma
Maximum (T_J = 25°C)	1.0ma	0.5ma

Oscillator Discharge Current

	UC1842/45			UC1842A/45A		
	MIN	TYP	MAX	MIN	TYP	MAX
At T_J = 25°C (mA)	7	10	13	7.8	8.3	8.8
Overtemp. Range	6	—	14	7.5	—	8.8

Output Saturation

	UC1842/45	UC1842/45A
During UVLO	1V @ 0.2ma	1V @ 10ma

The reduced start-up current is of particular concern in offline supplies where the IC is "powered-up" from the high voltage DC rail, then bootstrapped to an auxiliary winding on the main transformer. Power is then dissipated in the start-up resistor which is sized by the IC's start-up current. Lowering this by 50% in the "A" version family will reduce the resistors power loss by the same percentage.

Precision operation at high frequencies with an accurate maximum duty cycle can now be obtained with the "A" family of devices due to its trimmed oscillator discharge current. This nullifies the effects of production variations in the initial discharge current or deadtime.

Another significant improvement has been made in the output section, specifically to the lower totem-pole transistor's operation during undervoltage lockout. The "A" series of devices prevent the power MOSFETs from parasitically turning-on at powerup due to the "Miller" effect. This new technique allows the IC to sink higher currents at lower saturation voltages than it's predecessors.

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Design Note

UC3840/UC3841/UC3851 PWM CONTROLLERS
SUMMARY OF FUNCTIONS AND DIFFERENCES

The UC3840/UC3841 and UC3851 PWM controllers incorporate numerous protection features for switch mode power supplies. The list includes programmable undervoltage lockout thresholds, programmable current limit thresholds, overvoltage protection, soft-start and external stop/reset capability. While these controllers are similar in concept, there are subtle differences amongst them in the operation of the error latch circuitry, specifically, the external stop and reset inputs. The UC3841 and UC3851 ICs feature an improved circuit design which simplifies the interface to the internal protection circuitry. A summary of the functions and modes of operation is listed below.

EXTERNAL STOP

	UC3840	UC3841/51
Low (<0.8V)	Stop	Defeat E/L Operation
High	Normal	Stop
Open	Normal	Normal
Cap. to GND During Power-up	Not Recommended	Delay E/L Operation at ≈ 13msec/µF

E/L= Error Latch

RESET

	UC3840	UC3841/51
High (>3.2V)	Latch	Latch
Low (<2.8V)	Requires UV Cycle to Reset	Reset

SOFT START

	UC3840	UC3841/51
After UV or Reset	Unlatched	Latched ($V_{SS} \leq 0.40V$)

The UC3851 controller incorporates two additional features, a toggle flip-flop for an accurate 50% maximum duty cycle clamp, and a 1 amp peak totem-pole output for driving power MOSFETs. Maximum duty cycles and output configurations for each device is shown below.

MAXIMUM DUTY CYCLE (T_J = 25°C)

	UC3840/41	UC3851
R_T = 20k, C_T = 1nF	0-95%	0-46%

PWM OUTPUT

	UC3840/41	UC3851
1A (PK)	Open Collector Active Low	Totem Pole Active High

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UC3842A FAMILY
FREQUENCY FOLDBACK TECHNIQUE PROVIDES PROTECTION

Excessive power dissipation in switching devices can occur during start-up and overload conditions in many switchmode power supplies. Many sophisticated PWM controllers provide the means for protection against these conditions; however, simple low-cost controllers will require additional circuitry. The circuit described below utilizes only one additional resistor and transistor to enhance the performance of the UC3842A family of controllers.

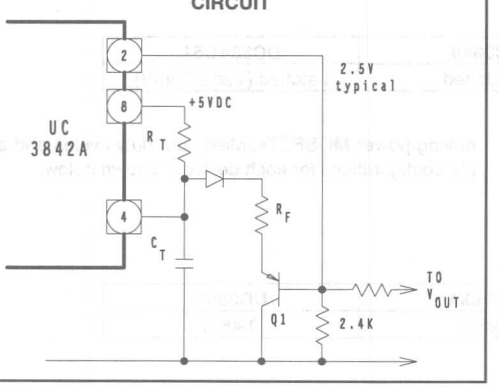
The power supply output voltage is fed to the error amplifier inverting input (pin 2) at a 2.5 volt amplitude under normal operating conditions. During start-up or overload, however, this voltage can drop to zero. The circuit shown uses this feedback voltage to divert normal charging current from the IC's timing capacitor to ground whenever the feedback voltage is below the 2.5 volt nominal. A linear three-to-one reduction of oscillator frequency is obtainable for most applications. This technique lengthens the potential maximum on-time and reduces the programmed deadtime. In many circuits, however, the peak current limit threshold is reached early in the cycle under these overload conditions, and this is not a problem. For most applications, the foldback resistor value (R_F) should equal that of the timing resistor (R_T).

EXAMPLE:

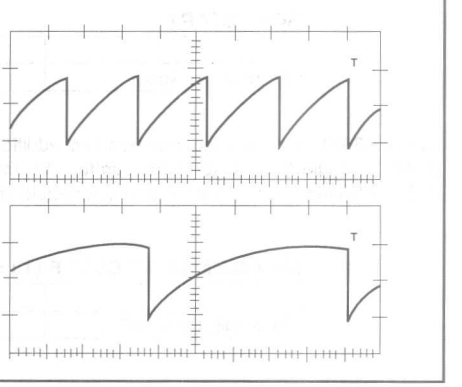
100 kHz operation, R_T = 15k, C_T = 1 nF, R_F = 15k, Q_1 = 2N2907A

OPERATING MODE	NORMAL	OVERLOAD
$V_{E/A}$ - (pin 2)	2.50V	0.00V
Oscillator Freq.	105 kHz	36 kHz

FREQUENCY FOLDBACK TECHNIQUE CIRCUIT



OSCILLATOR FREQUENCY



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PROGRAMMABLE ELECTRONIC CIRCUIT BREAKER

The design of a programmable electronic circuit breaker is shown below which utilizes the UC3843A control IC to facilitate a high speed turn-off following an overcurrent condition. This low cost, industry standard IC contains the required protection features and drive capability in a single 8 pin device.

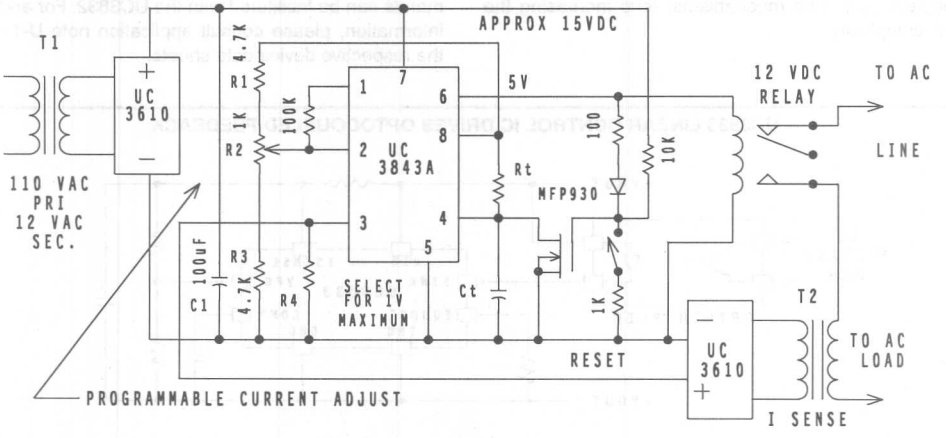
CIRCUIT OPERATION

Power to the controller is provided by a simple, low cost 60Hz transformer from the AC line which delivers 12 VAC at the secondary. The output current is determined primarily by the relay used with an additional 10 milliamps, or so, drawn by the IC. Undervoltage lockout prevents any operation until 10 VDC is obtained across capacitor C1, when the UC3843A will turn on. The PWM output at pin 6 goes high which drives the relay ON and switches the load across its respective power source. The load current is sensed by the current transformer T2, multiplied by its turns ration(N) and develops a voltage across the sense resistor R4. This resistor is scaled to delivery 1 volt maximum at the full load current and is one input to the PWM comparator.

While the output at pin six is high transistor Q1 is also turned ON which disables the ICs oscillator, locking the output high until toggles by the PWM. A 10k resistor (R5) to the supply voltage (pin 7) supplies bias to Q1 after the output has gone low, providing a latched OFF condition. This can easily be reset by pulling Q1's gate low through 1k ohms to ground as shown.

SCHEMATIC DIAGRAM

ELECTRONIC CIRCUIT BREAKER FEATURES HIGH SPEED CURRENT LIMITING



The other input to the PWM comparator is represented by the voltage at pin 1, the error amplifier output which can be adjusted by resistor R2. Internally, this voltage is reduced by two diode drops then attenuated to one-third its amplitude. The PWM circuitry compares this voltage with that of the current sense input at pin 3. When the current sense input exceeds the threshold set by resistor R2, the comparator is tripped and the ouptput at pin 6 is latched OFF.

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Design Note

OPTOCOUPLER FEEDBACK DRIVE TECHNIQUES

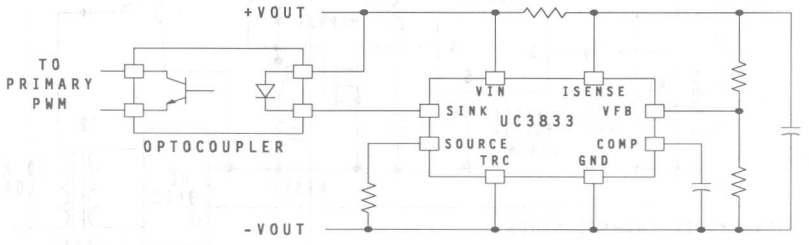
The use of optocouplers in the feedback path of switch-mode power supplies is probably one of the most common practices in the industry. Benefits of this method include low component cost, high voltage isolation and simplicity of design and implementation. Although adequate for many existing designs, the need for additional loop gain bandwidth occurs as switching frequencies are pushed towards the megahertz region.

One of the most popular ways to drive an optocoupler utilizes a TL431 Adjustable Shunt Regulator. It is configured on the output side of the power supply to modulate the optocoupler's photo diode current as a function of the power supply output voltage. Across its isolation boundary, the optocoupler transistor is connected to the PWM controller's error amplifier on the primary side of the power supply. Variations in the output voltage are optically transferred back to the error amplifier and control loop for correction. Providing additional features like over current protection or external shutdown require extra optocouplers and drive mechanisms, thus increasing the circuit complexity.

A linear regulator control IC, such as the UC3832, UC3833 or UC3836 can be substituted for the '431 while providing numerous additional features besides regulating the output. Overcurrent limiting and fault protection can be combined with the error voltage to drive the optocoupler and override it when necessary. Handshaking with external control logic, such as shutdown and sequencing is greatly simplified since the control IC is referred to the same ground. The most obvious benefit, however, is the introduction of the supplementary error amplifier in the feedback loop with programmable compensation.

Depending on the specific application, current limiting can be tailored to accommodate a programmable foldback characteristic, constant current or complete overcurrent shutdown. The UC3832 and UC3833 provide an addition level of versatility by offering a programmable duration event timer in the current limit circuitry. An adjustable trip threshold to accommodate varying load demands can be facilitated with the UC3832. For additional information, please consult application note U-116 and the respective device data sheets.

UC3833 LINEAR CONTROL IC DRIVES OPTOCOUPLED FEEDBACK



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OPTOCOUPLER FEEDBACK DRIVE TECHNIQUES USING THE UC 3901 AND UC3903

Numerous techniques and devices are available to the designers of optocoupler feedback circuits. The more traditional approaches utilize either an adjustable shunt regulator like the TL431 device or an op-amp and voltage reference as the optocoupler driver. While these approaches do satisfy the basic requirements in many applications, quite often they lack the performance that is achievable from a more sophisticated circuit. Too often, these low cost solutions necessitate additional protection circuitry elsewhere in the control circuit to overcome the deficiencies in the feedback path.

A variety of low cost supervisory ICs contain the required building blocks for the more demanding optocoupler feedback drive applications. Initially developed to address other specific power supply tasks, several control ICs excel in the role as precision optocoupler control and drivers.

The basic building blocks necessary for optocoupler feedback control are a precision reference, an error amplifier and a drive stage capable of approximately 20 milliamps. In a typical application, the power supply output voltage is monitored and compared to a reference voltage to the error amplifier inputs. Loop compensation and gain are programmed around the amplifier, and the resultant error voltage (Ve) modulates the optocoupler drive current, hence feedback.

In addition to the simple regulation of output voltage, several other housekeeping functions can be performed on the secondary side of the power supply - all with a single integrated controller. Fault protection, for example, from an over voltage or an over current condition can be detected and used to override the normal optocoupler drive. An undervoltage lockout feature could prevent false feedback information during power-up and power down sequences of the power supply. Also, a POWER-OK indicator could separately communicate with the primary side controller, or used to gate the optocoupler drive at the secondary side.

Basic Optocoupler Driver Circuit

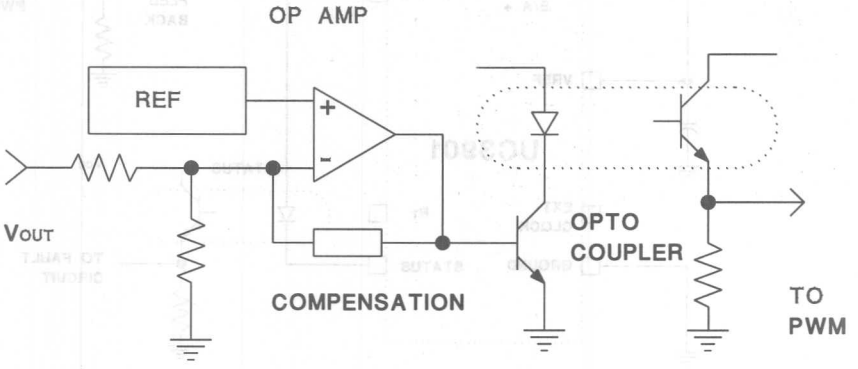


Figure 1.

THE UC 3901 ISOLATED FEEDBACK GENERATOR

Many isolated feedback applications required higher performance than can be obtained from an optocoupler feedback technique. Generally, these fall into one of two categories; high frequency switchers (above 250kHz) and those with very high voltage isolation requirements (greater than 5kV). The UC 3901 was developed to amplitude modulate a high frequency carrier applied to a transformer in place of the optocoupler. A peak detection circuit is used to reconstruct the error voltage waveform across the isolation boundary.

By disabling the internal oscillator, no chopping occurs and the outputs operate as linear drivers. When placed across an optocoupler this configuration yields similar results to other drive techniques - with two advantages. First, a closed loop startup of the power supply can be obtained since both inputs to the error amplifier are made available. Rather than using the traditional approach of soft-starting the error amplifier output, the noninverting, or reference input is gradually ramped up. This technique prevents a large overshoot from occurring as the output approaches regulation. In contrast to the prior method, the amplifers loop compensation network is not abnormally biased during startup - causing the output excursions. Additionally, an over and under voltage detection is available at the UC3901 "Status output" pin. This open collector output can drive a separate fault indication optocoupler for communication to the PWM controller.

Optocoupler Drive Circuit Features Additional Protection

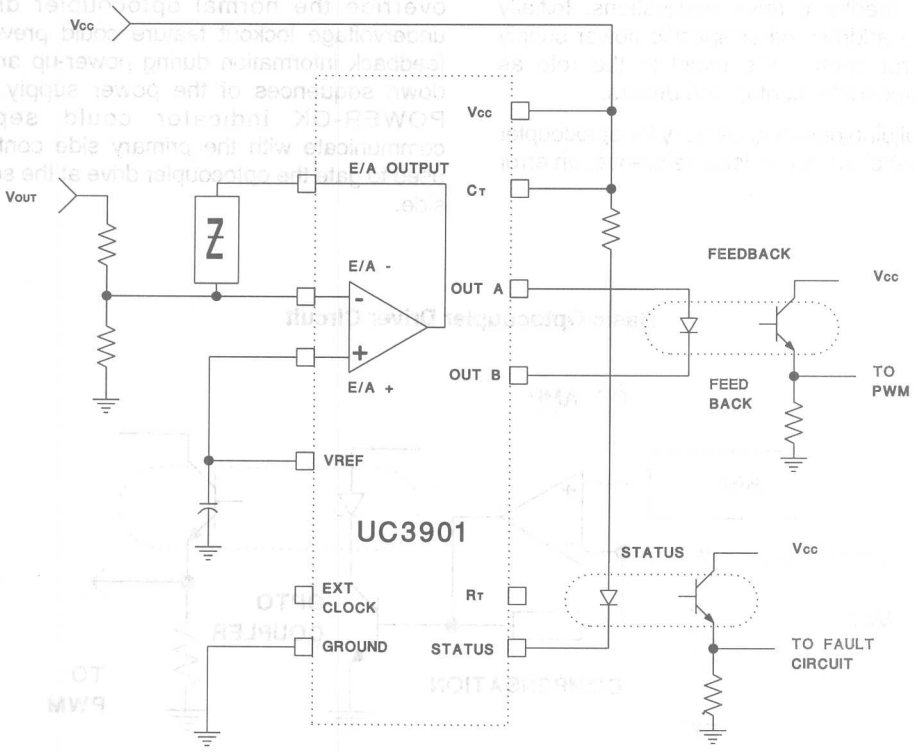


Figure 2.

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IGBT DRIVE USING MOSFET GATE DRIVERS

John A. O'Connor

IGBT Drive Requirements

Insulated gate bipolar transistors (IGBTs) are gaining considerable use in circuits requiring high voltage and current at moderate switching frequencies. Typically these circuits are in motor control, uninterruptible power supply and other similar inverter applications. Much of the IGBTs popularity stems from its simple MOSFET-like gate drive requirement. In comparison to bipolar transistors which were formally used in such designs, the IGBT offers a considerable reduction in both size and complexity of the drive circuitry. Recent improvements in IGBT switching speed has yielded devices suitable for power supply applications, thus IGBTs will compete with MOSFETs for certain high voltage applications as well. Many designers have therefore turned to MOSFET drivers for their IGBT drive requirements.

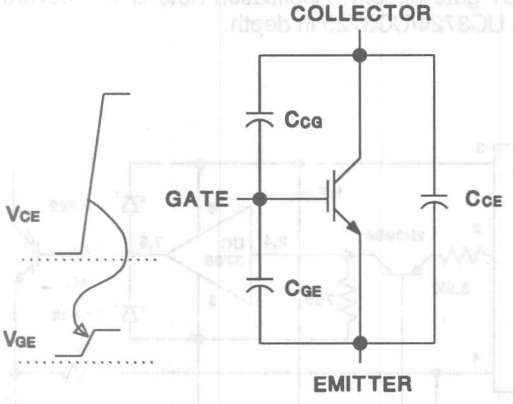


Figure 1. High dv/dt at the collector couples to the gate through parasitic capacitance.

IGBT drive requirements can be divided into two basic application categories: Those that do not apply high dv/dt to the collector/emitter of the IGBT when it is off, and those that do. Examples of the former are buck regulators and forward converters, where only one switch is employed or multiple switches are activated synchronously. High dv/dt is applied during the off-state in most bridge circuits such as inverters and motor controllers, when opposing devices are turned on. Simultaneous conduction of opposing devices can occur in such circuits, often with catastrophic results if proper gate drive and layout precautions are not followed. This behavior is caused by parasitic collector to gate (miller) capacitance, effectively forming a capacitive divider with the gate to emitter capacitance and thus inducing a gate to emitter voltage as illustrated in figure 1.

When high off-state dv/dt is not present, the IGBT can be driven like a MOSFET using any of the gate drive circuits in the UC37XX family as well as from the drivers internal to many switching power supply controllers. Normally 15 volts is applied gate to emitter during the on-state to minimize saturation voltage. The gate resistor or gate drive current directly controls IGBT turn-on, however turn-off is partially governed by minority carrier behavior and is less effected by gate drive.

There are several techniques which can be employed to eliminate simultaneous conduction when high off-state dv/dt is present. The most important technique, which should always be employed, is a Kelvin connection between the IGBT emitter and the driver's ground. High di/dt present in the emitter circuit can cause substantial transient voltages to develop in the gate drive circuit if it is not properly referenced. The Kelvin drive connection also minimizes the effective driver impedance for maximum attenuation of the dv/dt induced gate voltage. This requirement adds complication to driving multiple ground referenced IGBTs due to finite ground circuit impedance. Substantial voltages may develop across the ground impedance during switching, requiring level shift or isolation circuitry at the command signal to allow Kelvin drive circuit connections.

Bipolar Gate Driver

A Kelvin connected unipolar driver may often be adequate at lower switching speeds, however negative gate bias must be applied during the off-state to utilize the IGBT at higher rates. This becomes apparent when one considers that the gate to emitter threshold voltage drops to approximately 1.4 volts at high temperature. With high dv/dt at the collector , a very low and impractical drive

impedance is required to assure that the device remains off. By utilizing a negative turn-off bias, an adequate voltage margin is easily achieved, allowing the use of a more practical gate drive impedance. Fortunately most gate drivers have sufficient voltage capability to be used with bipolar

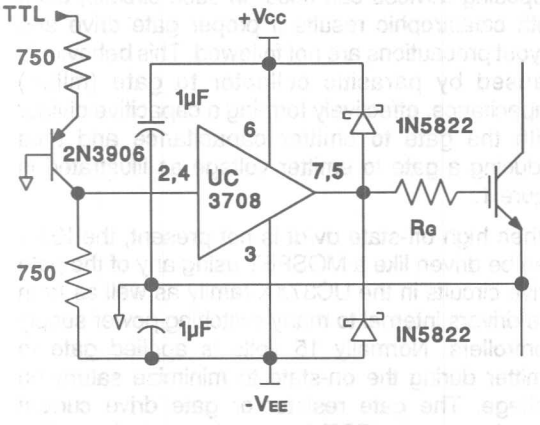


Figure 2. Bipolar IGBT gate drive using the U3708

power supplies. The UC3708 shown in figure 2 can deliver up to 6 amps peak with both output's paralleled, and is particularly suited to driving IGBTs. For added reliability during power sequencing, its output's "self bias", actively sinking current when insufficient supply voltage is present. The positive supply,+Vcc, is normally 15 to 16 volts and the negative supply, -VEE, typically ranges between -5 and -15 volts depending on circuit conditions. A PNP level shift circuit references the drive signal to ground. Opto-couplers are also commonly employed, and may be interfaced directly to the gate driver by referencing the signal to the negative supply. Note that this is a very demanding application for optocouplers, and only devices rated for high CMRR should be used.

Isolated Gate Driver

A bipolar IGBT gate driver with over-current protection can be implemented using the UC3724/UC3725 isolated gate driver pair as shown in figure 3. The UC3724/UC3725 transmits both power and signal across a small pulse transformer, thereby achieving low cost, high voltage isolation. An additional transformer winding develops a negative voltage, providing a bipolar supply for the UC3708. The UC3724/UC3725 can also be used for circuits which do not require negative turn-off bias by simply eliminating the negative supply and external driver, and using the UC3725 to drive the IGBT gate directly. Application note U-127 covers the UC3724/UC3725 in depth.

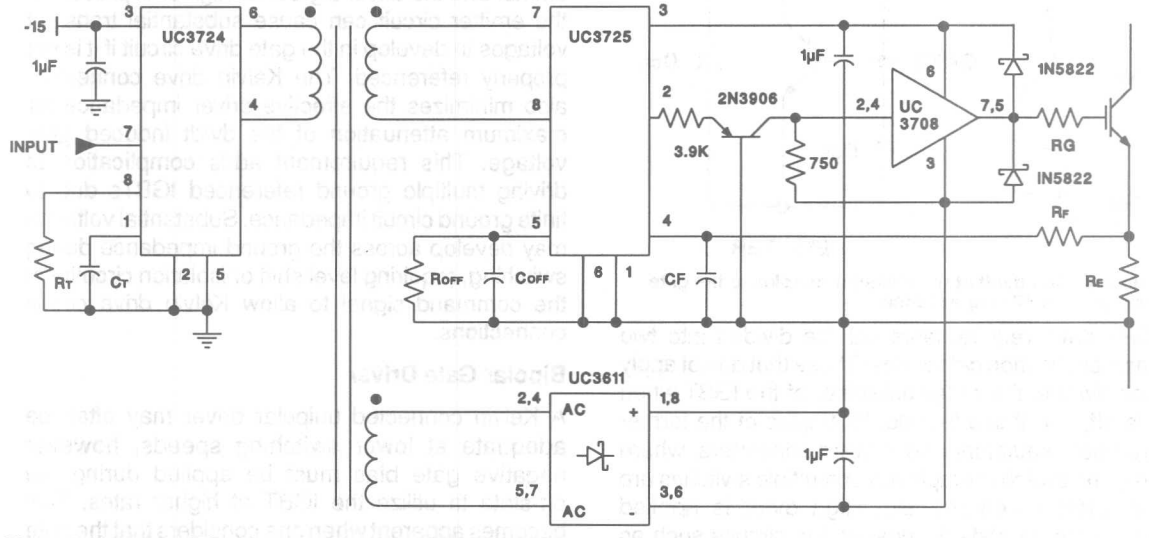


Figure 3. Power and signal are coupled to the UC3708 through the UC3724 / UC3725 Isolated Gate Driver Pair.

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UC1525B/UC1527B DEVICES
Comparison Summary to UC1525A/27A Devices

The UC1525B and UC1527B devices are enhanced versions of the previous generation of UC1525A and UC1527A devices. They are pin-for-pin compatible and direct replacements for the "A" versions in almost all applications. Significnt improvements have been made in the 5.1V reference voltage and the output drivers as itemized in the tables below.

PARAMETER	NEW: UC1515B/27B	OLD: UC1525A/27A
REFERENCE VOLTAGE		
V_{REF} (min)	5.062 V	5.05 V
V_{REF} (max)	5.138 V	5.15 V
Line Regulation (max)	+/-10 mV	+/-20 mV
Load Regulation (max)	+/-15 mV	+/-50 mV
Temperature Stability (max)	+/-30 mV	+/-50 mV
Total Output Variation (max)	5.036 V to 5.164 V	5.00 V to 5.20V
Long Term Stability (max)	+/-10 mV	+/-50 mV
Temperature Coefficient (typ)	8 ppm/deg. C	
PWM OUTPUT SECTION		
Minimum On-Time (typ)	350 nS	600 nS
Cross Conduction	30 nC	150 nC
SUPPLY CURRENT		
ICC Increase (40 kHz to 400 kHz)	15 mA (max)	40 mA (typ)
ESD PROTECTION		
Discharge Withstand Voltage (typ)	2 kV (typ all pins)	no protection

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UNIQUE "CHEAP AND DIRTY" CONVERTER FOR LOW POWER BIAS SUPPLIES

Bill Andreycak

Regulated output voltage is obtained - regardless of input voltage

Most power supply designs use PWM controller ICs and MOSFET switches which require 10 to 15 volt bias supplies for proper operation. A common application problem is to first generate an auxiliary supply within this range. Although simple in many applications, developing this supply with a variable low voltage input can be challenging especially when the input amplitude goes both below and above the desired output voltage. The circuit shown below is a unique, inexpensive solution to this problem.

Basically, the topology is a two transistor flyback (buck-boost) converter which provides a noninverting output polarity. By varying the duty cycle, the output voltage can be either higher or lower than the input amplitude. This attribute makes this approach ideally suited for many widerange input or automotive applications. Likewise, this technique is equally applicable to power factor correction applications. Additionally, the inductor can be operated in either the continuous or discontinuous current modes.

BUCK-BOOST CONVERTER (2 XTOR)

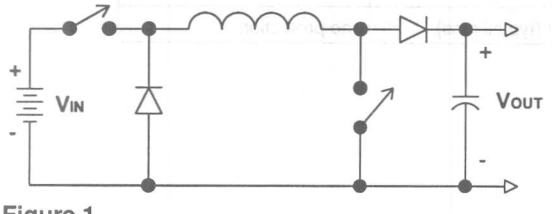


Figure 1.

Implementation of this technique will require a "high side" switch connected to the input voltage (VIN) and a low side switch to ground. Both of these are activated together, placing the inductor across the input supply while the switches are on. At turn off, the inductor is placed across the output capacitor and the two diodes conduct until the current reaches zero (discontinuous mode) or the next switching cycle is initiated (continuous mode). Inductor voltage and current waveforms are shown at maximum duty cycle for clarity.

INDUCTOR VOLTAGE AND CURRENT

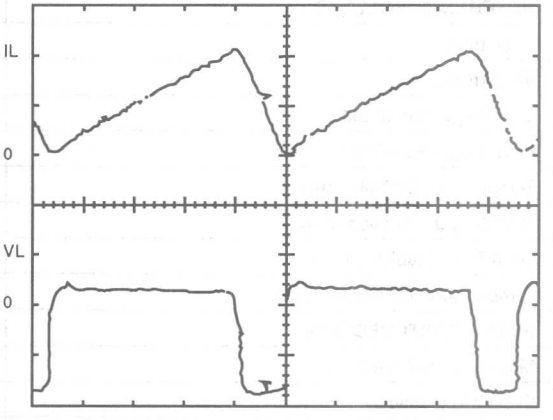


Figure 2.

At first, most PWM controllers may seem to be likely candidates for implementation of this technique. However, only one PWM features the ability to simultaneously switch both outputs together. The UC494A provides this operational mode by grounding its output control (O/C) input. Also limiting the IC selection is the fact that one IC output must go high and the other low each cycle. This is accomplished by connecting each of the UC494A's output collectors and emitters as required.

Switching at 200kHz in this application, the UC494A is programmed by a 9.1 K timing resistor (RT) and 470 pF capacitor (CT). High frequency conversion facilitates the use of a small (surface mount) inductor and output storage capacitor. Output voltage is regulated by using the ICs "A" amplifier as the voltage error amplifier. The 15 volt output is divided

down to 5 volts across the 15 K ohm resistor at pin 1 and compared to the reference voltage at pin 14. The 30K ohm resistor to Vout can be changed to provide different output voltages if required. Amplifier "B" is not used, but can be configured to provide overcurrent or overvoltage protection if desired. Schottky (1N5820) diodes are used in the power stage to maximize efficiency. Standard silicon diodes can be substituted in cost sensitive applications with some performance degradation. Efficiency for the 400 mW converter shown in figure 3 is approximately 50% for inputs between 7 and 16 volts and decreases slightly at higher and lower inputs. Consult Unitrode Design Note DN-37 for further information about 5 volt PWM operation.

BUCK BOOST CONVERTER USING THE UC 494A PWM CONTROLLER

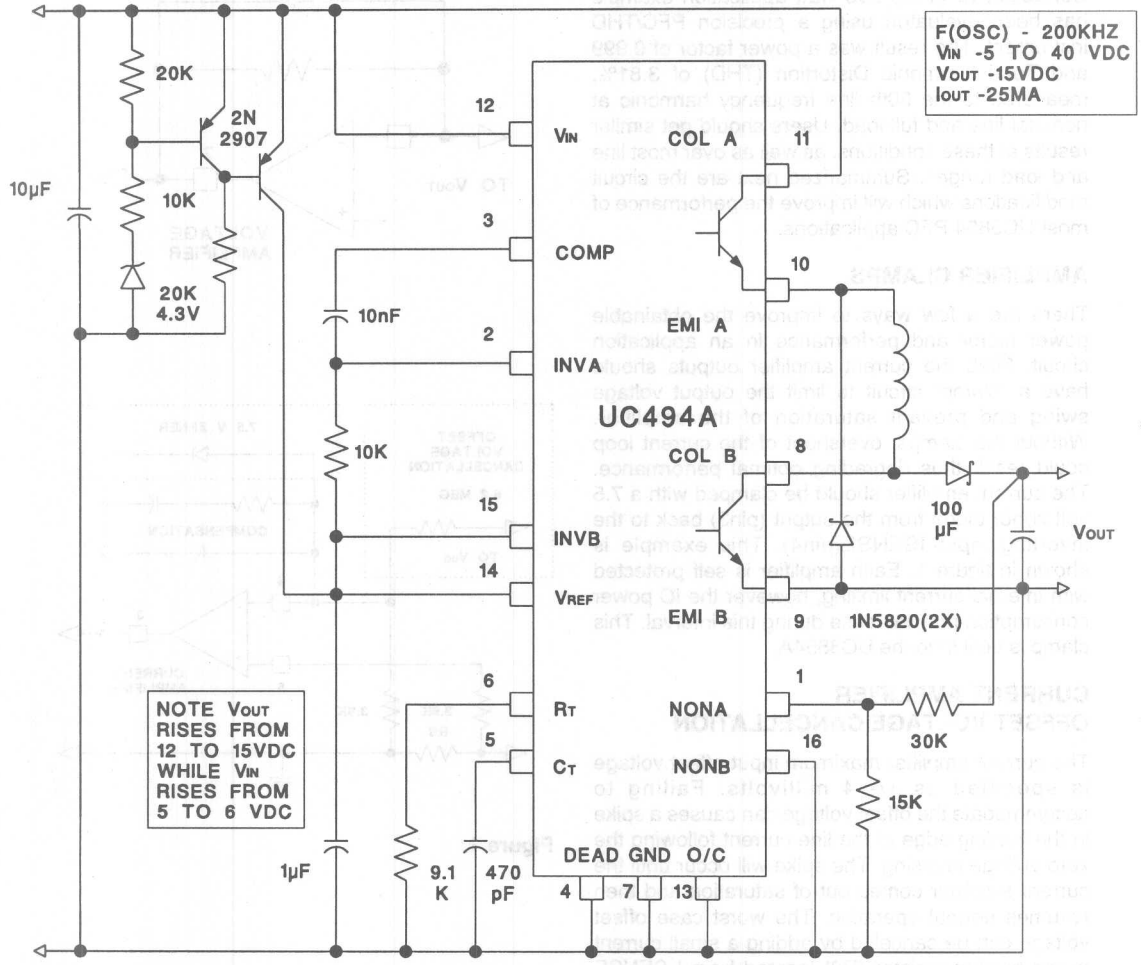


Figure 3.

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Design Note

OPTIMIZING PERFORMANCE IN UC3854 POWER FACTOR CORRECTION APPLICATIONS

by Bill Andreycak

The performance of the UC3854 Power Factor Correction IC in the 250 watt application example has been evaluated using a precision PFC/THD instrument. The result was a power factor of 0.999 and Total Harmonic Distortion (THD) of 3.81%, measured to the 50th line frequency harmonic at nominal line and full load. Users should get similar results at these conditions. as well as over most line and load ranges. Summarized next are the circuit modifications which will improve the performance of most UC3854 PFC applications.

AMPLIFIER CLAMPS

There are a few ways to improve the obtainable power factor and performance in an application circuit. First, the current amplifier outputs should have a "clamp" circuit to limit the output voltage swing and prevent saturation of the amplifier. Without the clamps, overshoot of the current loop could result thus degrading optimal performance. The current amplifier should be clamped with a 7.5 volt zener diode from the output (pin3) back to the inverting input ISENSE(pin4). This example is shown in figure 1. Each amplifier is self protected with internal current limiting, however the IC power consumption may increase during this interval. This clamp is built in to the UC3854A.

CURRENT AMPLIFIER OFFSET VOLTAGE CANCELLATION

The current amplifier maximum input offset voltage is specified as +/- 4 millivolts. Failing to accommodate the offset voltage can causes a spike in the leading edge of the line current following the zero voltage crossing. The spike will occur until the current amplifier comes out of saturation and then resumes normal operation. The worst case offset voltage can be canceled by adding a small current to the biasing resistor (R3) located from I SENSE (pin 4) to ground. This cancellation current (1.1µA), when multiplied by the bias resistor value (3.9K) should be designed to provide the four millivolt offset.

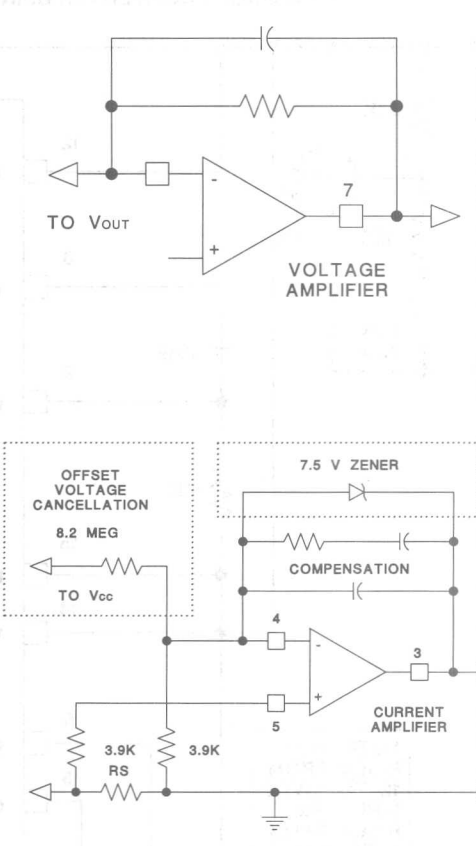


Figure 1.

This offset cancellation current should be obtained from the UC3854 supply voltage. Although a constant current source is optimal, a resistor from

Vcc to the I SENSE input will provide acceptable results as shown also in figure 1. An 8.2 megohm resistor will develop a 1.1 microamp current into the 3.9 K ohm resistor used in the design example. This will generate a 4.28 millivolt offset at the worst case of operation where Vcc is 9 volts. It is adviseable to generate this bias from Vcc and not the UC3854 reference which is inactive until the undervoltage lockout threshold is reached. Bias cancellation circuits from the reference could cause the current amplifier to saturate before the devices crosses its UVLO turn-on threshold. This condition will increase the start-up current of the UC3854 above its 2 milliamp specification and may prevent start-up in certain off-line applications.

CURRENT SENSE AMPLITUDE

The current sense signal should be made as high as possible, and a one volt full scale signal is recommended. Since resistive sensing can cause high power loss many users elect to generate only 100 to 200 millivolts at full load. In comparison, ground noise and slight amplifier offset voltages represent a higher percentage of the total current sense signal. Best results are obtained with the one volt (max) input and lower performance could be incurred with lower current sense signals. especially at light loads and high line voltages. Alternatives to resistive current sense are given below .

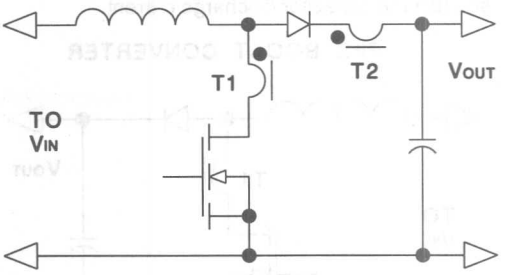
CURRENT SENSE TECHNIQUES

An optional technique to resistive current sensing should be considered to reduce power loss in the current sense circuitry. Two current sense transformers can be installed to sum both the switch and diode currents which will recreate the actual inductor current as shown in figure 2. These transformers must be designed to operate over the full range of duty cycles for the PFC converter design which approaches 100% as the line voltages nears zero.

Another current sensing option is to use a DC current sense module or transformer which is typically Hall Effect based. Two application concerns are the cost and accuracy of this technique which may limit its usage to only specialized applications.

A single current sense transformer in series with the PFC switch can also be used. This technique will require some additional circuitry to accurately reconstruct the primary current signal as shown in

PFC BOOST CONVERTER



TRANSFORMER COUPLED CURRENT SENSE

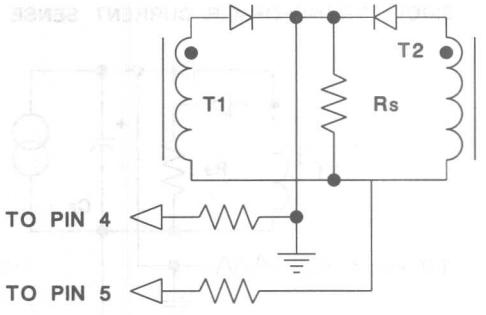


Figure 2.

figure 3. Generating the inductor current signal while the switch is on is a simple task. The difficulty is in reconstructing the inductor current while the switch is off while no current is flowing in the current sense transformer.

Inductor current sensing can be simplified to use only one current sense transformer and a current sink circuit. The current sense signal is developed across resistor RI through diode DI while the switch is on. A second diode to the current sense transformer develops an identical voltage across capacitor CI as determined by the current sense resistor primary current and turns ratio. When the PFC switch turns off capacitor CI maintains the peak amplitude of the previous current sense signal. Charge is removed by an ideal current sink circuit which lowers the capacitor voltage linearly during one switching cycle. The current is scaled to discharge at the rate proportional to Vout minus Vin(t) divided by the

inductor value, L. The input voltage (Vin) is constantly varying throughout the AC line cycle and so must the capacitor discharge current.

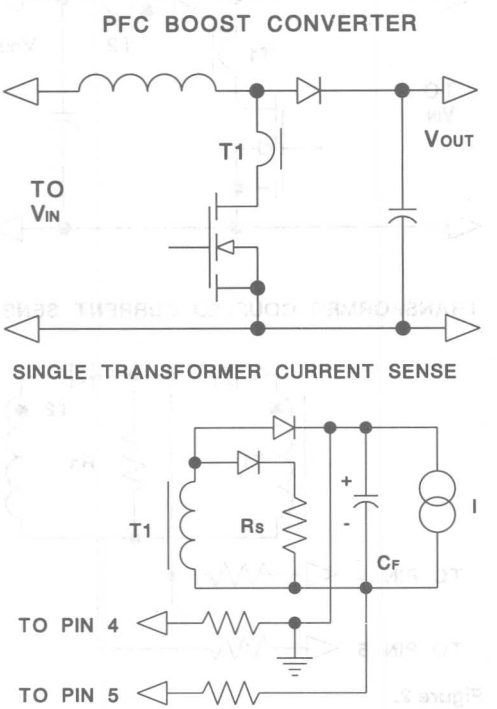


Figure 3.

The circuitry shown in figure 4 will modulate the current sink inversely with the instantaneous line voltage. This will result in the correct discharge of capacitor C1 to reconstruct the actual inductor current. Polarity has been optimized for use with the UC3854 which requires a current sense signal below the ground reference. Another option is to develop a few volts of current sense signal to improve noise immunity and resistively divide this down to the one volt maximum input to the UC3854 controller.

Transistors QI through Q4 should be identical for best results. Transistors QI and Q3 are for temperature compensation of the base emitter junctions of Q2 and Q3. Emitter ballasting (50 to 100 mV) will also improve performance. The emitter currents of QI and Q2 should be similar and equal to Vin/Rin. This current is diverted away from the bases of Q3 and Q4 which limits the total range of sink current to the current sense filter capacitor, CFILT.

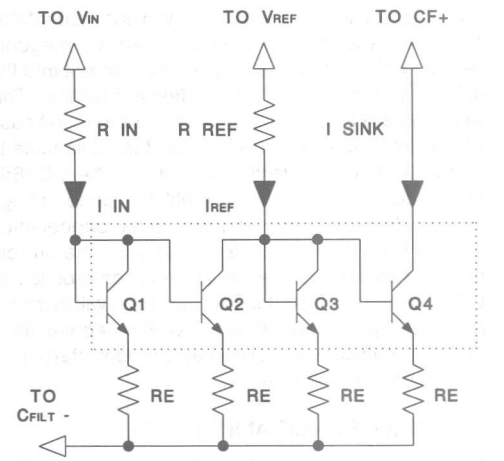
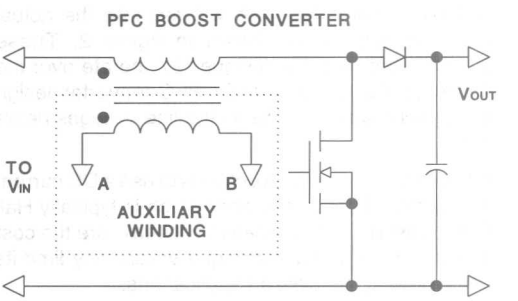


Figure 4.

SCHOTTKY PROTECTION DIODES

Each pin of the UC3854 must be protected from negative voltages exceeding minus three hundred millivolts (-0.3V) maximum. In most applications, only three pins of the IC need external protection Schottky diodes. The gate drive output (pin 16) requires a 1N5820 3 amp Schottky diode to protect against parasitic inductive effects with high speed switching. The multiplier output (pin 5) and peak current limit (pin 2) need Schottky diode protection during abnormal overcurrent conditions and during the initial inrush currents upon power-up. A 1N5817 Schottky diode will provide adequate clamping since the currents are low due to series resistors to the current sense circuitry.



REGULATED AUXILIARY SUPPLY

A secondary winding on the PFC boost inductor can be used to deliver a regulated auxiliary bias supply with few external components as shown in figure 5. Unlike more conventional and unregulated single

REGULATED AUXILIARY BIAS

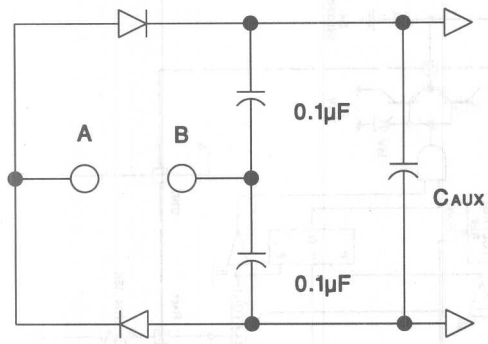


Figure 5.

diode or bridge rectifier techniques, this approach uses two diodes in a full wave configuration.

This arrangement develops two separate voltages across capacitors C1 and C2 each with 120 Hz components. However, when these two are summed at capacitor C3, the line variations are canceled, and a regulated auxiliary bias is obtained. The number of turns on the secondary winding will adjust the bias supply voltage. Additional windings on the boost inductor with similar rectification and filter circuitry can be used to deliver other semi-regulated isolated outputs.

UC 3854 POWER FACTOR CORRECTION EVALUATION KIT

LIST OF COMPONENTS

CAPACITORS (25 VDC)

C1 = 0.47 µF/250 VAC
C2 = 450 µF/450 VDC
C3 = 270 pF
C4 = 1 µF
C5 = NOT USED
C6 = 47 nF
C7 = 0.47 µF
C8 = NOT USED
C9 = 100 mF
C10 = 10 nF
C11 = 1 nF
C12 = 0.1 µF
C13 = 62 pF
C14 = NOT USED
C15 = 620 pF
C16 = 1 µF

DIODES

D1 =4 AMP/800VDC BRIDGE
D2 = UHVP806 FAST RECOVERY
D3 = 18 V ZENER
D4 = 1N5821 SCHOTTKY 3A
D5 = 1N4148
D6 = 1 AMP/100V BRIDGE
D7 = 1N5817 Schottky
D8 = 1N5817 Schottky

FUSE

F1 - 6A/250VAC FUSE

INDUCTOR

L1 = 1 milliHenry Inductor

TRANSISTORS

Q1 = 500V/0.25 ohm NMOS FET
Q2 = 450V/0.5A NPN
Q3 = 50V/.5A NMOS FET

RESISTORS (1/2 WATT)

R1 - 0.25 ohm/5 WATT
R2 = 3.9 K
R3 = 3.9 K
R4 = 1.6 K
R5 = 10 K
R6 = 24 K
R7 =240 K
R8 = 910 K (400V)
R9 = 91 K
R10 = 20 K
R11 = 220 K
R12 = 27 K
R13 = 75 K
R15 = ZERO ohm
R20 = 3 K
R21 = 24 K
R22 = 30 K/3W
R23 = 470 K
R24 = USER SPECIFIED
R25 = 910 K (400V)
R26 = NOT USED (OPEN)

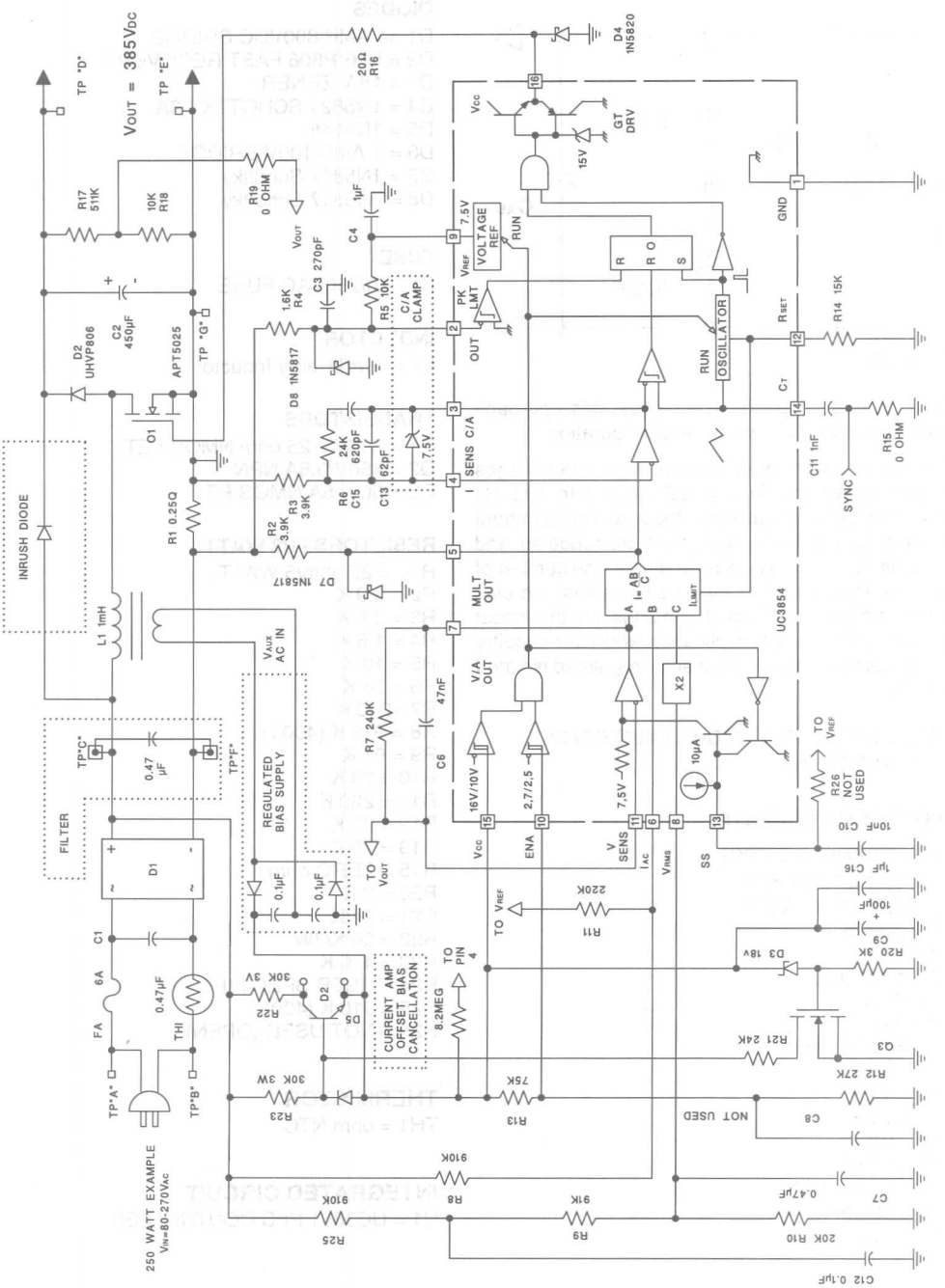
THERMISTOR

TH1 = ohm NTC

INTEGRATED CIRCUIT

U1 = UC3851 PFC CONTROLLER

UC3854 Evaluation PC Board Schematic
250 Watt Power Factor Correction Application



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Design Note

THE EFFECTS OF OSCILLATOR DISCHARGE CURRENT VARIATIONS ON MAXIMUM DUTY CYCLE AND FREQUENCY IN UC3842 AND UC3842–"A" PWM ICs

by YEAM CHONG HOCK

Many designers try to program a precise maximum duty cycle and operating frequency by careful selection of the oscillator timing components, Rt and Ct. Because of the variations in oscillator discharge current, very accurate programming is not easily obtainable. However, it is possible with ICs which contain a "trimmed" discharge current which has specified limits. This Design Note will detail programming frequency and maximum duty cycle with both types of oscillators. Simplified equations will be used to develop obtainable ranges for these parameters over IC tolerances.

ON-TIME

Maximum on-time directly corresponds to the maximum charging time of the timing capacitor. Charging time (TC) is determined by the timing capacitor value (Ct), the charging current (IRt) and the voltage amplitude between the upper and lower oscillator thresholds.

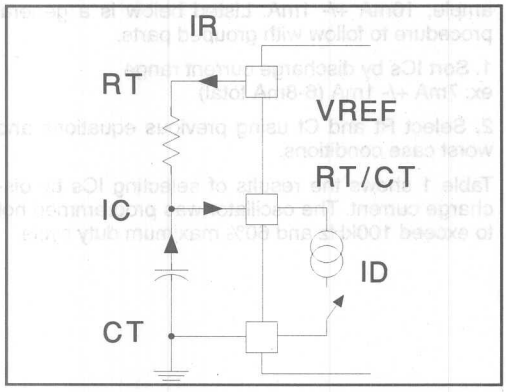


Figure 1: Basic UC3842 Oscillator Circuit

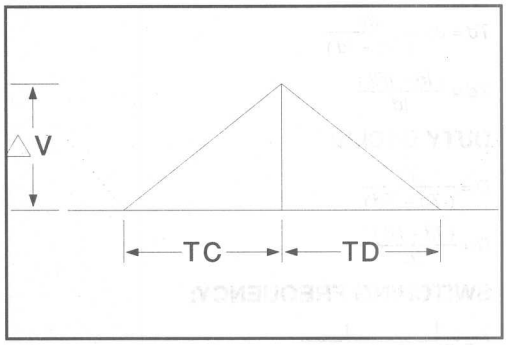


Figure 2: Timing Waveforms and Design Equations

OFF-TIME (DEADTIME)

The off-time occurs while the timing capacitor is discharged from the oscillator upper threshold to its lower threshold. The discharge current actually sinks two currents to ground. One current is flowing from the discharging timing capacitor. Another current flows from the timing resistor (Rt) pulling to Vref. Therefore, the effective timing capacitor discharge current (ICt) is the ICs discharge current (Id) minus the timing resistor charging current (IRt). Maximum duty cycle and switching frequency can

be controlled by accurately setting the ratio of these currents and capacitor value. The related equations are listed below.

CHARGING:

$$ICt = C \times \frac{dV}{Tc} ICt = C \times dV / Tc$$

$$ICt = \frac{5V}{Rt} (approximation)$$

$$TC = c \times \frac{dV}{IRt}$$

DISCHARGING:

$$ICt = Id - IRt$$

$$Td = c \times \frac{dv}{(IRt - Id)}$$

$$Td = \frac{(Id - IRt)}{Id}$$

DUTY CYCLE:

$$D = \frac{Tc}{(Tc + Td)}$$

$$D = \frac{(Id - Rt)}{Id}$$

SWITCHING FREQUENCY:

$$F = \frac{1}{Tper} = \frac{1}{(Tc + Td)}$$

$$F = \frac{(Id - IRt)}{(Id \times Tc)}$$

EXAMPLE 1:

This example will calculate the potential variations in maximum duty cycle and frequency using a standard UC3842 device. A ten milliamp internal discharge current (Id = 10mA) will be used for initial programming. The worst case limits of 6 and 14 milliamp discharge currents will be used to analyze the possible variations. A target of 100kHz at 60% duty cycle will be used.

$Id = 10mA\ (typical)$

$Id\ (\min) = 6mA,\ Id\ (\max) = 14mA$

$F\ (typ) = 100kHz$

$D = 0.60\ (60\%)$

Based on the 10mA discharging current and the equations previously mentioned;

$IRt = 4mA$, and $Tc = 6us$

Using the same Rt and Ct values with a discharge current of 6mA results in:

$Dmax = 0.33\ (30\%)$

$F = 55kHz$

When the highest discharge current of 14mA is used, the results are:

$Dmax = 0.71\ (71\%)$

$F = 118kHz$

Therefore, the total possible range due to discharge current variations in maximum duty cycle and frequency is:

$Dmax = 33\ 71\ percent$

$Frequency = 55\ 118kHz$

In most applications this range is far too wide to use in a high volume production environment. One technique to minimize the effects of the discharge current is to have the ICs sorted into different groups. Each group can have a tight distribution or tolerance and will use a specific timing resistor and capacitor to achieve the desired frequency and duty cycle. Each other group will also need a specific Rt and Ct for that group. Keeping these groups separated can create problems in some production situations. One alternative is to have the ICs measured and "binned" at the factory. Another way is to use only ICs within one distribution group, for example, 10mA +/- 1mA. Listed below is a general procedure to follow with grouped parts.

1. Sort ICs by discharge current range
ex: 7mA +/- 1mA (6-8mA total)

2. Select Rt and Ct using previous equations and worst case conditions.

Table 1 shows the results of selecting ICs by discharge current. The oscillator was programmed not to exceed 100kHz and 60% maximum duty cycle.

I Discharge (+/- 1mA)	Rt (k)	Ct (nF)	Minimum Duty%	Maximum Duty%	Minimum Freq (kHz)	Maximum Freq (kHz)
7mA	1.56	11.3	47	60	77.8	100
9mA	1.25	14.1	50	60	83.3	100
11mA	1.04	16.9	52	60	86.7	100

TRIMMED DISCHARGE CURRENT:

Very repeatable and predictable high volume production can be rescued from these variations by using the right IC, one with a trimmed discharge current. The UC3842A, UC3843A, UC3844A and UC3845A devices have an internal factory trimmed discharge current with a tight distribution. This is set at 8.3mA typically, and can only vary between a low of 7.5mA and a high of 8.8mA. Programming these ICs for a 50% maximum duty cycle and 100kHz switching frequency will result in worst case variations of:

$D(\min) = 56\%$

$D(\max) = 62\%$

$F(\min) = 92.9kHz$

$F(\max) = 103.8kHz$

This is a significant improvement over the non "A: version devices. The accuracy of these ICs will improve when these ICs are used at wider maximum duty cycles, for example 65 to 85 percent. The UC3844A and UC3845A are intended for 50% maximum duty cycle applications and contain a flip flop to insure that 50% D(max) is never exceeded. The UC3842A and UC3843A have maximum duty cycles near 100% and can be adjusted lower using the appropriate Rt and Ct components.

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Design Note

EXTEND CURRENT TRANSFORMER RANGE

by PHILIP C. TODD

Transformers are used extensively for current sensing because they can monitor currents with very low power loss and they have wide bandwidth for good waveform fidelity. Current transformers perform well in applications with symmetrical AC currents such as push-pull or full bridge converter topologies. In single-ended applications, especially boost converters, problems can arise because of the need to accurately reproduce high duty factor, unipolar, waveforms. Unipolar pulses may saturate the current transformer and, if this happens, over current protection will be lost and, for current mode control, regulation will be lost and an over voltage condition will result.

The transformer core must be reset after each pulse so that the full range of the transformer will be available for the next pulse. Self reset of the current transformer is the most common techniques used but it has drawbacks. Self reset uses the energy stored in the current transformer core for reset and depends on the open circuit impedance of the current transformer to generate enough volt-seconds in a short period of time for reset. Current transformers operated above a 50% duty factor may not have enough stored energy to allow complete reset in the time available and this situation becomes worse as the duty factor approaches 100%.

The magnetizing inductance of the current transformer must be kept high because this determines the amount of droop the current waveform will exhibit over the pulse period. The higher the inductance the lower the droop will be. The waveform droop opposes slope compensation and should be kept to a minimum. High magnetizing inductance also means that the core stores very little energy which can be used to reset the core.

The current transformer turns ratio generally needs to be high to lower the power loss. The more turns put on the core, however, the greater the leakage inductance and the greater the parallel capacitance. The leakage inductance by itself is generally not a problem but it will limit the current rise and fall times. The parallel capacitance also limits the bandwidth of the current transformer but it is a greater problem during transformer reset. For the transformer to reset properly, all of the energy stored in the core must be removed. In self reset this energy must transfer from the magnetizing inductance to the parallel capacitance in a resonant manner. If the capacitance is too large, the resonant frequency will be too low and the magnetizing inductance will not be reset before the next pulse begins.

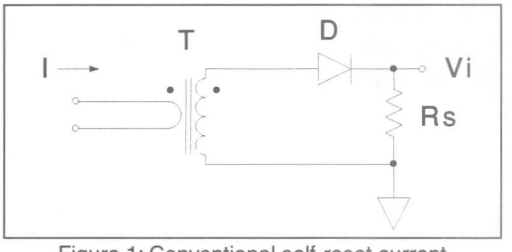


Figure 1: Conventional self-reset current transformer

Figure 1 shows a conventional current transformer circuit which uses self reset. The current I flowing in the primary, causes a current to flow through D and Rs to generate an output voltage proportional to Vc=IRs/N where N is the current transformer turns ratio. The problems discussed above occur during the reset interval when I=O. The core of T may not have enough energy to fully reset itself in the time available given the secondary capacitance of T plus the capacitance of D.

The problems with self reset of current transformers for unipolar pulse applications can be overcome with simple forced reset techniques derived from magnetic amplifiers. Duty factors above 90% are achievable with these techniques.

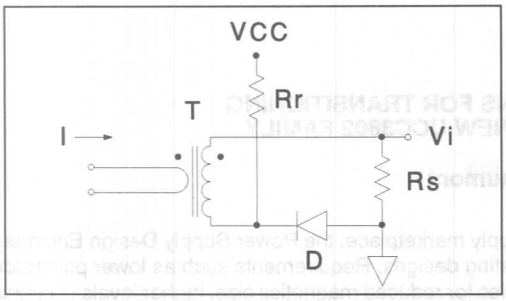


Figure 2: Current transformer with forced reset

Figure 2. shows the same circuit as Figure 1 configured for forced reset. The diode D has been moved from the high side of the transformer secondary winding to the ground side. This, of course, has no effect on the operation of the circuit and during the pulse this circuit behaves exactly as expected. During reset, however, Rr makes the circuit operation quite a bit different.

A current from Vcc through Rr can be much greater than the self reset current available from the magnetizing current of the transformer. This forcing current rapidly charges the parasitic capacitances and reverses the voltage on the secondary of the transformer. The applied volt-seconds can quickly reset the core so that high duty-factor operation is possible.

The forced reset may be high enough to drive the current transformer into saturation and this is an acceptable practice because the core will be saturated in the opposite direction (i.e. full reset) from the current pulse to be measured. This can be beneficial in some applications as it doubles the number of volt-seconds available from the transformer.

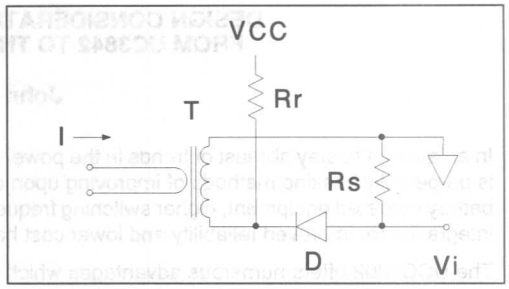


Figure 3: Negative output current sense

In some applications it may be desirable to generate a negative voltage from the current transformer. This can be accomplished without a negative voltage source to reset the transformer. Figure 3 shows the configuration. In this circuit there will be an error because the reset current subtracts from the sense current in Rs during the pulse. Care must be taken to minimize this effect.

There are other circuit configurations which are possible to force reset of the current transformer. Switches may be used to switch the reset current on and off. Additional windings or center tapped windings may be used also. Many circuits are possible and may provide a specific improvement at the expense of complexity. The circuits shown here are the simplest available and illustrate the basic concept.

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DESIGN CONSIDERATIONS FOR TRANSITIONING FROM UC3842 TO THE NEW UCC3802 FAMILY

John Gaumont

In an attempt to stay abreast of trends in the power supply marketplace, the Power Supply Design Engineer is perpetually seeking methods of improving upon existing designs. Requirements such as lower power for battery operated equipment, higher switching frequencies for reduced magnetics size, higher levels of circuit integration for improved reliability and lower cost have become necessities for survival.

The UCC3802 offers numerous advantages which allow the Power Supply Design Engineer to meet these challenging requirements. Features include:

- BI-CMOS Process
- Low Starting Supply Current: typically 100µA
- Low Operating Supply Current: typically 500µA
- Pin out Compatible with UC3842 and UC3842A families
- 5 Volt Operation (UCC3803, UCC3805)
- Leading Edge Blanking of Current Sense Signal
- On-Chip Soft Start
- Internal Full Cycle Restart Delay
- 1% Voltage Reference
- Up to 1 MHz Oscillator
- Self-Biasing Output Low During UVLO
- Very Few External Components Required
- 70ns Response from Current Sense to Output
- Available in Surface Mount or DIP Package

The UCC3802 family of devices are pin out compatible with the UC3842 and UC3842A families however, they are **NOT PLUG-IN COMPATIBLE**. In general, the UCC3802 requires fewer external components and consumes less operating current. The following UCC3802 family attributes should be considered **BEFORE** inserting the device into a UC3842/42A family socket:

1. Maximum supply voltage
2. Turn-on and Turn-off thresholds
3. Oscillator Rt, Ct values
4. Schottky diodes may not be required on output
5. No current sense filter required
6. No soft start circuitry required
7. Auxiliary power (bootstrap winding) may not be required

Detailed Pin By Pin Description

PIN 1 COMP--The UCC3802 has a true low output impedance error amplifier which both sources and sinks current. The error amplifier associated with the UC3842 family is an open collector in parallel with a current source. The UCC3802 has power-up soft start and fault soft start built on-chip with a fixed COMP rise time to 5V in 5ms. Therefore, **NO EXTERNAL SOFT START CIRCUITRY IS REQUIRED** saving 1 resistor, 1 capacitor, and 1 PNP transistor.

PIN 2 FB--The UCC3802 features a 2 MHz bandwidth error amplifier versus 1 MHz on the UC3842. Feedback techniques are identical to the UC3842 family. Stray capacitance on FB should be kept as small as possible, and the lead length as short as possible to achieve best stability.

PIN 3 CS--The UCC3802 current sense is significantly different from its predecessor. The UC3842 current sense input connects to only the PWM comparator. The UCC3802 Current Sense input connects to two comparators; the PWM comparator and the over-current comparator. Internal leading edge blanking masks the first 100ns of the current sense signal. This **MAY ELIMINATE THE NEED FOR AN RC CURRENT SENSE FILTER AND PREVENT FALSE TRIGGERING** due to leading edge noise. Connect CS directly to MOSFET source current sense resistor. The gain of the current sense amplifier on the UCC3802 family is typically 1.65 V/V versus typically 3 V/V with the UC3842 family.

PIN 4 RC--The UCC3802's oscillator allows for operation to 1 MHz versus 500KHz with the UC3842. Both devices make use of an external resistor to set the charging current for the capacitor which determines the oscillator frequency. For the UCC3802 and UCC3804

$$F_{Hz} = \frac{1.5}{R_{OHMS} \bullet C_F}$$

For the UCC3803 and UCC3805

$$F_{Hz} = \frac{1.0}{R_{OHMS} \bullet C_F}$$

The two equations are different due to different reference voltages. The recommended range of timing resistor values is between 10K and 200K; the recommended range of timing capacitor values is between 100pF and 1000pF. The peak to peak amplitude of the oscillator waveform is 2.45 Volts versus 1.7 Volts. For best performance, keep the timing capacitor lead to GND as short as possible. Separate ground traces for the timing capacitor and all other pins are recommended. The maximum duty cycle for the UCC3802/03 is approximately 99%; the maximum duty cycle for the UCC3803/04 is approximately 49%. The duty cycle **CANNOT** be easily modified by adjusting RT and CT, unlike the UC3842A family. The maximum duty cycle limit is set by the ratio of the external oscillator charging resistor RT and the internal oscillator discharge transistor on-resistance, like the UC3842. However, maximum duty cycle limits less than 90% for the UCC3802/03 and less than 45% for the UCC3804/05 can not reliably be set in this manner. For better control of maximum duty cycle, consider using the UCC3807.

PIN 5 GND--Both devices same.

PIN 6 OUT--The output of the UCC3802 is a CMOS output versus a Bipolar output on the UC3842. Peak output current remains the same +/- 1 Amp. The CMOS output provides very smooth rising and falling waveforms, with virtually no overshoot or undershoot. Additionally, the CMOS output provides a low resistance to the supply in response to overshoot, and a low resistance to ground in response to undershoot. Because of this, **SCHOTTKY DIODES MAY NOT BE NECESSARY** on the output. Furthermore, the UCC3802 has a self-biasing, active low output during UVLO. This feature **ELIMINATES THE GATE TO SOURCE**

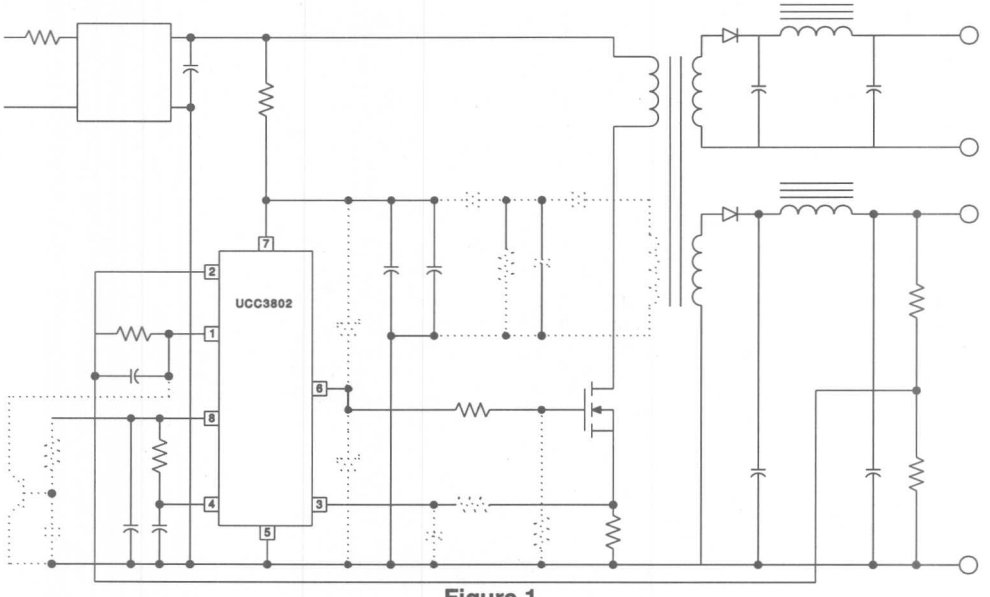


Figure 1

Figure 1 illustrates a nonisolated off-line flyback. Dotted components may be eliminated using the UCC3802 family.

"BLEEDER" RESISTOR associated with the MOSFET gate drive. Finally, **NO MOSFET GATE VOLTAGE CLAMP** is necessary with the UCC3802 as the on-chip zener diode automatically clamps the output to VCC.

PIN 7 VCC--The UCC3802 has a lower VCC (supply voltage) clamp of 13.5 Volts typical versus 30 Volts on the UC3842. For applications which require a higher VCC voltage, a resistor must be placed in series with VCC to increase the source impedance. The maximum value of this resistor

$$Rmax = \frac{VIN(min) - VCC(max)}{ICC + Qgate \bullet F}$$

Additionally, the UCC3802 has an on-chip zener diode to regulate VCC to 13.5 Volts. The turn-on and turn-off thresholds for the UCC3802 family are significantly different: 12.5V and 8V for the UCC3802 and UCC3804; 4.1 V and 3.6V for the UCC3803 and UCC3805. 5 Volt PWM operation is now possible. To ensure against noise related problems, filter VCC with an electrolytic and bypass with a ceramic capacitor to ground. Keep the capacitors close to the IC pins.

PIN 8 REF--The UCC3802 and UCC3804 have a 5 Volt reference. The UCC3803 and UCC3805 have a 4 Volt reference; both +/- 1% versus +/- 2% on the UC3842 family. The output short circuit current is lower...5mA versus 30mA. REF must be bypassed to ground with a ceramic capacitor to prevent oscillation and noise problems. REF can be used as a logic output; as when VCC is lower than the UVLO threshold, REF is held low.

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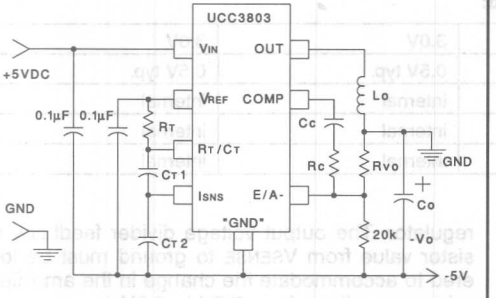
Simple Techniques to Generate a Negative Voltage Bias Supply from a Positive Input Voltage

by Bill Andreycak

Developing a low power negative supply voltage from a positive input supply can be accomplished using some very common PWM control ICs. Typical applications include generating a negative five through twelve volt (-5V to -12V) supply for analog function ICs (OP amps), RS-232 communication circuits, and MOSFET or IGBT gate drives at power levels below a few Watts.

Many PWM ICs contain a high current totem pole output which goes high during the device's ON-time or pulse width. The exact pulse width is modulated to regulate a converter's output voltage during changes in input voltage and output current. The IC's totem pole output can also be used as the main switch in low power applications. One example of this is a Flyback converter configured as shown in Figure 1.

Figure 1: Low Power Negative Output Voltage +5V to -5V Inverter



With this arrangement, the inductor (L) charges when the IC output is high and discharges or flies-back when the IC output goes low. Energy stored during the inductors charging time is transferred to the output capacitor (Cout) during the flyback, or OFF portion of the cycle. When a BiCMOS PWM control IC is used, the external diode can be replaced by the MOS channel and body diode of the IC's lower totem pole transistor thus saving one component. Reverse recovery characteristics are not a concern since current also flows through the MOS transistor channel in parallel with the body diode.

The circuit can be designed for either continuous or discontinuous inductor current operation, depending on the application. Discontinuous mode is generally preferred at lower power levels to minimize inductor size. Continuous inductor current operation is more applicable with higher load currents. High frequency switching and surface mount packaging options minimize overall size.

Conventional duty cycle control (voltage mode) is less complex to implement as the control technique than current mode control. The principal difficulty is sensing the inductor current which is not referenced to the IC's return connection, -Vout instead of ground. Adding a current sense transformer is possible, but will increase cost and complexity. Overcurrent protection is obtained by using the IC's internal maximum current limit at the switch.

Note that the BiCMOS UCC3803 device used in the example circuit of Figure 1. has a maximum low impedance input supply voltage rating of 12VDC. This limits it's applications to less than negative seven volts outputs (-7V max) with a +5V DC input. Higher voltage outputs, for example -12V to -15V, can be obtained by using a UC3843 with a higher maximum input voltage (30VDC). Here too there are some limitations. These fully bipolar ICs draw higher supply current and have higher undervoltage lockout (UVLO) thresholds, but are acceptable choices for some applications.

The IC datasheet should be referred to for additional information. Application Notes within the IC databook contain general information about the design of the Flyback converter, and others. For further assistance contact a Unitrode Field Application Engineer or the factory.

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Design Note

UC3854A and UC3854B Advanced Power Factor Correction Control ICs

by Bill Andreycak

The UC3854A and UC3854B Power Factor Correction (PFC) control ICs are advanced versions of the industry standard UC3854. The new devices are pin-for-pin compatible with the original version and feature numerous improvements. The UC3854A IC can be used in most existing UC3854 PFC designs with no modifications to the printed circuit board. New PFC preregulator designs and upgrades of existing ones can realize enhanced performance and reduced parts count with minimal design effort.

Specification Differences :

Parameter	UC3854	UC3854A	UC3854B
Supply Current, Off	2.0mA max.	400µA max.	400µA max.
Supply Voltage Vcc	35V max.	22V max.	22V max.
Vcc Turn-on threshold	16V typ.	16V typ.	10.5V typ.
Vcc UVLO hysteresis	6V typ.	6V typ.	0.5V typ.
Current Amplifier Bandwidth	1 MHz typ.	5 MHz typ.	5 MHz typ.
Current Amplifier offset	+4mV, -4mV max.	+0mV, -2mV max.	+0mV, -2mV max.
MULTOUT voltage (high)	2.5V typ.	5V typ.	5V typ.
Multiplier Gain tolerance	not specified	-0.9 to -1.1	-0.9 to -1.1
ENABLE propagation delay	not specified	300ns typ.	300ns typ.

Other Improvements and Changes - Non Specified:

VSENSE Input	7.5V	3.0V	3.0V
IAC voltage	6V typ.	0.5V typ.	0.5V typ.
Voltage Amplifier clamp	none	internal	internal
Current Amplifier clamp	none	internal	internal
VREF "good" circuitry	none	internal	internal

Application Information:

Converting an existing PFC design from the UC3854 to use the UC3854A or UC3854B device will eliminate five components from the control circuit. These are: one diode used to clamp the voltage amplifier output, a zener diode used to clamp the current amplifier output, one resistor to offset the bias current from the 6 volt amplitude of the IAC node, one resistor from Vcc to the current amplifier input to accommodate the worst case +4mV offset voltage, and a Schottky diode to clamp the overcurrent protection (PKLMT) input from going far below ground during power-up of the PFC preregulator. The output voltage divider feedback resistor value from VSENSE to ground must be lowered to accommodate the change in the amplifier's reference voltage from 7.5V to 3.0V. In most applications, existing production printed circuit boards do not have to be modified to take advantage of the newer devices. Locations used for the five components can remain on the boards but do not need to be populated.

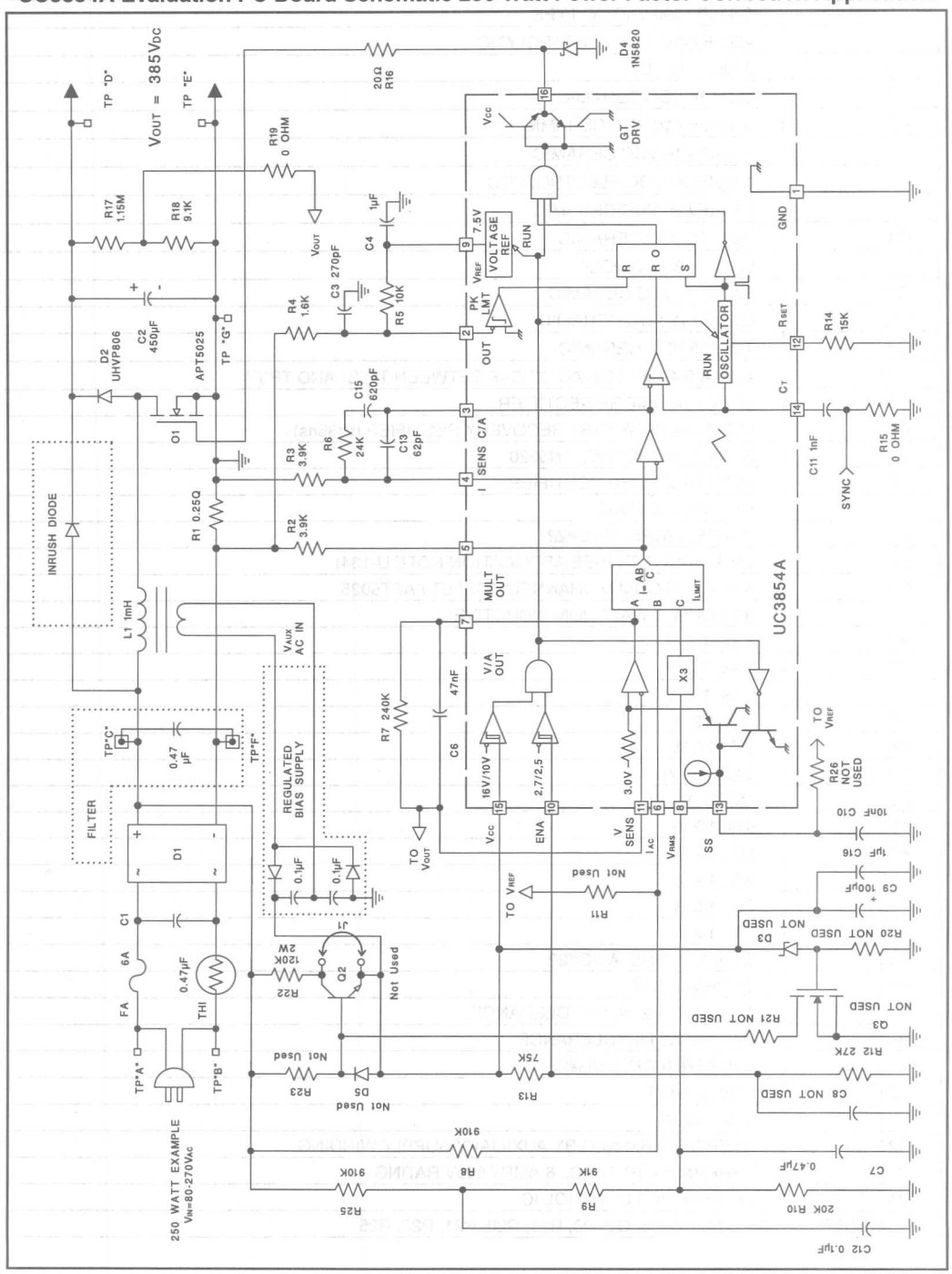
For further application information consult Unitrode Application Note U-134 and Design Note DN-39D, or contact a Field Applications Engineer.

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UC3854A EVALUATION BOARD LIST OF MATERIALS

C1	0.47µF / 300 VAC "X" TYPE
C2	450µF / 450 VDC ELECTROLYTIC
C3	270pF / 16 VDC
C4	1µF / 16 VDC CERAMIC
C6	0.047µF / 16 VDC CERAMIC
C7	0.47µF / 16 VDC CERAMIC
C9	100µF / 35 VDC ELECTROLYTIC
C10	0.01µF / 35 VDC CERAMIC
C11	1µF / 16 VDC CERAMIC
C12	0.1µF / 63 VDC POLY
C13	62pF / 16 VDC CERAMIC
C15	620pF / 16 VDC CERAMIC
C16	1µF / 35 VDC CERAMIC
C*	ADD A 0.47µF / 300VAC "X" CAP BETWEEN TP"C" AND TP"F"
D1	600 V / 6A BRIDGE RECTIFIER
D2	600 V / 8A VERY FAST RECOVERY RECTIFIER (trr35ns)
D4	20 V / 3A SCHOTTKY, 1N5820
D6	40 V / 1A BRIDGE RECTIFIER
F1	6A / 300 VAC FUSE
J1	JUMPER WIRE, AWG#22
L1	1mH INDUCTOR (SEE APPLICATION NOTE U-134)
Q1	500 V, 0.25 OHM N CHANNEL MOSFET / APT5025
R1	0.25 OHM, 5 WATT NON-INDUCTIVE
R2	3.9k, 1/2 W
R3	3.9k, 1/2 W
R4	1.6k, 1/2 W
R5	10k, 1/2 W
R6	24k, 1/2 W
R7	240k, 1/2 W
R8	1MEG, 1/2 W
R9	91k, 1/2 W
R10	20k, 1/2 W
R12	27k, 1/2 W
R13	75k, 1/2 W
R14	15k, 1/2 W
R15	JUMPER WIRE, AWG#22
R16	20 OHM, 1/2 W
R17	1.15 MEG, 1/2 W, 1% TOLERANCE
R18	9.1k, 1/2 W, 1% TOLERANCE
R19	JUMPER WIRE, AWG#22
R22	120k, 2 WATT
R23	910k, 1/2 W
R24	USER DETERMINED BY AUXILIARY SUPPLY WINDING
TH1	THRERMISTOR, N.T.C., 6 AMP / 500V RATING
U1	UC3854A PFC CONTROL IC
NOT USED : C5, C8, C14, D3, D5, Q2, Q3, R11, R20, R21, R23, R26	

UC3854A Evaluation PC Board Schematic 250 Watt Power Factor Correction Application



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Design Note

UC3846, UC3856 and UCC3806
Push Pull PWM Current Mode Control ICs

by Jack Palczynski

The UC3856 is a pin for pin compatible high performance bipolar version of the industry standard UC3846. It can replace the UC3846 with few circuit modifications and features increased speed, higher gate drive current and reduced propagation delays. The UCC3806 is a BiCMOS pin for pin compatible ultra low power version ideal for battery, low power and high speed applications. The UCC3806 may also replace the UC3846 with few circuit changes.

Specification Differences :

	UC3846	UC3856	UCC3806
Process	**40V Bipolar**	**40V Bipolar**	**18V BiCMOS**
General:			
Startup Current (max)	21mA	23mA	100µA
Operating Current	21mA	23mA	1.4mA
Output Section:			
Supply Vc (max)	40V	40V	15V
Drive Voltage Supply	40V (max)	40V (max)	18V (max)
Rise and Fall Time	300ns (max)	80ns (max)	65ns (max)
Peak Output Current	0.5A	1.5A	0.5A
Oscillator Section:			
Oscillator Discharge I	---------	6.7 to 8.8mA	2.2 to 2.9mA
Initial Accuracy	43kHz ±9.3%	200kHz ±15%	49kHz ±22%
Sync V_{OH} (min)	3.9V	2.4V	2.4V
Sync V_{OL} (max)	2.5V	0.4V	0.4V
Sync V_{IH} (min)	3.9V	2.0V	2.0V
Sync V_{IL} (max)	2.5V	0.8V	0.8V
Sync I_{INPUT} (max)	1.5mA	10µA	1µA
Sync I_{OUTPUT} (max)	-5mA	±10mA	±30mA
Error Amp Section:			
Input I_{OFFSET}(max)	250nA	500nA	500nA
Open Loop Gain	105dB (typ)	100dB (typ)	100dB (typ)
Unity Gain BW	1MHz (typ)	1.5MHz (typ)	3MHz (typ)
PSRR (typ)	105dB	100dB	100dB
Current Sense Amp Section:			
Input CM Range	0V to (V_{IN} - 3V)	0V to 3V	0V to (V_{IN} - 3.5V)
Shutdown Terminal Section:			
Threshold Voltage	0.35V (typ)	1V (typ)	1V (typ)
Input Voltage Range	0V to V_{IN}	0V to 5V	0V to V_{IN}
Delays:			
I_{SENSE} amp to Output	500ns (max)	250ns (max)	175ns (max)
Shutdown to Output	600ns (max)	110ns (max)	100ns (max)
Sync Delay to Output	300ns (typ)	50ns (typ)	50ns (typ)

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Applications Information:

When replacing the UC3846 with a **UC3856**, extra care must be taken to decouple VIN, VC and VREF with ceramic capacitors close to the leads of the IC. In applications where high output currents are seen, very fast rise and fall times can cause source ripple which can induce problems for PWM ICs which are not properly decoupled. Note also that the shutdown voltage changes from 350mV to 1V. Oscillator frequency is calculated differently, however similar mechanisms generate the oscillator frequency and dead times. As with any bipolar PWM IC, outputs should be protected from negatively biasing the substrate. This is typically done by using Schottky diodes from ground to each output. Failure to do this could cause spurious interruption and restart of the oscillator, dropping of output pulses and a significant increase in propagation delays. The input of the current sense amplifier is slew rate limited allowing lower values of filter capacitors to be used to eliminate leading edge noise. As with the UC3846, the UC3856 uses a differential current sense amplifier which can eliminate ground loop problems and increase noise immunity.

When replacing the UC3846 with the **UCC3806**,output Schottky diodes can be eliminated because the totem pole output is made of MOSFETs which may conduct current in either direction. As with any MOS device, higher impedances require proper decoupling with ceramic capacitors close to the IC. VIN, VC and VREF should all be properly decoupled. Note that the UCC3806 has a limiting regulator to limit VIN to 15V and the shunted current must be limited to 10mA. To determine oscillator frequency; a 1.25V source through RT (min 12.5k) creates a current which is mirrored to CT. This current charges CT from zero to 2.5V, at which point the outputs are turned off. Both outputs remain low while CT discharges to zero volts from a 2.6mA current sink. The Shutdown threshold voltage (pin 16) is 1V. The specific Shutdown mode is determined by a switched internal 190µA sink between pin 1 and ground, turned on when a shutdown is triggered. If the Shutdown voltage falls below 350mV, a restart is triggered. Otherwise, the oscillator remains latched off. As with the UC3856, the UCC3806 current sense amplifier is slew rate limited allowing less leading edge filtering to be used. This amplifier is also fully differential, eliminating ground loop problems associated with noisy environments. For additional information consult Application Note U-144 or contact a Unitrode Field Applications Engineer.

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Design Note

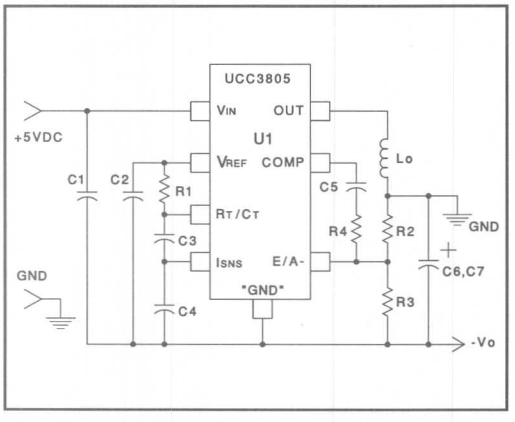
Highly Efficient Low Power DC to DC Inverter Converts +5V Input to -3V Output

* Achieves 73% Efficiency at 0.2 Watt

by Bill Andreycak

Operational Notes : The UCC3805 PWM control IC is used in this Flyback inverter application to perform three functions; control, switching and output rectification. During the PWM ON-time, the upper totem pole switch of the IC's output is turned on applying the 5 volt input across the inductor (Lo) which stores energy. The PWM output goes low when the correct duty cycle is achieved to regulate the output voltage, Vo. This turns off the upper totem pole switch and turns on the lower one, connecting the inductor to the output voltage (-3V) rail. The lower totem pole switch acts as a synchronous rectifier in parallel with the internal MOS body diode. This condition necessitates discontinuous inductor current operation at all times to avoid high cross-conduction currents in the IC output stage.

Circuit Schematic



The duty cycle is controlled using conventional voltage mode operation. The IC's oscillator timing waveform (R_T/C_T) is capacitively divided down to the appropriate amplitude (1V max) and fed into the ISNS pin. A regulated output is obtained by resistively dividing down the output to 2.0 volts above the IC's "ground" (which is at -3V) and input to the error amplifier's inverting input (E/A-). A 400kHz oscillator frequency results in 200kHz switchmode power conversion due to the IC's internal divide-by-two toggle flip-flop. This is done to limit the maximum duty cycle to below 50% while maintaining the benefits of high frequency operation.

A 200 milliwatt converter was constructed to deliver -3.0 volts at approximately 65 milliamps from a +5 volt input supply. Peak efficiency at full load measured 73% with V_{IN} = +5.5V, 69% with +5.0V and 60% at +4.75V input.

Higher switching frequencies are a practical choice to reduce the inductor volume, although some degradation in efficiency is to be expected. The use of surface mount components results in a very compact DC to DC converter, suitable for "on-card" regulators and distributed power applications.

List of Materials

C1	0.1µF / 16V
C2	0.1µF / 16V
C3	100pF / 6V
C4	270pF / 6V
*C5	1nF / 6V
C6	1.0µF / 6V
C7	100µF / 6V
SPRAGUE	#592D-107X06R3R2
L1	150µH / 0.4µJ
COILCRAFT	# DT3316-154
R1	30k / 0.1W
R2	11.0k / 0.1W
R3	20.0k / 0.1W
*R4	100k / 0.1W
U1	UCC3805 PWM

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Other Applications:

+5V to -2V : A minus two volt (-2V) output can be obtained with the same circuit by simply replacing resistor R2 with a short circuit. The inductor value may need to be modified depending on the desired output current.

+5V to -5V : A minus five volt (-5V) output is obtained by using a 30k ohm value for resistor R2. Note that the UCC3803 device is recommended (without the toggle flip flop) to achieve a higher maximum duty cycle. The inductor value needs to be calculated based upon output current and switching frequency. Higher overall efficiency can be obtained than in the -3V application due to the higher output voltage (-5V).

Consult Unitrode Design Note DN-43 for other simple DC-DC inverter applications, or contact a Unitrode Field Applications Engineer.

* Coilcraft telephone number: 1-800-322-COIL

* Sprague telephone number: 1-207-324-4140

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Design Note

Simple Voltage Inverter Circuit Converts -48V Input to +5V Output

by Bill Andreycak

Generating a positive output voltage from a negative input supply voltage can be done easily using the circuit shown in Figure 1. A flyback converter is implemented with the control and switching functions performed by the UC2577HV Easy Switcher IC. The high voltage (HV suffix) rating of the device is ideal for Telecommunication and distributed power applications which typically incorporate a positive or negative 48V input. Depending on the input supply variations, this circuit can also be used to develop a +12V output provided the IC maximum supply rating of 65V is not exceeded.

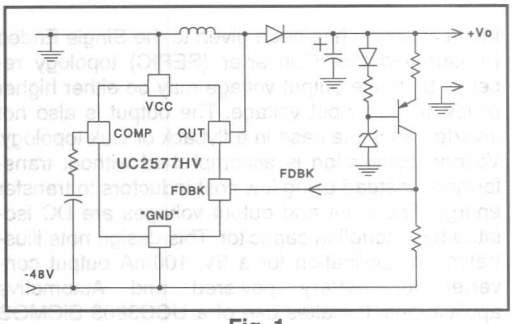


Fig. 1

The output voltage is regulated by constructing a current mirror between the positive output voltage and ground, and level shifting this current to the artificial "ground" (-48V) of the IC. This feedback technique is simple and effective for most applications.

For more demanding needs, the feedback circuit of Figure 2 can be utilized instead. Output voltage and current are sensed by the UC3838A Controller IC's dual transconductance amplifiers, and their outputs are diode OR'd into the IC's high voltage output driver section forming a current source. This similarly level shifts the feedback information from the power supply output to the artificial "ground" of the UC2577 IC. The UC3838A can be powered by an input voltage up to it's 40V (Vm) maximum, and the high voltage PNP output stage can withstand minus 140 volts between the emitter supply (Vm) and the RESET output. Originally intended as a Magnetic Amplifier (MAG AMP) controller and driver, this IC is equally suitable for high voltage precision control and feedback applications.

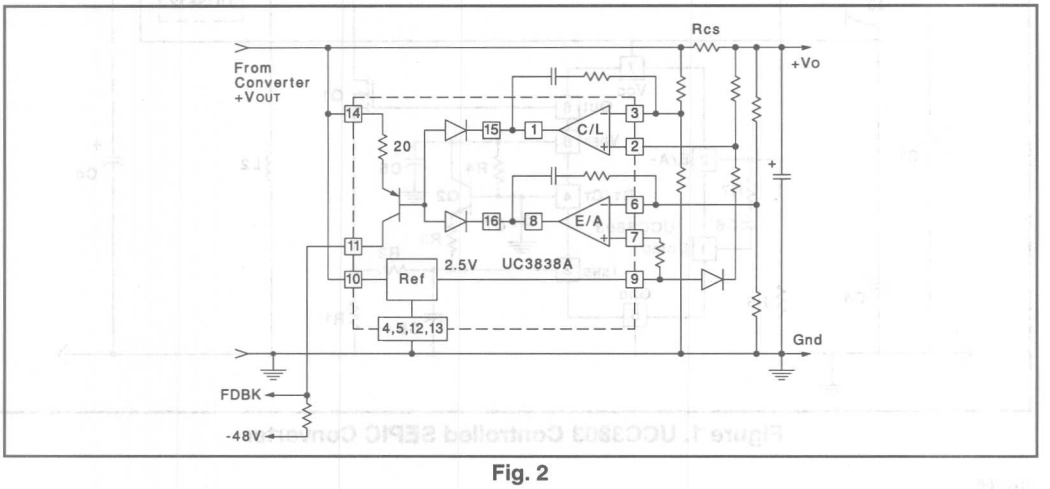


Fig. 2

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Design Note

Versatile Low Power SEPIC Converter Accepts Wide Input Voltage Range

by Jack Palczynski

Much attention has been given to the Single Ended Primary Inductor Converter (SEPIC) topology recently because output voltage may be either higher or lower than input voltage. The output is also not inverted as is the case in a flyback or Cuk topology. Voltage conversion is accomplished without transformers, instead using low cost inductors to transfer energy. The input and output voltages are DC isolated by a coupling capacitor. This design note illustrates an application for a 5V, 100mA output converter for battery powered and Automotive applications. It makes use of a UCC3803 BiCMOS current mode controller to provide a 5V output at full load of 100mA from an input of 2.5V to 13.5V after an initial start-up at 5 volts.

This SEPIC converter uses current mode control to simplify stabilization of the control loop. Peak current in the FET is limited by the pulse by pulse current limiting of the UCC3803. Switching frequency is 500kHz, allowing low output current handling and low output ripple with small inductors and capacitors while remaining in the continuous inductor current mode (CCM). Once started, the low voltage operation of the UCC3803 is extended by bootstrapping from the output through a UC3612 Schottky diode. By including slope compensation (Q2, R3), the duty cycle may exceed 50% without experiencing subharmonic oscillations.

This topology places higher stresses on both the switch and the diode than with other PWM topologies. Peak switch and diode stresses are both $V_{IN}+V_{OUT}$ and $I_{IN} + I_{OUT}$. Peak to peak ripple current in the coupling capacitor is $I_{IN} + I_{OUT}$.

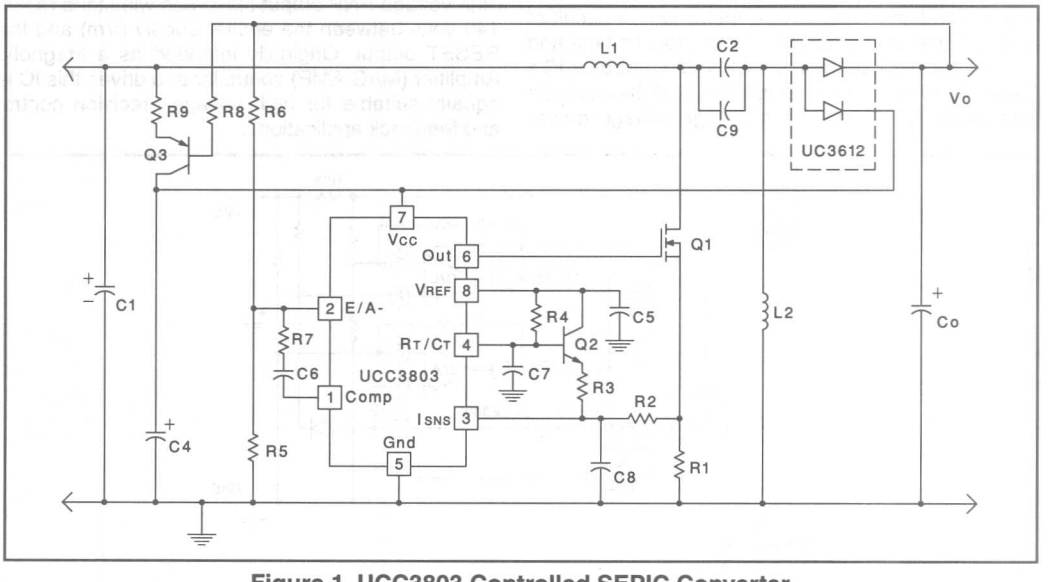


Figure 1. UCC3803 Controlled SEPIC Converter

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Specifications :

VIN (initial start-up) 5V
VIN ..... 2.5V to 13.5V
IOUT ..... 45mA to 100mA
Switching Frequency 500kHz
Output Regulation ..... ±3%
Output Ripple ..... 150mV (max)

SEPIC Converter Design Guide:

1. Choose a switching frequency, fs.

$fs = 500kHz$

2. Calculate minimum duty cycle (DMIN):

$$DMIN = \frac{VO}{VO + VIN(max)}$$

$$DMIN = \frac{5V}{(5V + 13.5V)} = 0.27$$

3. Calculate maximum duty cycle (DMAX):

$$DMAX = \frac{VO}{VO + VIN(min)}$$

$$DMAX = \frac{5V}{(5V + 2.5V)} = 0.67$$

4. Find an appropriate inductor so that IDIODE is not less than zero (note that this value should be used for both inductors):

$$L > \frac{VIN(max) \bullet DMIN}{fs \bullet Io(min)\left(\frac{VO}{VIN(max)} + 1\right)}$$

$$L1 = L2 > \frac{13.5V \bullet 0.27}{500kHz \bullet 45mA\left(\frac{5}{13.5} + 1\right)} = 118\mu H$$

Note that the COILCRAFT inductor selected is specified at twice this value of inductance at light load, and decreases at high loads.

5. Calculate IIN(max) at maximum output current:

$$IIN(max) = \frac{Io(max) \bullet D(max)}{1 - D(max)}$$

$$IIN(max) = \frac{0.1 \bullet 0.67}{1 - 0.67} = 202mA$$

6. Find RMS current ripple and choose an appropriate Ccc:

$$\sqrt{Io(max)^2 \bullet D(max) + IIN(max)^2 \bullet (1 - D(max))}$$

$$\sqrt{0.1^2 \bullet 0.67 + 0.2^2 \bullet (1 - 0.67)} = 141mA$$

Select a capacitor to handle this ripple current.

7. Choose an output capacitor for ripple voltage:

$$dIO(max) = IIN(max) + \frac{VIN(max) \bullet D(max)}{2Lfs}$$

$$dIO(max) = 202mA + \frac{2.5V \bullet 0.67}{2 \bullet 220\mu H \bullet 500kHz} = 209mA$$

then, ripple voltage

$$dV > dIo(max)\left(\frac{1}{2\pi fs \bullet C} + ESR\right)$$

$$150mV > 209mA\left(\frac{1}{2\pi \bullet 500kHz \bullet 33\mu F} + 0.7\right) = 148mV$$

Some iterations with different capacitors will yield an acceptable voltage ripple.

It may become necessary to run the converter in discontinuous inductor current mode (DCM) when minimum load is a very small percentage of the maximum load. D will become dependent on output load and output voltage regulation will vary more than in CCM. The CCM system double pole occurs at

$$fdp = \frac{1}{\sqrt{2} \bullet \pi (L1 + L2)Ccc}$$

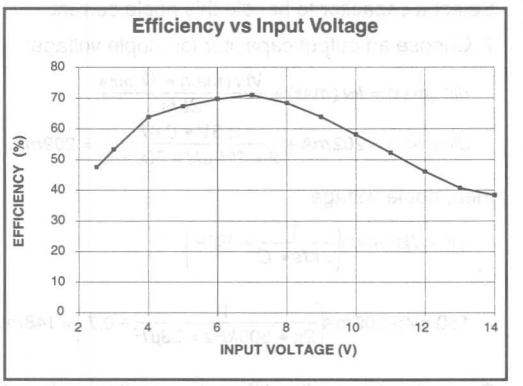
and the ESR zero occurs at

$$fz = \frac{1}{2 \bullet \pi \bullet ESR \bullet Co}.$$

A plot of efficiency is shown below for the range of input voltage. Efficiency may be increased by using lower switching frequencies at a cost of larger components. This might be desirable in equipment with small batteries that demand lower power consumption for extended life.

The SEPIC converter may be used for a wide range of output voltages over a range of input voltages. Other outputs tested were 3V and 12V with circuits

similar to that of this design note. As output current increases, conduction losses in the switch and output diode begin to degrade efficiency and ripple current in the coupling capacitor may be excessive. In high power applications, a transformer isolated converter or cascaded stages may be more practical.



Parts List:

D1, D2	Unitrode UC3612D Dual Schottky phone # (603) 429-8610
C1-3, C9	33µF 25V Sprague 293D336X0025E2T phone # (207) 324-4140
C4,C5,C6	0.1µF Ceramic
C8	150pF Ceramic
L1, L2	220µH COILCRAFT DT3316-102-224 phone # (708) 639-1469
Q1	Siliconix Si9410DY phone # (800) 554-5565
Q2	2N2222S
Q3	2N2907AS
R1	1 ohm 1/4W
R2	1k 1/8W
R3, R6	10k 1/8W
R4	30k 1/8W
R5, R7	6.2k 1/8W
R8,R9	50 ohm 1/8W
U1	Unitrode UCC3803D BiCMOS PWM IC

REFERENCES:

[1] W. Andreycak U-133 "UCC3800/1/2/3/4/5 BiCMOS Current Mode Control ICs" Unitrode Application Note

[2] L. Dixon "High Power Factor Preregulator Using the SEPIC Converter" Unitrode Seminar SEM-900 pp. 6.1-6.12

[3] L. Dixon "Control Loop Design SEPIC Preregulator Example" Unitrode Seminar SEM-900 pp. 7.1-7-6

[4] U-97 "Modeling, Analysis and Compensation of the Current-Mode Converter" Unitrode Applications Handbook A-100 pp. 260-266

[5] U-100 "UC3842 Provides Low-Cost Current-Mode Control" Unitrode Applications Handbook A-100 pp.278-291

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Design Note

UC2577 Controls SEPIC Converter for Automotive Applications

by Jack Palczynski

The Single Ended Primary Inductance Converter (SEPIC) can convert an input voltage to an output voltage that is higher, lower or equal to the input. Conversion is performed without the use of expensive transformers, making this a good choice for low cost, non-isolated applications. The UC2577 provides the switch and control to take advantage of this topology with a minimum of additional parts.

The circuit shown in Figure 1 was designed to provide a 5V or 12V output from an input voltage ranging between 3V and 40V. The coupling capacitor is chosen to handle the high ripple current seen in this topology, with a peak-to-peak current of approximately $I_{IN} + I_{OUT}$. The converter switches at 52kHz and operates in both continuous inductor current mode (CCM) and discontinuous inductor current mode (DCM). Note that both the diode and the switch have a peak voltage stress of approximately $V_{IN} + V_{OUT}$, and peak current stress of approximately $I_{IN} + I_{OUT}$. Note that when the converter is in CCM, the ratio of $V_{OUT}/V_{IN} = D/(1-D)$ where D is the duty ratio. To calculate components for other inputs and outputs, assume CCM as a starting point and use about 1/2 max output current as a min value. For further details, consult Unitrode Design Note DN-48.

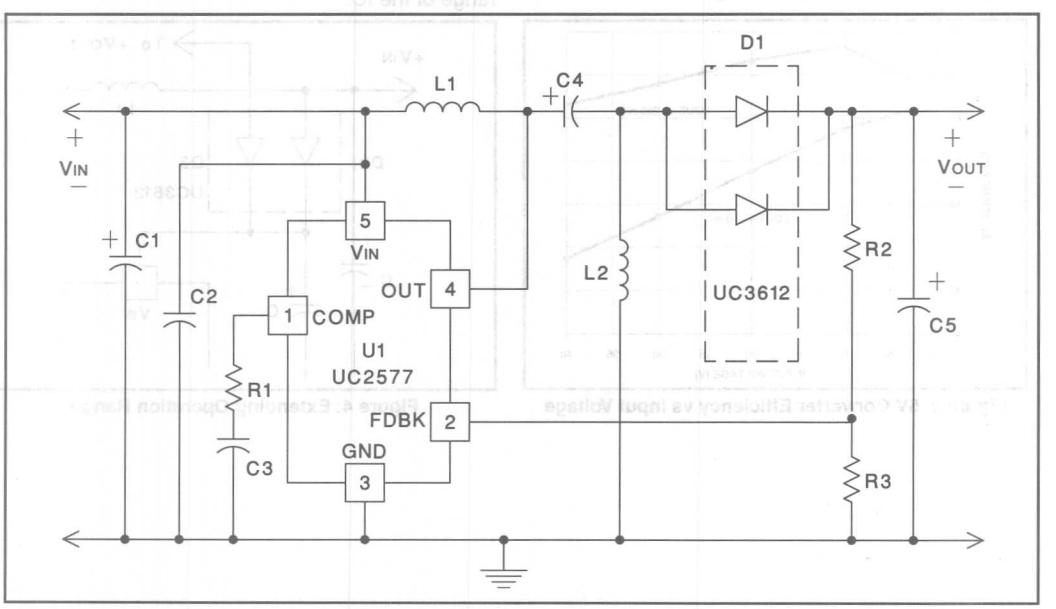


Figure 1. Easy SEPIC Converter Schematic

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Parts List:

U1	UC2577
D1	UC3612 Dual Schottky
L1,L2	100µH ECI # M1088 phone (413) 562-7684
C1	47µF/50V Sprague 515D476M050AA6A phone (207) 324-4140
C2	0.1µF ceramic
C3	0.47µF ceramic
C4	220µF/50V Sprague 515D227M050CD6A
C5	220µF/6V Sprague 595D227X9006D7 (5V output)
* C5	12V output only, use four 68µF/16V Sprague 293D686X0016D2T
R1	100 ohm 1/8W
R2	3.01k 1/8W
R3	1k 1/8W (5V output)
* R3	330 ohms 1/8W (12V output)
* D2,3	UC3612 Dual Schottky (Extended Operating Range)

Efficiency was measured for the 5V (Figure 2) and 12V (Figure 3) output at two power levels for the full range of Automotive input voltages.

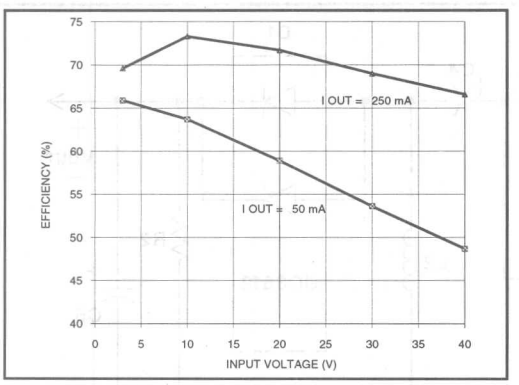


Figure 2: 5V Converter Efficiency vs Input Voltage

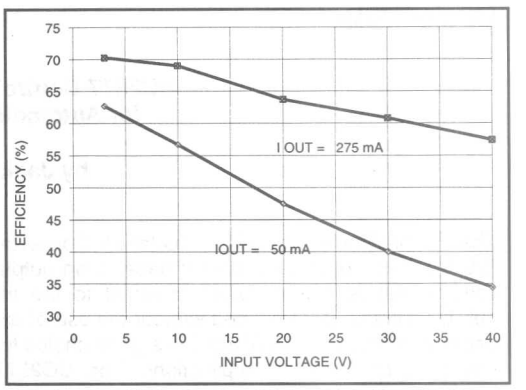


Figure 3: 12V Converter Efficiency vs Input Voltage

As seen in Figure one, a simple design is used to convert power for automotive applications. If longer hold up times are needed or operation at low input voltages demanded, the circuit in Figure 4 may become useful. By adding two diodes, the output voltage bootstraps the IC and allows operation even after the input voltage drops below the operating range of the IC.

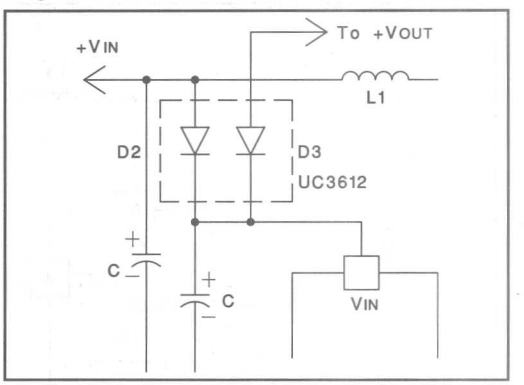


Figure 4: Extending Operation Range

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Simple Techniques for Isolating and Correcting Common Application Problems with UC3625 Brushless DC Motor Drives

by Mickey McClure

The UC3625 brushless DC motor control IC incorporates many useful features which greatly simplify the design of low cost and reliable brushless DC motor drive systems. Although the controller IC is designed for ease of circuit implementation, a few precautions must be taken to insure proper operation. This design note highlights a few areas where the IC may not operate correctly if suitable design techniques are not followed.

REFERENCE VOLTAGE

A common application problem is inadequate decoupling and/or excessive loading on the VREF pin of the UC3625. As the data sheet indicates, the maximum recommended current drain on this node is 30mA DC. Much of the UC3625 internal logic is also referenced off of this node and any transient or noise spikes on the VREF pin can result in improper circuit operation. When the VREF pin is affected by noise, the result is usually a "lock up" condition where the motor drive outputs become disabled. This may result from a false trip of the under-voltage lock-out circuit, a false trip of soft start, or an improper decode of the Hall sensors. Other protection signals such as RC-Brake or ISENSE may be affected as well.

A simple trouble shooting technique can be used to determine when an upset of the UC3625 internal logic is causing the lock up condition. The VREF pin of the IC should be isolated from the rest of the circuit and decoupled with at least 0.1µF. Any external +5V circuitry should be powered off of a separate bench supply. The problem should immediately go away if the VREF pin is the culprit. The motor should now operate normally, with no lock up condition.

The solution to this problem will usually involve both reducing the external current drain on VREF and increased decoupling. Every effort should be made to reduce the DC current drain as low as possible so that any AC currents will have less impact on VREF.

The Hall sensors should be powered by something other than VREF, such as VCC. While there is no general rule on how much DC current is too much, as DC currents approach 30mA, there will be more reason to suspect that VREF is the source of the lock up condition.

AC current will be drawn from the VREF point when it is used to provide the pull up voltage for the Hall inputs to the UC3625. Noise spikes caused by this current drain may be severe enough to latch false logic states on the internal protection circuitry if adequate decoupling is not provided. The reference voltage should **always** be decoupled to ground with a high quality ceramic capacitor of at least 0.1µF located as close as possible to VREF and ground pins. An electrolytic capacitor should be placed in parallel with the ceramic capacitor if there is any significant DC loading on the reference voltage. A value of 10µF is usually sufficient. The placement of the electrolytic capacitor is not as critical, but it should be located as close to the ceramic capacitor as practicality will allow. Figure 1 shows the recommended power connections and decoupling for a typical UC3625 motor drive system.

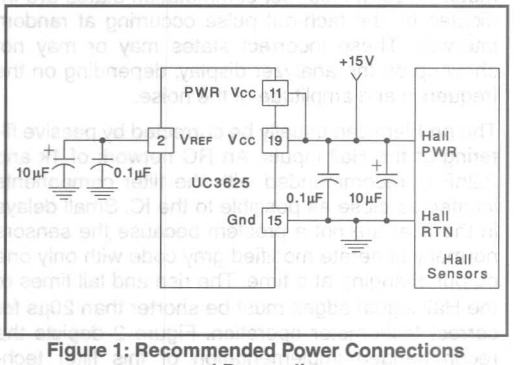


Figure 1: Recommended Power Connections and Decoupling

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HALL INPUTS

High power motor drive systems are frequently characterized by large noise spikes induced by high frequency switching. Under certain conditions these noise spikes can trigger Hall sensor inputs to latch improper commutation states. If an improper commutation state is latched, the correct state is then locked out for the duration of the tach-out pulse. The result is not generally a lock out condition, but rather a motor that responds in a sluggish or unpredictable manner.

As indicated by the UC3625 data sheet, any change in the H1, H2, or H3 inputs loads data from the position sensor latches. Because the position latches are inhibited for the duration of the user programmable tach-out pulse, a noise induced state will lock out the correct commutation state. The power amplifier will then energize the wrong windings of the motor, possibly resulting in reduced torque, or zero or negative torque depending on which incorrect state is latched in. The controller will allow a new state to latch once the tach-out pulse times out. Normal operation may resume at this time, or the noise related problems may continue. The response of the motor is therefore erratic and unpredictable.

This problem can be traced with a logic analyzer or four channel oscilloscope connected to the three Hall inputs and the tach-out pulse. For normal operation, the logic analyzer should display the correct sequence of the Hall signals, and the tach-out pulse should occur at regular intervals proportional to the motor velocity. Incorrect commutation states are indicated by the tach-out pulse occurring at random intervals. These incorrect states may or may not show up on the analyzer display, depending on the frequency and amplitude of the noise.

The problem can usually be corrected by passive filtering of the Hall inputs. An RC network of 1k and 2.2nF is recommended with the filter components located as close as possible to the IC. Small delays in the filter are not a problem because the sensors normally generate modified gray code with only one output changing at a time. The rise and fall times of the Hall signal edges must be shorter than 20µs for correct tachometer operation. Figure 2 depicts the recommended implementation of this filter technique.

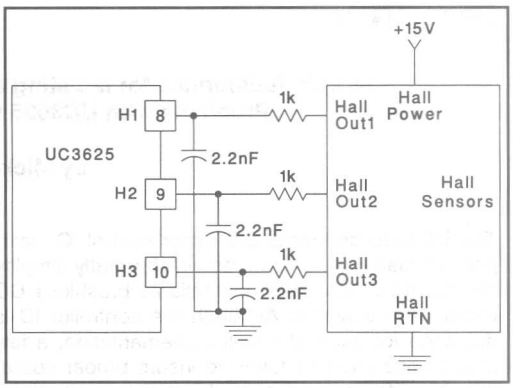


Figure 2: Recommended Hall Filtering

A more noise tolerant solution involves inserting comparators between the Hall sensors and the UC3625 if the passive technique is not sufficient. Because Hall sensors are typically open collector drivers, their outputs can easily become corrupted when driving long cables in a high noise environment. Much greater signal integrity can be achieved by using comparators configured with a large amount of hysteresis to attain greater noise margin. They must be configured in the noninverting mode so that the correct Hall states will be latched by the UC3625. Figure 3 shows an example circuit for driving the Hall inputs with comparators.

CURRENT SENSE CIRCUITRY

The UC3625 current sense circuitry must also be configured correctly to prevent improper circuit response. Noise problems may cause the UC3625 to supply less current to the motor than the controller commands, resulting in poor motor response, and possibly undesired torque limiting.

The most important factor in achieving proper current limit response is a correct differential measurement of the voltage across the current sense resistor. Separate traces must be run from the ISENSE1 and ISENSE2 inputs directly to the current sense resistor. If an input filter is used, it should be balanced, and the filter resistors should tie directly to the current sense resistor. Recommended component values for the differential filter are 270Ω and 4.7nF. **Never** should one ISENSE input line be simply grounded and the other input driven single

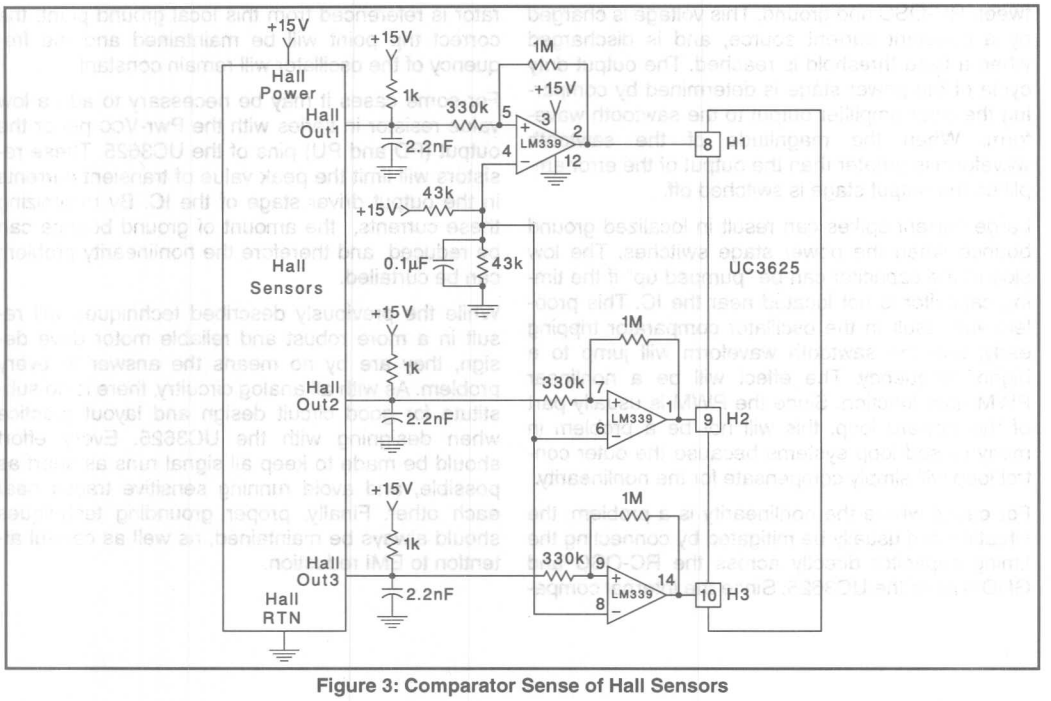


Figure 3: Comparator Sense of Hall Sensors

ended. The recommended circuit layout for the ISENSE1 and ISENSE2 input signals is shown in Figure 4.

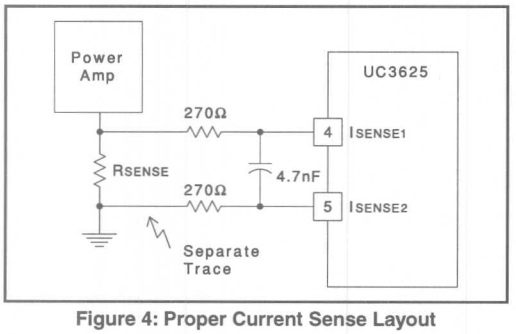


Figure 4: Proper Current Sense Layout

Additional noise immunity can be achieved by adding a capacitor from the ISENSE output to ground. This capacitor should be located as close as possible to the ISENSE pin, and a low impedance path to ground for its low side is essential. Filtering at this point has the advantage of allowing fast signal inversions to be correctly processed by the absolute value circuit before filtering takes place.

If high levels of common mode noise or ground bounce are affecting the ISENSE inputs it may be necessary to decouple the ISENSE inputs (pins 4 and 5) to ground with 470pF capacitors. These capacitors will shunt out any high frequency common mode noise, and allow for a more accurate measurement of true motor current.

NONLINEARITY PROBLEMS ASSOCIATED WITH NOISE ON THE TIMING CAPACITOR

Switching noise can result in discontinuities in the linear response of the PWM circuitry if the timing capacitor on the RC-OSC pin is not located properly. The UC3625 creates the sawtooth waveform by measuring the voltage across the capacitor tied be-

tween RC-OSC and ground. This voltage is charged by a constant current source, and is discharged when a fixed threshold is reached. The output duty cycle of the power stage is determined by comparing the error amplifier output to the sawtooth waveform. When the magnitude of the sawtooth waveform is greater than the output of the error amplifier, the output stage is switched off.

Large current spikes can result in localized ground bounce when the power stage switches. The low side of the capacitor can be "pumped up" if the timing capacitor is not located near the IC. This problem will result in the oscillator comparator tripping early, and the sawtooth waveform will jump to a higher frequency. The effect will be a nonlinear PWM gain function. Since the PWM is usually part of the forward loop, this will not be a problem in many closed loop systems because the outer control loop will simply compensate for the nonlinearity.

For cases where the nonlinearity is a problem, the situation can usually be mitigated by connecting the timing capacitor directly across the RC-OSC and GND pins of the UC3625. Since the internal comparator is referenced from this local ground point, the correct trip point will be maintained and the frequency of the oscillator will remain constant.

For some cases it may be necessary to add a low value resistor in series with the Pwr-Vcc pin or the output (PD and PU) pins of the UC3625. These resistors will limit the peak value of transient currents in the output driver stage of the IC. By minimizing these currents, the amount of ground bounce can be reduced, and therefore the nonlinearity problem can be curtailed.

While the previously described techniques will result in a more robust and reliable motor drive design, they are by no means the answer to every problem. As with all analog circuitry, there is no substitute for good circuit design and layout practice when designing with the UC3625. Every effort should be made to keep all signal runs as short as possible, and avoid running sensitive traces near each other. Finally, proper grounding techniques should always be maintained, as well as careful attention to EMI reduction.

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Design Note

Programming the UCC3806 Features

by Jack Palczynski

INTRODUCTION

The UCC3806 is a pin for pin compatible BiCMOS replacement for the UC3846 and UC3856. Some functions in the UCC3806 are programmed differently and these methods are explained here. In particular, the CUR LIM ADJ pin programs the maximum peak current for the current sense amplifier. This function is completely compatible with previous ICs. The second function on this pin is the latch/non-latch feature for the shutdown pin. Programming latch or non-latch mode differs from the UC3846 and UC3856 and these changes will be explained here.

Current Limit Adjust

To review, the CUR LIM ADJ pin adjusts the maximum current peak on the current sense amplifier (pin 4 to 3) by the formula: $Vcl=1/3 * [(R2*V_{REF})/(R1+R2) -0.5]$. This can be verified by carefully following the path from the current sense amplifier to the CUR LIM ADJ pin. A second function is for shutdown mode programming. When the shutdown pin voltage exceeds 1V, the UCC3806 outputs shut down. At this point, a 190µA (typ) current sink pulls current from the CUR LIM ADJ pin to ground. If the voltage at the CUR LIM ADJ is above

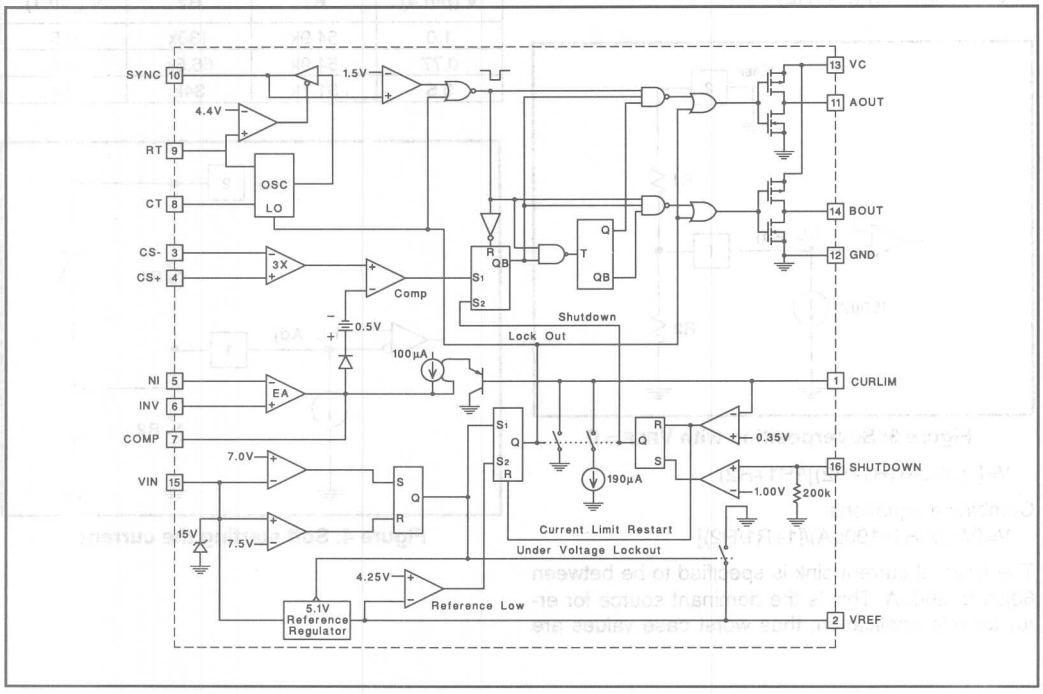


Figure 1: UCC3806 BiCMOS Current Mode PWM Block Diagram

350mV (typ), then the IC remains latched off. If this voltage falls below 350mV at any time, the shutdown is unlatched and the IC restarts. Calculating the actual voltage on the CUR LIM ADJ pin is a simple, two source superposition problem.

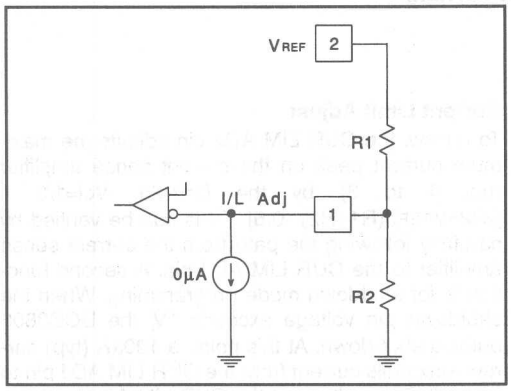


Figure 2: Superposition with current sink = 0

$V = (V_{REF} * R2)/(R1+R2)$

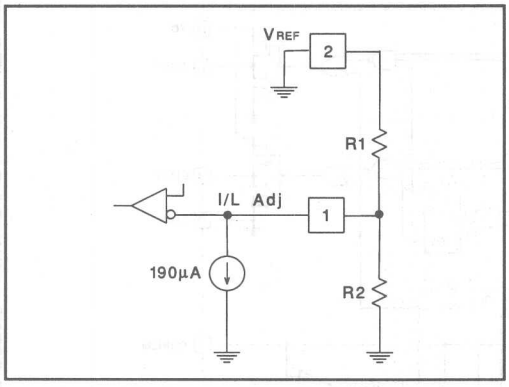


Figure 3: Superposition with V_{REF} = 0

$V=[-190\mu A*(R1*R2)]/(R1+R2)$

Combining equations:

$V=(V_{REF}-R1*190\mu A)/[1+R1/R2)]$

The internal current sink is specified to be between 80µA to 300µA. This is the dominant source for error for this application, thus worst case values are inserted into the above equation to determine latch and non-latch modes.

I LIM ADJ Latching Mode Voltage:

$V=(V_{REF}-R1*300\mu A)/[1+R1/R2)] > 350mV$

I LIM ADJ Non-Latching Mode Voltage:

$V=(V_{REF}-R1*80\mu A)/[1+R1/R2)] < 350mV$

Solving either of these equations and solving the equation for a desired current limit pin voltage simultaneously gives closed form solutions for R1 and R2. Some solutions are shown below.

Table of Approximate Resistor Value:

Latching Mode:			
V (pin 4)	**R1**	**R2**	**V (pin 1)**
1.0	16.5k	38.3k	0.1
0.77	15k	18.2k	0.3
0.5	14.7k	9.76k	0.3

Non-Latching Mode:			
V (pin 4)	**R1**	**R2**	**V (pin 1)**
1.0	54.9k	130k	0.5
0.77	54.9k	66.5k	0.4
0.5	51.1k	34k	0.4

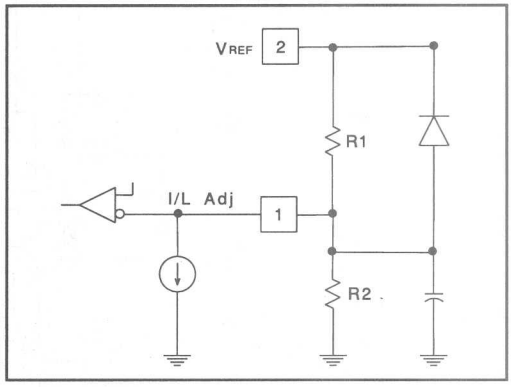


Figure 4: Soft starting the current

Softstart

The CUR LIM ADJ may also be used as a convenient soft start point. By adding a capacitor across R2, maximum current sense ramps up as the soft start capacitor charges. A diode may be added to force a quick discharge of the capacitor when IC power is removed.

SUMMARY

With a systematic approach, one may achieve a variety of maximum current peak levels and the desired shutdown mode. In addition, the UCC3806 allows for a programmed softstart by adding a capacitor to the CUR LIM ADJ pin. By understanding the internal workings of the UCC3806, designers will find many features which can be of great help in reducing parts count and current requirements.

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(2) J. Palczynski, "UCC BiCMOS Current Mode Control IC" Unitrode Integrated Circuits Corporation Applications Note U-144.

(3) W. Andreycak, "Practical Considerations in Current Mode Power Supplies" Unitrode Integrated Circuits Applications Note U-111, Unitrode Product & Applications Handbook '93-'94, pp. 9-134 to 9-151.

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Adjustable Electronic Load for Low Voltage DC Applications

*Operates down to 2.5V

by Bill Andreycak and John Wiggenhorn

Testing power supply regulation over a specified output current range is greatly simplified with the use of an adjustable electronic load. Load current can be varied from zero to the full rated value with the twist of a panel mounted potentiometer or by a digital interface. This design note will feature the design of a self biased, constant current adjustable electronic load which is fully operational with input voltages down to 2.5V.

Most electronic loads rely on the available load voltage to power the control and drive circuits. Since a majority of supplies have output voltages of 5 volts, or more, it has been relatively simple to obtain integrated control circuits which operate at those levels. But the emerging trend towards lower supply voltages, for example 3.3V, 3.0V, 2.7V and even 2.5V logic ICs has eliminated many popular control ICs and techniques from consideration. The UC39432 Precision Analog Controller is fully operational from a supply voltage as low as 2.2V and is usable for this electronic load application, in additional to numerous others. This IC features a precision 1.3V reference voltage, a general purpose operational amplifier and a 100mA open collector NPN transistor. Although primarily intended for optocoupler driving in a feedback loop, the UC39432 is a programmable transconductance amplifier and is adaptable to fulfill many low voltage control requirements. Additional information can be obtained from the device's datasheet

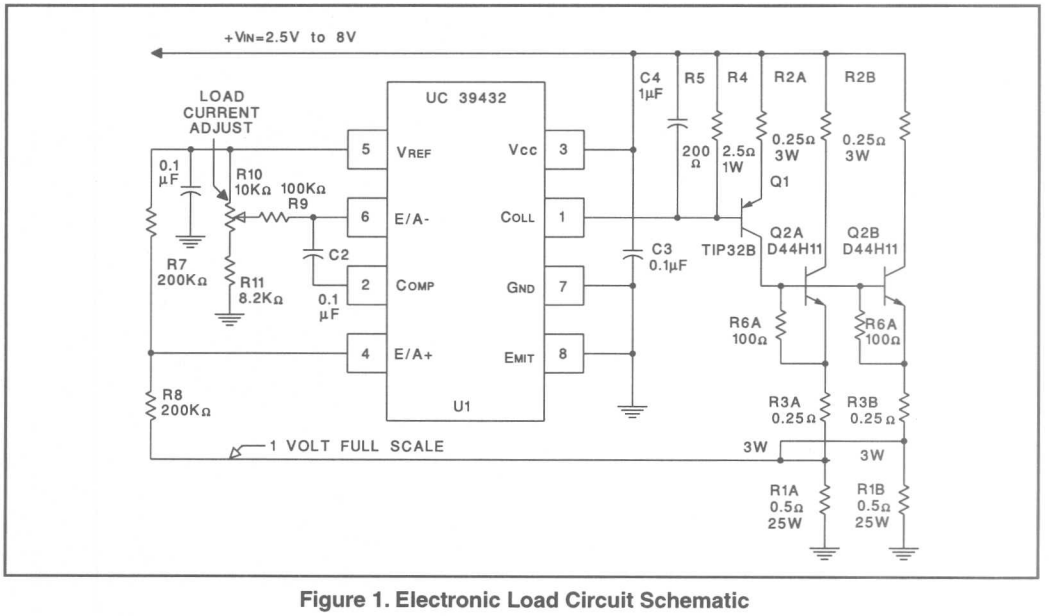


Figure 1. Electronic Load Circuit Schematic

Electronic Load Circuit Operation:

The UC39432 error amplifier noninverting input (pin 4) senses the voltage developed across the paralleled current sense resistors, R1A and R1B. This amplitude is level shifted up by two resistors (R7 and R8) to the ICs reference voltage to maintain the input within its useable common mode range. The inverting input (pin 6) of the amplifier is connected to the wiper of the current adjust potentiometer which programs load current. A 100k ohm series resistor (R9) balances the input impedances while the 8.2k ohm resistor (R11) provides offset to the potentiometer for better resolution. Compensation uses a 0.1µF capacitor (C2) which turns the amplifier into an integrator for good DC load stability. Both the input supply voltage to the IC (pin 3) and the 1.3V reference (pin 5) are bypassed with 0.1µF capacitors (C4 and C1) for noise rejection.

The power stage of this load consists of a PNP driver (Q1) to the NPN power transistors (Q2A and Q2B) in a Darlington configuration. Very common D44H11 (10A/80V) TO-220 type NPN transistors are conservatively utilized. They provide plenty of flexibility for higher output voltages and higher current applications. Heatsinking incorporates two AAVID Engineering type #E5301 parts and number #150 spring clips for the TO-220 devices. Specifications indicate a 65 degree C rise for 10 Watts of power dissipation without forced air. This is worst case operation for each transistor with an 8V input and 4A load current. Emitter ballast resistors (R3A and R3B) are included to balance the load current evenly between the NPN transistors. These two devices are held off by 100 ohm base to emitter resistors (R6A and R6B). Series collector resistance (R2A and R2B) is used to further reduce the transistor power dissipation while still enabling 2.5V operation at full load. Base drive for both is provided by a TIP32B (3A/80V) PNP transistor (Q1). Emitter resistance (R4) is used to reduce the system gain and R5 holds Q1 off with no base drive. A 1µF capacitor (C4) between the input supply and the base increases stability and reduces the potential for a load surge at power-up.

This general purpose, constant current electronic load can be easily modified for higher current and higher voltage applications with few changes. Additional NPN transistor and heatsink stages can be paralleled to draw higher currents and to divide the heat evenly amongst more transistors. The only other change needed is to the current sense resistor value which should be scaled to develop 1 volt at full current. Low voltage operation may also warrant reducing the value of R4 to provide more base drive with the same voltage drop.

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Design Note

Design Considerations for Synchronizing Multiple UC3637 PWMs

by Mickey McClure

As motion control and power interface systems become more complex, the need for more sophisticated control circuitry arises. One common application involves the need for synchronizing multiple pulse width modulators (PWMs). This requirement may result from the need to eliminate beat frequencies when multiple PWMs reside on the same printed circuit board, or from timing considerations in redundant systems where voting between drivers is required.

The UC3637 is an extremely versatile PWM used in many motor control and power driver applications, and the need for synchronization often arises. In order to properly accomplish this, a few simple design rules must be followed. These rules apply primarily to resetting the part's current limit latches.

Figure 1 shows a block diagram of the UC3637. In a single PWM configuration, the triangle waveform, and therefore the operating frequency of the PWM is developed by charging and discharging a capacitor at pin 2, and comparing the voltage across this capacitor to the threshold voltages applied at pins 1 and 3. The design equations for this circuit are discussed extensively in Unitrode Application Note U-102, "Switched Mode Controller For PWM DC Motor Drive."

The most common configuration for synchronized PWMs is a single master PWM driving one or more slave PWMs. In this case the triangle wave is developed by the master exactly as it is in the single PWM case. The master triangle wave is then used to drive the PWM comparators on the one or more slave ICs. The only major concern is resetting the slave current limit comparators.

Figure 2 shows a simple circuit for operating synchronized UC3637 PWMs in a master/slave configuration. The important point to note about this circuit is that the pulse be pulse current limiting feature of the UC3637 is not used. The triangle wave is developed by the master, and used to drive its own PWM comparators as well as the slave PWM comparators. The threshold levels and the CT pin of the slave IC are tied off to levels which force the current limit comparators to stay in the nonlimit state. With the slave CT grounded, and the slave +VTH tied to a negative

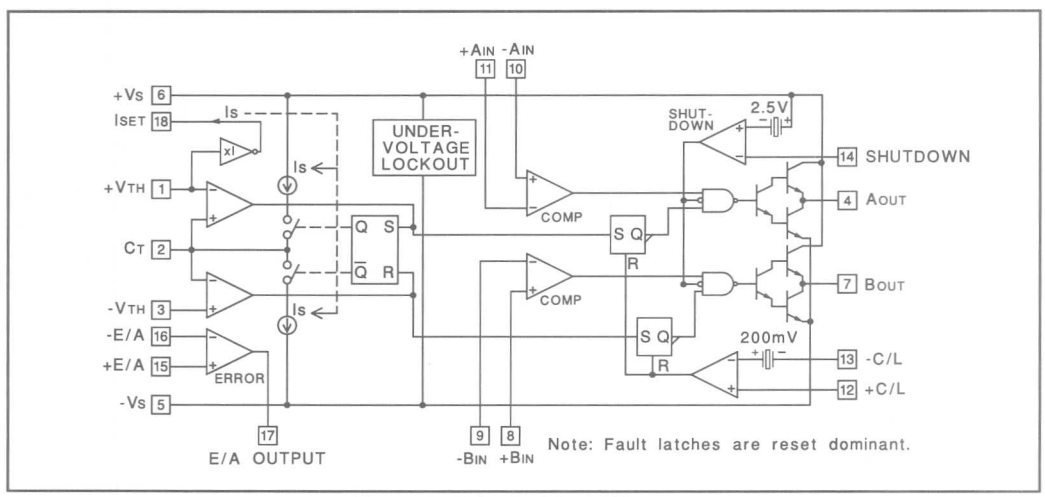


Figure 1. UC3637 Block Diagram

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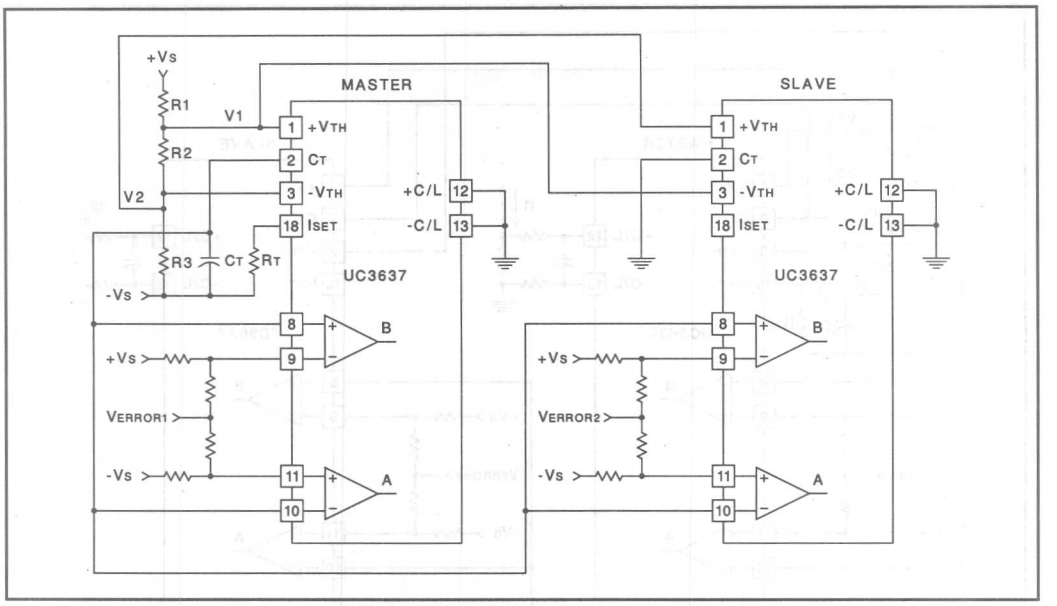


Figure 2. Synchronized PWMs with No Current Limiting

level, the A output current limit comparator will always keep the drive active. The B drive will also be active because -VTH is tied to a positive level. The threshold levels can not simply be tied to the supply rails because those voltages are outside of the common mode range for the comparators.

As long as CT is kept greater than 1000pF, the input capacitance of the slave comparators will not affect the oscillator frequency. If long signal runs are required, or many PWMs need to be synchronized, it is best to buffer the triangle wave with an op amp at the master IC.

While the circuit of Figure 2 is quite simple, current limiting requirements often rule out its use. The circuit shown in Figure 3 should be used for those applications where both current limiting and synchronization are required. In this circuit, the current limit comparators of the slave PWM are tied to threshold levels of the same polarity but lower magnitude than the threshold levels of the master. Independent pulse by pulse current limiting is accomplished by guaranteeing that the slave current limit comparators get reset each cycle. This can be assured by setting the difference between the master and slave threshold levels (dV) so that even with worst case offsets in both the master and slave ICs the magnitude of the master triangle wave will always be great enough to reset the comparators. The following equations outline a procedure for determining the minimum dV for the positive threshold. The dV for the negative threshold is determined by the same procedure:

1) $dV = V1 - V3$

The minimum dV must be able to compensate for the worst case offset errors of the threshold comparators. These errors result from both offset voltage and bias currents:

2) $V_{ERROR1} = (I_{BIAS}) \bullet Req$

3) $Req = \dfrac{R1 \bullet (R2+R3+R4+R5)}{R1+R2+R3+R4+R5}$

4) $V_{ERROR2} = V_{OS} = 150mV$

The worst case error occurs when the offsets of the master are opposite to the offsets of the slave. The offsets than add to each other to give the minimum dV requirement:

5) $dVmin = 2 \bullet (V_{ERROR1} + V_{ERROR2})$

The set point for dV is determined by adding the

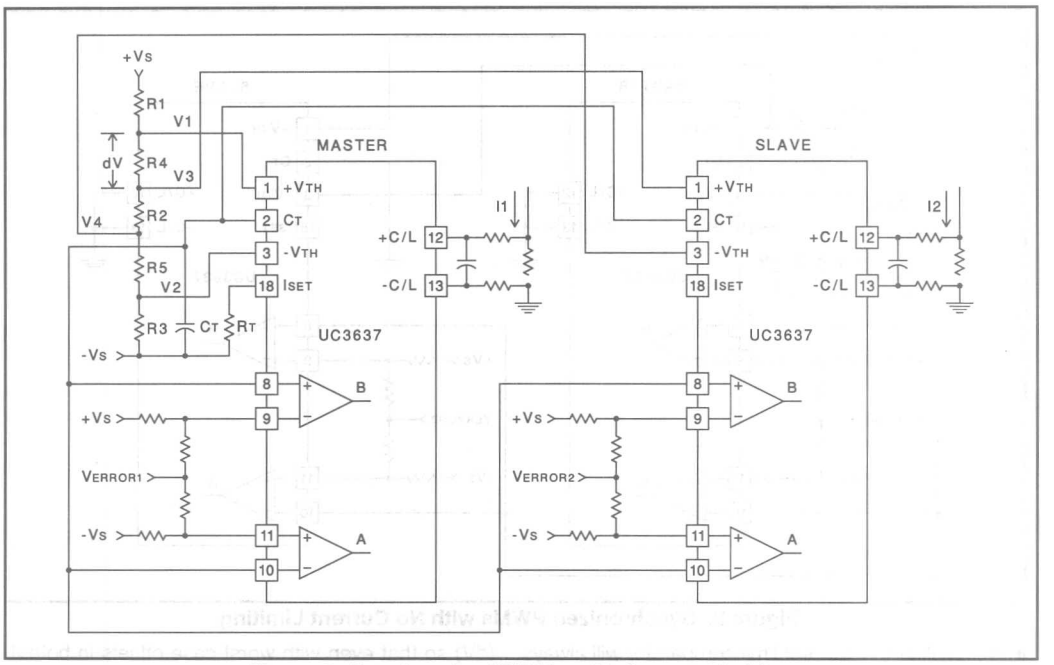


Figure 3. Synchronized PWMs with Current Limiting

maximum tolerance on dV to the minimum dV value. Because dV is set by a resistor divide network with independent terms in both the numerator and denominator of its voltage equation, the total error term is a function of twice the resistor tolerance, as well as the supply voltage. Taking these error sources into account yields the set point for dV:

6) $dV_{SET} = dV_{min} + dV_{min} \bullet (2) \bullet$ (resistor tolerance) $\bullet$ (power supply tolerance)

We now select R4 by:

$$7)\ dV_{SET} = \frac{(+Vs - (-Vs)) \bullet R4}{R1+R2+R3+R4+R5} \quad \text{or}$$

$$R4 = \frac{dV_{SET} \bullet (R1+R2+R3+R5)}{(+Vs - (-Vs)) - dV_{SET}}$$

It should be noted that deriving the threshold levels for the slave PWM off of the same divide network as the master allows for much better tracking of dV. Since the difference between the master and slave threshold levels is small compared to the absolute voltage levels, the resistor tolerance becomes much less significant. If the slave threshold levels were derived off of separate networks, the resistor tolerance would affect the absolute threshold level by the tolerance of the resistors, resulting in a much higher percentage change in dV.

While these two simple circuits will suit the requirements of most synchronized systems, there may be cases where more complex circuitry is required. If a digital square wave clock is used to synchronize many PWMs, an integrator may be required to derive the triangle waveform. For certain critical systems, a phase lock loop may be more desirable as a synchronization mechanism. As always, the individual designer must evaluate the system requirements before a final design configuration can be selected.

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Innovative Buck Regulator Uses High Side N-Channel Switch Without Complex Gate Drive

Converts +5 VDC to +3.3 VDC (or others) and draws only 40 microamps in standby mode

by Bill Andreycak

Obtaining very high efficiency in a voltage step-down (Buck regulator) application often requires the use of N channel, low on-resistance MOSFET switches. The difficulty in driving these enhancement mode devices on the high side of a converter is that they require a gate voltage above the input supply to turn-on. This necessity demands an additional supply voltage solely for the high side gate drive. Although P channel devices are a viable alternative for the sake of gate drive simplicity, their associated cost and higher on resistance limits the number of applications. Typically, P channel FETs are used in Buck regulators with output currents below 4 amps, or so. However, the demand of many 1.8 volt through 3.3 volt logic systems is often in the neighborhood of 10 amps, forcing the use of N channel devices.

The circuit shown in Figure 1. incorporates the UCC3803 BiCMOS PWM controller in a conventional voltage mode controlled Buck regulator application. Normally, the IC needs to be supplied with a separate 12 volt supply from the input to the Buck converter. As the MOSFET is switched on, it's source approaches it's drain voltage (5V) and the gate is driven seven volts higher to the IC's 12 volt supply. Logic level MOSFETs are required for this application which become fully enhanced with only five (or so) volts gate to source in comparison to standard devices which require about ten volts. When Q1 is turned off, the gate is driven to ground by the IC's output and diode Do then conducts the full output current of the regulator.

What's unique about this circuit configuration is the way in which Vcc is supplied to the IC. Diode D1 is used to route the initial power to the UCC3803's Vcc pin from the 5 volt input. Notice

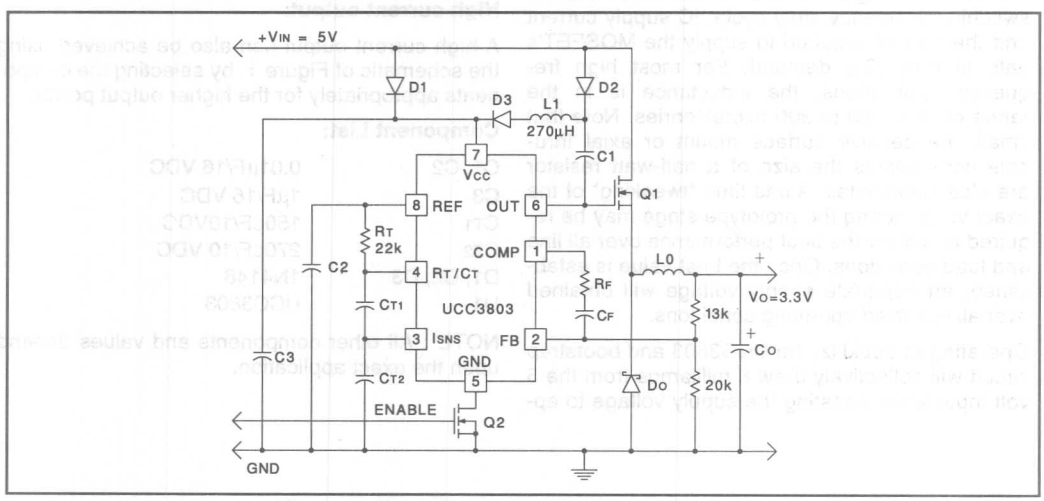


Figure 1. Buck Regulator with High Side NMOS

that diode D2 and capacitor C1 are connected between VIN and the IC's output, pin 6. While the IC is off, it's output is low and capacitor C1 is charged to VIN, or 5 volts. Once the 4.1 volt undervoltage lockout threshold of the IC is crossed, it's PWM output begins switching and goes high. The upper totem-pole transistor within the IC forces the lower end of capacitor C1 (connected to pin 6) up towards the IC's supply voltage, VCC. The initial charge stored by the 5V across C1 is then directed to VCC through diode D3. Essentially, a quasi-resonant tank circuit is formed by the following components; the UCC3803's output, C1, L1 and D3. This simple circuit configuration replenishes the supply voltage (VCC) each time the PWM output switches. After a few initial switching cycles, the ICs supply voltage (VCC) is increased to approximately twice VIN, or about 10 volts. This is a sufficient amplitude to properly drive Logic Level N Channel FETs on the high side of a Buck Regulator. The UCC3803's internal 12 volt supply clamp can also be used to supply a better regulated supply voltage, however any excess current will be shunted to ground. This will reduce overall efficiency slightly, but will immunize the supply voltage from any duty cycle related variations.

The ideal value of inductor L1 is determined by several operating conditions. The critical ones are switching frequency, duty cycle, IC supply current and the current required to supply the MOSFET's gate charge (Q_g) demand. For most high frequency applications, the inductance is in the range of about 50 to 300 microHenries. Note that small, inexpensive surface mount or axial thruhole components the size of a half-watt resistor are ideal candidates. A one time "tweaking" of the exact value during the prototype stage may be required to deliver the best performance over all line and load conditions. Once the best value is established, an adequate supply voltage will obtained over all specified operating conditions.

Operating at 500kHz, the UCC3803 and bootstrap circuit will collectively draw 8 milliamps from the 5 volt input while boosting the supply voltage to approximately 9 volts. Input current rises to around 12mA in order to raise the supply voltage to 11.5 volts. This amplitude is just below the VCC supply clamp voltage threshold of the UCC3803 IC. In most applications, the DC current from the 5 volt input source required to charge the MOSFET gate will be around 20mA, which adds to the IC and bootstrap circuit demands. Typical consumption of the entire working control circuit will be in the 30 to 50mA range, depending on frequency and MOSFET selections.

A low current standby mode can be obtained by using a small logic level MOSFET to switch the IC's ground connection in and out of circuit. When disabled, the entire circuit draws approximately 40 microamps from a 5 volt input. Other adaptations are possible, as shown in Application Note U-133 of the Unitrode IC databook.

Circuit Modifications:

Other output voltages (2.0, 2.2, 2.5, 2.75, 3.0 VDC) :

Any desired output voltage between 2.0V and VIN can be developed using the exact circuit schematic of Figure 1. The modifications required are only to the component values used in the Buck regulator section (LOUT, COUT and R1), although some adjustment of L1 may also be needed.

High current output:

A high current output can also be achieved using the schematic of Figure 1. by selecting the components appropriately for the higher output power.

Component List:

C1, C2	0.01µF/16 VDC
C3	1µF/16 VDC
CT1	150pF/10VDC
CT2	270pF/10 VDC
D1, D2, D3	1N4148
U1	UCC3803

NOTE : All other components and values depend upon the exact application.

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150W Isolated DC/DC Converter for Distributed Power Applications

by Jack Palczynski, MSEE

This Design Note describes a compact, isolated 150W, 12V converter designed for 30V to 60V DC input voltages. The UC3828 is used as the main PWM, and the UC3907 load share IC is utilized in the output section as part of the control loop. This allows parallel operation of several modules equally sharing the total output current. Switching frequency for this converter is 250kHz and common, standard parts are utilized. A parts list and schematic describe the circuit. By varying components, one can see the various functions of the UC3828. Substitution of parts will result in a design which may suit other requirements. To more fully understand the design and specifications of this demo board, please refer to applications note U-147.

INTRODUCTION

The UC3828 features provide functions to ease design and enhance protection in a PWM controlled power supply. The IC is turned on when the ENABLE pin rises above 2.1V and off when below 2.0V. The SHUTDN pin provides added protection by shutting off the IC when greater than 1.5V is present on the pin. The pulse by pulse current limit of 1V is enhanced by a 1.5V shutdown feature. Outputs are actively held low when the IC is below the UVLO threshold or when a shutdown has been activated. Soft start is programmed by a single capacitor. In addition, the maximum duty cycle is accurately programmed in the clock set up and programmable leading edge blanking can eliminate problems usually associated with current turn on spikes. The IC runs on a wide range of input voltages up to 65V and the output is separately powered and limited to 12.4V by an internal regulator. The 5.1V reference is regulated to 2% and the current sense limit held to 5%.

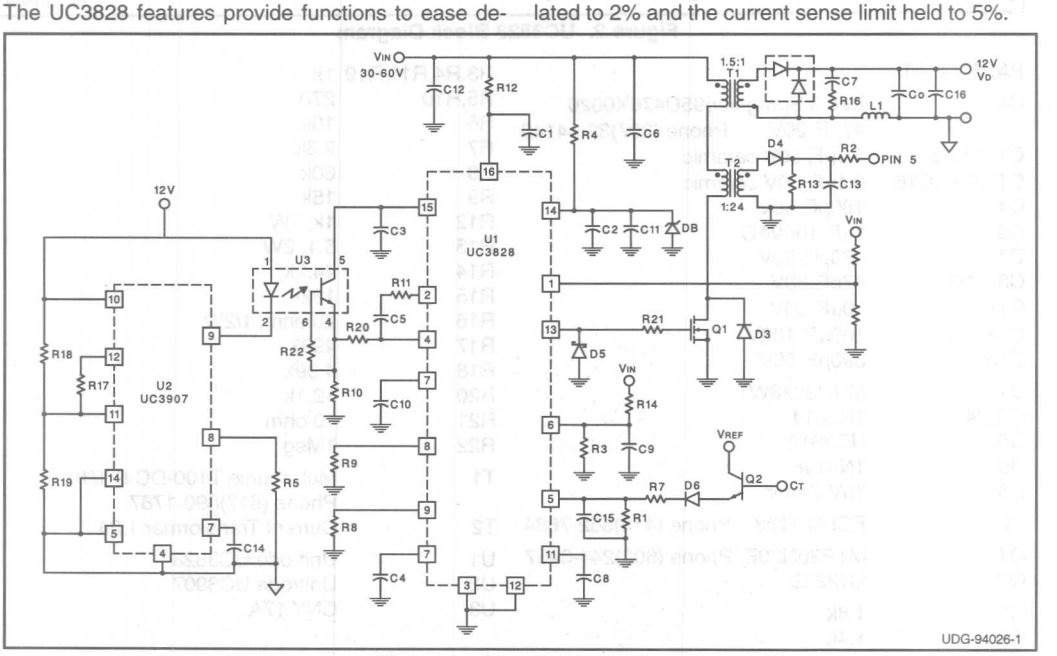


Figure 1. Circuit Schematic

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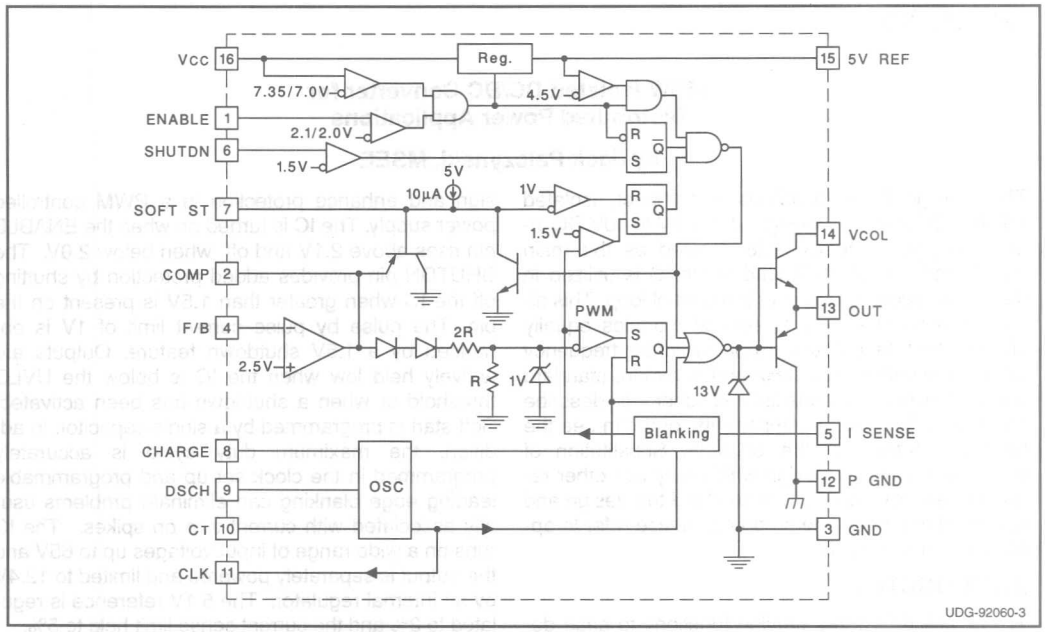


Figure 2. UC3828 Block Diagram

PARTS LIST

Co	Use 3 Sprague 595D476X0020 47µF, 20V Phone (207)324-4140	R3,R4,R11,R19	1k
C1-C3,C5	0.1µF, 50V ceramic	R5,R10	270
C13,C14,C16	0.1µF, 50V ceramic	R6	10k
C4	180pF, 50V	R7	9.3k
C6	1µF, 100VAC	R8	60k
C7	470pF, 50V	R9	15k
C8-C10	47pF, 50V	R12	1k, 2W
C11	10µF, 20V	R13	5.1, 2W
C12	100µF, 100V	R14	44.2k
C15	390pF, 50V	R15	132k
D1	MUR3020WT	R16	20 ohm, 1/2W
D3,D4	1N5614	R17	499k
D5	UC3612	R18	4.99k
D6	1N4148	R20	12.1k
D8	15V Zener	R21	10 ohm
L1	ECI M-1138 Phone (413)562-7684	R22	1Meg
Q1	MTP20N20E Phone (602)244-3467	T1	Multisource T100-DC-6-1/10 Phone (617)890-1787
Q2	2N2222	T2	Current Transformer 1:24
R1	1.8k	U1	Unitrode UC3828
R2	1.4k	U2	Unitrode UC3907
		U3	CNY-17A

An efficiency near 85% is achieved at full load with a 48V input. A spread sheet may be set up to account for various losses in the switch, magnetics and associated circuitry in order to choose a switching frequency and other parameters suitable for other applications.

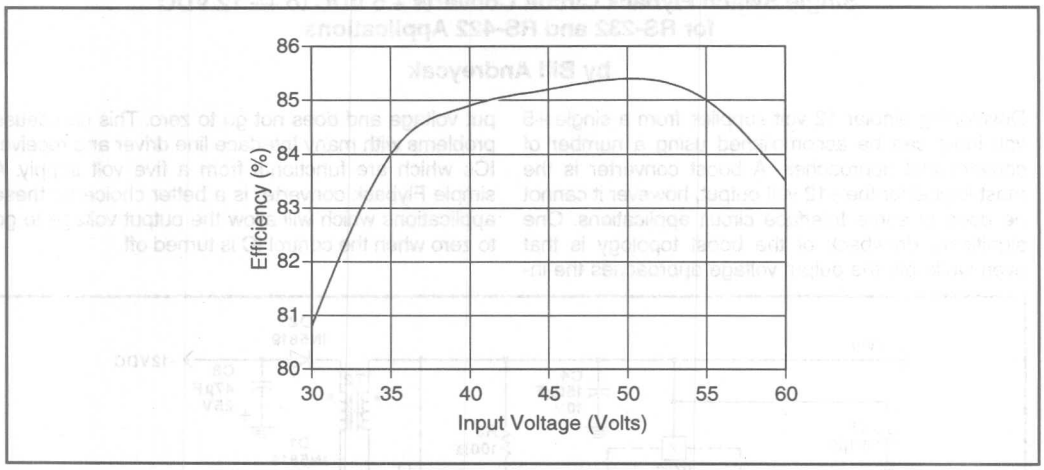


Figure 3. Efficiency vs. Input Voltage

RESULTS

The converter will run with a large heat sink and no forced air at ambient temperatures in the 25 degree C range at full load. Output ripple and noise are less than 100mV peak to peak and regulation is better than 2% over line and load. Minimum load is 1A and the converter will protect itself in the event of a short circuit. This can be demonstrated by increasing the output load and observing that the output voltage falls when peak current limit is triggered. Likewise, if the enable pin is held high, the max duty cycle limit will be reached and the output voltage will drop as input voltage is lowered.

REFERENCES

[1] J. Palczynski, "UC3828 Provides Improvements and Added Features Over the UC3842" Unitrode Applications Note U-147.

[2] P. Todd, "Snubber Circuits: Theory, Design and Application" Unitrode Seminar SEM-900 Topic 2.

[3] W. Andreycak, "1.5 MHz Current Mode IC Controlled 50 Watt Power Supply" Unitrode Applications Note U-110.

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Single Switch Flyback Circuit Converts + 5 VDC to +/- 12 VDC for RS-232 and RS-422 Applications

by Bill Andreycak

Developing bipolar 12 volt supplies from a single +5 volt input can be accomplished using a number of conventional approaches. A boost converter is the most logical for the +12 volt output, however it cannot be used in some Interface circuit applications. One significant drawback of the boost topology is that even while off, the output voltage approaches the input voltage and does not go to zero. This can cause problems with many Interface line driver and receiver ICs which are functional from a five volt supply. A simple Flyback converter is a better choice for these applications which will allow the output voltage to go to zero when the control IC is turned off.

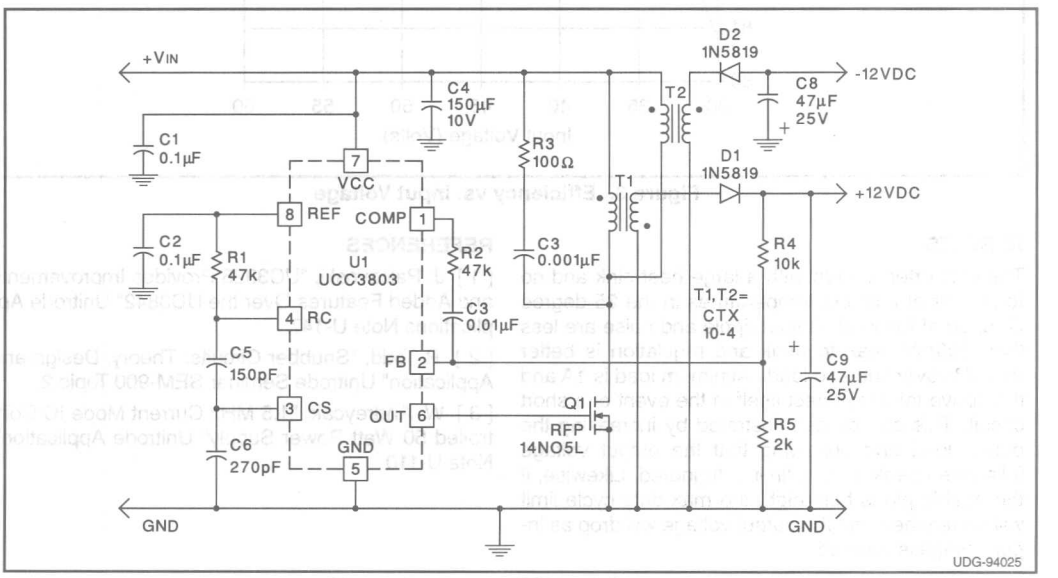


Figure 1. +5 to ±12V/80mA Converter

The negative supply also can be generated from the same Flyback transformer used for plus twelve volt output if an additional winding is provided. The result is a three winding transformer, and often cross regulation problems between the outputs. One way to avoid this is by incorporating two separate, but identical transfomers, one per output. Each of these requires only two windings (primary and secondary) and may be a lower cost solution to a single three winding Flyback transformer. In many applications, even Local Area Networking (LAN) data line isolation transformers, or common mode EMI chokes can be used. The Appendix section of this Design Note lists several potential vendors, products and phone numbers.

In many Interface circuit power supply applications the load currents drawn from the bipolar supplies are fairly similar. When this applies, the positive output voltage will vary proportionately with the negative supply. To simplify voltage regulation, the positive

voltage alone can be measured and used for feedback to the PWM control IC. The negative output voltage will track along reasonably well, and is adequate for many applications. This adaptation significantly reduces the complexity of regulating both outputs simultaneously, which would otherwise require two separate converters and control ICs.

The circuit shown in Figure 1. develops a plus and minus 12 volt output at 80 milliamps each from a +5V input supply. Excellent regulation is obtained with identical loading on both outputs, and degrades only slightly with differential loading. A small amount of preloading can be added to improve cross-regulation for more demanding conditions. Note that both transformer primaries are electrically in a parallel configuration, and energy is stored and released from both simultaneously. This is advantageous during differential loading, as energy stored in one core can be delivered to the other transformer's secondary. The result is a significant improvement in overall and cross regulation if they have low leakage inductances. Magnetic modelling [1,2] can be used to further gain familiarity with this application.

REFERENCES

1. DIXON, Lloyd : " Coupled Inductor Design ", UNITRODE Power Supply Design Seminar Manual SEM-900, Topic 8

2. DIXON, Lloyd : " How to Put Leakage and Wiring Inductances in the High Frequency Circuit Model ", reprinted in the Reference section of UNITRODE Power Supply Design Seminar Manual SEM-900, Topic M4

APPENDIX - List of some Transformer Manufacturers and Products

COILCRAFT : DLF, LAX, P104, TTDLF, TRF, and WB Series', phone # 1-800-322-2645 (U.S.A.)

COILTRONIX : CTX series of two winding coupled inductors, also the VERSAPACK series of multiple winding transformers is applicable, phone # 1-561-241-7876 (U.S.A.)

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Power Dissipation Considerations for the UC3726N/UC3727N IGBT Driver Pair

by Mickey McClure
Application Engineer
Motion Control Products

Optimized for driving Insulated Gate Bipolar Transistors (IGBTs), the UC3726N/UC3727N IGBT driver pair is a very versatile and cost effective solution for applications where voltage isolation is required. However, care must be taken to insure that the junction temperatures of both the UC3726N and UC3727N are kept below levels which assure reliable operation. The purpose of this design note is to outline the proper thermal design procedure for using this chip set.

BACKGROUND

In order to assure reliable operation, the junction temperatures of both ICs should be kept below 125°C. Although the absolute maximum rating is 150°C, the failure rates for silicon integrated circuits increase significantly at temperatures above 125°C. Also note that the electrical specifications of commercial grade ICs are no longer guaranteed at junction temperatures above 70°C. This does not mean that the device will not function, it simply means that some electrical parameters may fall out of their specified range. Since power devices typically operate with junction temperatures as high as 125°C, it is assumed for purposes of this analysis that operation at these temperatures is acceptable for the application. As always with power drivers, design verification in the lab is recommended. What follows is a thermal analysis of the example circuit designed in Unitrode Application Note U-143A, "New Chip Pair Provides Isolated Drive For High Voltage IGBTs."

POWER DISSIPATION IN THE UC3726N

Power losses in the UC3726N consists of output stage conduction and switching losses, as well as bias losses for the chip itself. Output stage conduction losses result from supplying the UC3727N bias current, the IGBT gate drive current,and the transformer magnetizing current. Each loss component can be calculated individually, and the results added to obtain the total power dissipation.

Since power is only transferred across the pulse transformer during the "full" voltage time period, all of the current required to power the UC3727N and the IGBT gate must be supplied during this 1/3 portion of the duty cycle. To calculate the loss associated with this power transfer, the rms value of the average current required to power the UC3727N and the IGBT gate must be calculated. For the example circuit described in U-143A, the average IGBT gate current is equal to:

$$1)\ I_G = 2 \bullet Q_G \bullet F = 2 \bullet 110nC \bullet 15kHz = 3.3mA$$

The typical bias current for the UC3727N is 24mA, resulting in a total average supply current of 27.3mA. Since the average current must be delivered in 1/3 of the duty cycle, the peak current is determined by:

$$2)\ I_{SUPPLY} = \frac{27.3mA}{0.33} = 82.7mA$$

To determine the loss resulting from this current (PLSUPPLY), the rms value of the current is multiplied by the rms value of the total voltage drop of the upper and lower drive stages of the UC3726N:

$$3)\ PL_{SUPPLY} = (2.3V \bullet \sqrt{0.33})(82.7mA \bullet \sqrt{0.33}) = 63mW$$

To determine the loss resulting from the transformer magnetizing current, the rms value is determined for both the "full" time (IMAGFULL) and "half" time (IMAGHALF) currents. With a peak magnetizing current level of 35mA, the corresponding rms currents are calculated as:

$$4)\ I_{MAGFULL} = 35mA \bullet \sqrt{\frac{0.33}{3}} = 11mA$$

$$5)\ I_{MAGHALF} = 35mA \bullet \sqrt{\frac{0.66}{3}} = 16mA$$

The losses resulting from these currents are a function of the rms value of the appropriate voltage drops in the UC3726N. For the "full" time the voltage drop is the total saturation drop of the output drivers. For the "half" time the voltage drop is the sum of the drop across the half on driver (Vcc - 0.6 • Vcc) and the drop across the full on driver (0.4V):

$$6)\ PL_{MAGFULL} = 11mA \bullet 2.3V \bullet \sqrt{0.33} = 14mW$$

$$7)\ PL_{MAGHALF} = 16mA \bullet 12.4V \bullet \sqrt{0.66} = 161mW$$

The power dissipated due to switching loss is difficult to calculate, and some simplifying assumptions must be made. Since the transition from half to full voltage occurs when the transformer current reaches zero, it is assumed that the switching loss is very close to zero for this transition. For the transition from full to half voltage it is assumed that the transformer current remains constant as the sum of the peak magnetizing current and the peak supply current throughout the whole transition. This is a reasonable worst case assumption since the load is highly inductive. Furthermore, the fall time for the full to half driver is much slower than the rise time for the zero to full driver, and therefore the full to half driver is the primary contributor to switching loss.

Referring to Figure 3 of U-143C, the half driver fall time is 200ns, yielding a duty cycle of 0.08 for this calculation. Since the voltage transitions from 28 to 18V, the switching loss component is calculated as:

$$8)\ PL_{SWITCH} = (35mA + 82.7mA) \bullet \sqrt{0.08} \bullet \left(2 \bullet \sqrt{0.08} + 10 \bullet \sqrt{\frac{0.08}{3}}\right) = 72mW$$

The 2V term comes from the saturation drop of the output driver, and the 10V term comes from the 10V swing from 28V to 18V. In order to take into account other miscellaneous switching losses, the PLSWITCH term is rounded up to 100mW.

The final dissipation calculation is the bias loss for the UC3726N itself. Using a single +30V supply, the typical bias current for the UC3726N is 26mA. This takes into account an additional 0.4mA/V ICC component for each volt above the 20V supply level specified in the data sheet. The resulting power loss is:

$$9)\ PL_{BIAS} = 30V \bullet 26mA = 780mW$$

If an external +5V logic supply is available, it is highly recommended to power the logic supply (VL) from this source. The bias loss in this case becomes a function of the reduced Vcc bias current and the bias current requirement for the external logic supply:

$$10)\ PL_{BIAS} = 30V \bullet 16mA + 5V \bullet 13mA = 545mW$$

The total power dissipation for the IC is calculated by adding the individual power loss components. If an external logic supply is not used, the total power dissipation is calculated as:

$$11)\ PL_{TOT} = 0.063W + 0.014W + 0.161W + 0.100W + 0.780W = 1.12W$$

With an external logic supply, the total power dissipation is 0.88W.

For a 16 pin plastic "batwing" package (N package) the worst case θJA is 50°C/W for typical PC board mount, resulting in a temperature rise of 56°C with no external logic supply. Using a max junction temperature of 125°C, the maximum ambient temperature for the IC in this application is 69°C. With an external 5V power supply, the worst case temperature rise is 44°C. If higher ambient temperatures are required, or if keeping the junction temperature below 70°C is required, heat sinking will be necessary.

POWER DISSIPATION IN THE UC3727N

The power dissipation calculations for the UC3727N are much more straight forward. The losses consist only of the bias loss for the IC, and the output stage conduction and switching losses. In order to determine the average output stage loss, the gate drive energy (WGD) is determined by:

$$12)\ W_{GD} = 2 \bullet \tfrac{1}{2} \bullet C_G \bullet V^2 = \left(\frac{Q_G}{V}\right) \bullet V^2 = Q_G \bullet V$$

The factor of 2 results from the fact that the gate drive circuit must charge and discharge the gate every electrical cycle. Each time the gate is charged or discharged, the gate drive circuit will dissipate an amount of energy which is equal to the amount of energy supplied to the gate. This leads to the power lost due to the gate drive:

$$13)\ PL_{GD} = \frac{W_{GD}}{T} = \frac{Q_G \bullet V}{T} = Q_G \bullet V \bullet F = 110nC \bullet 20.5V \bullet 15kHz = 34mW$$

This is a worst case assumption since the power loss will actually be shared by the output driver and the gate resistor. In most cases there will be significant

sharing of this loss with the gate driver resistor since the output impedance of the driver stage is low. Because this calculation takes into account the total energy transferred to the gate, both switching loss and conduction loss are included.

To determine the power loss due to bias current, the total voltage drop of the UC3726N is subtracted from Vcc, and this result is multiplied by the bias current:

$$14)\ PL_{BIAS} = (30V - 2.3)(24mA) = 664mW$$

The resulting total power loss is calculated as:

$$15)\ PL_{TOT} = 0.034W + 0.664W = 0.698W$$

For a 20 pin plastic package (N package) the worst case θ_{JA} is 79°C/W for typical PC board mount, resulting in a temperature rise of 55°C. This leads to a maximum ambient temperature of 70°C for this application. Again, if it is desired to operate in a higher ambient, or to keep the junction temperature lower, heat sinking will be necessary.

TEST RESULTS

The UC3726/UC3727 IGBT Driver Pair Evaluation Board (See U-143C) was used to test the thermal characteristics of the driver pair. The evaluation board represents a typical PC board layout, where no heat sinking is provided except for a small copper ground plane. All electrical parameters for the circuit were programmed as described in U-143C. With a Vcc of 30V, and no external logic supply, driving the IGBT at 15kHz resulted in a lead temperature of 70°C for the UC3726N, and a case temperature of 47°C for the UC3727N. Assuming a θ_{JL} of 12°C/W for the UC3726N results in a junction temperature rise of 58°C, very close to the predicted rise.

Assuming a θ_{JC} of 35°C/W for the UC3727N results in a junction temperature rise of 46°C, which is significantly lower than the predicted value, indicating that the IC is dissipating less power than predicted. While this is a positive development in this case, it further points out the need to bread board circuits to prove out theoretical calculations.

Using an external +5V logic supply resulted in a lead temperature of 57°C for the UC3726N, and as expected had no effect on the case temperature of the UC3727N. The corresponding temperature rise of the UC3726N junction is 42°C. This difference in temperature rise of 16°C can be highly significant depending on the application.

As stated previously, properly heat sinking the ICs will result in much lower junction temperatures. While this technique leads to additional cost and complexity, it can lead to much greater design flexibility, particularly for driving IGBTs with very high levels of gate charge. Also, since the UC3726N features a "batwing" style package, heat is very effectively conducted to the center leads. Increasing the ground plane connected to these leads beyond what is shown on Figure 17 of U-143C will further reduce the junction temperature.

If other IC packages are used than those described in this design note, the power loss and maximum junction temperature calculations are the same. Refer to Packaging Section of the Unitrode Product and Applications Handbook for thermal impedance data.

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Design Note

UCC3912 Programmable Electronic Circuit Breaker – Performance Evaluation and Programming Information

by Bill Andreycak

The UCC3912 Demonstration Kit will enable designers to evaluate the performance of The UCC3912 Electronic Circuit Breaker in a typical application circuit. This kit features a number of programming options which include : individual "Hot Swap" of input and output connections, maximum current, Fault current level, and Shutdown. Each of these is programmed via switches located on the board. An LED indicates when the Current Fault Level comparator has been triggered and the device is in a low duty cycle mode.

List of switches, connections and functions:

SWITCH	CONNECTION (IC pin #)	FUNCTION
SW1	V_{IN} (2,3)	"Hot Swapping" of the input supply
SW2	V_{OUT} (14,15)	"Hot Swapping" of the output supply
SW3-1	I_{MAX} (10)	Sets maximum current level
SW3-3	B_3 (6)	Current Limit DAC Bit#3 input
SW3-4	B_2 (7)	Current Limit DAC Bit#2 input
SW3-5	B_1 (8)	Current Limit DAC Bit#1 input
SW3-6	B_0 (9)	Current Limit DAC Bit#0 input
SW3-8	Shutdown (1)	Shutdown input to disable IC

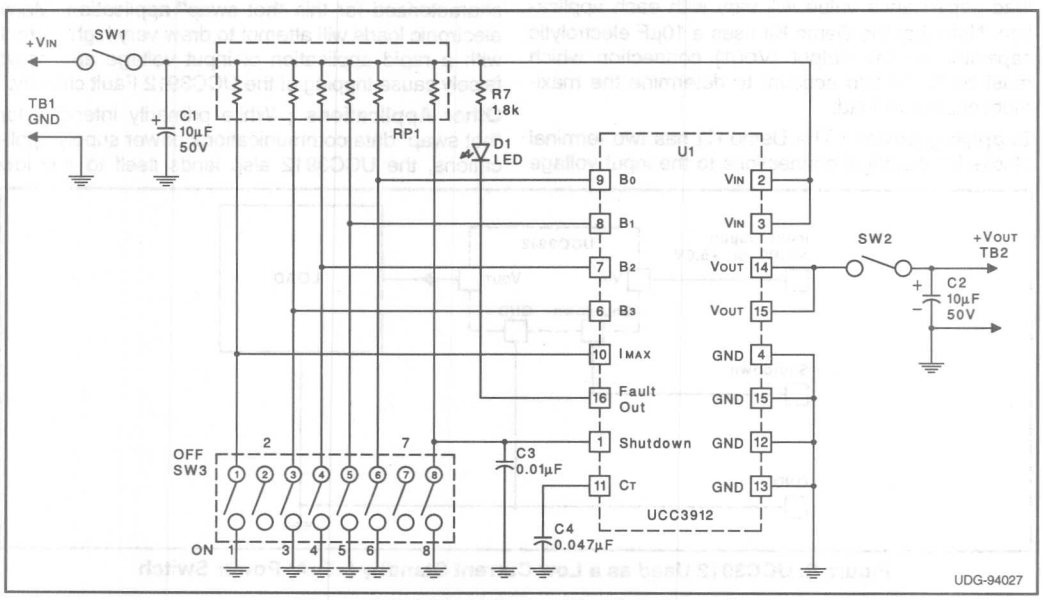


Figure 1. UCC3912 Demo Circuit Schematic

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Programming the switches : Switch SW3 is a standard eight position DIP switch, but only six of these provide programming functions. The two switches located at positions 2 and 7 (SW3-2, SW3-7) are not used. Moving the switches toward the corresponding switch position number, or the "ON" direction GROUNDS the input and provides a digital "low", or zero. A digital "high" input is provided when the switches are in the "OFF" position, or facing towards switches SW1 and SW2.

Timing functions : The UCC3912 Demo Kit incorporates a 0.047 microfarad timing capacitor to provide fault protection. Using the equations found in the device's datasheet, the actual timing intervals can be determined by:

$FAULT = C_T \bullet 28 \bullet 10^3 = 1.3 \text{ milliseconds}$

$T_{SHUTDOWN} = C_T \bullet 10^6 = 47 \text{ milliseconds}$

The exact duty cycle during a fault condition is :

$$\text{duty cycle} = \frac{FAULT}{T_{SHUTDOWN}} = \frac{1.3ms}{47ms} = 2.8\%(typical)$$

Maximum load capacitance : The maximum load capacitance can also be calculated using the equations found in the UCC3912 datasheet. Since a wide range of maximum load currents, output voltages and timing capacitors can be used, the maximum load capacitance value will vary with each application. Note that the Demo Kit uses a 10µF electrolytic capacitor on the output (VOUT) connection which must be taken into account to determine the maximum capacitive load.

Supplying power : The Demo Kit has two terminal blocks for electrical connections to the input voltage supply and the output load. Terminal block TB1 is used for the input supply (VIN) and TB2 is used to connect the kit to an appropriate load. Observe the correct polarity (+/-) of the connections as indicated on the printed circuit board, or damage could result.

Input voltage range : 3 volts minimum to 8 volts maximum

Output load : An adjustable electronic load can be used to draw varying amplitudes of current through the UCC3912 Demo Kit. This type of load is much easier to use than fixed value power resistors to determine the exact current limiting threshold. One example of an adjustable electronic load is shown in Unitrode Design Note #DN-52 which can sink over 5 amps of DC current and dissipate over 35 Watts of heat without a fan. This design is adequate for comprehensive testing of the UCC3912 Demo Kit.

Output current range : 0 to 4 amps, 0 to 32 watts (approximate)

"Hot swap" testing should be performed using power resistors and/or capacitors to draw the specific load current and characteristics required. These should be placed across the Demo Kit output connections and testing performed by switching SW2 on and off while monitoring the load current and voltage. DO NOT USE AN ELECTRONIC LOAD unless it has been characterized for this "hot swap" application. Many electronic loads will attempt to draw very high current with a rapid application of input voltage and could falsely cause tripping of the UCC3912 Fault circuitry.

Other Applications : While primarily intended for "hot swap" data communications power supply applications, the UCC3912 also lends itself to any low

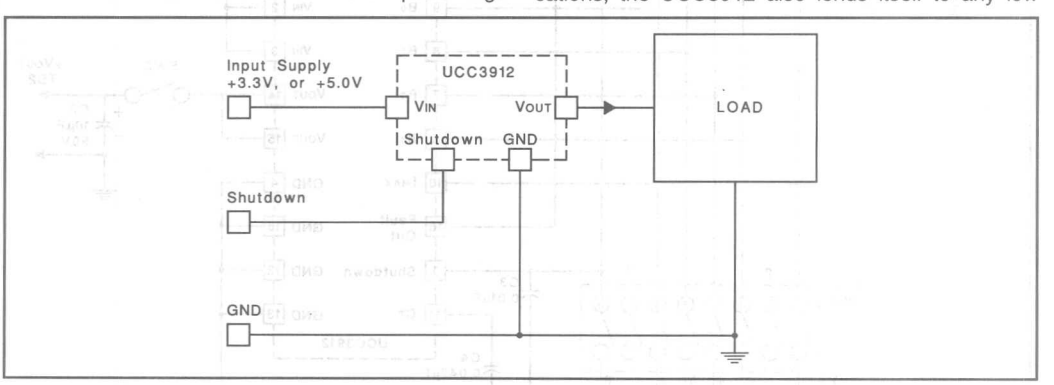


Figure 2. UCC3912 Used as a Low Current Standby (<5µA) Power Switch

voltage circuit breaker or protection application below 4 amps. Some of these include battery powered tools and equipment, PCMCIA card power switching and many 3.0V, 3.3V and 5.0 volt power supplies.

Summary: The features of the UCC3912 Electronic Circuit Breaker offer design flexibility and programmable maximum current protection for a wide variety of power applications including : data communications, computer, battery powered and portable equipment, PCMCIA card power, industrial controls and many low voltage power supplies.

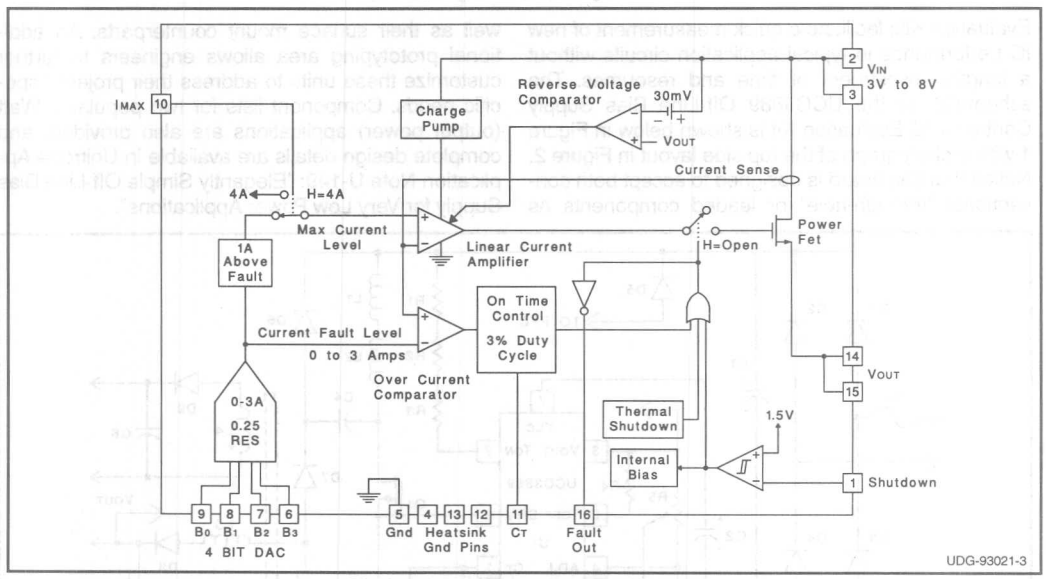


Figure 3. UCC3912 Block Diagram

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Design Note

UCC3889 Bias Supply Controller Evaluation Kit – Schematic and Lists of Materials

by Bill Andreycak

Evaluation Kits facilitate a quick measurement of new IC performance in typical application circuits without a lengthy investment of time and resources. The schematic for the UCC3889 Off-Line Bias Supply Controller IC Evaluation Kit is shown below in Figure 1 with a photograph of the top side layout in Figure 2. Notice that this board is designed to accept both conventional "through-hole" or leaded components as well as their surface mount counterparts. An additional prototyping area allows engineers to further customize these units to address their projects' specific needs. Component lists for two popular 1 Watt (output power) applications are also provided, and complete design details are available in Unitrode Application Note U-149: "Elegantly Simple Off-Line Bias Supply for Very Low Power Applications".

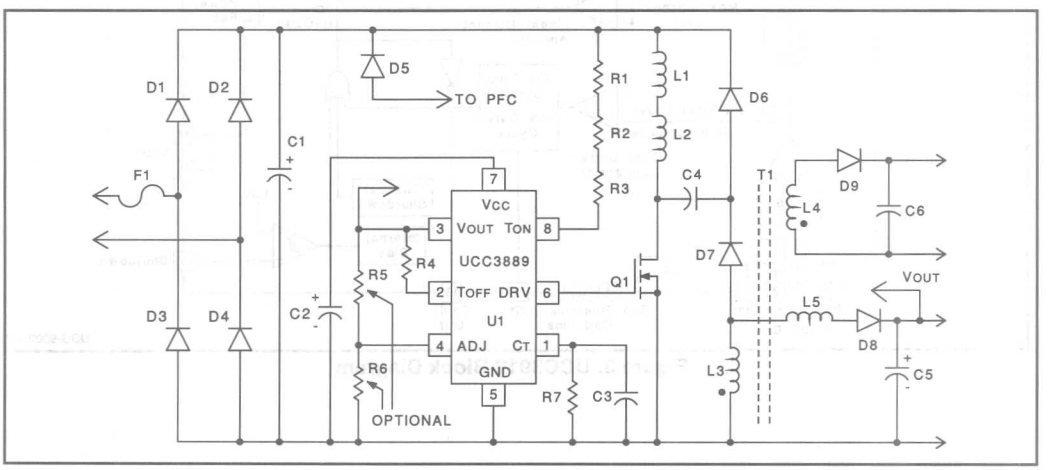


Figure 1. UCC3889 Evaluation Kit Schematic

Nonisolated 85 to 265VAC Universal Input, 12VDC / 1 Watt Converter

C1 = 2.2µF/450 VDC Electrolytic
C2 = 2.2µF/35 VDC Electrolytic
C3 = 150pF/16 VDC Ceramic Disc
C4 = 0.1µF/100 VDC Polyester foil
C5 = 33µF/25VDC Electrolytic (low ESR)
D1-D4 = 1A/800V Rectifier (1N4006)
D6,D7 = 1A/600V Fast Recovery Rectifier (1N4937)
D8 = 1A/200VDC Fast Recovery Rectifier (1N4935)
F1 = 0.2 ADC/250VAC Fuse
L1,L2 = 1mH (each) Inductor, 200 mA peak, 250 VDC rating
L3 = 390µH Inductor, 250mA peak
L5 = Jumper Wire, AWG#20 (short circuit)
Q1 = 600V/2A MOSFET, (MTP1N60 or IRFBC10)
R1,2,3 = 110k, 1/2W, 5%, 150VDC rating each (three used)
R4 = 150k, 1/4W, 5%
R7 = 2 Meg, 1/4W, 5%
U1 = UCC3889 Control IC

Components **NOT USED** in this design:
C6, D5, D9, L4, R5, R6

Optional component list:
D5 = 1A/800V DIODE (1N4006) - used with DC input from PFC or UPS
R5,R6 = 1/4W, 5% resistors - used to program other output voltages

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Transformer Isolated 85 to 265VAC Universal Input, 12VDC / 1 Watt Converter

C1 = 2.2µF/450 VDC Electrolytic
C2 = 1µF/35 VDC Electrolytic
C3 = 150pF/16 VDC Ceramic
C4 = 0.1µF/150 VDC Polyester foil
C5,6 = 33µF/25VDC Electrolytic (low ESR)
D1-4 = 1A/800V Rectifier (1N4006)
D6,7 = 1A/600V Fast Recovery Rectifier (1N4937)
D8,9 = 1A/200VDC Fast Recovery Rectifier (1N4935)
F1 = 0.2ADC/250VAC Fuse
L1,2 = 1mH (each) Inductor, 200mA peak, 250VDC rating
L4 = Transformer; 1:1 Turns ratio, 300µH (Coilcraft # E3497A)
L5 = 10µH, 750mA peak
Q1 = 600V/2A MOSFET, (MTP1N60 or IRFBC10)
R1,2,3 = 110k, 1/2W, 5%, 150VDC rating each (three used)
R4 = 150k, 1/4W, 5%
R7 = 2 Meg, 1/4W, 5%
U1 = UCC3889 CONTROL IC

Components **NOT USED** in this design:
D5, L3, R5, R6

Optional component list:
D5 = 1A/800V DIODE (1N4006) - used with DC input from PFC or UPS
R5,R6 = 1/4W, 5% resistors - used to program other output voltages

Note that the control technique and cascade Flyback configuration used in these examples can be extended to higher power levels and a variety of applications. This is accomplished by selecting the converter's power components accordingly. Higher current ratings for the power MOSFET, rectifiers and inductors, along with lower inductance values are usually all that's required. Other topologies, for example, the simple (non-cascaded) flyback, forward and boost converters can be controlled by the UCC3889 IC. Many distributed DC power and DC to DC converters make likely candidates for this control technique. Power Factor Correction (PFC) can also be achieved with this IC when used in a discontinuous inductor current boost configuration. Consult Unitrode Application Note U-132 for information on the controlled on-time, variable off-time PFC control technique which can be implemented with the UCC3889 without the need for current sensing. For further information, contact a local Unitrode representative or Field Application Engineer.

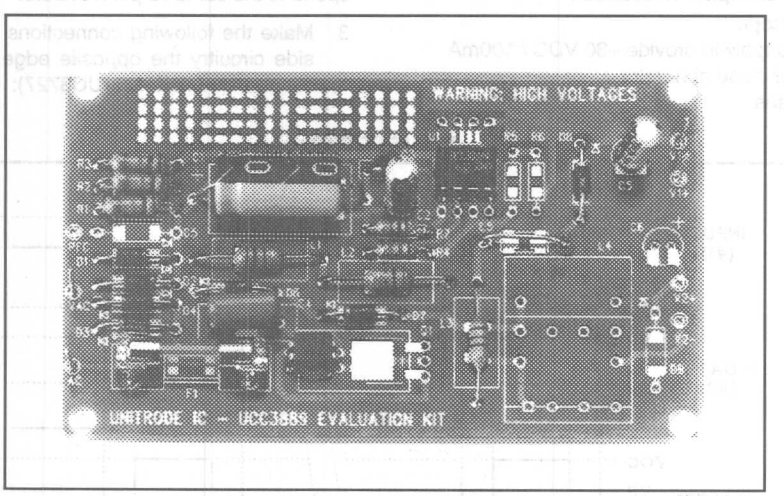


Figure 2. Top Side PC Board Photo

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Design Note

UC3726 / UC3727 IGBT Isolated Driver Pair Evaluation Kit Testing Procedure

by : Bill Andreycak

The UC3726/UC3727 IGBT isolated driver pair evaluation kit is available for design engineers to verify the performance and functionality of this unique solution for isolated gate drive applications. Also relevant are datasheets for each IC and Unitrode Application Note U-143A describing each device's features, operation, programming and operational waveforms. A copy of Design Guide DG-200A containing Design Note DN-57 which addresses power dissipation issues, and a simplified test procedure for the evaluation kit is also beneficial. Users should take the time to familiarize themselves with the numerous performance features and fault protection options available with these devices for a variety of applications. This general Testing Procedure is usable for the UC3726/UC3727 Evaluation Kit as well as for debugging any prototype circuits or first run printed circuit boards. Refer to Figure 15 of Application Note U-143A for a complete circuit schematic and Table 1 for the List of Materials.

Laboratory Equipment Needed :

Oscilloscope
Power Supply to provide +30 VDC / 100mA
Signal or pulse generator
Test Leads

Laboratory Test Procedure

** Turn off all equipment prior to making any connections and verify that there is a single electrical ground connected to "earth" ground for all equipment.

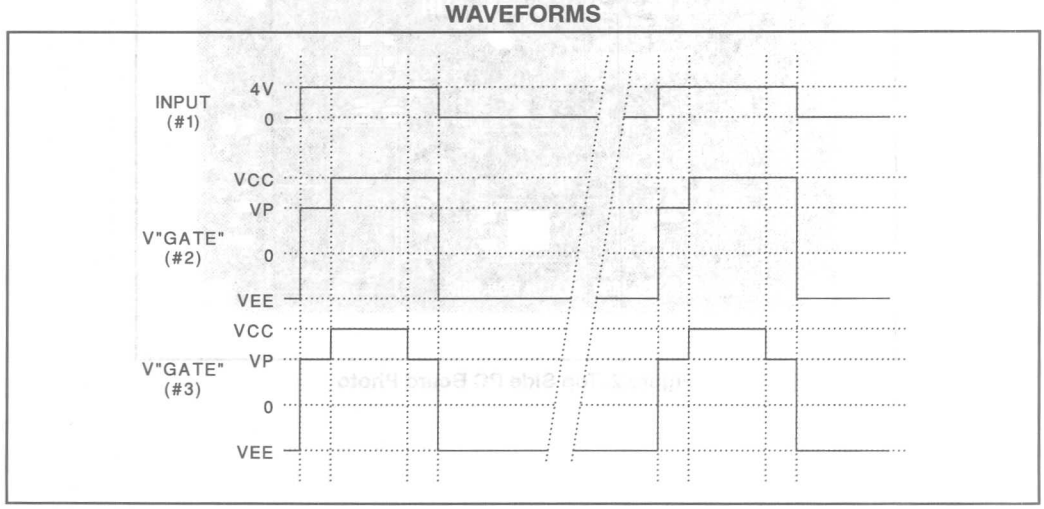
1. Configure the pulse generator to output a square wave pulse train with an amplitude of 4VDC at a frequency of 10kHz and a duty cycle of 10% (10ms on-time). See waveform #1 for reference.
2. Make the following connections to the 8 pin header connector near U1 (UC3726):

Signal	Connector Pin
+30VDC	7
Ground (return)	8
Pulse generator (+) output	4
Pulse generator (-) output (GND)	8

* Note that the header pin numbers do NOT correspond to the same IC pin numbers.

3. Make the following connections to the isolated side circuitry the opposite edge of the printed circuit board near U2 (UC3727):

WAVEFORMS



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A. Connect the "COLLECTOR" pin to the "EMITTER" pin using a jumper wire with clip leads.

B. Connect the "EMITTER" pin to the ground connection at pin 8 of the header near U1.

C. Connect the oscilloscope ground to circuit ground at the 8 pin header, pin 8.

D. Connect the oscilloscope probe to the "GATE" pin near U2.

Testing Procedure

1. Apply +30 VDC power to the evaluation kit
2. Turn ON the pulse generator
3. Verify Waveform #2 on the scope at the "GATE" pin.
4. Remove the test clip connection from the "COLLECTOR" pin
5. Verify Waveform #3 on the scope at the "GATE" pin.
6. Slowly increase the on-time (duty cycle) of the pulse generator until the "GATE" waveform latches off and remains at approximately –9VDC.
7. Reconnect the test lead to the "COLLECTOR" pin (from the "EMITTER")
8. Verify that the "GATE" waveform remains at approximately –9VDC.
9. Reduce the on-time (duty cycle) of the pulse generator back to 10µsec (10%).
10. Briefly connect header pins 6 and 2 (Vlogic to Freset)
11. Verify Waveform #2 on the scope at the "GATE" pin.

This concludes the basic testing of the UC3726/ UC3727 IGBT Evaluation Kit through verification of the gate drive waveforms. Verify isolation between the "low" and "high" side of the evaluation kit before testing in an isolated application circuit. Beware of ground loops and nonisolated power source. Whenever in doubt, use a low current (<1/4A) fuse in series with any test leads or equipment ground connections to prevent damage. The fuse will blow with any current flowing due to the attempted connections being nonisolated. Observe proper safety precautions as high voltage may be present in many IGBT applications. For complete operational details of the ICs, please refer to the datasheets and Applications literature.

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Design Note

A High Performance Linear Regulator for Low Dropout Applications

by: Dave Zendzian

Introduction

Today's microprocessors are placing ever greater demands upon power system design. Most state of the art devices now require a 3.3V bus and therefore necessitate some means of stepping down and regulating the existing 5V system supply. To complicate matters further, the performance of these devices is directly related to supply voltage. This results in a need for tight regulation and excellent transient response if the maximum potential of the processor is to be realized. As of late, the trend has been to implement the function using a switching regulator, primarily due to the high efficiencies obtainable with this topology. However, when the difference between input and output voltage is low, the efficiency advantage of the switcher is no longer as great. A linear regulator design offers several desirable features including low output noise and wide bandwidth resulting in excellent transient load response.

This design note presents a linear regulator capable of maximizing the performance of these digital systems. The regulator is designed to meet the following system requirements:

V_{IN} = 5V, ±10%
V_{OUT} = 3.3V, ±5%
I_{OUT} = 3.5A typical, 4A maximum

Transient Response:
5% to 75% I_{OUTmax} in 100nsec, V_{REG} = ±5%

Topology Review

The regulator is implemented using a UC3833, precision linear controller. This IC includes all of the functions required to design a very low dropout, precision regulator, including a 1% reference, error amplifier and an uncommitted output stage. Providing a driver with both source and sink capabilities allows the use of a variety of power devices including NPN or PNP bipolar devices and N or P-channel MOSFETs. An innovative, switchmode current limiting technique is also implemented by the UC3833, significantly reducing power dissipation during fault conditions.

The crux of the design lies in the selection of a pass device. Requirements for the selected power device include operation under very low input/output differential voltages while still providing reasonable efficiency. Traditionally the PNP bipolar transistor has been applied in low dropout applications, primarily due to its low saturation voltage compared to a Darlington and simpler base drive than an NPN configuration. However, the gain of these devices is typically quite low, resulting in the need for significant base drive current. As the output requirements of the regulator increase the base current losses quickly become excessive, thereby decreasing the efficiency, along with the advantages of the linear regulator.

This leaves the P-channel MOSFET as the most likely candidate. While older generation P-channel devices are plagued with high on-resistance, recent advancements in high cell density technology have led to substantial reductions in R_{DSon}. Motorola's new HDTMOS devices boast 50% lower on-resistance than the previous generation of P-channel devices. The MTP50P03HDL is a 50A, 30V, logic level P-channel device with a maximum on-resistance of only 30mΩ. The maximum gate threshold voltage of 2.0V is necessary due to the 5V input requirement of this application. An additional advantage of the MOSFET power stage is the minimum amount of drive current required. Since the device is voltage controlled and operating in transconductance mode it can be biased with minimal drive current, further improving the efficiency of the regulator.

Bulk output capacitance is added to the design in order to help meet the 100nsec load transient requirement. As with any control system, the voltage loop has a finite bandwidth and cannot instantaneously respond to a change in load conditions. In order to keep the output voltage within the specified tolerance, sufficient capacitance must be provided to source the increased load current throughout the initial portion of the transient period. During this time charge is removed from the capacitor and its

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voltage correspondingly decreases until the control loop can catch the error and correct for the increased load. The amount of capacitance used must be enough to keep the voltage drop within specification according to the charge relationship I = CdV/dt. Unfortunately, the equivalent series resistance (ESR) and inductance (ESL) of the capacitor generate an additional voltage transient, the total of which must be kept within specification. In order to limit this transient, the ESR and ESL of the selected devices will usually dictate a much larger value of capacitance than might normally be expected.

Design Details

Figure 1 illustrates the final design. Resistors R4 and R5 provide the bias for the pass transistor, Q1. By including emitter resistor R5, the UC3833 drive transistor's β is eliminated from the loop gain expression, thereby simplifying the compensation. Resistors R6 and R7 provide voltage feedback to the UC3833 while components R3, C2 and C3 compensate the voltage and current loops. Further compensation of the current loop is provided by the pole-zero pair introduced by R8, C7 and C8.

Current control is provided via the UC3833's internal amplifier and overcurrent comparator. When the voltage across R1 crosses the 100mV comparator threshold, the UC3833 begins to modulate the output driver. The duty cycle is approximately 5% with on and off-times set by timing components C1 and R2. During the on-time, the current sense amplifier provides constant output current by maintaining 135mV across R1. Duty cycle protection offers significant heat sinking advantages when compared to conventional, constant current solutions. Since the average power during a fault condition is reduced as a function of the duty cycle, the heat sink need only have adequate thermal mass to absorb the maximum steady state power dissipation, and not the full short circuit power.

Output capacitors were chosen based upon their ESR/ESL specifications and package style. The output capacitance is implemented using three surface mount, solid tantalum capacitors in parallel. This acts to reduce the equivalent ESR and ESL by 1/3, keeping the associated voltage transients within specification. Sprague 595D capacitors were used, providing an equivalent impedance of approximately 13mΩ typical and 60mΩ max at 100kHz. The surface mount package helps to further reduce the parasitic effects induced by component leads.

In order to achieve the expected performance, careful attention must be paid to circuit layout. The circuit should be laid out using a single point ground referenced to the return of the output capacitor. In addition, all high current carrying traces should be made as short and wide as possible in order to

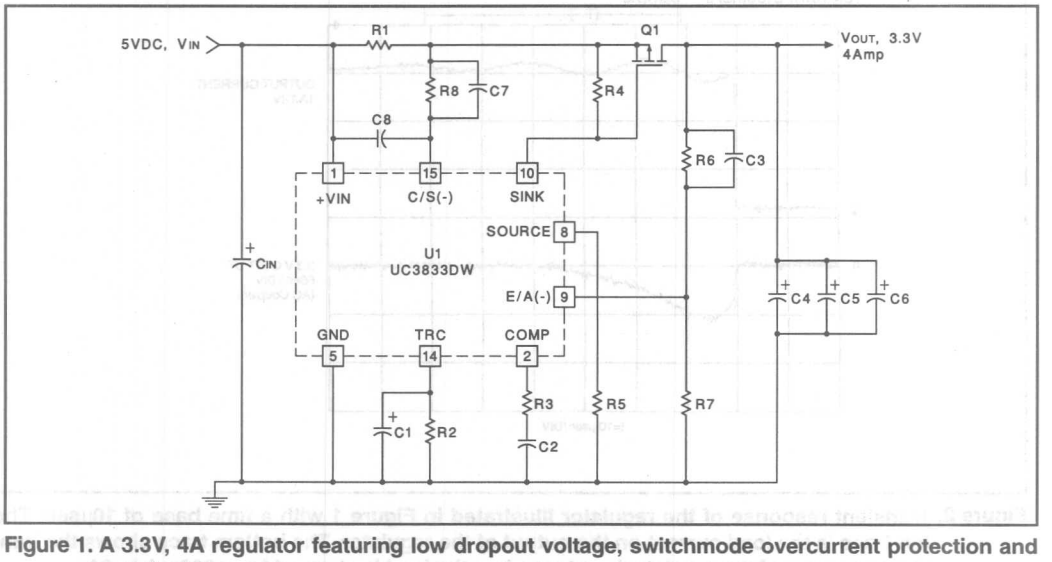


Figure 1. A 3.3V, 4A regulator featuring low dropout voltage, switchmode overcurrent protection and excellent transient response.

minimize the effects of parasitic resistance and inductance. To illustrate the importance of these concepts, lets examine the effect of a 1.5" PCB trace located between the output capacitor and the UC3833 ground reference. A 0.07" wide trace of 1oz. copper results in an equivalent resistance of 10.4mΩ. At a load current of 3A, 31.2mV is dropped across the trace, contributing almost 1% error to the DC regulation! Likewise, the inductance of the trace is approximately 3.24nH, resulting in a 91mV spike during the 100nsecs it takes the load current to slew from 200mA to 3A. Each of these effects can be minimized by optimizing the layout and using generous amounts of copper on all high current runs.

Thermal control is provided by heatsinking the power MOSFET pass device. Any heatsink of 7.5°C/W or lower will keep the junction temperature of the MOSFET below 125°C at ambient temperatures up to 50°C and worst case operating conditions.

Performance

In a typical application of 3A out with 5.0V in, the efficiency of the regulator is 65.5%. Under maximum load and worst case conditions the efficiency drops to 60%. During a short circuit, the regulator limits the peak output current to approximately 6A by design. At the 5% duty cycle set by C1 and R2, the average current is limited to 300mA, resulting in only 2W of power dissipated in the MOSFET as opposed to the potential dissipation of 32W in a constant current application!

Worst case DC regulation of ±3% is accomplished using the UC3833 in conjunction with 1% feedback resistors. If a tighter tolerance is required the UC3832 can be substituted for the UC3833 along with 0.1% resistors. The UC3832 includes provisions for an external voltage reference, allowing increased performance over the UC3833's 1% internal reference.

The AC characteristics of the voltage loop determine how fast the regulator can respond to sudden load disturbances. Figure 2 illustrates how the design behaves during the specified 100nsec load transient. Starting with 200mA of load current, a step change to 3A was applied to the regulator. This load current waveform is shown in the upper trace of Figure 2. Notice that in the lower trace, following the increase in load, the output drops approximately 50mV and then recovers to a stable state within 40μsec. Figure 3 shows the same response with a timebase expanded to 250nsec. In this plot

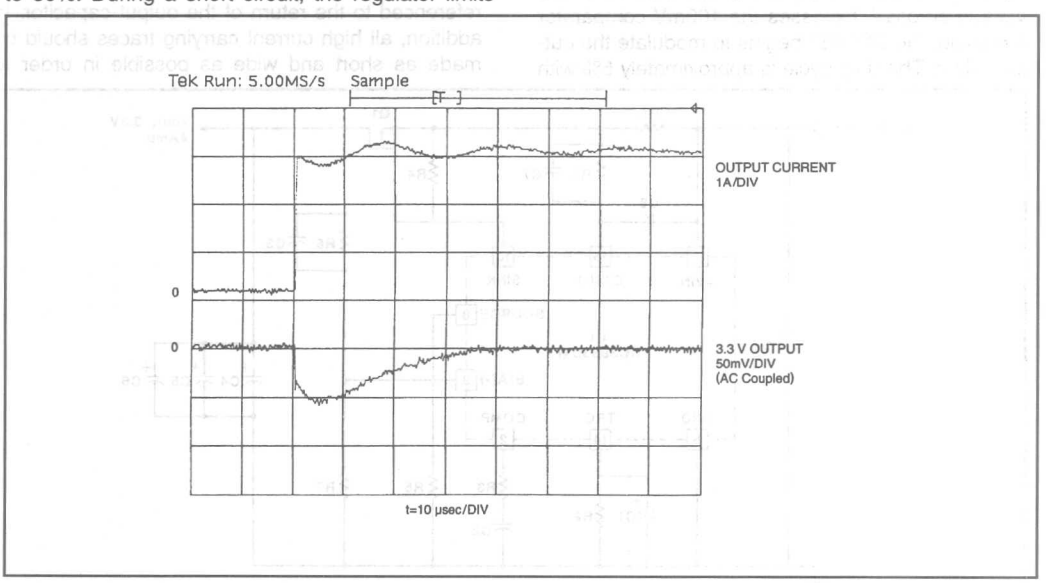


Figure 2. Transient response of the regulator illustrated in Figure 1 with a time base of 10μsec. The top trace is the load current on the output of the regulator. The bottom trace shows the transient recovery of the regulator's output when the load is stepped from 200mA to 3A.

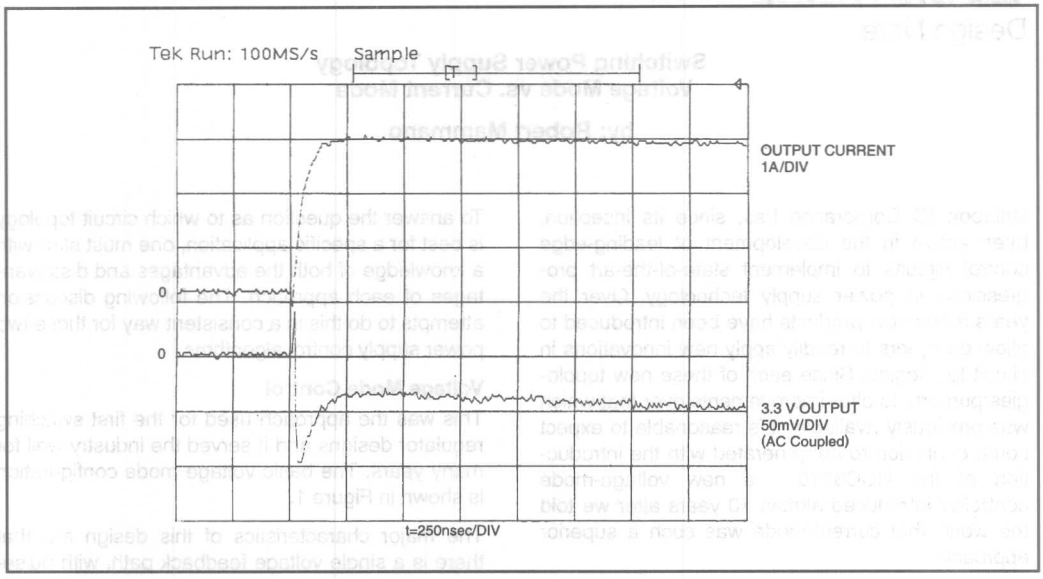


Figure 3. Transient response of the regulator illustrated in Figure 1 with a timebase of 250nsec. The top trace is the load current on the output of the regulator. The bottom trace shows the initial output transient resulting from the equivalent impedance of the output capacitor during a load step from 200mA to 3A.

the initial transient resulting from the equivalent impedance of the output capacitor is clearly visible. The parallel combination of the three output capacitors and careful layout limits the transient to roughly 100mV.

The circuit described in this design note can be easily modified to accommodate a variety of output voltage and current requirements. For additional information regarding the UC3832/3 linear controllers consult Unitrode application note U-116. Additional information on HDTMOS MOSFETs and low impedance capacitors is available from Motorola (602-244-3377) and Sprague (603-224-1961) respectively.

Parts List:

Resistors	Capacitors	Transistors	Integrated Circuits
R1 = 0.022Ω	C1,C8 = 1μF	Q1 = MTP50P03HDL	U1 = UC3833
R2 = 200k	C2,C3 = 0.1μF		
R3,R8 = 100Ω	C4,C5,C6 = 270μF		
R4 = 300Ω	C7 = 3300pF		
R5 = 20Ω			
R6 = 1.3k			
R7 = 2.0k			

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Design Note

Switching Power Supply Topology
Voltage Mode vs. Current Mode

by: Robert Mammano

Unitrode IC Corporation has, since its inception, been active in the development of leading-edge control circuits to implement state-of-the-art progressions in power supply technology. Over the years many new products have been introduced to allow designers to readily apply new innovations in circuit topologies. Since each of these new topologies purports to offer improvements over that which was previously available, it is reasonable to expect some confusion to be generated with the introduction of the UCC3570 - a new voltage-mode controller introduced almost 10 years after we told the world that current-mode was such a superior approach.

The truth, however, is that there is no single topology which is optimum for all applications. Moreover, voltage-mode control - if updated with modern circuit and process developments - has much to offer designers of today's high-performance supplies and is a viable contender for the power supply designer's attention.

To answer the question as to which circuit topology is best for a specific application, one must start with a knowledge of both the advantages and disadvantages of each approach. The following discussion attempts to do this in a consistent way for these two power supply control algorithms.

Voltage Mode Control

This was the approach used for the first switching regulator designs and it served the industry well for many years. The basic voltage mode configuration is shown in Figure 1.

The major characteristics of this design are that there is a single voltage feedback path, with pulse-width modulation performed by comparing the voltage error signal with a constant ramp waveform. Current limiting must be done separately.

The advantages of voltage-mode control are:

1. A single feedback loop is easier to design and analyze.

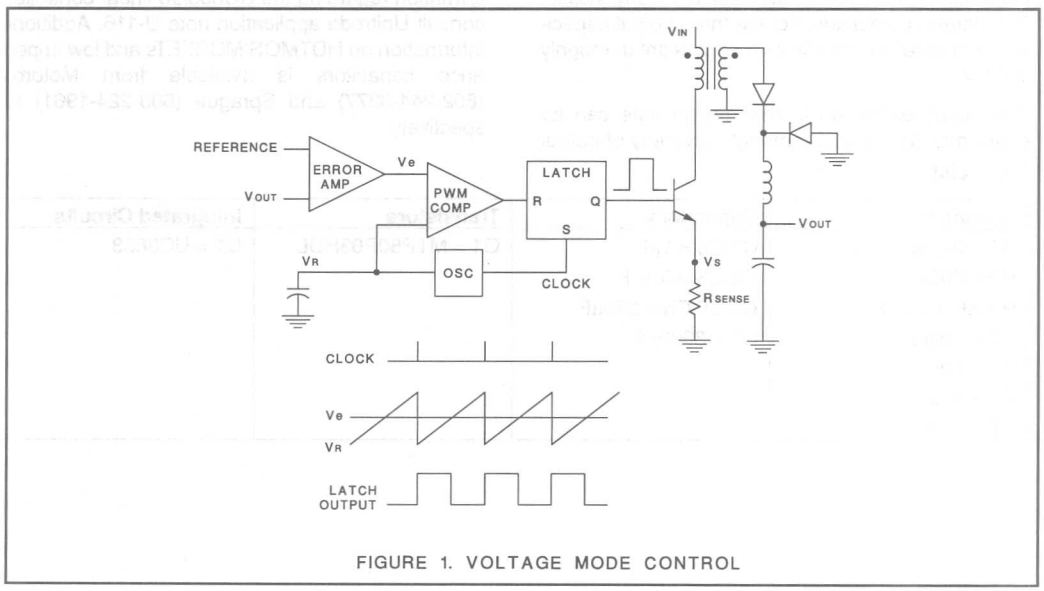


FIGURE 1. VOLTAGE MODE CONTROL

Figure 1. Voltage Mode Control

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2. A large-amplitude ramp waveform provides good noise margin for a stable modulation process.
3. A low-impedance power output provides better cross-regulation for multiple output supplies.

Voltage-mode's disadvantages can be listed as:

1. Any change in line or load must first be sensed as an output change and then corrected by the feedback loop. This usually means slow response.
2. The output filter adds two poles to the control loop requiring either a dominant-pole low frequency roll-off at the error amplifier or an added zero in the compensation.
3. Compensation is further complicated by the fact that the loop gain varies with input voltage.

Current Mode Control

The above disadvantages are relatively significant and since all are alleviated with current-mode control, designers were highly motivated to consider this topology upon its introduction. As can be seen from the diagram of Figure 2, basic current-mode control uses the oscillator only as a fixed-frequency clock and the ramp waveform is replaced with a signal derived from output inductor current.

The advantages which this control technique offers include the following:

1. Since inductor current rises with a slope determined by Vin-Vo, this waveform will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage.
2. Since the Error Amplifier is now used to command an output current rather than voltage, the effect of the output inductor is minimized and the filter now offers only a single pole to the feedback loop (at least in the normal region of interest). This allows both simpler compensation and a higher gain bandwidth over a comparable voltage-mode circuit.
3. Additional benefits with current-mode circuits include inherent pulse-by-pulse current limiting by merely clamping the command from the Error Amplifier, and the ease of providing load sharing when multiple power units are paralleled.

While the improvements offered by current-mode are impressive, this technology also comes with its own unique set of problems which must be solved in the design process. A listing of some of these is outlined below:

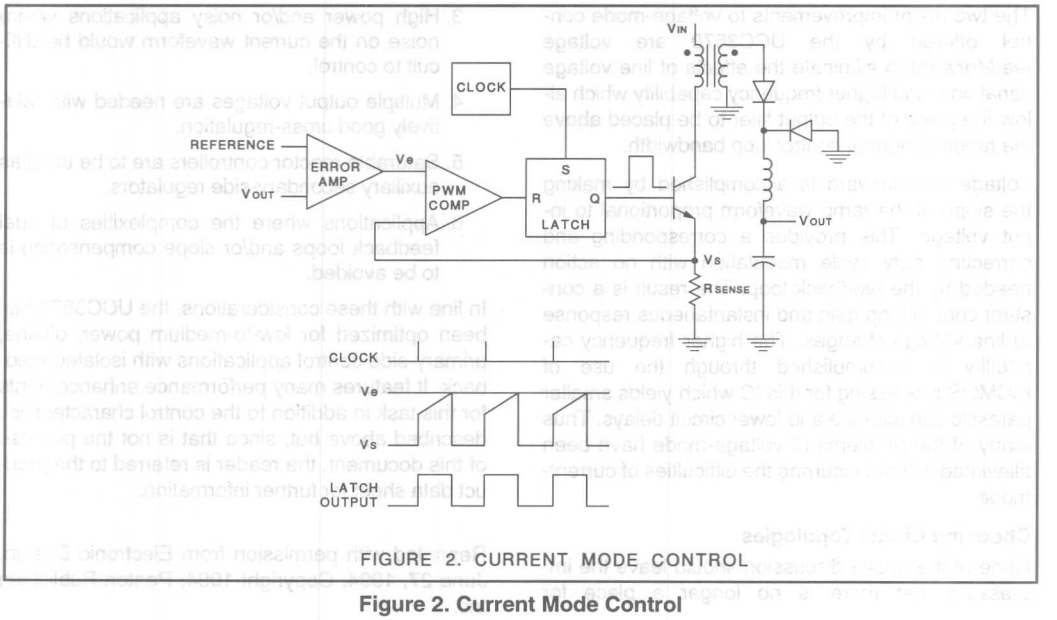


FIGURE 2. CURRENT MODE CONTROL

Figure 2. Current Mode Control

1. There are now two feedback loops, making circuit analysis more difficult.
2. The control loop becomes unstable at duty cycles above 50% unless slope compensation is added.
3. Since the control modulation is based on a signal derived from output current, resonances in the power stage can insert noise into the control loop.
4. A particularly troublesome noise source is the leading edge current spike typically caused by transformer winding capacitance and output rectifier recovery current.
5. With the control loop forcing a current drive, load regulation is worse and coupled inductors are required to get acceptable cross-regulation with multiple outputs.

So from the above we can conclude that while current-mode control will ease many of the limitations of voltage-mode, it also contributes a new set of challenges to the designer. However, with the knowledge gained from more recent developments in power control technology, a re-evaluation of voltage-mode control indicated that there were alternative ways to correct its major weaknesses and the result was the UCC3570.

Voltage-Mode Revisited

The two major improvements to voltage-mode control offered by the UCC3570 are voltage feed-forward to eliminate the effects of line voltage variations, and higher frequency capability which allow the poles of the output filter to be placed above the range of normal control loop bandwidth.

Voltage feed-forward is accomplished by making the slope of the ramp waveform proportional to input voltage. This provides a corresponding and correcting duty cycle modulation with no action needed by the feedback loop. The result is a constant control loop gain and instantaneous response to line voltage changes. The higher frequency capability is accomplished through the use of BiCMOS processing for this IC which yields smaller parasitic capacitance and lower circuit delays. Thus many of the problems of voltage-mode have been alleviated without incurring the difficulties of current-mode.

Choosing Circuit Topologies

None of the above discussion should leave the impression that there is no longer a place for current-mode control - only that both topologies are viable choices in today's environment. There are considerations which could point to one or the other as more optimum for each particular application. Some of these are outlined below:

Consider the use of current-mode if:

1. The power supply output is to be a current source or very high output voltage.
2. The fastest dynamic response is needed with a given switching frequency.
3. The application is for a DC/DC converter where the input voltage variation is relatively constrained.
4. Modular applications where parallelability with load sharing is required.
5. In push-pull circuits where transformer flux balancing is important.
6. In low-cost applications requiring the absolute fewest components.

Consider voltage-mode (with feed-forward) if:

1. There are wide input line and/or output load variations possible.
2. Particularly with low line - light load conditions where the current ramp slope is too shallow for stable PWM operation.
3. High power and/or noisy applications where noise on the current waveform would be difficult to control.
4. Multiple output voltages are needed with relatively good cross-regulation.
5. Saturable reactor controllers are to be used as auxiliary secondary-side regulators.
6. Applications where the complexities of dual feedback loops and/or slope compensation is to be avoided.

In line with these considerations, the UCC3570 has been optimized for low-to-medium power, off-line, primary-side control applications with isolated feedback. It features many performance enhancements for this task in addition to the control characteristics described above but, since that is not the purpose of this document, the reader is referred to the product data sheet for further information.

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The Current-Doubler Rectifier: An Alternative Rectification Technique For Push-Pull And Bridge Converters

by Laszlo Balogh

This design note describes an alternative rectification method which offers simpler structure and better utilization of the isolation transformers in push-pull, half-bridge and bridge power stages where usually full-wave rectification is required on the secondary side of the transformers. Converters using the current-doubler rectifier can achieve lower and better distributed power dissipation and smaller size in the magnetic components.

The common property of the push-pull, half-bridge and bridge topologies which makes the full-wave rectification necessary is that they utilize bipolar voltage across the secondary side of the transformer.

Figure 1 illustrates the commonly used circuit arrangement for full-wave rectification. For proper operation the secondary winding has to be center-tapped with one terminal connected to the reference potential (ground) of the circuit. The center-tapping splits the secondary winding into two inductors which are coupled strongly but not perfectly within one magnetic structure.

This design note assumes a full-bridge power converter using the phase-shifted control method. Consequently, the primary of the isolation transformer is short circuited in the free-wheeling mode which has a profound effect on the current distribution in the secondary windings during that period. In all other aspects, the operation of the push-pull, half-bridge and the conventional full-bridge converters are identical to the description below.

Based on the polarities and signal names of Figure 1, operation is as follows:

During the first active period when energy is transferred from the primary to the secondary side, the voltage across TR1 is positive. D1 is forward biased while the negative voltage appearing across TR2 keeps D2 reverse biased. The current of the output inductor, LO, is forced to flow through TR1 while TR2 carries no current. During the free-wheeling period, the voltages across TR1 and TR2 become zero. In theory the output current is evenly distributed between the secondary windings TR1 and TR2. In practice, because of leakage inductance

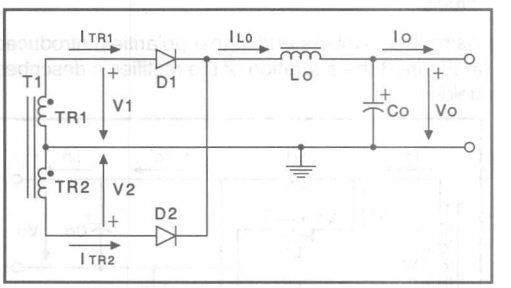


Figure 1. Full-Wave Rectifier

associated with real magnetic structures, the output current is not shared evenly. TR1 still conducts most of the output inductor current while the current slowly builds up in TR2 depending on the value of the leakage inductance and the available voltage across it. In the next active interval, V2 is positive, in which case TR2 and D2 carries all the current of LO while D1 is reverse biased by TR1 having no current through them. In the next period V1 and V2 are zero again and similarly to the previous free-wheeling period the output inductor current will keep flowing in TR2.

Figure 2 shows the most important waveforms of operation.

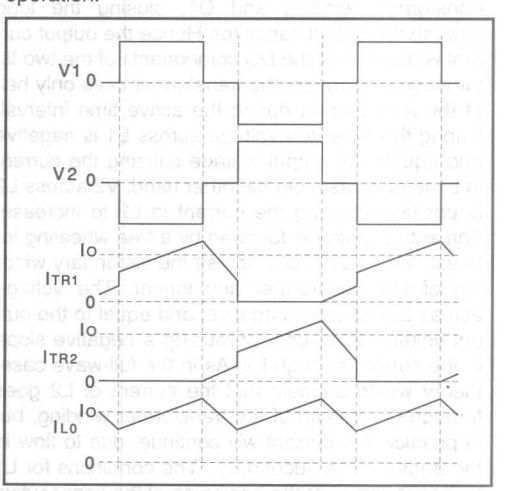


Figure 2. Waveforms of the Full-Wave Rectifier

The proposed current-doubler rectifier is presented in Figure 3. It is composed of the secondary winding of the isolation transformer which is not center-tapped now, the same two rectifier diodes, two individual but identical filter inductors and an equal output capacitor to the one of the full-wave rectifier circuit.

Using the symbols and signal polarities introduced in Figure 3 the operation of the rectifier is described below:

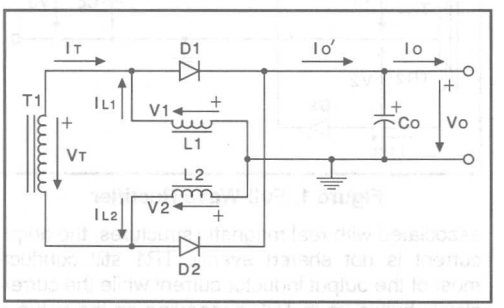


Figure 3. Current-Doubler Rectifier

Starting at the first active period the voltage across the secondary winding of the transformer, V_T is positive. Current flows in positive direction in both filter inductors, L1 and L2. During this period D1 is forward biased while D2 is kept off by V_T. It means that the current path for L1 runs through D1 and the output capacitor, basically kept away from the secondary winding of the transformer. The current of the second filter inductor L2 flows through the transformer winding and D1, closing the loop through the output capacitor. Hence the output current is the sum of the DC components of the two filter inductor currents, the transformer sees only half of the load current during the active time interval. During this time, the voltage across L1 is negative and equals the output voltage causing the current in L1 to decrease. On the other hand, V2 across L2 is positive, causing the current in L2 to increase. The active period is followed by a free-wheeling interval. V_T is not forced across the secondary winding of the transformer any longer. The voltage across L2 becomes negative, and equal to the output voltage amplitude, producing a negative slope in the current through L2. As in the full-wave case, theory would suggest that the current of L2 goes through D2 instead of the transformer winding, but in practice this current will continue, due to flow in the transformers secondary. The conditions for L1 do not change. At the beginning of the consecutive active interval, a negative voltage appears on the output of the transformer. D1 turns off while D2 is forward biased. The current rapidly changes direction in the transformer winding, and is equal to the current of L1. The current of L2 is not flowing through the transformer any longer and keeps decreasing by the rate determined by the inductance value and the output voltage. Having a positive voltage across L1, the current starts building up in the inductor. The full operating cycle is completed by another free-wheeling period when V_T becomes zero, $-V_O$ appears on L1 causing its current to decrease and there is no change in the condition of L2.

The essential waveforms of the current-doubler rectifier are indicated in Figure 4.

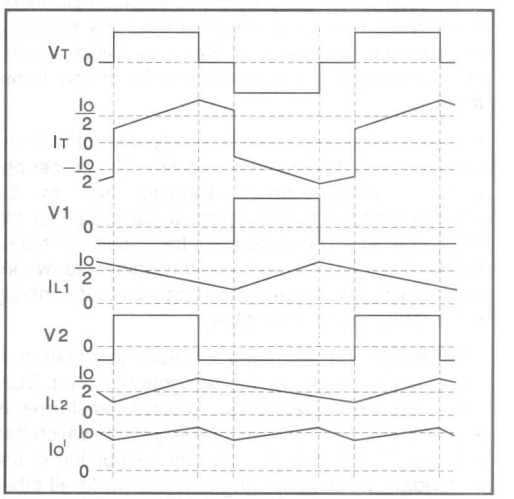


Figure 4. Waveforms of the Current Doubler Rectifier

Summarizing the most important properties of the current-doubler rectifier as revealed by the circuit diagram, the description of operation and the different waveforms, the following conclusions can be drawn:

- there is no need for center-tapping
- finer steps in turns ratio are possible
- transformer structure is simpler
- transformer carries approximately half of the output current (only the secondary winding)
- operation on the primary side, including duty-cycle is unchanged

- diode and output capacitor stresses are identical to the full-wave technique
- additional filter inductor required
- each filter inductor carries only half of the DC output current
- ripple currents cancel on common output capacitor
- requires current-mode control to ensure equal currents in the filter inductors

In order to correctly judge the merit of this rectification technique for practical applications, a quantitative comparison is presented. Assume, that two converters operate with a clock frequency of fs, have the same input and output voltages, equal load currents and equal ripple currents in the output capacitors. For these cases, the most important design parameters are given in an easy to use form in Table 1. For simplicity, the current values are not reflecting the effect of the AC components of the inductor currents.

Table 1. Comparison of Full-Wave and Current-Doubler Rectifiers

Technique >	**Full-Wave**			**Current-Doubler**		
Magnetics>	**TR1**	**TR2**	**Lo**	**Tr**	**L1**	**L2**
Transformer Operating Frequency	$\frac{fs}{2}$			$\frac{fs}{2}$		
Transformer Primary Number of Turns	N			N		
Transformer Secondary Number of Turns	1	1	-	2	-	-
Transformer Secondary Current (DC average; multiplier is the duty-cycle of the secondaries)	$Io \bullet 0.5$	$Io \bullet 0.5$	-	$\frac{Io}{2} \bullet 1$	-	-
Secondary current reflected to the primary (DC average)	$Io \bullet \frac{1}{N} \bullet D$			$\frac{Io}{2} \bullet \frac{2}{N} \bullet D$		
D1; D2 Breakdown Voltage (minimum)	$V_{IN} \bullet \frac{1+1}{N}$			$V_{IN} \bullet \frac{2}{N}$		
Output Inductor Operating Frequency	-	-	fs	-	$\frac{fs}{2}$	$\frac{fs}{2}$
Output Inductor Current (DC Average)	-	-	Io	-	$\frac{Io}{2}$	$\frac{Io}{2}$
Output Inductance (minimum) ** function of duty-cycle*	-	-	Lo	-	≤Lo*	≤Lo*

Summary: the presented current-doubler rectifier provides an alternative rectification technique for converters employing push-pull, half-bridge or bridge topologies. The method simplifies the power transformer and adds one more filter inductor to the circuit. Depending on the particular application, the total volume of the two filter inductors might be equal or smaller than the choke of the full-wave rectifier due to their lower operating frequency and lower current rating.

Further trade-offs can be made in order to reduce inductor sizes by lowering the inductance value and relying more strongly on the ripple current cancellation of the two inductors. Additionally, the current-doubler rectifier offers the potential benefit of better distributed power dissipation which might become a vital benefit in densely packed power supplies. Because of its added circuit complexity, this solution could probably be justified in medium to higher power and/or high output current applications.

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Design Note

Inductorless Bias Supply Design for Synchronous Rectification and High Side Drive Applications

by Bill Andreycak

Developing a bias supply which is higher than a power supply's input voltage is usually required in high side switch applications. Two such examples are Buck regulators and Synchronous Switch converters using N-channel MOSFETs as the switching device. Independent of the specific application, there are numerous requirements for cost effective bias supplies without the added complexity of inductors, switches, transformer windings or even an independent power supply. The circuit shown in Figure 1 exemplifies the need in a transformer coupled, Synchronous Switch application in a Forward converter.

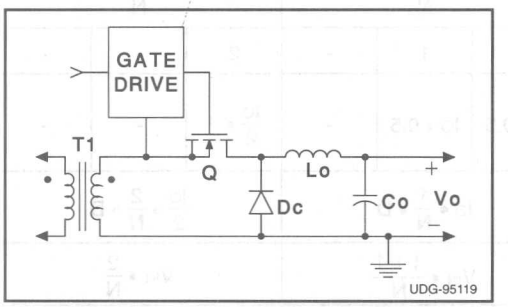


Figure 1. Synchronous Switch

A number of more demanding applications than the conventional Synchronous Switch examples exist, all with similar high side bias supply needs. For example, adding an overcurrent limit or circuit breaker function to the output will require a more sophisticated detection and gate drive circuit than the previous examples. A further extension would be the need to completely regulate the output voltage by pulse width modulating the switch. Note, however, that each of these will require the MOSFET switch to be "reversed" from that found in the Synchronous Switch example. This is necessary so that the MOSFET body diode does not always conduct while the input is greater than the output voltage. With this adaptation, its "channel" can be switched "on" to perform rectification only when required. Furthermore, this allows for the gate drive to be pulse width modulated to regulate the output voltage or to control output current. A diode, placed in series with the switch is required to prevent the MOSFET body diode from conducting when the transformer secondary voltage reverses. The basic circuit is shown in Figure 2.

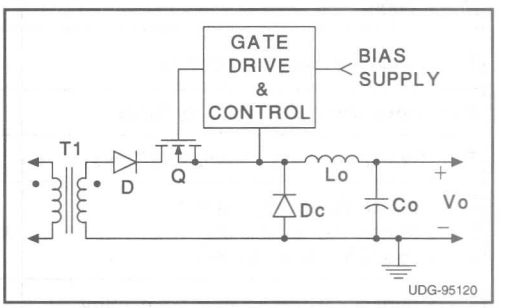


Figure 2. Controlled Switch with Series Diode

One problem with the configuration shown in Figure 2 is that the control circuit is "floating" and all control signals will require isolation which adds unnecessary complexity. An improved arrangement, shown in Figure 3, references the control circuit and gate drive to the supply's positive output rail. Note that the output filter stage consisting of the commutating diode (Dc), output filter capacitor (Co) and output inductor (Lo) has been reconfigured yet performs the same task. For simplicity, the output inductor has been moved to the lower (return) rail for two reasons. First, it enables the gate drive and control circuitry to be solidly referenced to the positive output voltage. Secondly, it eliminates the need for a "floating" gate drive which would have been required if the inductor were left in the positive output rail. Additional noise immunity in the control logic is generally gained with this configuration since its

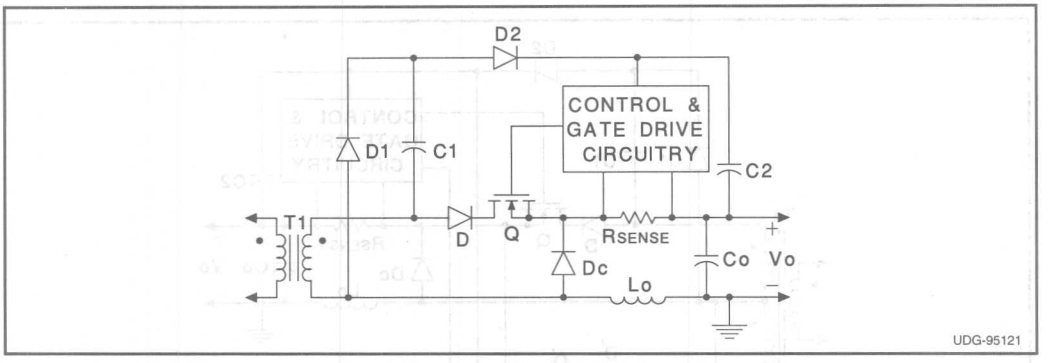


Figure 3. Improved Circuit Configuration

common mode range is reduced. Note that a direct measurement of output current is also available for overcurrent protection purposes or current mode control by using a sense resistor in series with the positive output.

Operation of the basic charge pump circuitry used to develop the high side bias is as follows. The sequence begins at turn-off of the main power supply switch on the transformer's primary side which causes the secondary voltage waveform to collapse. Power is transferred to the bias supply during the transformer's resetting or "backstroke". As the voltage across the secondary winding reverses, capacitor C1 is charged through diode D1 to the peak amplitude of the secondary reset voltage. Note that these components are "isolated" from the bias supply capacitor (C2) by diode D2 while C1 swings below the positive output rail and charges. During the normal transfer of power to the output stage the secondary transformer voltage is positive. As this occurs, Diode D1 is reversed biased and turns off while capacitor C1 is lifted along with the positive secondary transformer voltage. When the voltage across capacitor C1 exceeds that across the bias supply capacitor (C2), diode D2 conducts. Note that this takes place whether or not the power switch and diode are conducting. Charge stored in C1 is delivered to C2 beginning with the rise of secondary transformer voltage, replenishing C2. Eventually, diode D2 will discontinue conducting as C1's voltage drops below that of C2. The entire cycle is repeated beginning at the reset of T1 when the secondary voltage goes negative, starting the charge of C1 again. One noteworthy additional benefit of this circuit is that it may snub some of the parasitic energy across the transformer during its transient reset which can reduce the peak reverse voltage of the output (power) diode.

In center tapped transformer secondary applications, for example push-pull, half and full bridge topologies, the circuit can be replicated to accommodate the second high side switch and drive circuitry, as shown in Figure 4. This arrangement will provide power to the bias supply from both windings of the secondary. At first glance, the lower side circuitry may seem unnecessary, or even wrong. But when the time comes for it to transfer power to the output, this lower side becomes the upper side of the schematic and the need for it becomes apparent.

Many other arrangements of the basic diode and capacitor charge pump circuit are possible - without using inductors and/or additional switches for these low power applications. For more demanding ones, a linear or switchmode integrated circuit regulator can be considered to deliver a precisely regulated bias voltage.

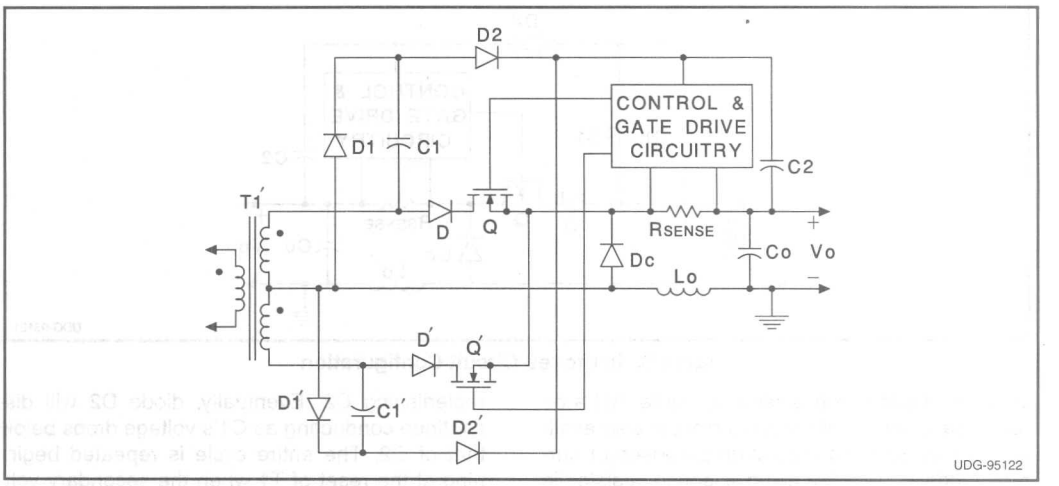


Figure 4. Center Tapped Application of Improved Circuitry

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Design Note

Considerations in Powering BiCMOS ICs

by Jack Palczynski

Bipolar linear integrated circuits have been with us for years in the form of PWM and PFC controllers, supervisory circuits and others. Since these devices have traditionally been built using relatively high voltage (35V) Bipolar processes, powering considerations were typically never a concern. In addition, many of these ICs contained high current protection zeners to keep higher voltages from damaging the device. With a number of new BiCMOS ICs now replacing traditional Bipolars, more consideration needs to be given to powering these low voltage controllers. This Design Note will provide more details regarding the device specifications and help simplify the powering and use of these energy saving devices.

The most prolific of PWM ICs are those of the UC3842 family which are easy to use and to power. The V_{CC} supply can be as high as 34V and an on-chip zener can sink up to 30mA of current. It consumes significantly more power in comparison to the replacement series of Unitrode UCC3802 BiCMOS PWMs. Requiring only about 10% of the current used by the UC3842, these BiCMOS parts are a logical replacement for previous UC3842 based designs. The tradeoff is that the maximum voltage is 13.5V. With these specifications in mind, several power methodologies will be described.

Upon first review of the UCC3802 data sheet, several seemingly contradictory specifications could be noted. The UVLO start threshold has a range of 11.5V to 13.5V, while the protection zener voltage can vary from 12.0V to 15.0V. However, the absolute maximum supply voltage of the IC is specified at 12.0V. This absolute maximum is defined as the lowest possible zener voltage when driven from a low impedance (voltage) source. Note, however, that the zener voltage is always higher than the UVLO start voltage. These two parameters track each other and the chip is tested to guarantee that the zener voltage will never be below that of the start voltage.

For low cost, off-line applications, these newly introduced control ICs offer savings in overall cost and power in comparison to their predecessors. For example, the UCC3802 PWM consumes only 1mA (approximate) for full operation – which can eliminate the need for a bias supply in many instances. To this 1mA, add estimates for the other currents consumed by the control circuitry (gate drive, slope compensation, etc.). Working backwards, calculate the resistor value for the circuit of Figure 1 to deliver this current from the rectified, filtered line voltage. Typically, the AC input voltage will range from $85V_{RMS}$ to $264V_{RMS}$, or about a 3:1 ratio. The corresponding DC input will vary accordingly from 124VDC to 374VDC. Calculate R1 to provide supply current at the lowest input voltage. 3mA minimum supply current is used for this example.

$$\frac{124VDC - 12VDC}{3mA} = 37.3k\Omega \text{ (use 36k).}$$

At high line, this current will increase to

$$\frac{374VDC - 12VDC}{36k} = 10.1mA$$

and dissipate more power. The resistor will guarantee that the ICs zener clamp will not be subjected to overcurrent since it shunts only 7.1mA, the other 3mA are consumed for operation. This configuration is generally referred to as a "current source" power supply. Before the IC starts, it only draws 100µA and C1 is charged with nearly the full supply current. Once C1 reaches the

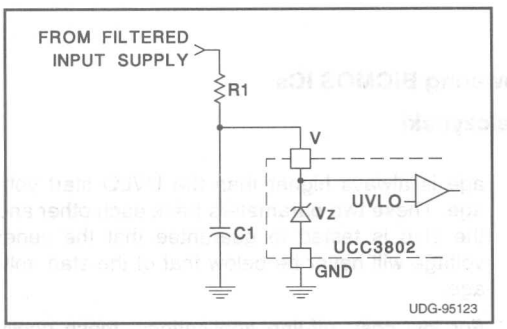


Figure 1. Off-line Current Source Power

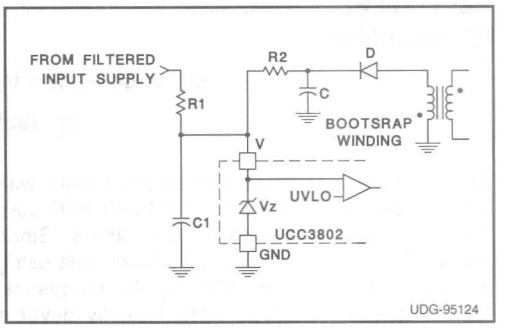


Figure 2. Adding a Bootstrap Supply

UVLO start threshold of about 13.5V, the UC3802 starts and then uses 1mA for itself, and an additional 2mA (this example) to power the gate drive and other functions.

A drawback to the above circuit is that a good percentage of power is dissipated in R1. If the input voltage range is very wide, or if a high frequency is used or a FET with high gate charge is used, it may not be possible to guarantee that the zener current is limited to 30mA at high line while still being able to provide enough current to run at low line. To create a more efficient input supply, a few alternatives are demonstrated. Figure 2 shows a typical bias supply with modifications for the BiCMOS IC. R1 limits current while the IC is in standby mode so that zener current is not exceeded as in the last example. In this case, the resistor may be made much larger since it will not be the major power source once the supply has started. Resistor R2 is placed in series with the bias supply coming from the transformer in order to again limit the zener current to 10mA. This circuit will result in a higher efficiency than that of the first - at the cost of additional components and a bias winding on the transformer. During start up, C1 again charges through R1 until the turn on threshold of the IC is reached. If R1 is very large, then the UVLO hysteresis of the UCC3802 allows the controller to continue running until it reaches its lower threshold. During this time, the bias supply starts supplying current and should take over as the primary IC power supply before the lower UVLO threshold is reached.

A third solution is to use the Unitrode UCC3889 bias supply control circuitry as seen in Figure 3.

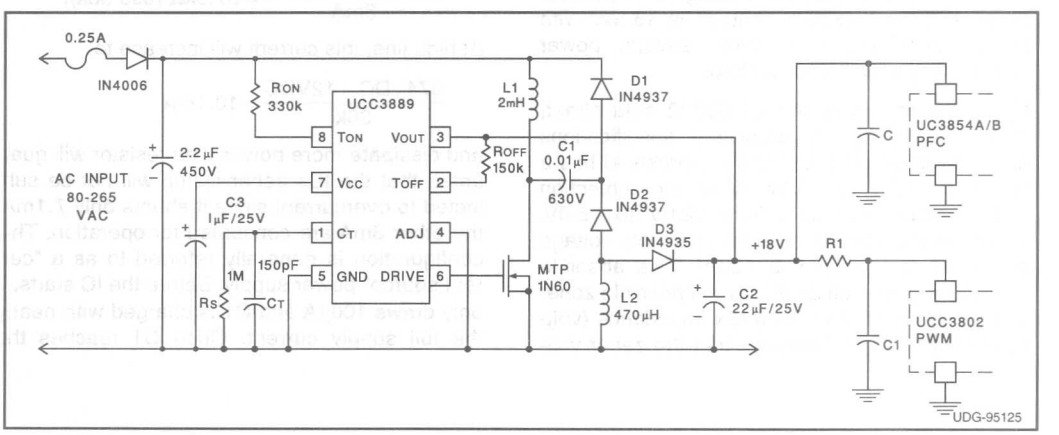


Figure 3. UCC3889 Powers Other Circuits

This patented control technology will provide a fully regulated supply from a high input voltage without the use of transformers. As with the last circuit, a series resistor from an 18V input to Vcc will limit current. With the UCC3889 IC, an input Power Factor Correction IC or other primary side PWM circuit may also be easily powered.

The UCC3802 and the entire family of Unitrode BiCMOS integrated circuits can provide added efficiency, higher speed, FET totempole output drivers (which eliminate the need for protection Schottky diodes) and other added features. With some care, input power can easily be designed to meet the ICs power requirements, and assist in designing new, more efficient switching power supplies.

References:

[1] W. Andreycak, "UCC3800/1/2/3/4/5 BiCMOS Current Mode Control ICs" Unitrode Applications Note U-132.

[2] J. Palczynski, "UCC3806 BiCMOS Current Mode Control IC" Unitrode Applications Note U-144

[3] W. Andreycak, "Elegantly Simple Off-Line Bias Supply for Very Low Power Applications" Unitrode Applications Note U-149

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Design Note

Unitrode - UC3854A/B and UC3855A/B Provide Power Limiting With Sinusoidal Input Current for PFC Front Ends

by Laszlo Balogh

This design note focuses on one of the major improvements introduced to the industry standard UC3854 high power factor boost controller. The new UC3854A/B versions eliminated the need for external components to clamp the voltage and current error amplifier outputs and optimized the voltage levels of some of the sense circuitry. All of these issues are already covered by DN-39 design note (present release is version E). The following aspects were expressed implicitly, in previous literature, and are now described in further details.

What makes intelligent power limiting possible with the UC3854A/B and with the newer UC3855A/B ZVS high power factor controllers, is that the maximum value of the multiplier output current is not directly related to the current of the R_{SET} resistor any more.

Instead, it is limited to be equal or smaller than twice the instantaneous value of the I_{AC} current. This new feature provides a very delicate and effective way to limit input power to the power factor corrector front-end while the converter still maintains a sinusoidal input current waveform. It has to be emphasized here that the power limiting scheme of the UC3854A/B does produce sinusoidal input current waveform even if the load is a negative impedance, like DC-DC converters. In these cases, special care has to be taken to guarantee that the output voltage of the boost power factor corrector is greater than the peak value of the input line voltage at all operating equilibrium. This can be insured by setting the power limiting of the DC-DC converter below the maximum power handling capability of the PFC stage.

In order to establish a straightforward design procedure for the multiplier setup, first a basic relationship should be shown. The ratio of the multiplier output current, (I_{MO}) and the I_{AC} current is constant within one cycle of the AC input because:

$$I_{AC}(t) = \frac{V_{RMS} \bullet \sqrt{2} \bullet \sin(\omega \bullet t)}{R_{AC}} \quad (1)$$

and

$$I_{MO}(t) = \frac{I_{AC}(t) \bullet (V_{EA} - 1.5)}{K \bullet (A \bullet V_{RMS})^2} \quad (2)$$

where,

V_{RMS} is the RMS value of the AC input voltage;

V_{EA} is the voltage error amplifier saturation voltage (V_{OH});

K is the multiplier constant (K = 1);

A is the divider ratio to the V_{RMS} pin of the IC.

The ratio of $I_{MO}(t)$ to $I_{AC}(t)$ is given as:

$$R = \frac{I_{MO}(t)}{I_{AC}(t)} = \frac{V_{EA} - 1.5}{K \bullet (A \bullet V_{RMS})^2} \quad (3)$$

which is determined only by the RMS value of the input voltage and stays constant within one line cycle.

In the case of a well executed design, the ratio will be equal to two - right at the minimum input voltage where the rated output power is still expected to be delivered. Figure 1 shows the optimal ratio of I_{MO} and I_{AC} as a function of the

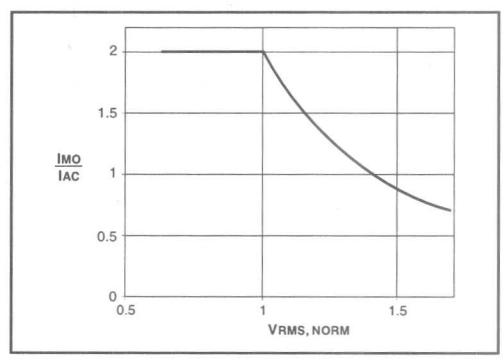


Figure 1. Ideal $\frac{I_{MO}}{I_{AC}}$ Ratio

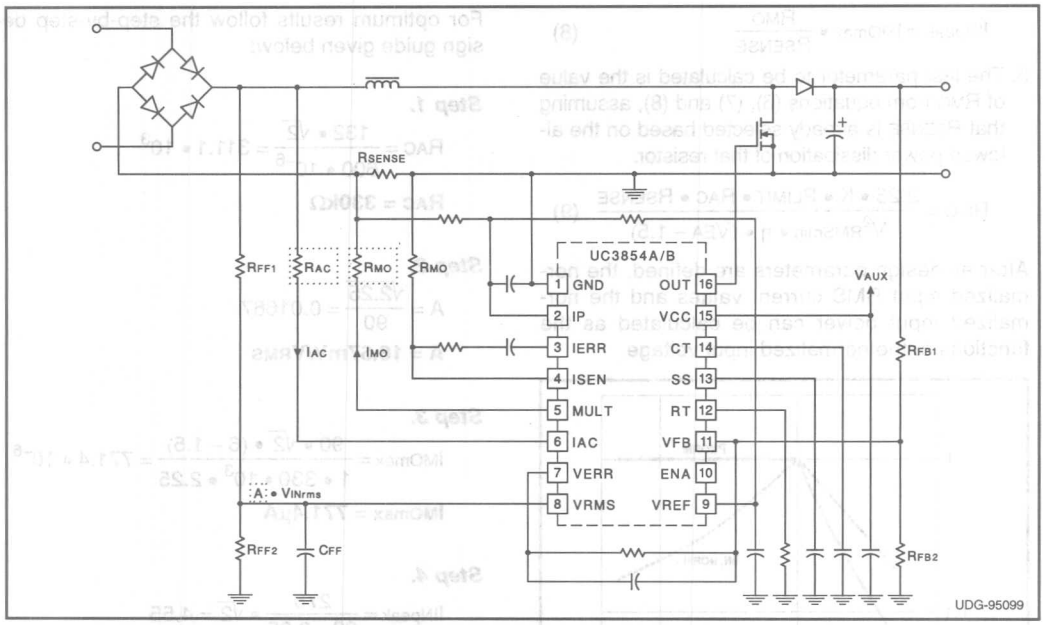


Figure 2. Multiplier Set Up Components in a Typical PFC Application

normalized input voltage. The horizontal axis of the graph is normalized for the minimum line voltage where full power can be obtained. For values below unity the converter will work in power limited mode.

To achieve precise power limiting the highlighted components of Figure 2 have to be calculated.

1. From the maximum peak input voltage and the highest allowable I_{AC} value calculate R_{AC}.

$$R_{AC} = \frac{V_{RMSmax} \bullet \sqrt{2}}{I_{ACmax}} \qquad (4)$$

where $I_{ACmax} \leq 600\mu A$ is given in the datasheet.

2. The factor "A" of equation (2) can be determined from the specified minimum input voltage value where the circuit has to supply full rated power. At that point, the voltage error amplifier output (V_{EA}) is about to saturate, and I_{MO} shall be at its theoretical maximum which is $2 \bullet I_{ACmax}$. The required value of "A" can be expressed from (3) using the conditions previously stated:

$$A = \frac{\sqrt{2.25}}{V_{RMSmin}} \qquad (5)$$

Now every parameter is given for equation (2), and I_{MO} is known for all operating conditions.

3. The next step is to calculate the peak value of the multiplier current (I_{MOmax}) at the minimum input voltage (V_{RMSmin}). From combining (2), (4) and (5),

$$I_{MOmax} = \frac{V_{RMSmin} \bullet \sqrt{2} \bullet (V_{EA} - 1.5)}{K \bullet R_{AC} \bullet 2.25} \qquad (6)$$

4. I_{MOmax} will define the maximum value of the input current (I_{INpeak}) which occurs at the peak of the minimum line voltage, (V_{RMSmin}) and at maximum load. The required peak input current is given as:

$$I_{INpeak} = \frac{P_{LIMIT}}{V_{RMSmin} \bullet \eta} \bullet \sqrt{2} \qquad (7)$$

The relation between I_{MOmax} and I_{INpeak} is defined by the two resistors R_{SENSE} and R_{MO} according to:

$$I_{INpeak} = I_{MOmax} \bullet \frac{R_{MO}}{R_{SENSE}} \quad (8)$$

5. The last parameter to be calculated is the value of R_{MO} from equations (6), (7) and (8), assuming that R_{SENSE} is already selected based on the allowed power dissipation of that resistor.

$$R_{MO} = \frac{2.25 \bullet K \bullet P_{LIMIT} \bullet R_{AC} \bullet R_{SENSE}}{V^2_{RMSmin} \bullet \eta \bullet (V_{EA} - 1.5)} \quad (9)$$

After all design parameters are defined, the normalized input RMS current values and the normalized input power can be calculated as the functions of the normalized input voltage.

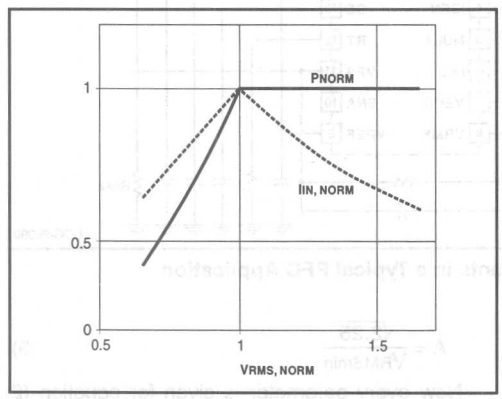


Figure 3. Power Limit and Maximum Input Current Values as a Function of Input Voltage (All Normalized)

As Figure 3 demonstrates, exact, and constant power limiting can be realized by the UC3854A/B high power factor controller ICs for the entire input voltage range. That is caused by the input voltage feedforward term in the multiplier equation, (2).

Design Example

The following example is to illustrate how to execute the procedure described above. The design example has the following start up parameters:

V_{IN} = 70 . . . 132 V_{ACRMS}

V_{INmin} = 90 V_{ACRMS}	(where full output power still obtainable)
P_{OUT} = 250W	(power limit of the load converter)
P_{LIMIT} = 275W	(set PFC power limit 10% above load converter)
η = 0.95	(expected efficiency)

For optimum results follow the step-by-step design guide given below:

Step 1.

$$R_{AC} = \frac{132 \bullet \sqrt{2}}{600 \bullet 10^{-6}} = 311.1 \bullet 10^3$$

R_{AC} = 330kΩ

Step 2.

$$A = \frac{\sqrt{2.25}}{90} = 0.01667$$

A = 16.67mV/V_{RMS}

Step 3.

$$I_{MOmax} = \frac{90 \bullet \sqrt{2} \bullet (6 - 1.5)}{1 \bullet 330 \bullet 10^3 \bullet 2.25} = 771.4 \bullet 10^{-6}$$

I_{MOmax} = 771.4μA

Step 4.

$$I_{INpeak} = \frac{275}{90 \bullet 0.95} \bullet \sqrt{2} = 4.55$$

I_{INpeak} = 4.55A

Step 5.

Assume the maximum power dissipation of the current sense resistor P_{RS} = 0.5W, then:

$$R_{SENSE} = \frac{P_{RS} \bullet V_{INmin}^2 \bullet \eta^2}{P_{OUT}^2} \quad (10)$$

$$R_{SENSE} = \frac{0.5 \bullet 90^2 \bullet 0.95^2}{275^2} = 0.04833$$

R_{SENSE} = 47mΩ

Step 6.

$$R_{MO} = \frac{2.25 \bullet 1 \bullet 275 \bullet 330 \bullet 10^3 \bullet 47 \bullet 10^{-3}}{90^2 \bullet 0.95 \bullet (6 - 1.5)}$$

$$= 277.1$$

R_{MO} = 270Ω

The design just completed will exhibit the required power limiting characteristics for the entire operating input voltage range. The described calculations can be easily programmed as it is shown in the Mathcad® worksheet in the Appendix.

APPENDIX

This MathCAD file calculates the power limiting characteristic of the UC3854A/B and UC3855A/B high power factor controllers for wide input voltage range application.

INPUT PARAMETERS:

$V_{INmin} := 70$	Input voltage (RMS) value, where the controller starts operating.
$V_{INlim} := 90$	Minimum input voltage (RMS) where the circuit must deliver its rated output power.
$V_{INmax} := 270$	Maximum input voltage (RMS).
$P_{LIM} := 275$	110% of the load power requirements.
$\eta := 0.93$	Expected efficiency of the PFC stage.
$I_{ACmax} := 600 \bullet 10^{-6}$	Maximum value of the I_{AC} current as defined in the datasheet.
$V_{EAsat} := 6$	Output voltage of the voltage amplifier when it is saturated high.
$K := 1$	The multiplier constant as it is given in the datasheet.
$R_S := 0.047$	The current sense resistor value, defined previously based on the acceptable maximum power dissipation.

DESIGN PROCEDURE:

Step 1. Estimate R_{AC} resistance:

$$R_{ACest} = \frac{V_{INmax} \bullet \sqrt{2}}{I_{ACmax}} \qquad R_{ACest} = 6.364 \bullet 10^5$$

Pick the closest **higher** standard value:

$R_{AC} := 6.8 \bullet 10^5$

Step 2. Divider ratio of the input RMS voltage to the V_{RMS} pin (8) of the IC.

$$A := \frac{\sqrt{2.25}}{V_{INlim}} \qquad A = 0.017 \qquad [mV/V_{RMS}]$$

Step 3. Determine the maximum multiplier output current. It occurs at the peak of the mains cycle at the minimum input voltage amplitude where full rated power is still obtainable.

$$I_{MOmaxpk} := \frac{V_{INlim} \bullet \sqrt{2} \bullet (V_{EAsat} - 1.5)}{K \bullet R_{AC} \bullet 2.25}$$

$I_{MOmaxpk} = 3.744 \bullet 10^{-4}$

Step 4. Calculate the highest peak input current value as defined by the rated output power and the minimum input voltage amplitude where full rated power is still obtainable.

$$I_{INpk} := \frac{P_{lim} \bullet \sqrt{2}}{V_{INlim} \bullet \eta} \qquad I_{INpk} = 4.646$$

Step 5. Estimate R_{MO} resistance.

$$R_{MOest} := \frac{I_{INpk}}{I_{MOmaxpk}} \bullet R_S \qquad R_{MOest} = 583.367$$

Pick the closest **lower** standard value:

$R_{MO} := 560$

DESIGN VERIFICATION:

Step := 20 Number of points to calculate.

i := 0..step Step variable.

Input voltage range definition:

$$V_{INRMS}(i) := V_{INmin} + \frac{V_{INmax} - V_{INmin}}{step} \bullet i$$

I_{AC} current as a function of the input voltage:

$$I_{ACRMS}(i) := \frac{V_{INRMS}(i)}{R_{AC}}$$

I_{MO} current as defined by the input voltage and applying the $I_{MO} < 2 \bullet I_{AC}$ limit.

$$I_{MORMSest}(i) := \frac{I_{ACRMS}(i) \bullet (V_{EAsat} - 1.5)}{K \bullet (A \bullet V_{INRMS}(i))^2}$$

$I_{MORMS}(i) := \text{if}(I_{MORMSest}(i) > 2 \cdot I_{ACRMS}(i), 2 \cdot I_{ACRMS}(i), I_{MORMSest}(i))$

Calculating the maximum input RMS current level limited by the multiplier output current.

$I_{INRMS}(i) := I_{INRMS}(i) \cdot \frac{R_{MO}}{R_S}$

The power limit of the power factor corrector.

$P_{INmax}(i) := V_{INRMS}(i) \cdot I_{INRMS}(i)$

Graphical representation of the obtained data:

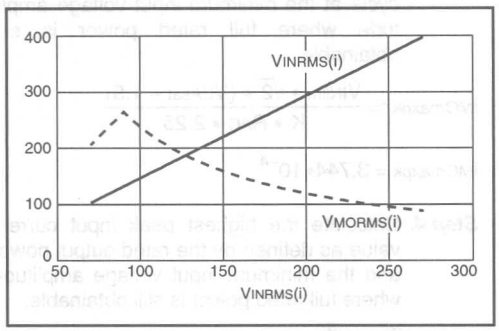


Figure 4. The I_{AC} and I_{MO} currents (in μAmps) as a function of the RMS input voltage.

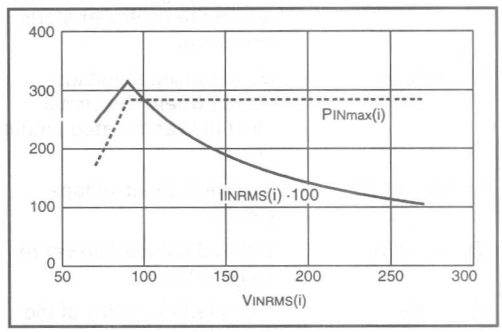


Figure 5. Input power [W] and input RMS current [A] (multiplied by 100 to fit the same scale) as a function of input RMS voltage.

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Design Note

UCC3913 Electronic Circuit Breaker for Negative Voltage Applications Evaluation Kit List of Materials for a -48V/1A Test Circuit

by Bill Andreycak

Many battery powered and Telecommunications power supplies use some form of protection to prevent high currents from flowing during a short circuit or overload condition. This function is often performed by a self-resetting circuit breaker -as opposed to a fuse, which would require manual replacement whenever triggered. Circuit breakers can be implemented in a number of different ways, but the most popular approach is use a MOSFET transistor which can be switched on and off as required. Load current is typically sensed with a low value resistor and compared to a reference level to determine when an overcurrent condition exists. This function can be achieved with discrete circuitry or with a fully integrated solution, such as the UCC3913 Negative Voltage Circuit Breaker. This Design Note highlights the UCC3913 Evaluation Board in a typical –48VDC, 1A application circuit. Complete details for programming the various features of the device can be obtained from the UCC3913 Datasheet, found in the Unitrode Product and Applications Handbook.

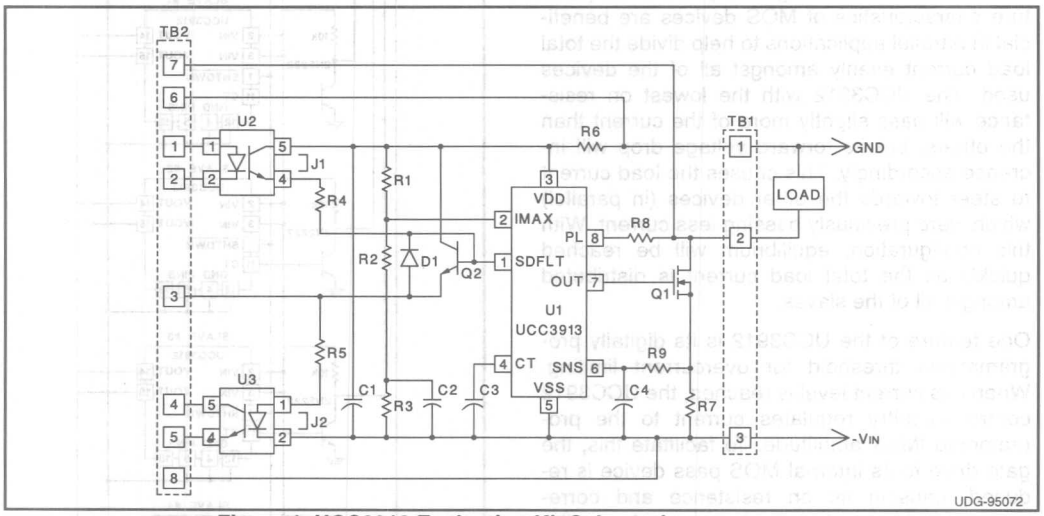


Figure 1. UCC3913 Evaluation Kit Schematic

List of Materials :

C1	1µF/16VDC Ceramic
C2	not used - open circuit
C3	1.5nF/16VDC
C4	not used - open circuit
D1	1N4148 Diode
Q1	IRF630 200V/5A MOSFET
Q2	2N2222 NPN
R1	24k, 1/4W
R2	510 ohms, 1/4W
R3	JUMPER - use AWG 22 wire
R4	47k, 1/4W
R5	1k, 1/4W
R6	3.3k, 1/4W or Qty (4) 13kΩ 1/8W SMT resistors in parallel
R7	50 milliohm shunt
R8	510k, 1/4W
R9	JUMPER - use AWG 22 wire
U1	UCC3913 IC
U2,3	4N29 Optocoupler

Test Equipment :

Power supply : 48VDC / 1.5ADC
Programmable electronic load to sink 1.5A at 48VDC

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Design Note

Paralleling UCC3912 Electronic Circuit Breaker ICs

By Paul Aloisi and Bill Andreycak

The UCC3912 IC is an integrated 3 Amp electronic circuit breaker which includes programmable overcurrent protection and retry timing following a fault. Other common uses for this function are in higher current (12A) and low "headroom" applications where a lower voltage drop is required. Each of these can be addressed by paralleling UCC3912 devices as shown in Figure 1.

To provide the circuit breaker function, the UCC3912 uses an internal FET switch having a typical on resistance of 0.150 ohms and 3 Amp continuous current rating. The positive temperature characteristics of MOS devices are beneficial in parallel applications to help divide the total load current evenly amongst all of the devices used. The UCC3912 with the lowest on resistance will pass slightly more of the current than the others, but its forward voltage drop will increase accordingly. This causes the load current to steer towards the other devices (in parallel) which were previously passing less current. With this configuration, equilibrium will be reached quickly as the total load current is distributed amongst all of the slaves.

One feature of the UCC3912 is its digitally programmable threshold for overcurrent limiting. When this current level is reached, the UCC3912 control circuitry regulates current to the programmed IMAX amplitude. To facilitate this, the gate drive to its internal MOS pass device is reduced, causing its on resistance and corresponding voltage drop to increase. As in the previous example for paralleled devices, this steers current to the other UCC3912s in parallel, forcing load sharing.

The duration of this allowable overcurrent condition is also programmable by selecting the appropriate timing capacitor value to the IC's fault timing (CT) pin. When the overcurrent condition is detected, two protection functions begin operation. First, the UCC3912 goes into a constant current mode to regulate current to the pro-

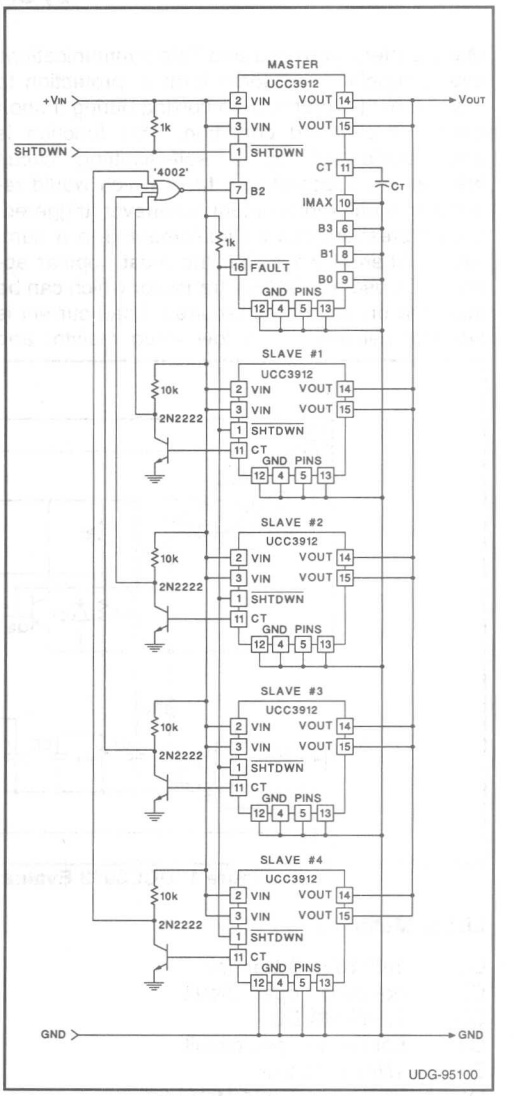


Figure 1. Paralleling UCC3912 Electronic Circuit Breakers

6/95A

grammed value of IMAX. Simultaneously, the device begins charging the fault timing capacitor and provides a digital indication at the open collector FAULT pin of the IC. The overcurrent duration concludes when the timing capacitor charges to a preset voltage and the MOS pass transistor is turned off. The off time is internally controlled to thirty times the programmed fault duration ($t_{OFF} = 30 \bullet t_{FAULT}$), resulting in an approximate three percent (3%) effective duty cycle to safely limit power dissipation into a short circuit. Note that the UCC3912 also features internal overtemperature shutdown protection should the timer be incorrectly programmed for too long of a fault duration or inadequate heatsinking provided. Consult the UCC3912 datasheet for complete details of the timing and fault protection circuitry operation into single and repetitive overcurrent conditions.

Circuit Operation

In this paralleled application of UCC3912 devices, a master/slave arrangement will be incorporated and the fault timing control will be governed entirely by the master. Slave devices are configured to give a digital representation of the overcurrent condition, and their individual CT outputs are "NOR"ed together as an input to the master. A generic CMOS '4002 digital IC is used for its low current and 3V operational characteristics. Note that each input requires a 2N2222 NPN signal level transistor with a 10k ohm pull up resistor from the input supply (V_{IN}) to its collector to complete the interface. This arrangement is necessary to achieve the proper digital inputs to the NOR gate while clamping the UCC3912 CT pin voltages to just a base-emitter diode drop (V_{BE}) above ground. This will override the internal timing circuits of the individual slaves which are being controlled by the master's fault timer.

In normal operation (prior to any overcurrent condition) the CT pin of each slave UCC3912 is low and the corresponding NPN transistor is off. The 10k ohm collector resistors place a digital high on the NOR gate's four inputs, and the output of this gate is low. When any of the slave UCC3912 devices goes into overcurrent protection its CT pin is pulled high by an internal current source. Normally, this would start charging the fault timing capacitor, but in this paralleled application, it forward biases the base-emitter junction of the respective 2N2222 transistor. This turns on the NPN device and forces a digital low input to the NOR gate. When all four of the NOR inputs go low, the output of the NOR gate goes high. This indicates that all four of the slaves are limiting current to their programmed maximum level and that an overcurrent condition exists.

The output of this NOR gate is used to digitally program one bit (BIT2) of the master UCC3912's overcurrent limit. The master was previously "off", not providing any load current since it's four overcurrent inputs (BITs 0 through 3) were all low. Any digital input below "0100" programs its output current to zero by turning off the power switch. But triggered by the overcurrent conditions of the slaves, the NOR gate output switches BIT2 of the master high. This turns the master on and programs its output current to 0.25A by the "0100" code at BITS 0 through 3. The master now allows 0.25 amps in addition to the slaves 12 amps to the load for a system total of 12.25A. This is the sum of the master (0.25A) and the four slave overcurrent programming thresholds of three amps each ($4 \bullet 3.0A$). Provided that the demanded load current is in excess of 12.25 amps, as would be the case with a short circuited load, the master then provides two functions. First, it regulates the current through the master to the programmed 0.25 amp level. Additionally, it begins a fault timing sequence, the duration of which is programmed by the value of the fault timing capacitor, CT. This capacitor charges during the overcurrent condition until it reaches the internal 1.5 volt fault threshold. Once triggered, the fault latch turns off the UCC3912's internal MOSFET switch (to provide the circuit breaker function) while also indicating the fault condition by providing a "low" on the IC's FAULT pin. Note that the master's FAULT output is connected to the slaved UCC3912s' SHTDWN pin which turns off all of the slaved devices at the same time that the master turns off.

The duration of the overcurrent event is programmed entirely by the master's CT timing capacitor value according to the UCC3912 datasheet information and design equations. The timing circuitry will deliver a current limited, pulsed mode fault protection and retry with a three percent (3%) duty cycle. While the timing capacitor is charging, each IC regulates and compares its load current to the programmed fault overcurrent level. Providing that the fault condition does exist, all UCC3912 ICs are turned off for the remaining ninety-seven percent (97%) of the programmed fault timing period. The resulting three percent duty cycle fault mode facilitates safe operation into a continuous overload or short circuited condition. It safely limits input power consumption and power dissipation in the circuit breaker switches. Additionally, no costly system downtime or manual replacement of a fuse or resetting of a circuit breaker is required.

Once the abnormal load condition has been removed, the circuit goes back into normal operation. The master's FAULT output returns to a "high" along with each of the slaves' SHTDWN inputs. If the load has not been removed, the master is retriggered by the NOR gate once each slave has detected an overcurrent condition, and the system goes back to the three percent duty cycle protection mode.

Note that the entire system is nominally triggered at 12.25A which is programmed by the four UCC3912 slaves' individual 3A thresholds and the 0.25A contribution of the master. However, this is unlikely to occur in a typical application because of two of the device's other ratings. First, is the maximum specified "trip" current of 3.5A for each slave switch and 0.45A for the master with the programmed overcurrent inputs (Bits 0 - 3). This would raise the highest trigger threshold to 14.45A. However, the more dominant factor is the high current capability of the UCC3912's switch which - is rated at four amps (4A) typical. In fact, each device can safely provide 5.2A (worst case) over all rated temperature and manufacturing conditions. One possible scenario should be reviewed using an instantaneous short circuit on the outputs. Even though all of the slaves properly triggered their internal fault logic at 3.5A (worst case), all four of the slaves could be delivering as much as 5.2 amps maximum (within the device's ratings) to the load. This would correspond to a maximum load current of 21.25 amps. And while unlikely to repetitively occur in a typical application, it does represent the worst case sum of the four slaves'(4 • 5.2A) plus the master's (0.45A) maximum current ratings. However, it's advised to evaluate this figure to that of other fault protection and overcurrent techniques, for example fuses, which can be significantly higher for short durations. More specific details and comparisons can be found in Unitrode Application Note U-151.

Other Applications

This design example utilized the UCC3912 device's rated current capability of 3A, but can be scaled for other applications with higher or lower requirements. Each slave can be individually programmed for a maximum current between 0.25A and 3A in 0.25A increments using the 4 bit digital inputs to the fault circuitry. This is beneficial in many low voltage supply applications which require a low headroom or dropout voltage (the voltage drop between the input and output connections of the circuit breaker) to meet the load's power supply specifications. In these, the UCC3912's could be paralleled to minimize the series voltage drop - and not to obtain the higher current capability of the system. This is one application where it is desirable to program the slave's overcurrent thresholds to a lower value than 3A each.

The 0.25A example of additional load current provided by the master can also be raised to deliver higher total system current to accommodate a transient load condition. Examples of this can be found in many battery powered energy management systems where only the required active circuitry is enabled and all others are switched off. When supplying power to these types of loads, often high inrush currents are needed to quickly charge up any local bypassing and filtering capacitors. This brief condition can be accommodated by programming the master UCC3912's overcurrent bits accordingly.

Although switching of only the master UCC3912's BIT2 is shown, its BIT3 input can also be switched for higher current capability. Additionally, BIT0 and BIT1 are shown grounded in the example circuit but can be programmed or switched with digital "1"s as well. Active digital programming of the master and all slave overcurrent BITs is also possible for the more demanding overcurrent protection applications. Each UCC3912 Electronic Circuit Breaker IC also features internal overtemperature protection with shutdown for complete system protection.

Additional Reference Material:

[1] UCC3912 Data Sheet

[2] Application Note U-151: "UCC3912 Programmable Electronic Circuit Breaker – Performance Evaluation and Programming Information"

[3] UCC3912 Evaluation Kit

[4] Design Note DN-58: "UCC3912 Programmable Electronic Circuit Breaker – Performance Evaluation and Programming Information"

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Design Note

An Intelligent Overvoltage Protection Scheme for 3V to 10V Power Supplies

by Chuck Melchin

Protecting sensitive circuitry from power supply overvoltage conditions is a concern for any system designer. Overvoltage conditions can be caused by transient load changes, loss of the power supply control loop, accidental miswiring or incorrect module installation. An intelligent protection scheme can be accomplished utilizing the UC3908 Programmable Voltage Clamp.

The UC3908 monitors a power supply output voltage and draws less than 100µA if no overvoltage condition is present. If an overvoltage condition occurs, the UC3908 will act as a shunt regulator and attempt to regulate the power supply voltage to a programmed level by internally shunting current from VC to ground. If the shunted current exceeds a maximum value, or if the overvoltage condition is of a long enough duration to trip the IC's internal thermal sense circuitry, the device provides a gate signal to an external SCR. The SCR crowbars the power supply output, while the UC3908 internally latches the shunt regulator fully on. The UC3908 also provides a overvoltage indicator signal through an open collector output any time an overvoltage condition occurs.

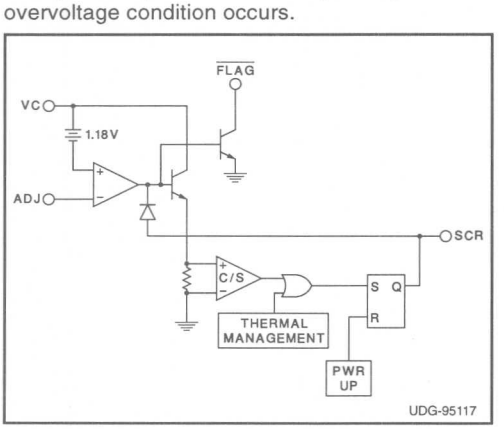


Figure 1. UC3908 Functional Block Diagram

Basic Operation of the UC3908 can be seen in the following flow chart:

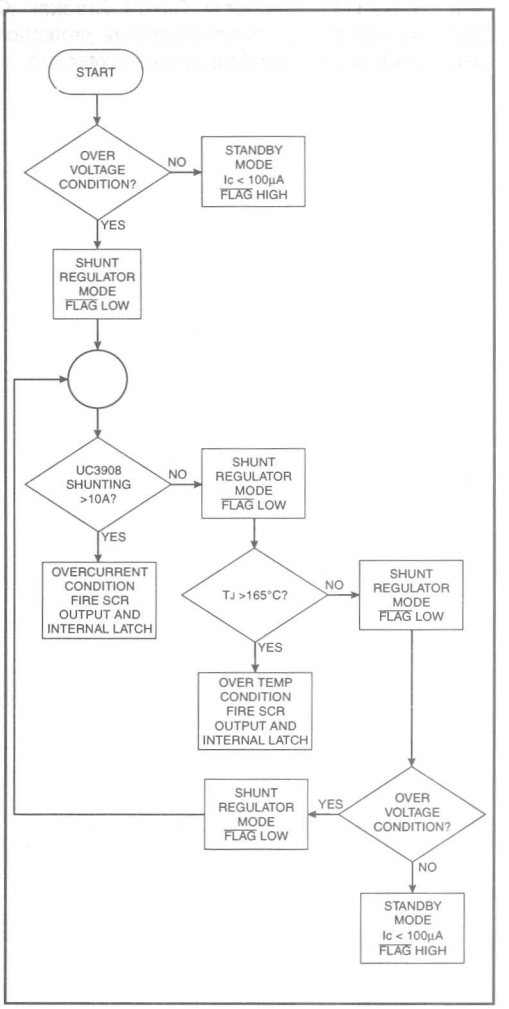


Figure 2. UC3908 Operational Flowchart

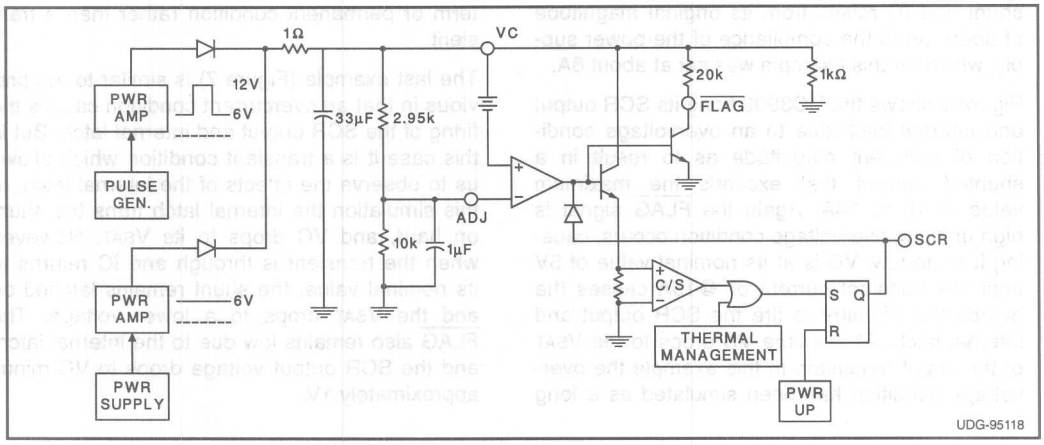


Figure 3. Lab Evaluation Circuit

Measured performance

The UC3908 can be evaluated using the circuit shown in Figure 3. It is intended to give the user the ability to simulate power supply overvoltage conditions with control over duration and magnitude of the transient. Four different real world scenarios using the UC3908 to protect the load of a 5V power supply were simulated using this circuit with the results described below.

The first condition shown (Figure 4) is an overvoltage transient with a magnitude resulting in less than 10A shunted by the regulator. The fault duration is small enough not to heat the device past its thermal trigger point. The resulting waveforms show $\overline{\text{FLAG}}$ going low to indicate a fault, 6A of shunted current for the duration of the transient and VC raising as a result of the shunted current. The SCR output stays low in the absence of an overcurrent or thermal firing of the internal latch.

The second set of waveforms (Figure 5) show an overvoltage condition of a duration and magnitude sufficient to cause a T_J of greater than 165°C. This causes a firing of the internal latch and SCR output through the thermal management circuitry. The $\overline{\text{FLAG}}$ output is low for the duration of the entire overvoltage condition. VC stays at 5V until the SCR output goes high and the internal latch turns on the shunt transistor hard. At this time VC drops to the V_{SAT} of the

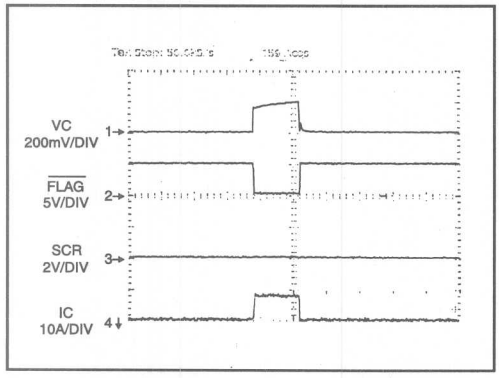


Figure 4. Shunt Regulation of O.V. Condition

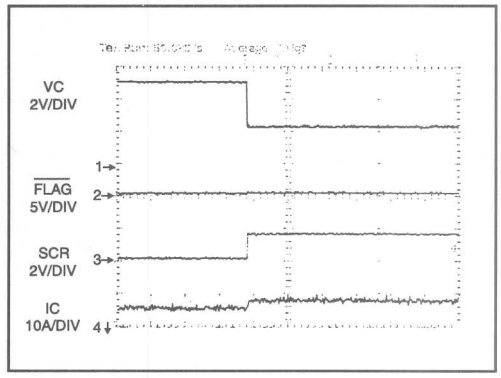


Figure 5. Thermal Firing of SCR Output

shunt and IC raises from its original magnitude of about 6A to the compliance of the power supply, which for this example was set at about 8A.

Figure 6 shows the UC3908 firing its SCR output and internal latch due to an overvoltage condition of sufficient magnitude as to result in a shunted current that exceeds the maximum value of 10 to 14A. Again the $\overline{\text{FLAG}}$ signal is high until the overvoltage condition occurs, causing it to go low. VC is at its nominal value of 5V until the transient current of @15A causes the overcurrent circuitry to fire the SCR output and internal latch. At this time VC drops to the V_{SAT} of the shunt transistor. In this example the overvoltage condition has been simulated as a long term or permanent condition rather than a transient.

The last example (Figure 7) is similar to the previous in that an overcurrent condition causes the firing of the SCR output and internal latch. But in this case it is a transient condition which allows us to observe the effects of the internal latch. In this simulation the internal latch turns the shunt on hard, and VC drops to its V_{SAT}. However, when the transient is through and IC returns to its nominal value, the shunt remains latched on and the V_{SAT} drops to a lower voltage. The $\overline{\text{FLAG}}$ also remains low due to the internal latch, and the SCR output voltage drops to VC minus approximately 1V.

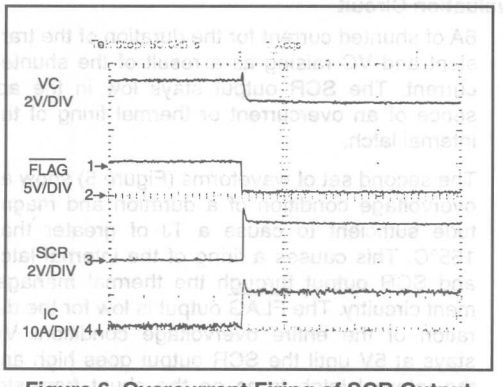


Figure 6. Overcurrent Firing of SCR Output

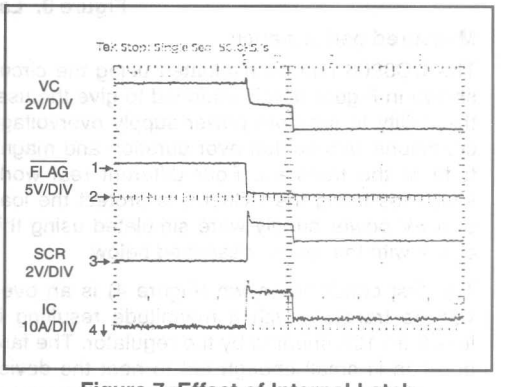


Figure 7. Effect of Internal Latch During Overcurrent Condition

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Design Note

UC3573 Buck Regulator PWM Control IC

Typical Application Circuit for +12VDC Input to +5VDC/1A Output
Also : Demonstration Kit Circuit Schematic and List of Materials

by Chuck Melchin and Bill Andreycak

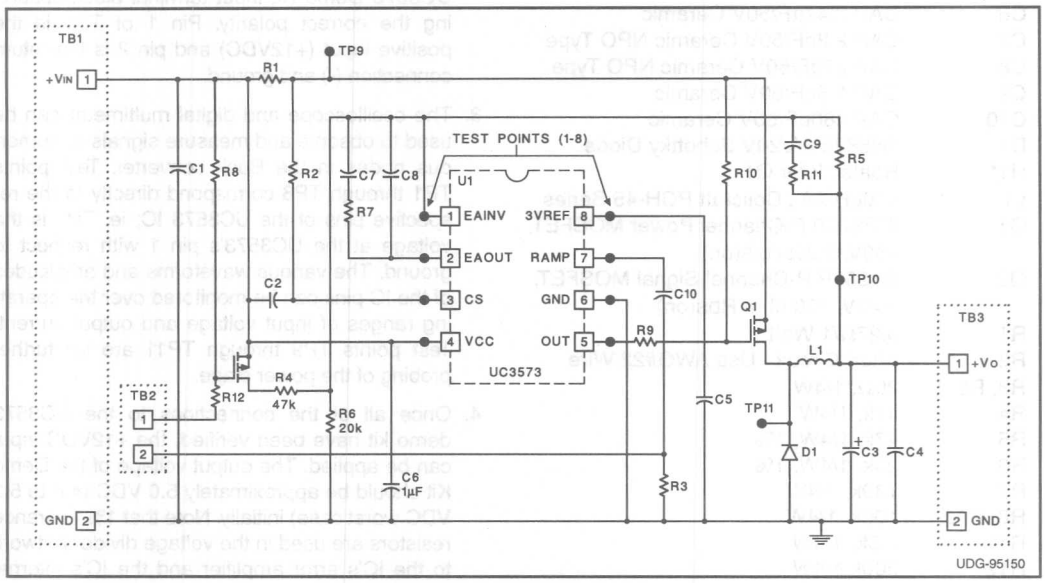


Figure 1. UC3573 Application Circuit Schematic

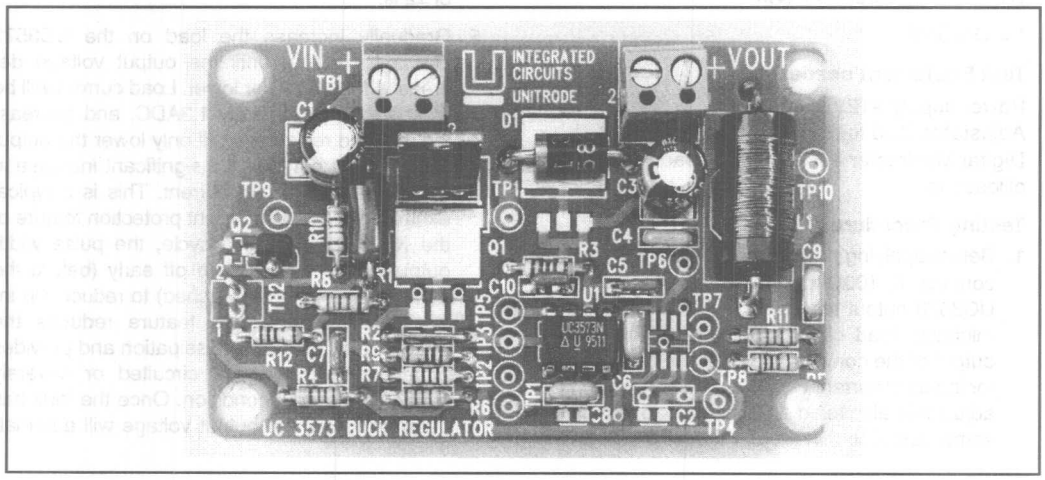


Figure 2. Photo of UC3573 Demo Kit

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List of Materials:

Reference	Value and Type
C1,C3	CAP 82µF/25V Electrolytic, ESR < 0.25Ω@100kHz (Panasonic HFQ or FA series)
C2	Not Used - Open Circuit
C4,C5	CAP 0.1µF/50V Ceramic
C6	CAP 0.47µF/50V Ceramic
C7	CAP 2.2nF/50V Ceramic NPO Type
C8	CAP 27pF/50V Ceramic NPO Type
C9	CAP 1.8nF/50V Ceramic
C10	CAP 680pF/50V Ceramic
D1	1N5820 3A/20V Schottky Diode
H1*	Heatsink for Q1
L1	220µH/2A : Coilcraft PCH-45 Series
Q1	IRF9Z30 P-Channel Power MOSFET, –50V, 0.2Ω RDS(on)
Q2	BS250P P-Channel Signal MOSFET, –45V, 100 ohm RDS(on)
R1	0.27Ω/1 Watt
R2	Short Circuit - Use AWG#22 Wire
R3, R9	20Ω, 1/4W
R4	47k, 1/4W
R5	47k, 1/4W, 1%
R6	20k, 1/4W, 1%
R7	130k, 1/4W
R8, R10	100k, 1/4W
R11	7.5k, 1/4W
R12	200k 1/4W
TB1, TB3	Terminal Block
U1	UC3573 PWM

* = Optional

Test Equipment needed:

Power supply +12VDC/2A max.
Adjustable load for 5VDC/2A max.
Digital Multimeter 100Ω, 1 Watt load resistor Oscilloscope.

Testing Procedure

1. Before applying power to the UC3573 Demo Kit, connect A 100Ω preload resistor across the UC3573 output terminals at TB3. This places a minimum load of 50 milliamps on the +5VDC output of the converter to keep the Buck regulator inductor current continuous. Also connect the adjustable electronic or resistive load across the same output terminals. Set the load to draw no current and observe correct ± polarity when using an electronic load. Pin 1 of TB3 is the positive output (+) and pin 2 is the negative (-) terminal, or ground. Also connect the digital multimeter to the output terminals to measure the output voltage.
2. Connect the 12VDC/2A power supply to the UC3573 Demo Kit input terminal block observing the correct polarity. Pin 1 of TB1 is the positive input (+12VDC) and pin 2 is the return connection (-) and ground.
3. The oscilloscope and digital multimeter can be used to observe and measure signals at numerous nodes in the Buck converter. Test points TP1 through TP8 correspond directly to the respective pins of the UC3573 IC; ie. TP1 is the voltage at the UC3573's pin 1 with respect to ground. The various waveforms and amplitudes of the IC pins can be monitored over the operating ranges of input voltage and output current. Test points TP9 through TP11 are for further probing of the power stage.
4. Once all of the connections to the UC3573 demo kit have been verified, the +12VDC input can be applied. The output voltage of the Demo Kit should be approximately 5.0 VDC (4.8 to 5.2 VDC worst case) initially. Note that 1% tolerance resistors are used in the voltage divider network to the IC's error amplifier and the IC's internal reference voltage (Pin 8) has an initial tolerance of ±2%.
5. Gradually increase the load on the UC3573 Demo Kit output until the output voltage decreases to 4.5VDC or lower. Load current will be limited to approximately 1.3ADC, and decreasing the load resistance will only lower the output voltage, and not cause a significant increase in the converter's output current. This is a typical exhibition of the overcurrent protection feature of the IC. Each switching cycle, the pulse width output of the IC is turned off early (before the normal pulse width is reached) to reduce the input power drawn. This feature reduces the MOSFET switch power dissipation and provides protection from a short circuited or severely overloaded output condition. Once the fault has been removed, the output voltage will automat-

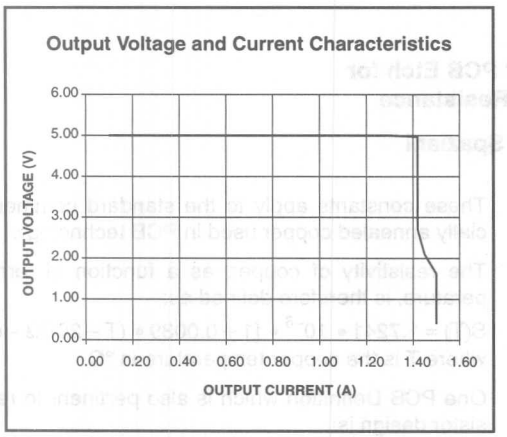


Figure 3. Converter Output Voltage Versus Current

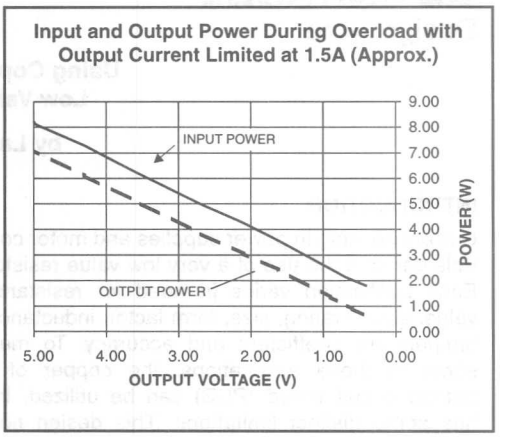


Figure 4. Converter Input and Output Power During Overload

ically return to the normal 5VDC amplitude. The exact profiles of output voltage versus output current is shown in Figure 3. and input power versus output power during overload conditions is shown in Figure 4.

Optional Features

Synchronization: Terminal block TB2 is for optional external synchronization of the UC3573 and for remote shutdown of the UC3573 Demo Kit. The required SYNC pulse input to TB2 (pin 2) is a brief pulse of approximately 1 volt amplitude. This adds to the IC's normal oscillator timing sawtooth waveform (RAMP, pin 7) to force the total waveform above the oscillator's internal upper threshold. Doing this will terminate the immediate switching cycle and initiate the next clock cycle. It is necessary that the synchronization frequency is higher than the UC3573 programmed oscillator frequency in order for this to work properly. Note that a low impedance, fairly high current drive circuit is required to force synchronization. More complete details can be found in Unitrode Application Note U-111 in the "Synchronization" section.

Remote Shutdown: The UC3573 controller can be placed into a low current (50µA typical) standby mode by forcing the error amplifier inverting input above 2.6VDC. The circuitry used to facilitate this on the Demo Kit consists of transistor Q2, resistors R4, R6 and R12. When pin 1 of terminal block TB2 is pulled low, a voltage divider to the gate of Q2 is formed between resistors R8 and R4. This drives the gate to source voltage of the P-channel MOSFET switch below its threshold causing it to turn on. Its drain voltage, connected to resistor R4 approaches that of the FET source node which is connected to the positive input voltage (+VIN). Now a voltage divider is activated between the input voltage and ground via R4 and R6 which forces the error amplifier inverting input voltage to rise above the 2.6VDC shutdown threshold, placing the device into its low current standby mode.

Other Applications

Many other voltage step down applications are addressable by the UC3573 Buck Regulator PWM Controller. Following a brief design exercise, the UC3573 Demonstration Kit can be repopulated with the exact components to evaluate other DC to DC converter designs. Consult the UC3573 Datasheet for additional information.

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Design Note

Using Copper PCB Etch for Low Value Resistance

by Larry Spaziani

INTRODUCTION

Current sensing in power supplies and motor controls demand the use of a very low value resistor. Each application varies in need for resistance value, power rating, size, form factor, inductance, temperature coefficient and accuracy. To meet some of these applications, the copper of a printed circuit board (PCB) can be utilized, but has some distinct limitations. This design note provides design equations and recommendations for designing resistors with PCB copper.

DESIGN OF A COPPER PCB RESISTOR

The resistance, as a function of temperature, for a piece of metal, is given by the equation:

$$R(T) = \frac{S(T) \bullet \ell}{a}$$

with the units

R = Resistance, Ω
S(T) = Resistivity, Ω–cm
ℓ = Length, cm
a = Area, cm^2

The characteristics of copper which are pertinent to the design of a copper PCB resistor are [1]

Electrical Resistivity:
$1.7241 \bullet 10^{-6} \Omega - cm$ @ 20°C

Temperature Coefficient of Resistivity:
+0.0039 per °C

Composition:
99.5% Pure Copper, typically

These constants apply to the standard commercially annealed copper used in PCB technology.

The resistivity of copper, as a function of temperature, is therefore defined as:

$S(T) = 1.7241 \bullet 10^{-6} \bullet [1 + 0.0039 \bullet (T - 20)] \Omega - cm$

where T is the copper temperature in °C.

One PCB Definition which is also pertinent to resistor design is:

1oz copper is defined as 1 ounce of copper deposited over 1 square foot of surface area. This results in a copper clad PCB with a typical copper thickness of 0.0014 inches ±0.0002 inches. 2oz copper is simply twice as thick.

Using these parameters to calculate the resistance of a given length, width, and thickness of copper PCB etch results in the formula:

$$R(T) = \frac{S(T)[\Omega - cm] \bullet Length[cm]}{Width[cm] \bullet Thickness[cm]}$$

$$= \frac{S(T)[\Omega - cm] \bullet \frac{1000 mils}{2.54 cm} \bullet Length(mils)}{Width(mils) \bullet Thickness(mils)}$$

The use of a low value sense resistor implies that the current in that resistor can be quite high. A copper etch on a PCB will self heat due to the power dissipated by the resistor. MIL-STD-275E [2] provides design guidelines relating copper etch current to temperature rise and etch dimensions. Figure 1 recreates sections of the MIL-STD-275E curves. A temperature rise, above ambient temperature, can be found by knowing the current and the area of the copper etch.

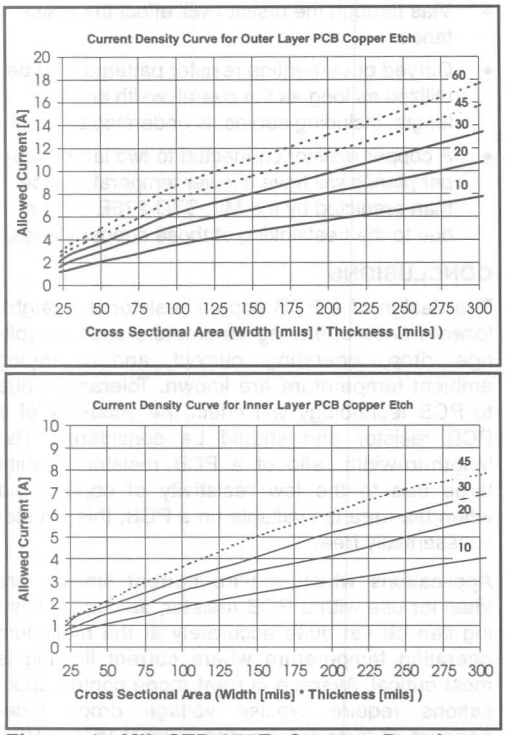


Figure 1. MIL-STD-275E Current Density vs Temperature Rise Curve for Outer and Inner Copper Layers

Example: Calculate the length and width of a 10mΩ MAXIMUM PCB resistor using 1oz on an outer layer of a PCB. The resistor must carry 10A maximum while maintaining no more than a 30°C temperature rise above ambient. Ambient temperature for normal operation is 10°C to 60°C.

Step 1:

Find the cross sectional area to carry 10A with ≤ 30°C rise, and solve for the minimum width of the resistor.

From Figure 1, 205 $mils^2$ are required to carry 10 Amperes. 1oz copper is 1.4mils thick, resulting in a minimum width for the resistor of 146mils.

Set Width = 150mils

Step 2:

Find the length of the resistor, insuring that it is designed for 10mΩ maximum at 60°C ambient +30°C rise (copper temperature is 90°C).

From the equations

$$S(90) = 1.7241 \bullet 10^{-6} \bullet [1 + 0.0039 \bullet (90 - 20)]\ \Omega - cm$$

and

$$R(90) = \frac{S(90)\left[\frac{\Omega - cm}{°C}\right] \bullet \frac{1000mils}{2.54cm} \bullet Length[mils]}{Width[mils] \bullet Thickness[mils]}$$

Solving for R(90°C) = 10mΩ, using150 mils for Width and 1.4 mils for Thickness results in Length = 2.43 inches.

Final Dimensions (inches): 2.43 (L) x 0.150 (W) x 0.0014 (T)

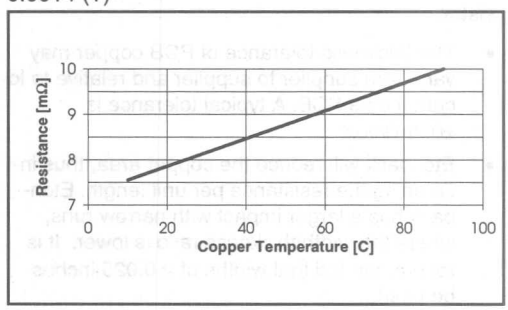


Figure 2. Resistance vs Copper Temperature for Example Design

The final resistance, as a function of the copper temperature, is shown in Figure 2.

Table 1 provides the required dimensions for a 1oz PCB copper resistor given a maximum current and desired voltage drop. Table 1 assumes a maximum operating ambient temperature of 60°C, with the width specified for a 30°C temperature rise. The required resistance is equal to V/I and is calculated at a copper temperature of 90°C.

AMPS	Desired Voltage Drop 10mV PCB Etch Length [in]	25mV	50mV	Width [in]
1	0.162	0.405	0.810	0.010
2	0.243	0.608	1.215	0.015
3	0.405	1.013	2.025	0.025
4	0.648	1.620	3.240	0.040
5	0.891	2.228	4.456	0.055
6	1.053	2.633	5.266	0.065
7	1.377	3.443	6.886	0.085
8	1.701	4.253	8.506	0.105
9	2.025	5.063	10.126	0.125
10	2.430	6.076	12.152	0.150
11	2.754	6.886	13.772	0.170
12	3.078	7.696	15.392	0.190

Table1. Dimension Solver for Given Current and Desired Voltage Drop for 90°C Maximum Copper Temperaturre

Some PCB physical and layout characteristics should be considered when designing a PCB resistor.

- The thickness tolerance of PCB copper may vary from supplier to supplier and relative to location on a PCB. A typical tolerance is ±0.2mils/oz.
- Etchback will reduce the copper area, thus increasing the resistance per unit length. Etchback has a larger impact with narrow runs, where the width/thickness ratio is lower. It is recommended that widths of ≥ 0.025 inches be used.
- The copper resistor, if it is on an outer PCB layer, should be solder masked over the entire resistive area. Solder on the copper will reduce the resistance.
- Vias through the resistor will effect the resistance.
- Curved or serpentine resistor patterns may be utilized as long as the overall width and length, including curves, is understood.
- A copper resistor connected to two larger copper planes will have a lower temperature rise than predicted by the MIL-STD-275E curves due to the heatsinking of those copper planes.

CONCLUSIONS

The design of a PCB copper resistor is straightforward once operating parameters such as voltage drop, operating current and operating ambient temperature are known. Tolerances due to PCB technology will effect the accuracy of a PCB resistor and should be considered. The length-to-width ratio of a PCB resistor is quite large due to the low resistivity of copper, but when the area is available on a PCB, this resistor is essentially free.

Applications which require current limiting are ideal for use with a PCB resistor, as current limiting can be set quite accurately at the maximum operating temperature where current limiting is most critical. Average current mode control applications require precise voltage drops independent of temperature and current levels. PCB resistors are therefore not recommended for use as an Average Current Mode control sense resistor.

REFERENCES

[1] Reference Data for Radio Engineers, Howard W. Sams & Co. Inc., Sixth Edition 1977.

[2] MIL-STD-275E, NOTICE 1, 8 July 1986, Military Standard Printed Wiring for Electronic Equipment.

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Lamp Ignitor Circuit

by Ron Fiorello

Both Fluorescent and HID lamps are becoming increasingly more popular due to their luminous efficiency and quality of the light output. These types of lamps, although they have many advantages over incandescent lamps, have more demanding starting requirements. This design note briefly describes a few different types of possible ignitor circuits and is not meant to be a complete description of all the possible circuit configurations.

Fluorescent Lamp Ignitor Circuit

The ignitor circuit shown in Figure 1 is typically used to start conventional Fluorescent lamps powered by an electronic ballast. Capacitor C

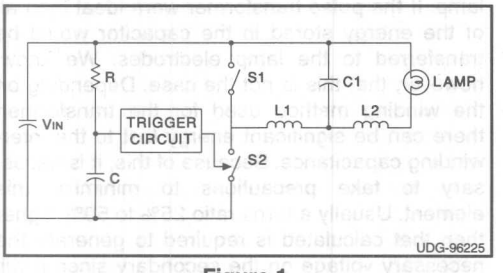


Figure 1.

charges upon application of the input voltage causing the trigger circuit to close switch S2 (where S1 and S2 are typically the power switches in a half bridge converter). This allows the series resonant circuit consisting of L1 and C1 to provide the high voltage (typically 500V) to ignite the lamp. Once the lamp has been lit, the trigger circuit is disabled. The trigger element is usually some type of semiconductor switch such as a DIAC.

Parallel Ignitor Circuit

The circuit in Figure 2 is a simple parallel ignitor circuit for a gas discharge lamp. The trigger cir-

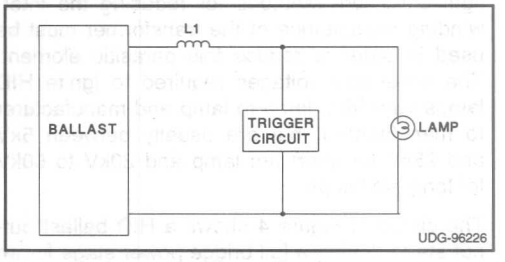


Figure 2.

cuit, which is usually part of the lamp, will repetitively trigger in order to generate the necessary voltage pulses to ignite the lamp. The pulses are due to the storage of energy in the inductor when the switch S1 turns on. The obvious advantage of this circuit is its simplicity since it consists of only two elements, an inductor and switch. Although a simple bimetal switch could be used, the disadvantage of the circuit is that the switch would need to be located in or near the lamp.

Series Ignitor Circuit for HID Lamp

The circuit in Figure 3 is typically used to ignite gas discharge lamps. The trigger circuit drives

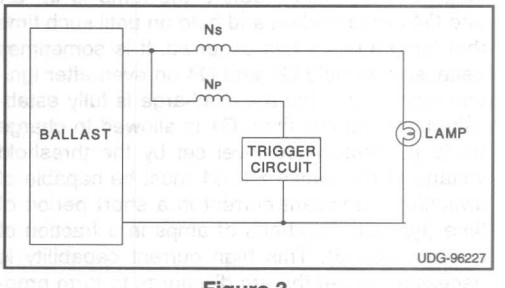


Figure 3.

the primary of a pulse transformer inducing a high voltage on the lamp electrodes. The main advantage of this series ignitor circuit is that the ballast is not exposed to the high voltage transients generated from the ignitor. The main disadvantage, which is true for most ignitor circuits, is that it should be located as close as possible to the lamp in order to minimize the parasitic effects of wiring. This effect could have significant impact on the rise time of the voltage pulse delivered to the lamp, increasing the chances of a no light condition. Methods for reducing the interwinding capacitance of the transformer must be used in order to reduce this parasitic element. The necessary voltages required to ignite HID lamps vary from lamp to lamp and manufacturer to manufacturer, but are usually between 5kV and 25kV for short arc lamp and 20kV to 50kV for long arc lamps.

The circuit in Figure 4 shows a HID ballast output stage driving a full bridge power stage for an AC lamp. Upon application of power to the output

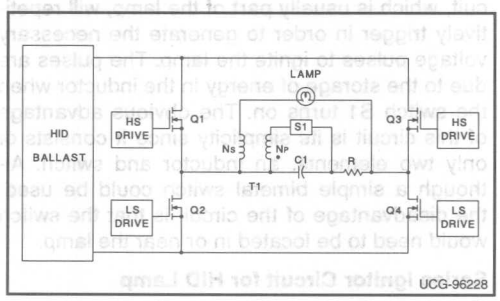


Figure 4.

stage of the ballast, before the lamp is lit, Q1 and Q4 are turned on and held on until such time that lamp ignition has occurred. It is sometimes necessary to hold Q1 and Q4 on even after ignition occurs until the arc discharge is fully established. During this time, C1 is allowed to charge up to predetermined level set by the threshold voltage of the switch S1. S1 must be capable of switching significant current in a short period of time (typically hundreds of amps in a fraction of a microsecond). This high current capability is necessary to get the arc discharge to form properly on the tips of the electrodes of the lamp. Once the arc discharge has occurred, the ignitor circuit is rendered inactive because the lamp impedance will drop drastically and the capacitor voltage will never reach the threshold level of the switch.

Assume, for instance, that the threshold voltage of S1 is 400V. C1 will be allowed to charge up to 400V before an ignition pulse occurs. This assumes that the open circuit output voltage of the ballast is limited to 600V before ignition of the lamp. The energy stored in the capacitor is $(1/2)CV^2$. Assuming a lossless switch for S1, all energy stored in C1 is then dumped into the transformer primary winding inductance. The primary inductance required to support this energy can be determined using the above assumption from:

$$(1/2) \bullet C1V^2 = (1/2) \bullet L_P I^2$$

The turns ratio from primary to secondary of T1 can be found based on the ignition voltage of the lamp. If the pulse transformer were ideal then all of the energy stored in the capacitor would be transferred to the lamp electrodes. We know, however, that this is not the case. Depending on the winding method used for the transformer, there can be significant energy lost to the interwinding capacitance. Because of this, it is necessary to take precautions to minimize this element. Usually a turns ratio 25% to 50% higher then that calculated is required to generate the necessary voltage on the secondary since it will not be possible to eliminate this capacitance entirely.

Care must be taken in choosing the secondary ignitor inductance since it is in series with the lamp and is being excited with an AC voltage. Too large an inductance will reduce the excitation voltage to the lamp. Luckily the excitation frequency of this voltage is typically between 200Hz and 1000Hz so the AC impedance can be kept to a minimum with a fairly large inductance value. The secondary inductance also provides some beneficial filtering of the current seen by the lamp. This filtering helps reduce the chance of acoustic resonances being excited in the arc

tube by the switching frequency current ripple of the ballast. These resonances can cause problems with the lamp optics as well as lead to destruction of the lamp if left unchecked. Because of this, AC HID lamps are typically driven with a low frequency square wave current.

References

[1] Waymouth "Electrical Discharge Lamps" MIT Press

[2] Murdoch "Illumination Engineering from Edison's Lamp to the Laser" Visions Communication

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Design Note

UCC3941 One Volt Boost Converter Demonstration Kit - Schematic and List of Materials

by Eddy Wells

The UCC3941-3/-5/-ADJ Demonstration Kit allows the designer to evaluate the performance of the UCC3941-3/-5/-ADJ One Volt Boost Converter in a typical application circuit. Figure 1 shows a schematic for the UCC3941-3/-5/-ADJ Demonstration Kit. The UCC3941control chip is available in three output voltage configurations (VOUT = 3.3V, 5V, or adjustable). The kit can be populated to evaluate any of these three versions.

For the fixed output voltages, R1 is not populated and R2 is a 0Ω jumper, connecting pin 6 to ground. With the adjustable version, pin 6 is connected to the inverting input of a comparator whose non-inverting input is internally connected to 1.25V. R1 and R2 are used to program the output voltage, where

$$VOUT = 1.25 \bullet \left(1 + \frac{R1}{R2}\right)$$

SD needs to be grounded, or set to a logic level low, in order for the chip to operate. If SD is floating, or set to a logic level high, the UCC3941 enters a low power shutdown state. R3 sets the power limit of the device (see the UCC3941-3/-5/-ADJ Data Sheet). A value of 6.2Ω will limit the output power to 500mW.

Table 1 contains a parts list for the demonstration kit (fixed output versions). Reference designators are printed on the circuit board next to the associated components.

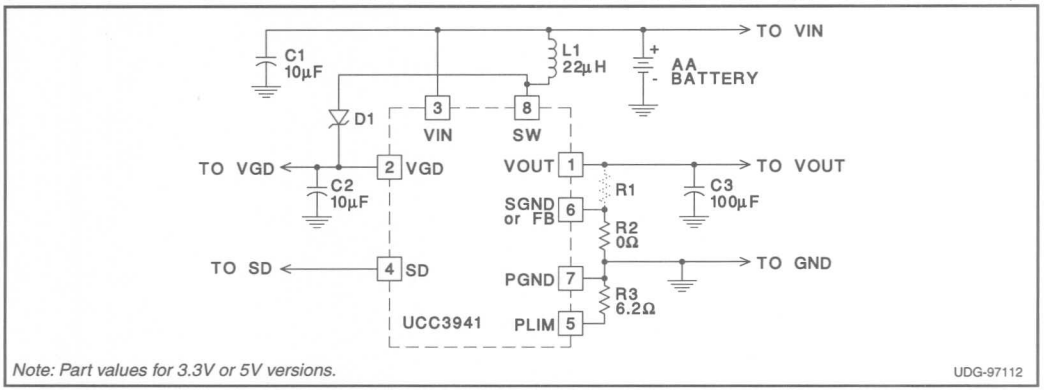
Alternate components can be substituted, however a few words of caution are in order.

High quality low ESL, low ESR, capacitors should be used in order to keep the output ripple voltage low and minimize noise that could effect circuit performance. Sprauge 594D/595D series, AVX TPS series, or Sanyo OS-CON series are good choices.

A 22µH inductor is recommended for most applications. An inductor value of less than 10µH should not be used since the rise and fall times will begin to approach internal timing limits of the IC. Larger values of inductors will typically result in larger ripple voltages on the outputs, due to the residual energy stored in the inductor. (Note: Data Sheet equations for the power limit and peak current assume a 22µH inductor). Inductors exist as standard part numbers from vendors such as Coilcraft, Coiltronics and Sumida.

A zener diode is used for D1 in order to guarantee that VGD does not rise above 10V during unloaded conditions.

For further information, contact a local Unitrode Representative or Field Applications Engineer at (603) 424-2410.



Note: Part values for 3.3V or 5V versions.

UDG-97112

Figure 1. Demonstration Kit Schematic

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Reference Designator	Part Description	Part Value	Part Manufacturer	Part Number
C1	Tantalum Capacitor	10µF, 16V	Sprague	595D106X0016B2T
C2	Tantalum Capacitor	10µF, 16V	Sprague	595D106X0016B2T
C3	Tantalum Capacitor	100µF, 6.3V	Sprague	595D107X06R3C2T
D1	Zener Diode	10V	Motorola	1SMB5925BT3
L1	Inductor	22µH	Coilcraft	DT3316P-223
R1	Not Populated			
R2	Jumper	0Ω	Panasonic	ERJ-3GSY0R00
R3	SMT Resistor	6.2Ω	IRC	WCR0805-6R2
U1	Control Chip		Unitrode	UCC3941-3, 5, ADJ
	AA Battery Holder		Digi-Key	BHAA-ND
	5-Pin Connector		Molex	22-12-2054

Table 1. Demonstration Kit Parts List

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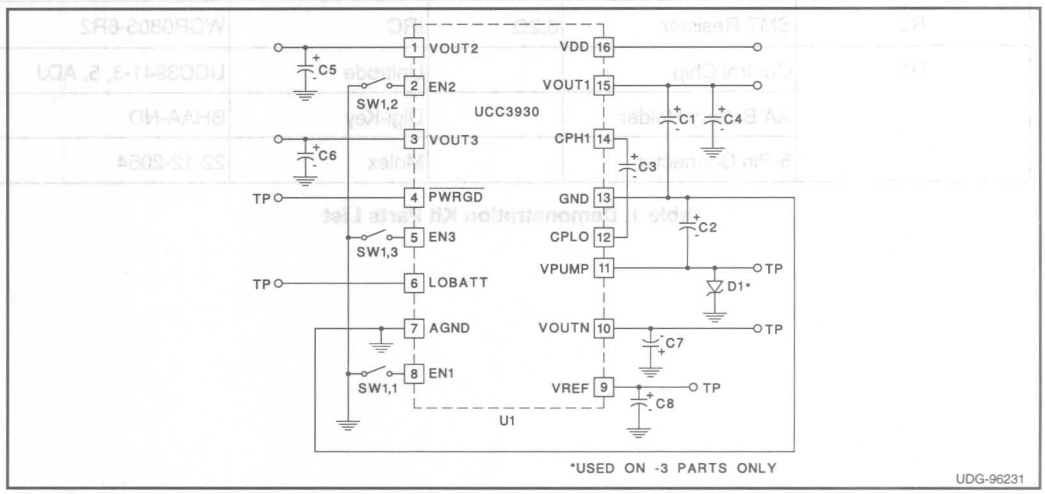
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Design Note

UCC3930 Cellular Telephone Power Converter Evaluation Kit Schematic and List of Materials

by Chuck Melchin

The Unitrode UCC3930 Cellular Telephone Power Converter integrates three positive, low dropout voltage regulators, a negative voltage power source for GaAs MESFET amplifiers, and low battery and power good signal logic in a 16 pin SSOP or DIP package. This evaluation kit is intended to enable a designer to appreciate the various features of this device. There are convenient easy clip pins to attach power and to measure pertinent test points. There are also dip switches connected to the output enable pins for selecting different output configurations. For complete details of the operation of the UCC3930, please refer to the UCC3930 datasheet included in the evaluation package.



List or Materials:

C1	10µF	Sprague #595D106X0010A2T
C2	2.2µF	Sprague #595D225X0010T2T
C3	0.1µF	#ECU - V1H104KBW
C4	2.2µF	Sprague #595D225X0010T2T
C5	2.2µF	Sprague #595D225X0010T2T
C6	1µF	Spraque #595D105X0020T2T
C7	1µF	Spraque #595D105X0020T2T
C8	0.1µF	#ECU - V1H104KBW
D1		SK12DICT
SW1		CTC2083
U1		UCC3930-3 or UCC3930-5

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Design Note

Using the UC3871 and UC3872 Resonant Fluorescent Lamp Drivers in Floating Lamp Applications

by Eddy Wells

The UC3871 and UC3872 family of resonant lamp drivers contain all of the necessary control circuitry to implement a highly efficient cold cathode fluorescent back-light driver. The grounded lamp circuit topology is discussed in detail in both U-141 and U-148. This design note describes how to modify the circuit to accommodate a floating lamp topology.

In many back-light systems, the physical spacing between the lamp and lamp wires with respect to the foil reflector and LCD frame can be tight. With tight spacing, distributed capacitance will form. High voltage capacitive coupling effects may result in uneven illumination across the tube and a slight degradation in efficiency. A floating lamp topology can reduce these effects. Figure 1 compares the AC voltage gradient of a grounded lamp and a floating lamp.

In the grounded lamp application, one end of the lamp has a high AC voltage while the other end of the lamp is connected to circuit ground. Although the current passing through the lamp is uniform, the voltage along the lamp (with respect to the ground plane) is not. The resulting electromagnetic field gradient causes a non-uniform phosphor glow as shown in Figure 1. At low currents, when the lamp is dimmed, the non-uniformity may be visible. This is known as the "thermometer effect". A floating lamp reduces the thermometer effect by cutting the voltage gradient in half.

To a lesser degree, a floating lamp will also improve circuit efficiency. Referring to Figure 1, the stray capacitance causes leakage currents from the lamp to circuit ground. Although the current through stray capacitance doesn't directly trans-

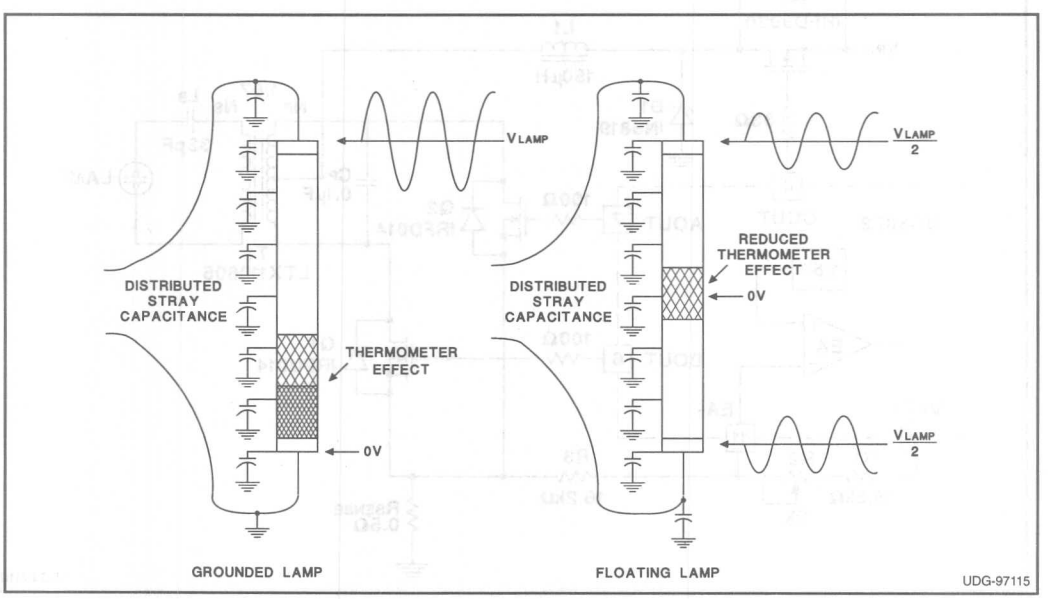


Figure 1.

floating topology cuts the average voltage along the lamp in half, this decreases the leakage current.

The UC3871 / 72 design can be converted to a floating lamp architecture as shown in Figure 2. A resistor added to the source of Q1 and Q2 is used to sense buck converter current. Buck current is proportional to the lamp current by the turns ratio of T1. A divider network connected between RSENSE, the inverting input of the error amplifier, and VREF is used to control lamp current. The non-inverting input of the error amplifier is internally derived off of VREF and should track within 0.5%. Resistors R1 and R3 should be chosen to have similar tolerances. When R2 is adjusted to zero ohms, lamp current is at a minimum. When R2 is adjusted to 2kΩ, lamp current is at a maximum. Several suppliers offer transformers for CCFL applications. A Coiltronics

Optional Open Lamp Detection with a Floating Lamp

During normal operation, the voltage at the output of the buck converter will appear as a full wave rectified sinusoid at the resonant frequency. If the lamp is opened, current that initially fed the lamp will begin to feed the resonant tank, increasing the tank voltage. The transformer voltage will then increase until the buck current and the losses in the tank reach equilibrium. This increase in secondary voltage may result in a break down of the transformer's insulation. Open lamp detection can reduce voltage stress on the CCFL transformer during an open lamp condition by decreasing the buck current feeding the resonant tank. In many designs, the tank voltage will not increase to destructive levels and open lamp detection is not necessary.

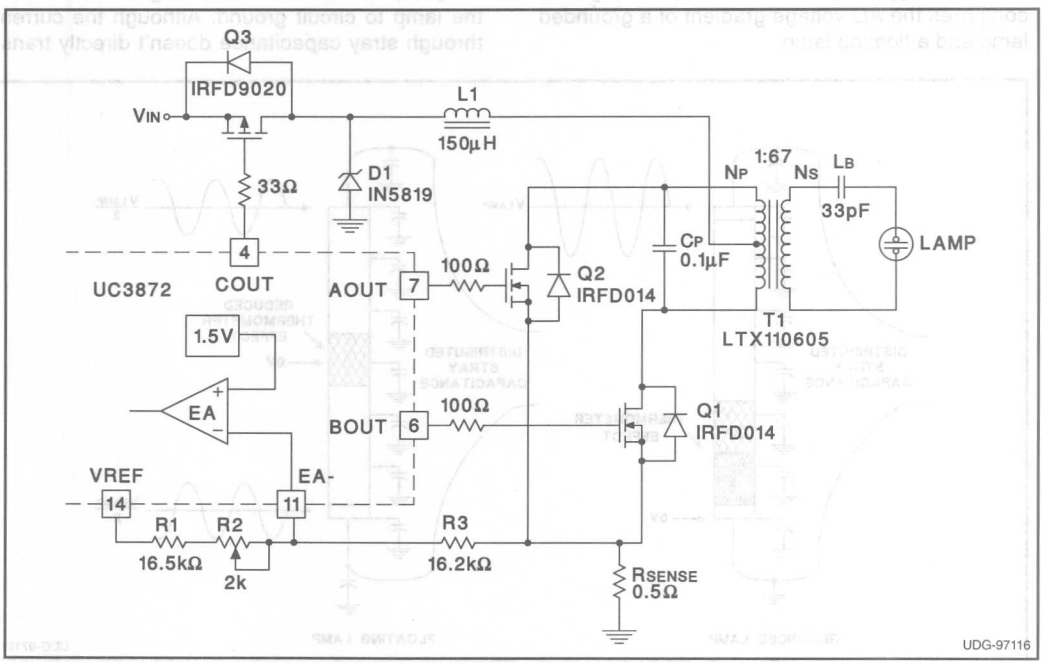


Figure 2. Floating Lamp with Primary Side Current Sense

The UC3871 / 72 open lamp detection circuitry will be invalidated by the floating lamp topology. Figure 3 shows a method for implementing open lamp detection with an open collector, quad comparator. If the buck output voltage increases above an acceptable level, comparator 1 will toggle high. A diode between the output and the positive input will latch the output high until power is cycled. A high output on comparator 1 will cause a low output on comparator 3, which is connected to the output of the error amplifier. Pulling low will force a minimum duty cycle on the buck coverter, decreasing the current feeding the tank, and the voltage on the transformer. Comparator 2 overrides the output of comparator 1 during soft start, allowing the tank voltage to ring up so the lamp can strike.

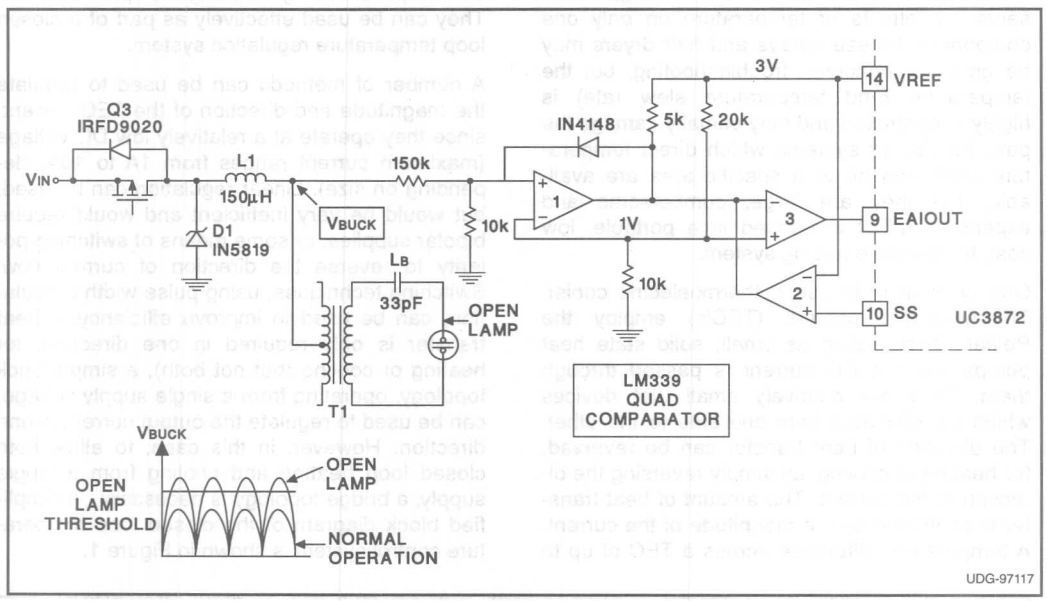


Figure 3. Optional Open Lamp Detection Circuit

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Closed Loop Temperature Regulation Using the UC3638 H-Bridge Motor Controller and a Thermoelectric Cooler

By David Salerno

Have you ever wanted to test an IC over temperature, but couldn't put the entire application circuit in the oven? Maybe you needed to access critical circuit nodes for troubleshooting, or observe the effects of temperature on only one component. Freeze sprays and hair dryers may be good for benchtop troubleshooting, but the temperature (and temperature slew rate) is highly uncontrolled and may actually damage the part. Forced air systems which direct temperature controlled air to a specific area are available, but they are large, cumbersome and expensive. What is needed is a portable, low cost, temperature forcing system.

One solution is to use a thermoelectric cooler. Thermoelectric coolers (TEC's) employ the Peltier effect, acting as small, solid state heat pumps when a DC current is passed through them. They are relatively small, flat devices which transfer heat from one side to the other. The direction of heat transfer can be reversed, for heating or cooling, by simply reversing the direction of the current. The amount of heat transfer is controlled by the magnitude of the current. A temperature difference across a TEC of up to 50°C or more can be achieved using a single element if proper heatsinking is provided on one side of the device. Larger temperature gradients can be produced by stacking multiple elements. They can be used effectively as part of a closed loop temperature regulation system.

A number of methods can be used to regulate the magnitude and direction of the TEC current, since they operate at a relatively low DC voltage (maximum current ranges from 1A to 10A, depending on size). Linear regulation can be used, but would be very inefficient and would require bipolar supplies, or some means of switching polarity to reverse the direction of current flow. Switching techniques, using pulse width modulation, can be used to improve efficiency. If heat transfer is only required in one direction, for heating or cooling (but not both), a simple buck topology, operating from a single supply voltage, can be used to regulate the output current in one direction. However, in this case, to allow both closed loop heating and cooling from a single supply, a bridge topology is necessary . A simplified block diagram of the closed loop temperature control system is shown in Figure 1.

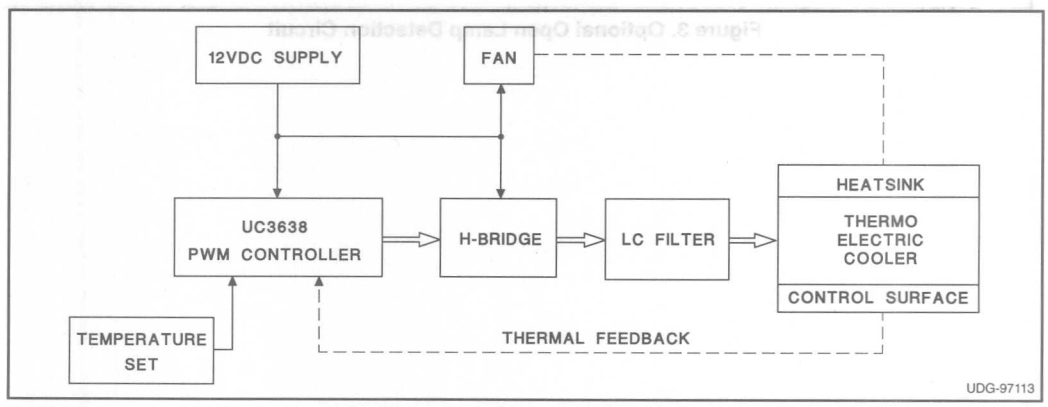


Figure 1. Temperature Controller Block Diagram

Pulse width modulation minimizes conduction losses in the control electronics, but requires a sophisticated PWM controller, especially to prevent problems such as bridge cross-conduction. The building blocks required for closed loop PWM control, such as a voltage reference, error amplifier, pulse width modulator, oscillator, current sense amplifier, and FET drivers, as well as features such as undervoltage lockout (UVLO) and pulse-by-pulse current limiting, are all contained in the UC3638. The biasing circuitry needed for single supply operation is also included. A block diagram of the IC is shown in Figure 2.

The circuit in Figure 3 uses the UC3638 H-bridge controller, four FET's, a differential LC filter and a TEC to form a closed loop temperature regulator. A PWM frequency of 100kHz is set by R15 and C13. This frequency was chosen as a compromise to limit switching losses in the bridge while minimizing the size of the LC filter components. The deadtime between commutation of the bridge switches is set by the voltage on the DB pin, using the divider of R12-R14. The voltage on PVSET determines the amplitude of the triangle wave oscillator used in the PWM modulator.

MOSFET's Q1-Q4 form the bridge, while BJT's Q5-Q8 act as high side FET drivers, since outputs AOUT1 and BOUT1 of the UC3638 are open collector. AOUT2 and BOUT2 can drive the low side MOSFET's directly. Schottky diodes D1 and D2 clamp any ringing below ground due to stray circuit inductance. Sense resistor R6 is chosen to limit the peak output current to 5 Amps. The current sense voltage is amplified by the UC3638, and any noise spikes are filtered by C12 and a 100Ω resistor internal to the IC.

The LC output filter, formed by L1, L2 and C2-C6, is required to convert the PWM output from the bridge back to a DC voltage. This is necessary because AC ripple is detrimental to the TEC, and its efficiency drops off rapidly. Less than 10% ripple is recommended. The resulting architecture is a low bandwidth class D amplifier,

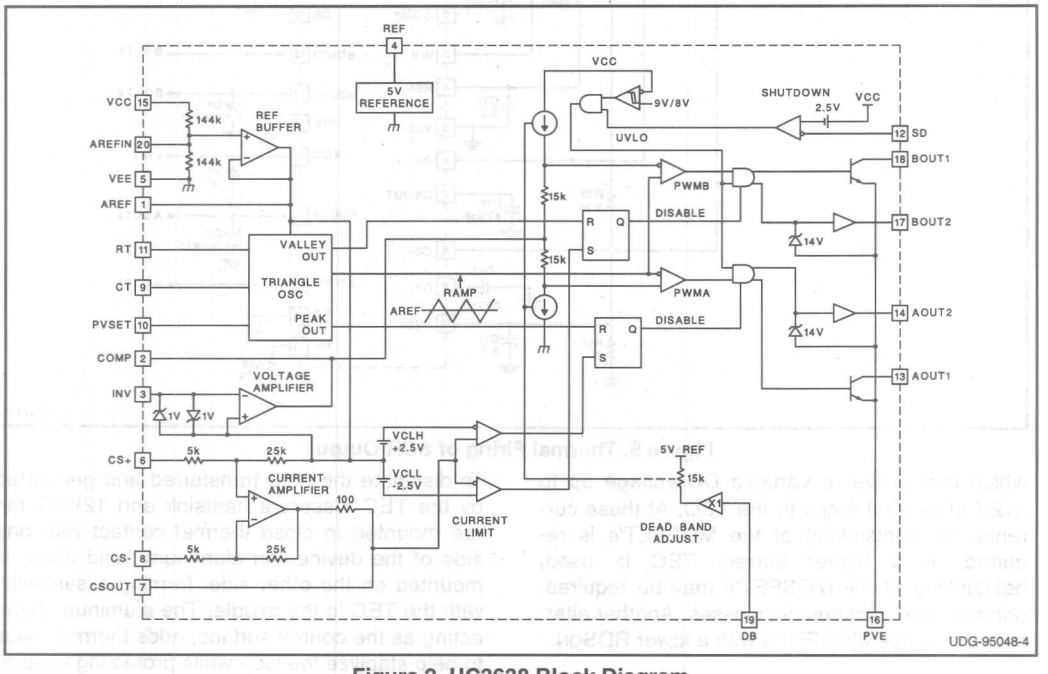


Figure 2. UC3638 Block Diagram

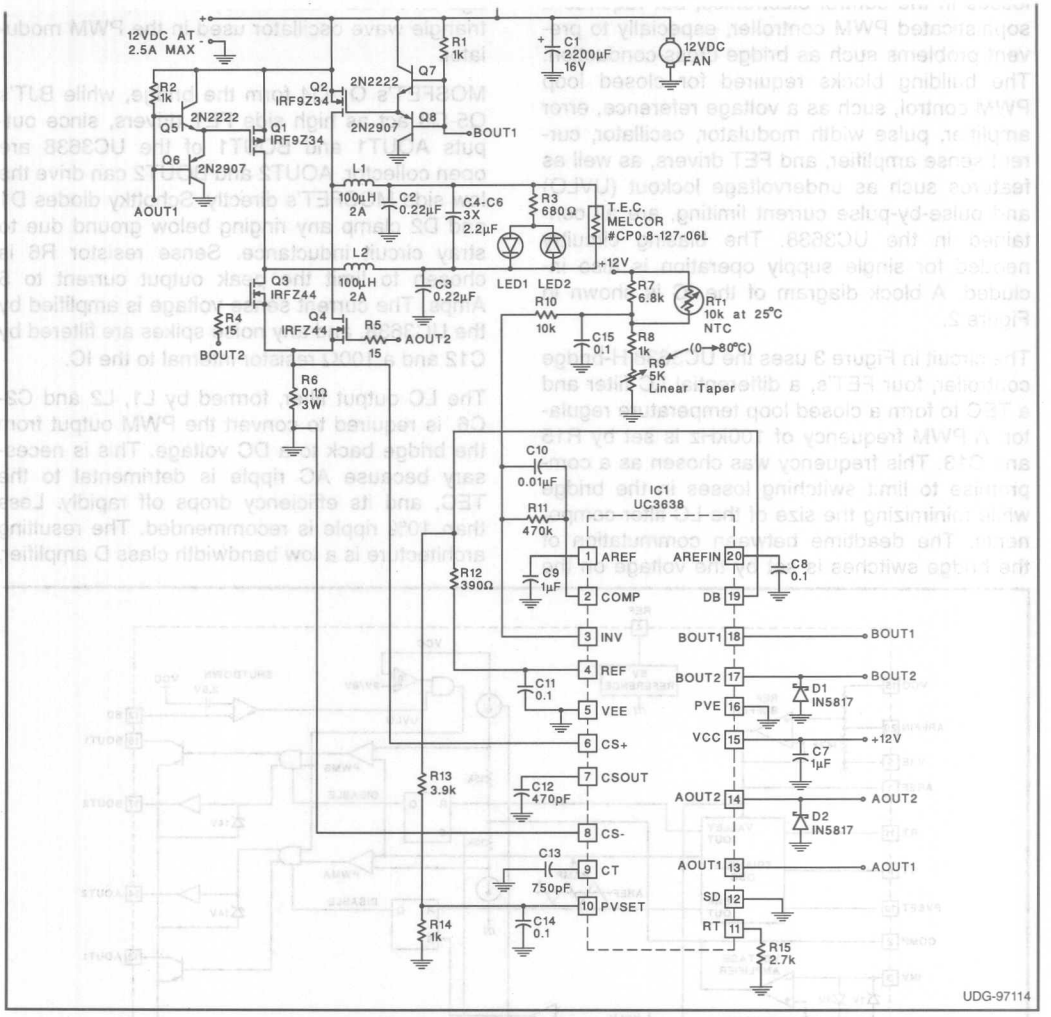


Figure 5. Thermal Firing of SCR Output

which can deliver a variable DC voltage up to ±12V at several amps to the TEC. At these currents, no heatsinking of the MOSFET's is required. If a higher current TEC is used, heatsinking of the MOSFET's may be required, primarily due to conduction losses. Another alternative is to use MOSFET's with a lower $R_{DS(ON)}$.

To dissipate the heat transferred and generated by the TEC losses, a heatsink and 12VDC fan are mounted in close thermal contact with one side of the device. An aluminum "cold plate" is mounted on the other side, forming a sandwich with the TEC in the middle. The aluminum plate, acting as the control surface, adds thermal mass to help stabilize the loop while protecting the brit-

tle ceramic surface of the TEC. This plate is placed in intimate thermal contact with the item to be temperature controlled.

RT1, an NTC thermistor, is placed in a hole in the side of the aluminum plate to provide good thermal feedback to close the loop. A parallel resistor helps to linearize the thermistor's response. This is not critical, since the temperature control pot will be calibrated, compensating for any non-linearities.

The UC3638 error amplifier compensation uses proportional gain, since it can be difficult to compensate an integral loop due to the long thermal time constant of the mechanical system. The DC gain of the error amplifier, determined by R10 and R11, is high enough so that a temperature error of <1°C will produce full output voltage to the TEC. C10 provides a pole to filter out any noise before reaching the modulator. Note that the amplitude of the triangle wave oscillator (set by R13 and R14) also affects overall loop gain.

Temperature control pot R9 is calibrated using a thermocouple temporarily mounted to the aluminum plate. Once calibrated, it is accurate and repeatable to within 1°C. LED's across the output of the filter give a visual indication of whether the TEC is heating or cooling, depending on the polarity of the output voltage.

The entire system, using the TEC shown, operates off a 12VDC, 2.5A power supply and provides closed loop temperature regulation of a surface about 1 inch square. The temperature of the control surface can be varied from 0°C to +80°C in a room ambient environment. Hotter and colder temperatures are possible if multiple devices are stacked and proper heatsinking is provided. Remember that cooling can only take place if the heat, including that produced by the efficiency losses in the TEC, can be dissipated on the opposite surface. Note that the maximum temperature is ultimately limited by the temperature rating of the solder within the TEC. Devices with ratings of up to +200°C are available.

TEC's can be used in many temperature control applications. They are available in a wide variety of shapes, sizes, power and voltage ratings from a number of manufacturers. Some manufacturers also supply heatsinks, cold plates and fans. However, low cost Pentium style heatsink and fan combinations can often be adapted.

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